ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	C3M0025065L-TR
Manufacturer:	Wolfspeed, Inc.
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

https://antrexco.com/product/details/wolfspeed-inc/c3m0025065l-tr.html

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Contact Information

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Quality & Trust

New & Original Components

Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

Secure sourcing support for OEM / EMS projects

Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

C3M0025065L

Silicon Carbide Power MOSFET

C3M™ MOSFET Technology

N-Channel Enhancement Mode

Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

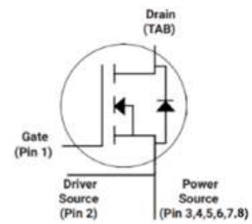
Typical Applications

- Datacenter Power Supplies
- Telecom Power Supplies
- Energy Storage Systems
- Solar (PV) inverters
- High Voltage DC/DC converters

Package

Halogen-Free

RoHS



Orderable Part Number	Package	Marking
C3M0025065L-TR	TOLL	C3M0025065L

Wolfspeed, Inc. is in the process of rebranding its products and related materials pursuant to the entity name change from Cree, Inc. to Wolfspeed, Inc. During this transition period, products received may be marked with either the Cree name and/or logo or the Wolfspeed name and/or logo.

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			650	V	$T_C = 25°C$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19	V	Transient	
Operational Gate-Source Voltage	$V_{GS\ op}$		-4/15		V	Static	Note 1
DC Continuous Drain Current	I_D			77	A	$V_{GS} = 15$ V, $T_C = 25$ °C, $T_J \leq 175$ °C	Fig. 19 Note 2
				59	A	$V_{GS} = 15$ V, $T_C = 100$ °C, $T_J \leq 175$ °C	
Pulsed Drain Current	I_{DM}			235	A	t_{Pmax} limited by T_{jmax} $V_{GS} = 15V$, $T_C = 25$ °C	Fig. 22
Power Dissipation	P_D			326	W	$T_C = 25$ °C, $T_J = 175$ °C	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	°C		
Solder Temperature	T_L			260	°C	According to JEDEC J-STD-020	

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design

Electrical Characteristics (T$_C$ = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.3	3.6	V	V_{DS} = V_{GS}, I_D = 9.22 mA	Fig. 11
			1.9		V	V_{DS} = V_{GS}, I_D = 9.22 mA, T_J = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	V_{DS} = 650 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		25	34	mΩ	V_{GS} = 15 V, I_D = 33.5 A	Fig. 4, 5, 6
			33			V_{GS} = 15 V, I_D = 33.5 A, T_J = 175ºC	
g_{fs}	Transconductance		24		S	V_{DS}= 20 V, I_{DS}= 33.5 A	Fig. 7
			23			V_{DS}= 20 V, I_{DS}= 33.5 A, T_J = 175ºC	
C_{iss}	Input Capacitance		2970		pF	V_{GS} = 0 V, V_{DS} = 400 V f = 1 Mhz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		186				
C_{rss}	Reverse Transfer Capacitance		11				
E_{oss}	C_{oss} Stored Energy		18		μJ	V_{DS} = 400 V, f = 1 Mhz	
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		226		pF	V_{GS} = 0 V, V_{DS} = 0... 400V	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		322		pF		
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		123		μJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 33.5A, $R_{G(ext)}$ = 2.5 Ω, L= 59 μH, T_J = 25ºC FWD = Internal Body Diode	Fig. 23
E_{OFF}	Turn-Off Switching Energy (Body Diode FWD)		14				
$t_{d(on)}$	Turn-On Delay Time		10		ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 33.5 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	Fig. 26
t_r	Rise Time		13				
$t_{d(off)}$	Turn-Off Delay Time		26				
t_f	Fall Time		8				
$R_{G(int)}$	Internal Gate Resistance		1.3		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		33		nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 33.5 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		32				
Q_g	Total Gate Charge		111				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 400V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 400V

Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.0		V	V_{GS} = -4 V, I_{SD} = 16.8 A, T_J = 25 °C	Fig. 8, 9, 10
		4.4		V	V_{GS} = -4 V, I_{SD} = 16.8 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		54	A	V_{GS} = -4 V, T_C = 25˚C	
$I_{S, pulse}$	Diode pulse Current		235	A	V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
t_{rr}	Reverse Recover time	14		ns	V_{GS} = -4 V, I_{SD} = 33.5 A, V_R = 400 V dif/dt = 4717 A/μs, T_J = 25 °C	
Q_{rr}	Reverse Recovery Charge	338		nC		
I_{rrm}	Peak Reverse Recovery Current	40		A		
t_{rr}	Reverse Recover time	16		ns	V_{GS} = -4 V, I_{SD} = 33.5 A, V_R = 400 V dif/dt = 2137 A/μs, T_J = 25 °C	
Q_{rr}	Reverse Recovery Charge	164		nC		
I_{rrm}	Peak Reverse Recovery Current	17		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.41	0.46	°C/W	

Typical Performance

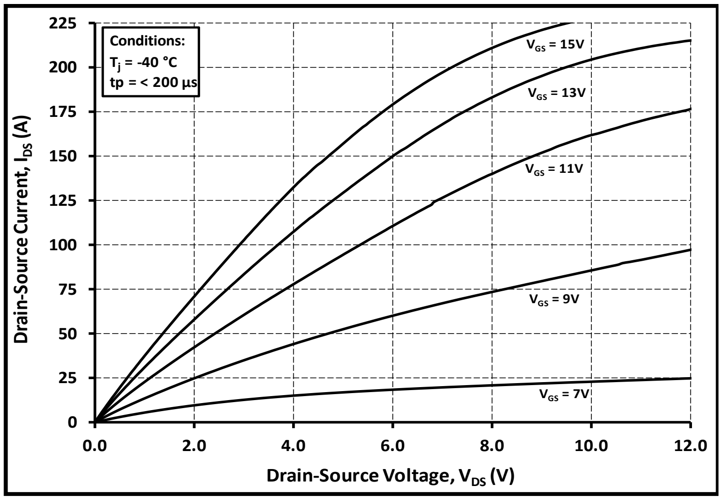


Figure 1. Output Characteristics T_J = -40 ºC

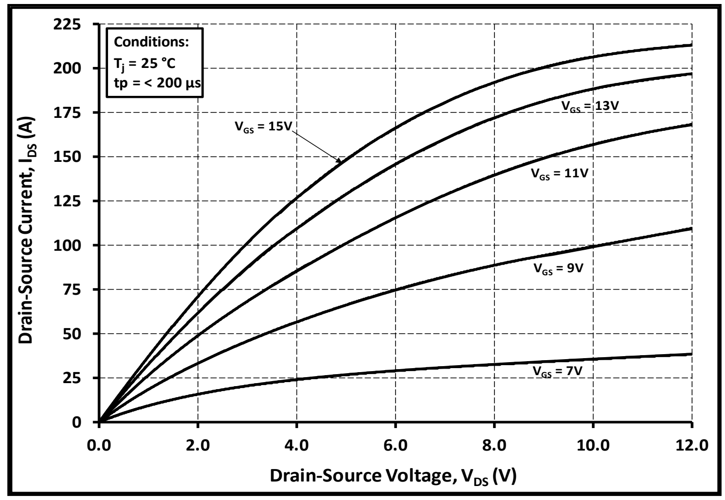


Figure 2. Output Characteristics T_J = 25 ºC

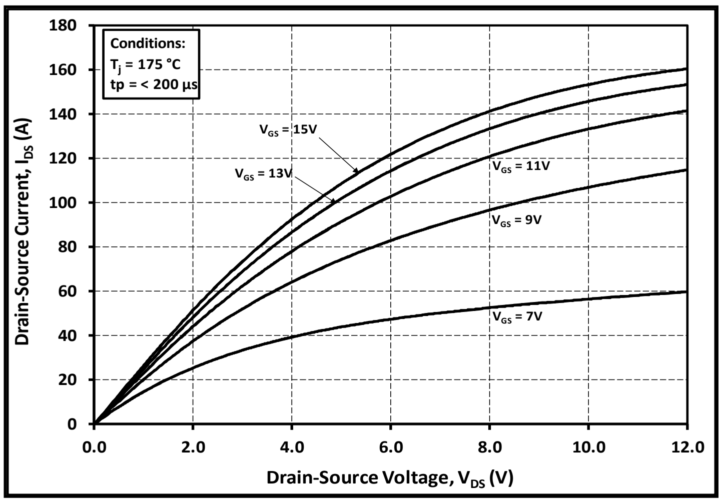


Figure 3. Output Characteristics T_J = 175 ºC

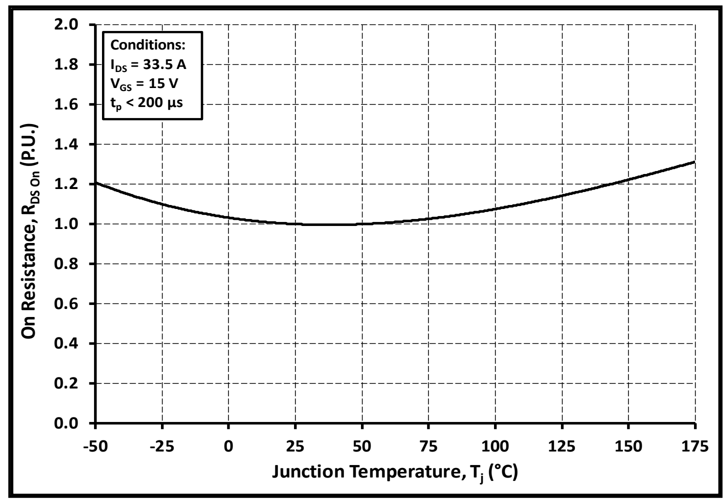


Figure 4. Normalized On-Resistance vs. Temperature

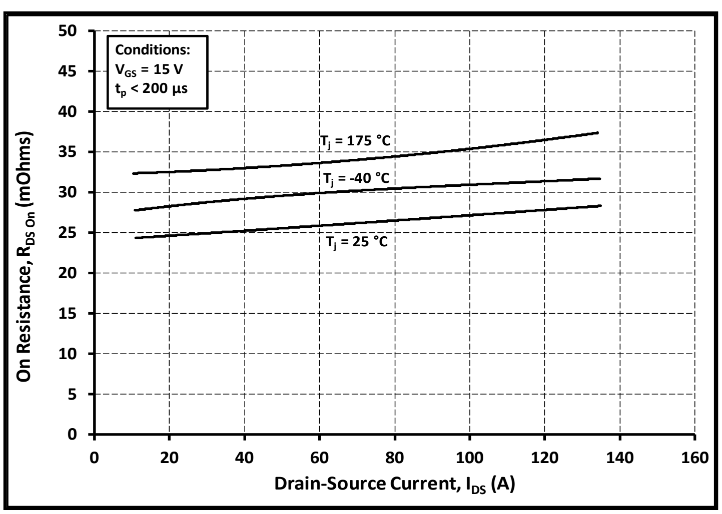


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

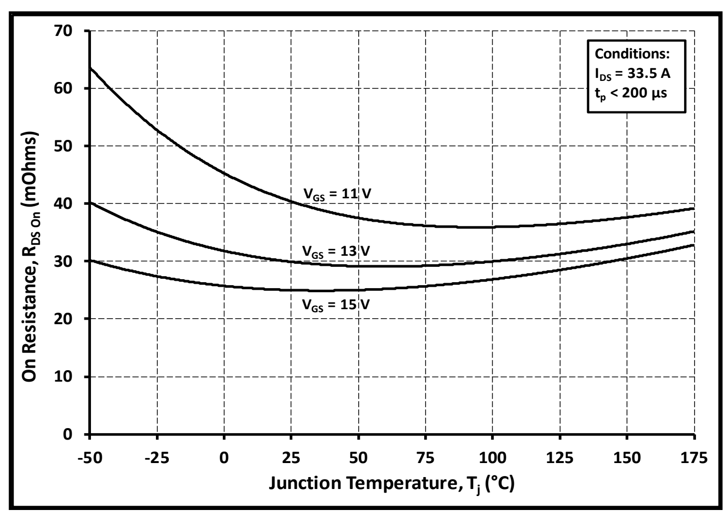


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

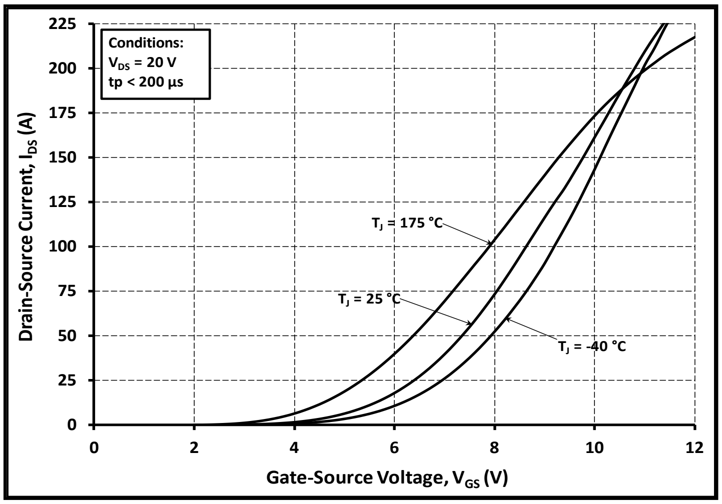


Figure 7. Transfer Characteristic for Various Junction Temperatures

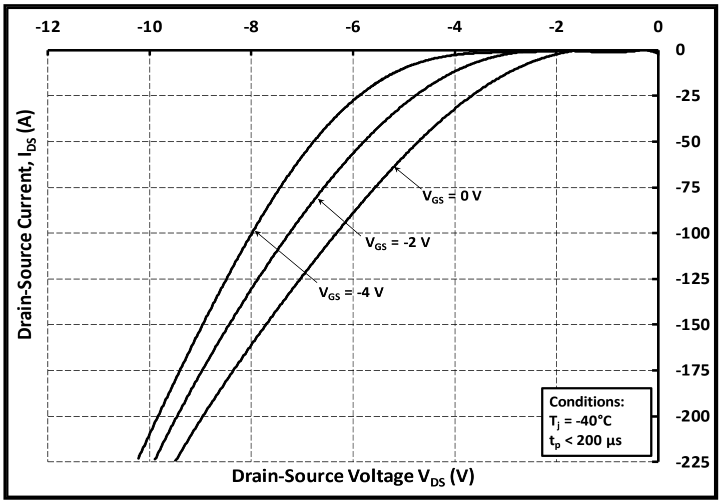


Figure 8. Body Diode Characteristic at -40 °C

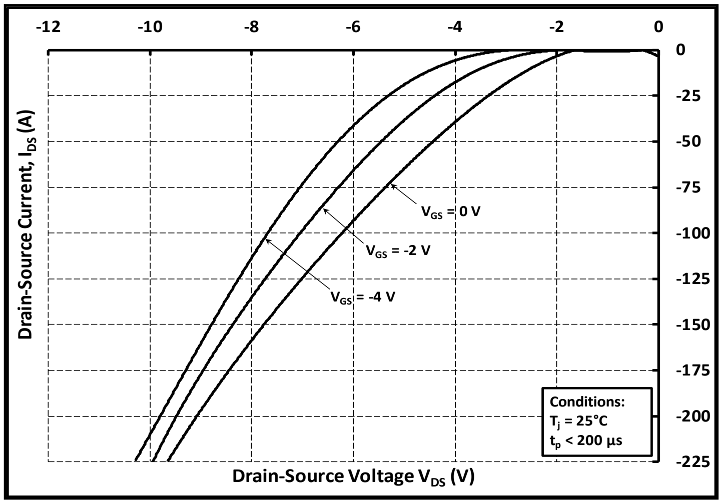


Figure 9. Body Diode Characteristic at 25 °C

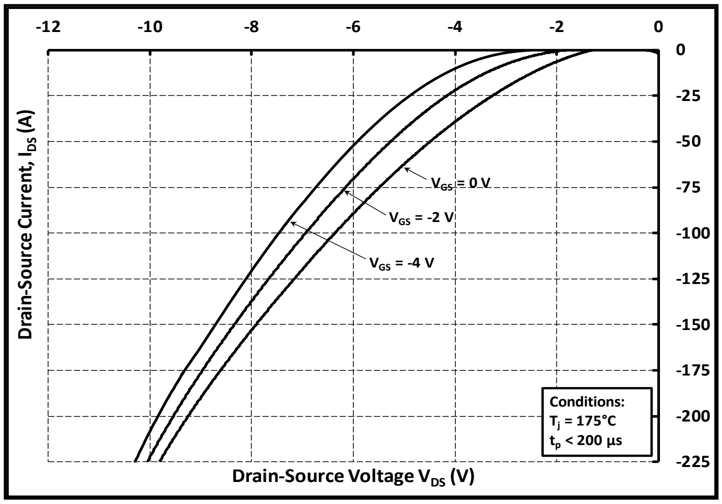


Figure 10. Body Diode Characteristic at 175 °C

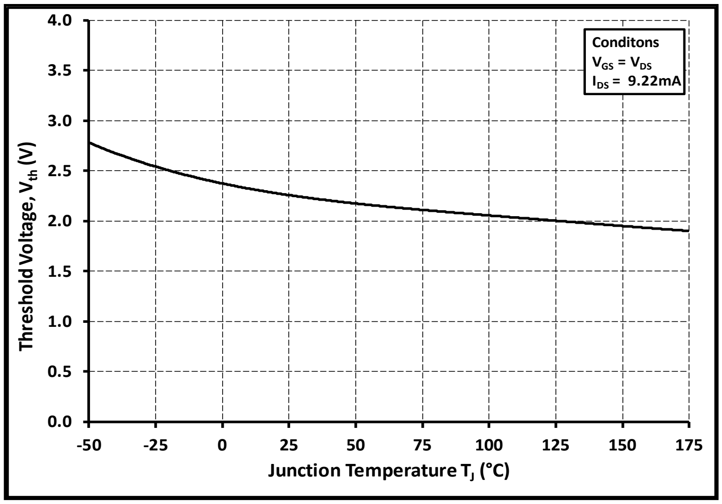


Figure 11. Threshold Voltage vs. Temperature

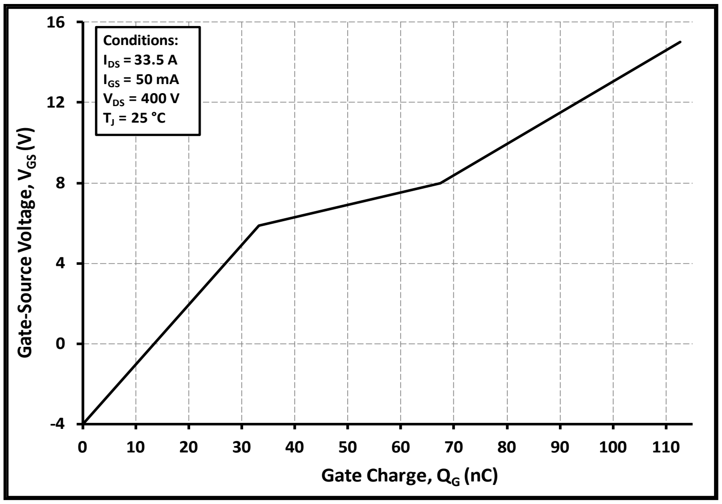


Figure 12. Gate Charge Characteristics

Typical Performance

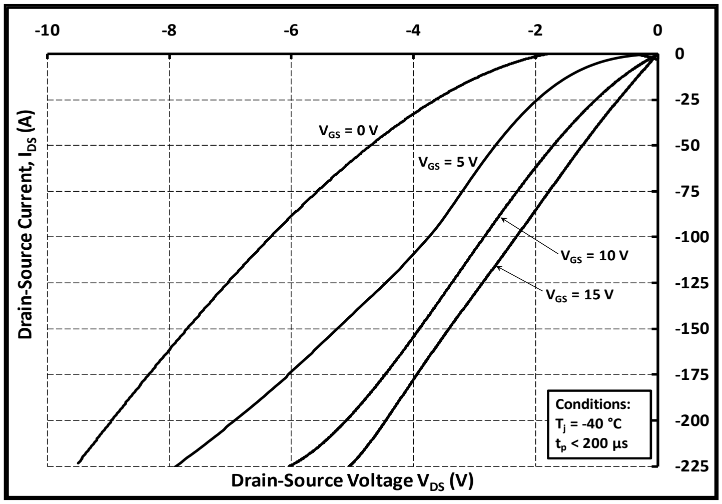


Figure 13. 3rd Quadrant Characteristic at -40 °C

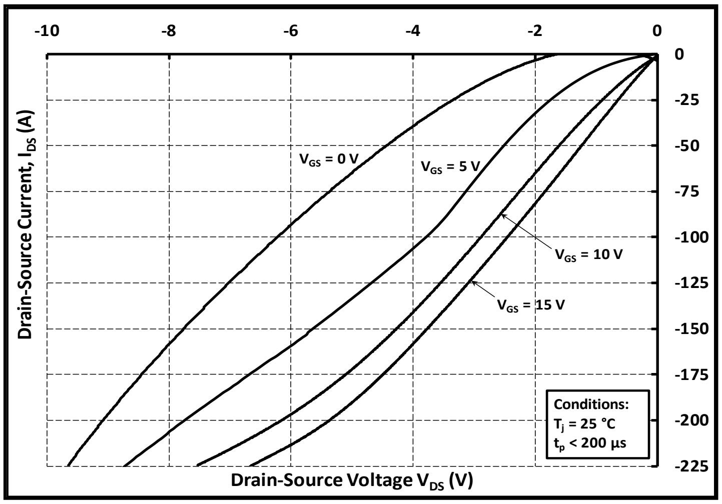


Figure 14. 3rd Quadrant Characteristic at 25 °C

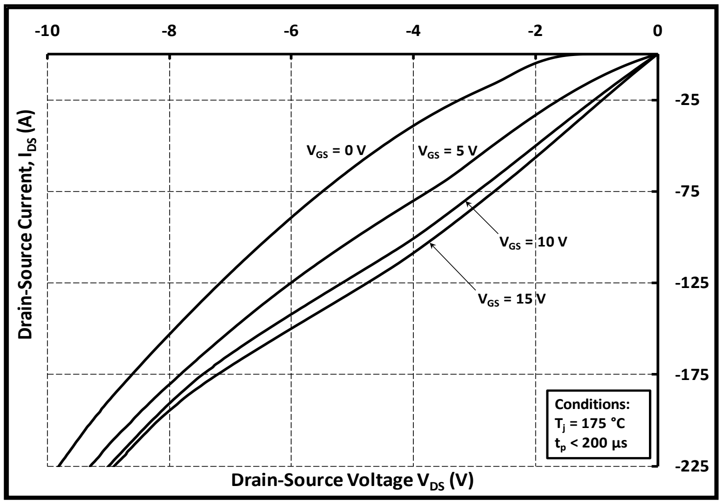


Figure 15. 3rd Quadrant Characteristic at 175 °C

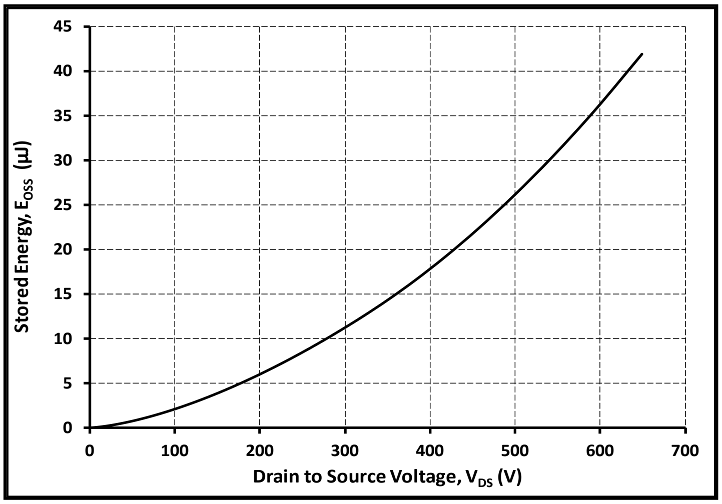


Figure 16. Output Capacitor Stored Energy

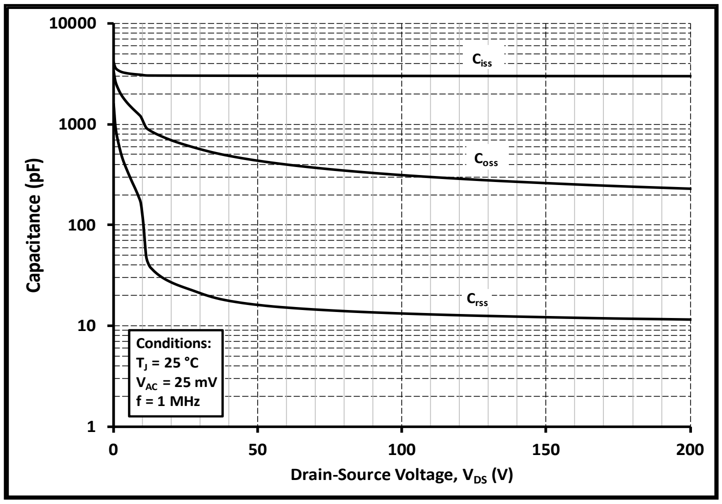


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

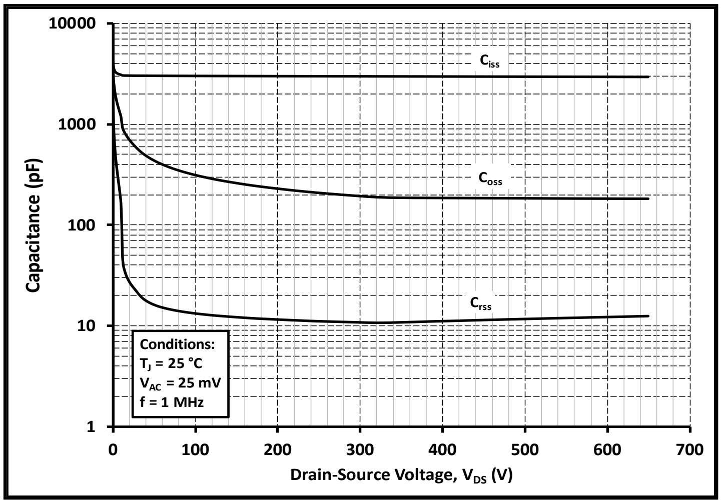


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)

Typical Performance

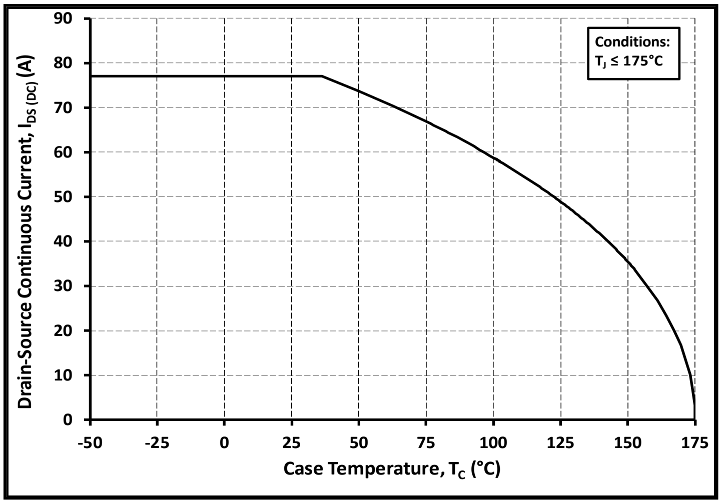


Figure 19. Continuous Drain Current Derating vs. Case Temperature

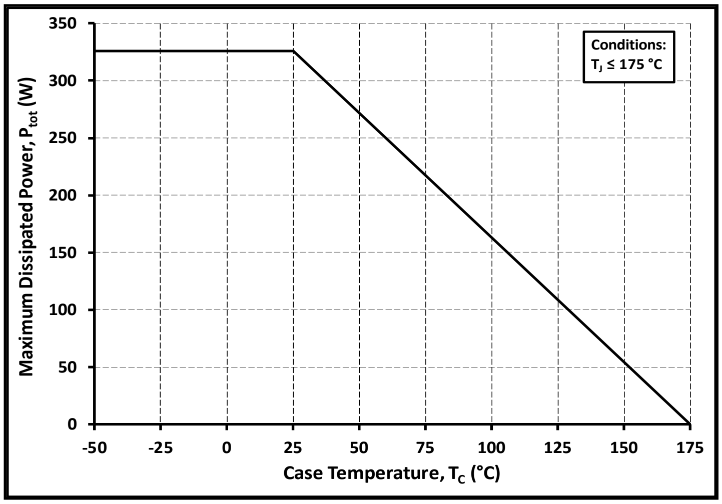


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

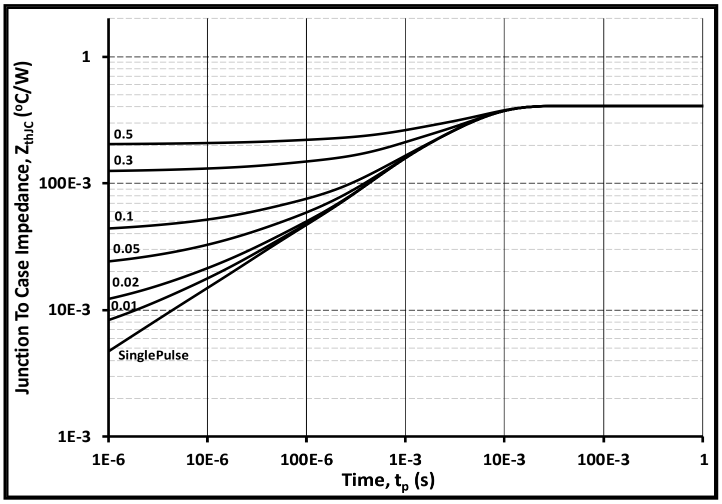


Figure 21. Transient Thermal Impedance (Junction - Case)

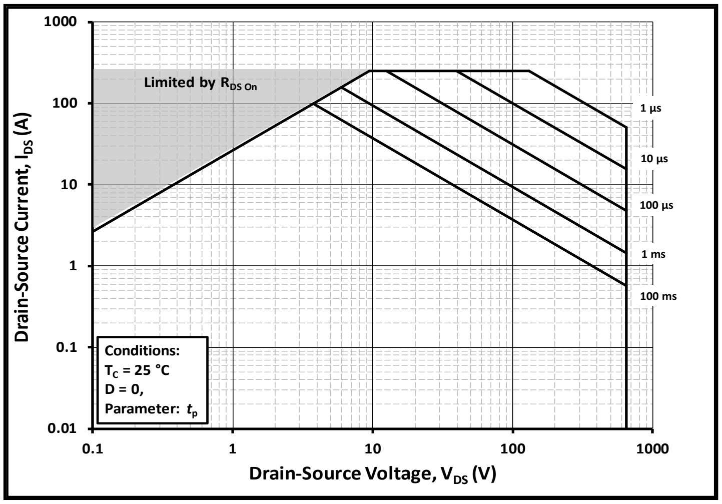


Figure 22. Safe Operating Area

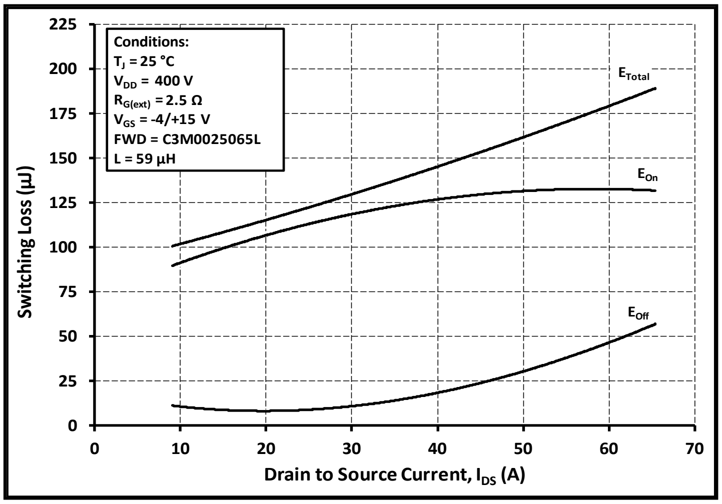


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 400V)

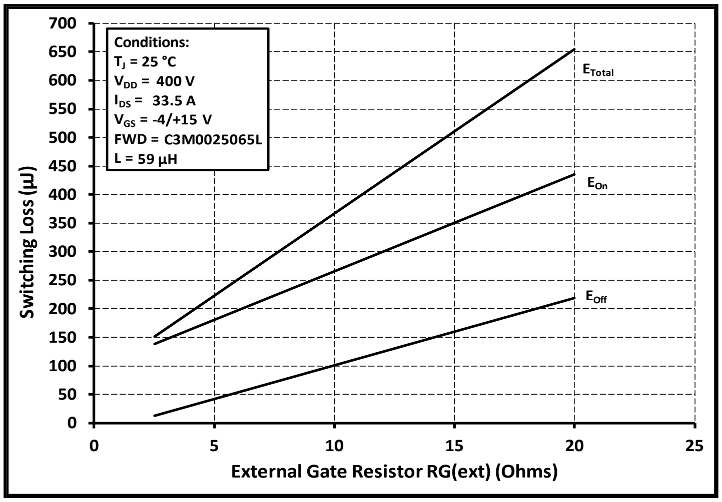


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

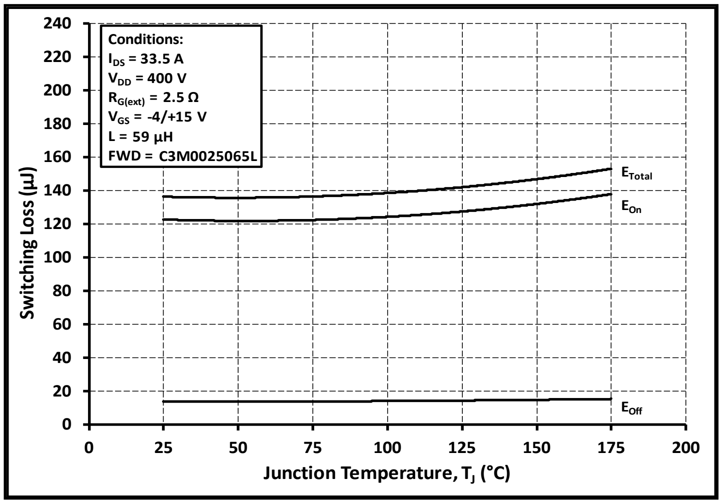


Figure 25. Clamped Inductive Switching Energy vs. Temperature

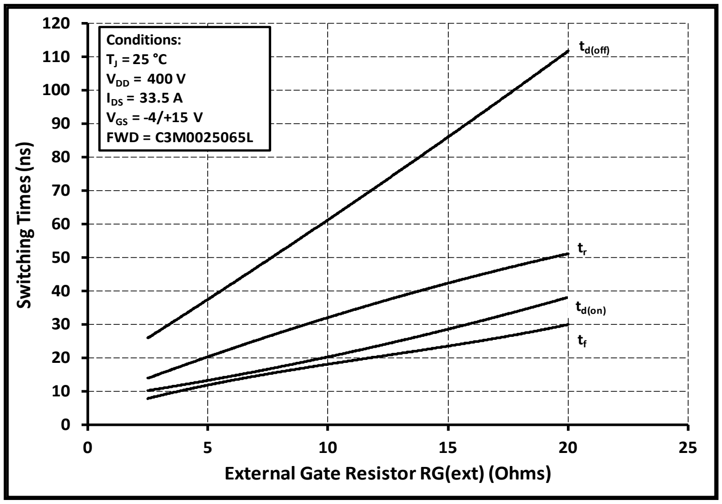


Figure 26. Switching Times vs. $R_{G(ext)}$

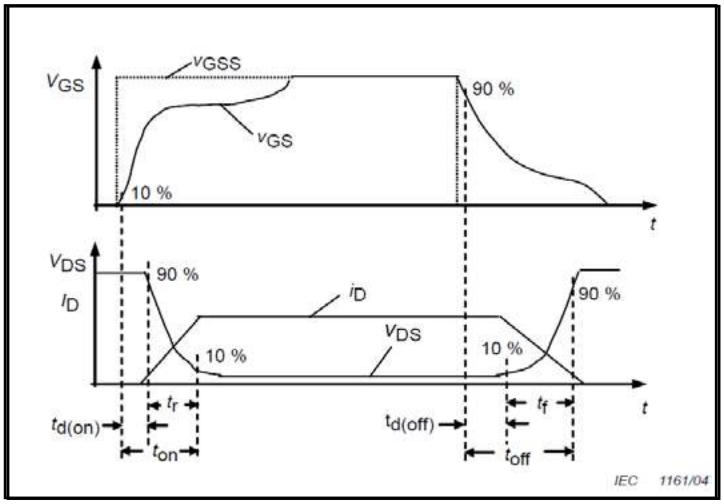


Figure 27. Switching Times Definition

Test Circuit Schematic

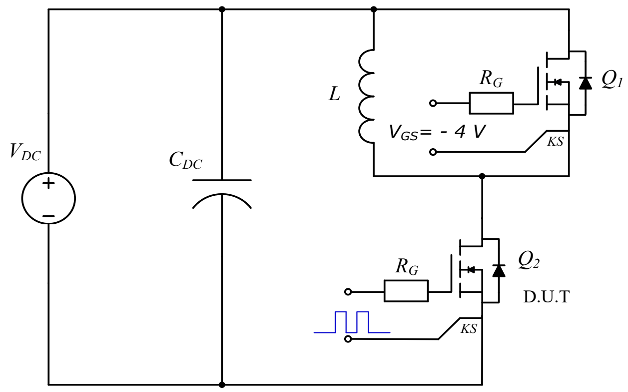
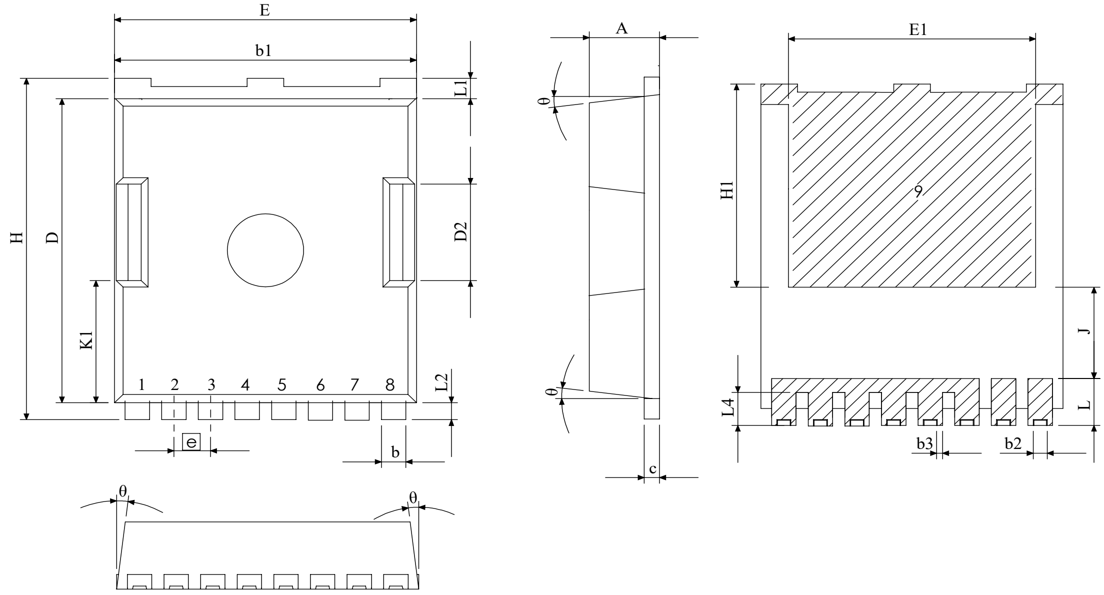


Figure 28. Clamped Inductive Switching Waveform Test Circuit

Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
b3	0.07	0.27
c	0.40	0.60
D	10.28	10.58
D2	3.10	3.50
E	9.70	10.10
E1	7.90	8.30
e	1.20 BSC	
H	11.48	11.88
H1	6.75	7.15
J	3.00	3.30
K1	3.98	4.38
L	1.40	1.80
L1	0.60	0.80
L2	0.50	0.70
L4	1.00	1.30
θ	4°	10°

1	GATE
2	KELVIN
3-8	SOURCE
9	DRAIN

NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Wolfspeed

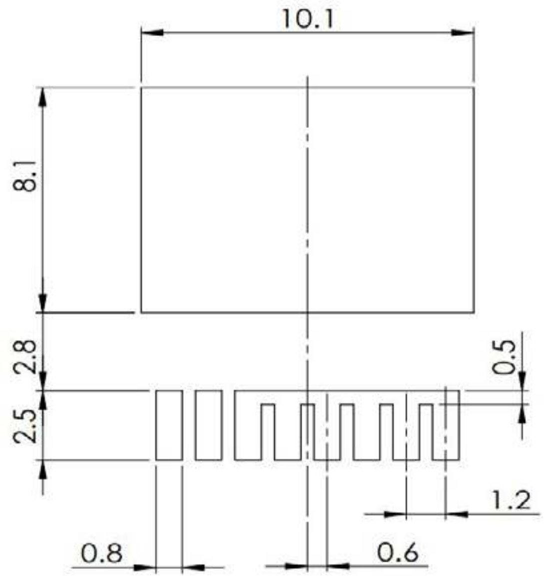
TITLE: PACKAGE OUTLINE DRAWING: TOLL

REVISION NO. 02 A4

Date: 11/08/22 PRD-06655 SCALE:1:1 SHEET 1 OF 1

Recommended Solder Pad Layout

(Note: All Dimensions are listed in Millimeters)



Revision history

Document Version	Date of release	Description of changes
1	October-2022	Initial datasheet
2	December - 2024	Legal Disclaimer, Table 1 layout revised

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REACh Compliance

REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

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