

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: SQM100P10-19L_GE3
Manufacturer: Vishay Siliconix
Package: Please confirm with sales
Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/vishay-siliconix/sqm100p10-19l-ge3.html>

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Supplier verification and packaging condition review

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

Automotive P-Channel 100 V (D-S) 175 °C MOSFET

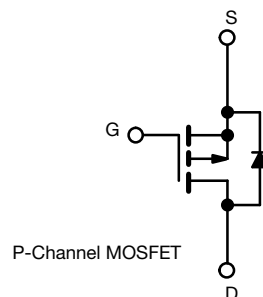
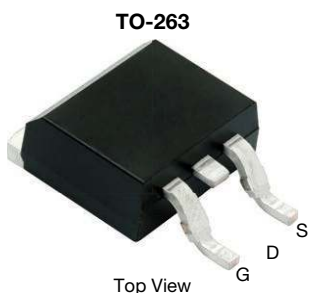
PRODUCT SUMMARY

V_{DS} (V)	-100
$R_{DS(on)}$ (Ω) at $V_{GS} = -10$ V	0.0190
$R_{DS(on)}$ (Ω) at $V_{GS} = -4.5$ V	0.0222
I_D (A)	-93
Configuration	Single
Package	TO-263

FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- 100 % R_g and UIS tested
- AEC-Q101 qualified ^d
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912

AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE


ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C = 25$ °C	A
		$T_C = 125$ °C	
Continuous Source Current (Diode Conduction) ^a	I_S	-120	
Pulsed Drain Current ^b	I_{DM}	-200	
Single Pulse Avalanche Current	I_{AS}	-70	
Single Pulse Avalanche Energy	E_{AS}	245	mJ
Maximum Power Dissipation ^b	P_D	$T_C = 25$ °C	W
		$T_C = 125$ °C	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	40	°C/W
Junction-to-Case (Drain)	R_{thJC}	0.4	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA		-100	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA		-1.5	-2.0	-2.5	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = -100 V	-	-	-1	μA
		V _{GS} = 0 V	V _{DS} = -100 V, T _J = 125 °C	-	-	-50	
		V _{GS} = 0 V	V _{DS} = -100 V, T _J = 175 °C	-	-	-250	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = -10 V	V _{DS} ≤ -5 V	-93	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = -10 V	I _D = -30 A	-	0.0155	0.0190	Ω
		V _{GS} = -10 V	I _D = -30 A, T _J = 125 °C	-	-	0.0342	
		V _{GS} = -10 V	I _D = -30 A, T _J = 175 °C	-	-	0.0432	
		V _{GS} = -4.5 V	I _D = -20 A	-	0.0177	0.0222	
Forward Transconductance ^b	g _{fs}	V _{DS} = -15 V, I _D = -30 A		-	50	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = -25 V, f = 1 MHz	-	10 800	14 100	pF
Output Capacitance	C _{oss}			-	800	1100	
Reverse Transfer Capacitance	C _{rss}			-	650	850	
Total Gate Charge ^c	Q _g	V _{GS} = -10 V	V _{DS} = -50 V, I _D = -50 A	-	220	350	nC
Gate-Source Charge ^c	Q _{gs}			-	37	-	
Gate-Drain Charge ^c	Q _{gd}			-	51	-	
Gate Resistance	R _g	f = 1 MHz		1	2.2	3.5	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = -50 V, R _L = 1 Ω I _D ≅ -50 A, V _{GEN} = -10 V, R _g = 1 Ω		-	20	30	ns
Rise Time ^c	t _r			-	21	35	
Turn-Off Delay Time ^c	t _{d(off)}			-	110	175	
Fall Time ^c	t _f			-	30	50	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	-200	A
Forward Voltage	V _{SD}	I _F = -70 A, V _{GS} = 0 V		-	-0.885	-1.5	V

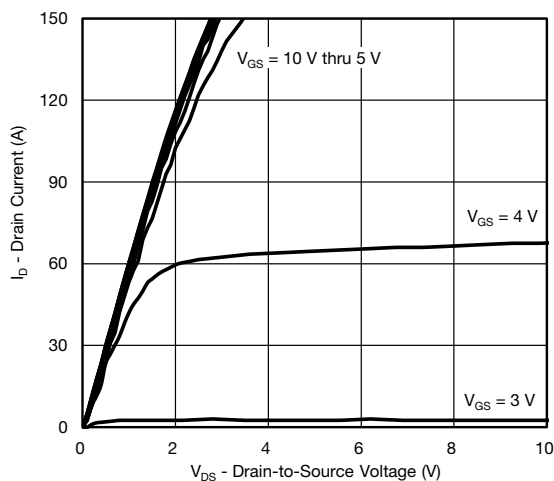
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

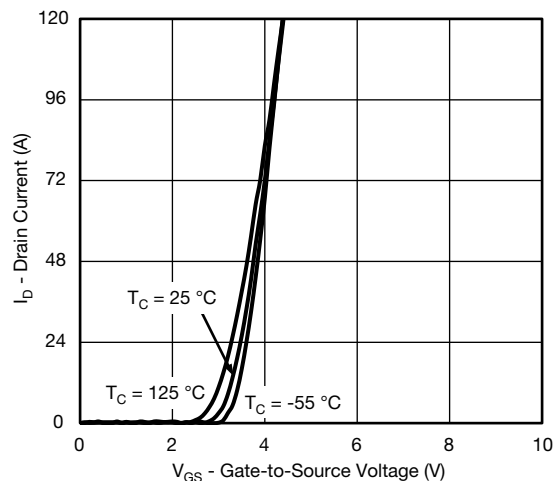
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



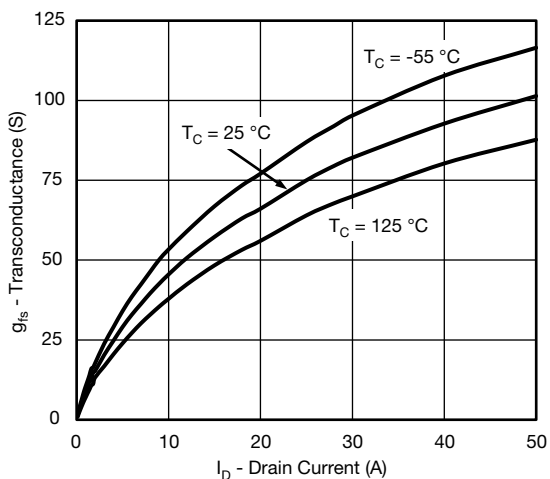
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



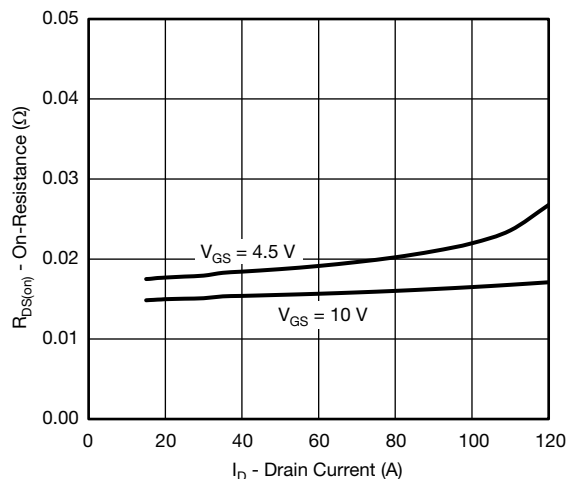
Output Characteristics



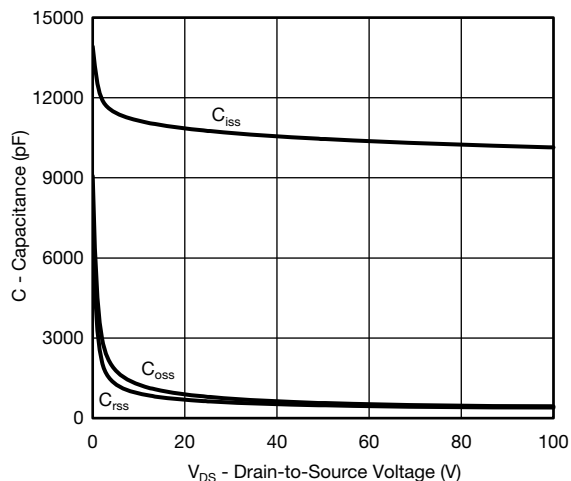
Transfer Characteristics



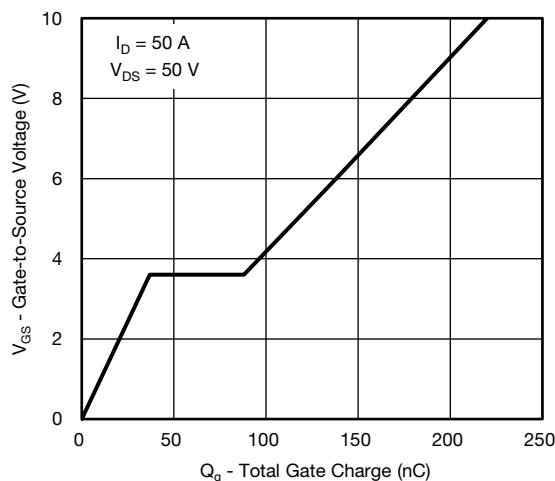
Transconductance



On-Resistance vs. Drain Current



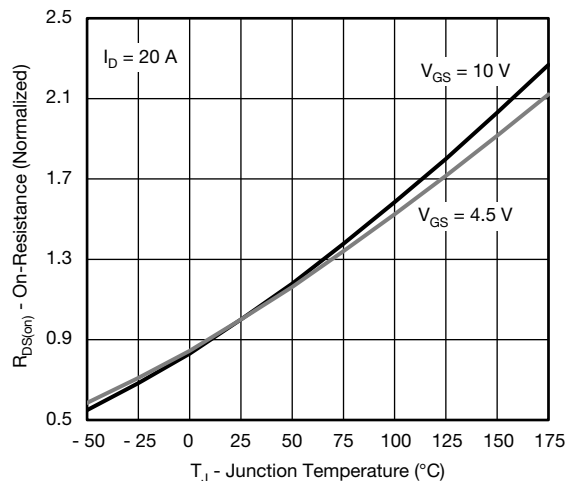
Capacitance



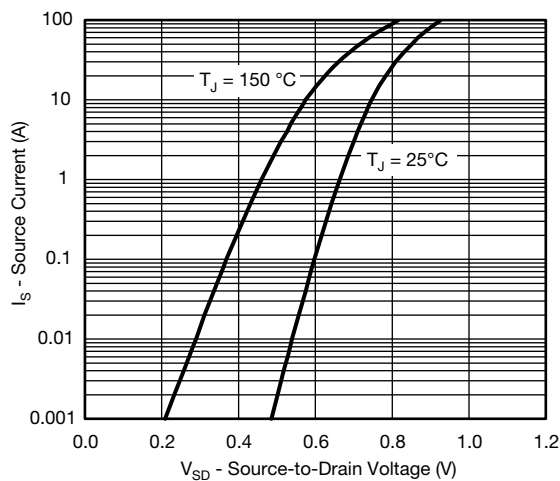
Gate Charge



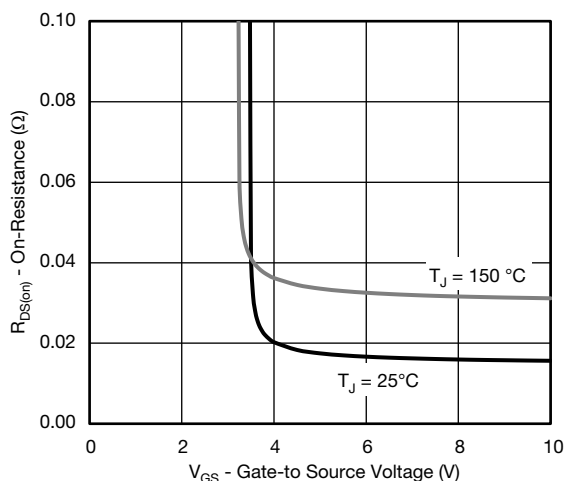
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



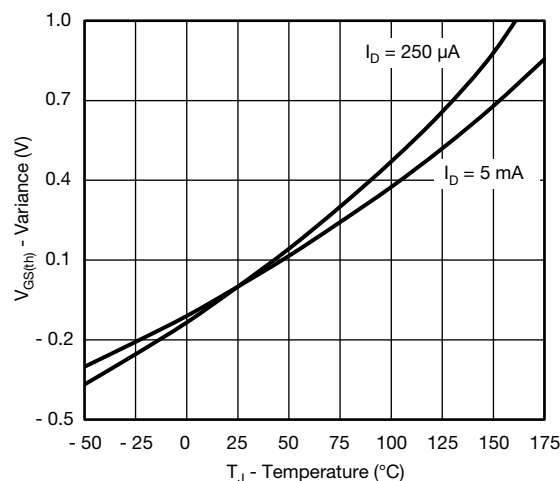
On-Resistance vs. Junction Temperature



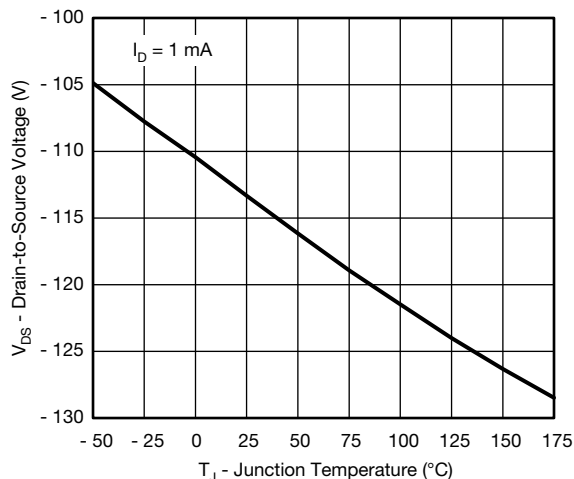
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



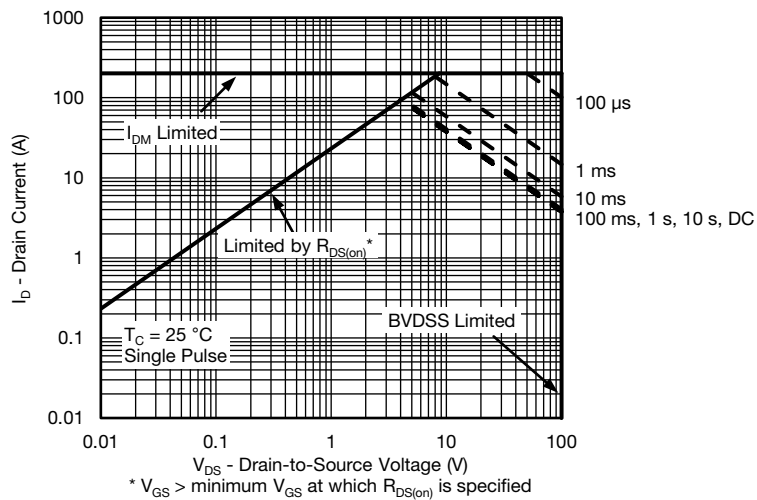
Threshold Voltage



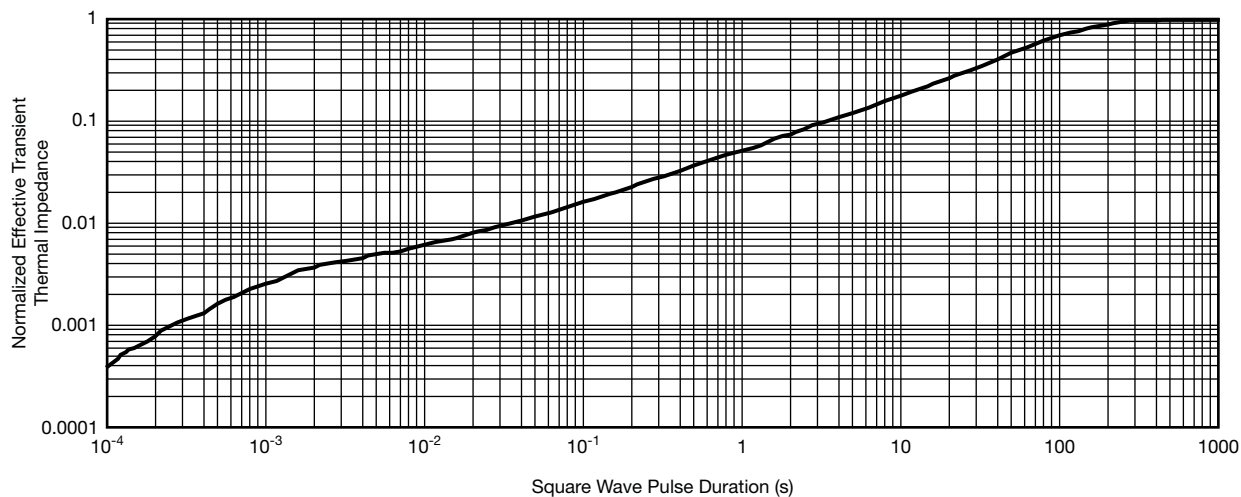
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



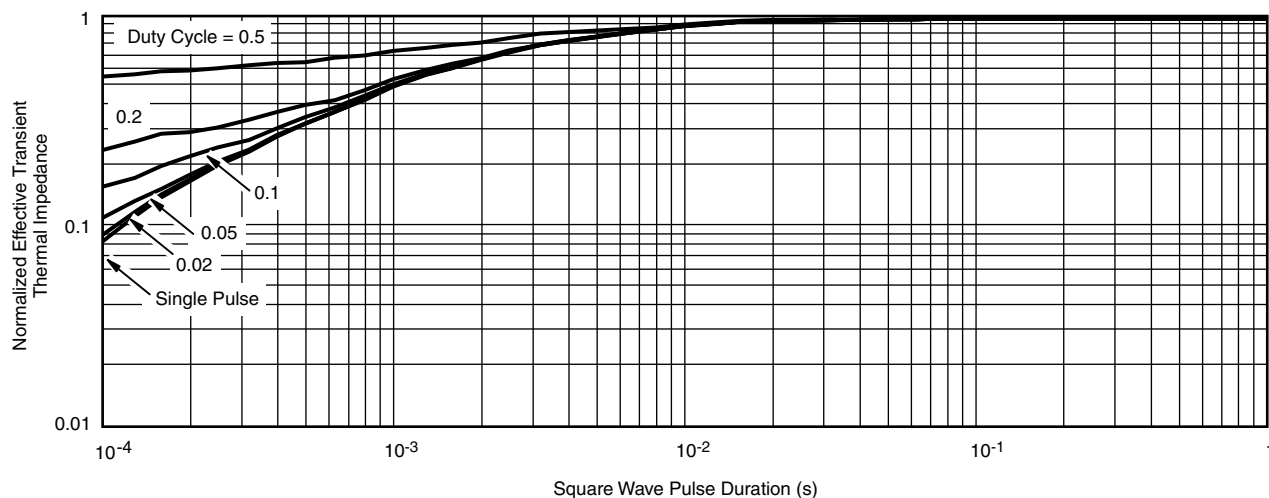
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

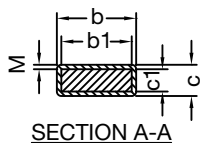
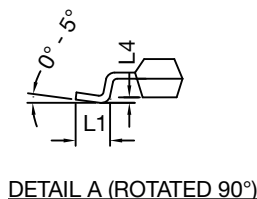
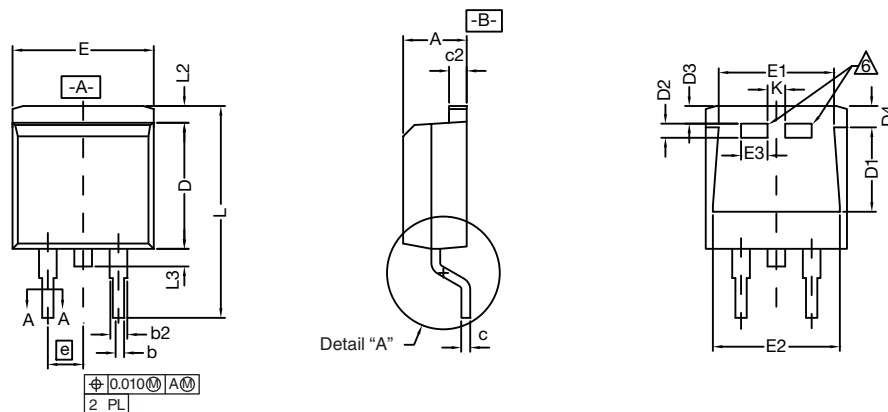
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75583.

TO-263 (D²PAK): 3-LEAD

VERSION 1: FACILITY CODE = T



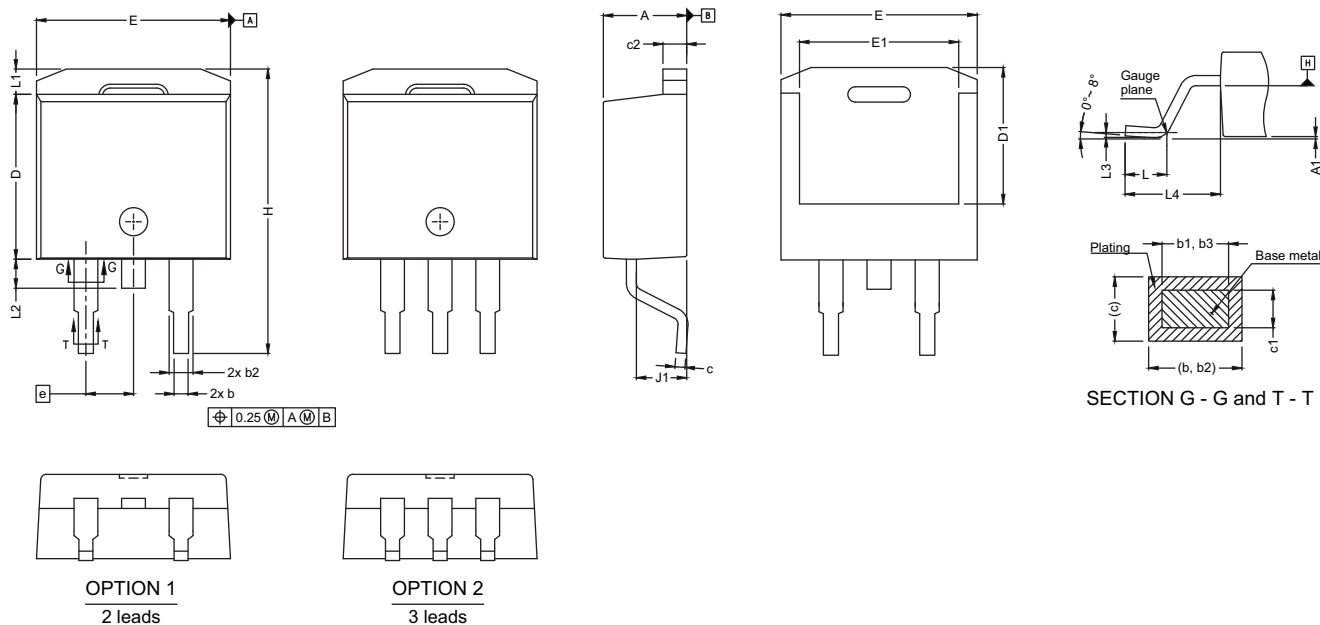
DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050

Notes

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
-  This feature is for thick lead.

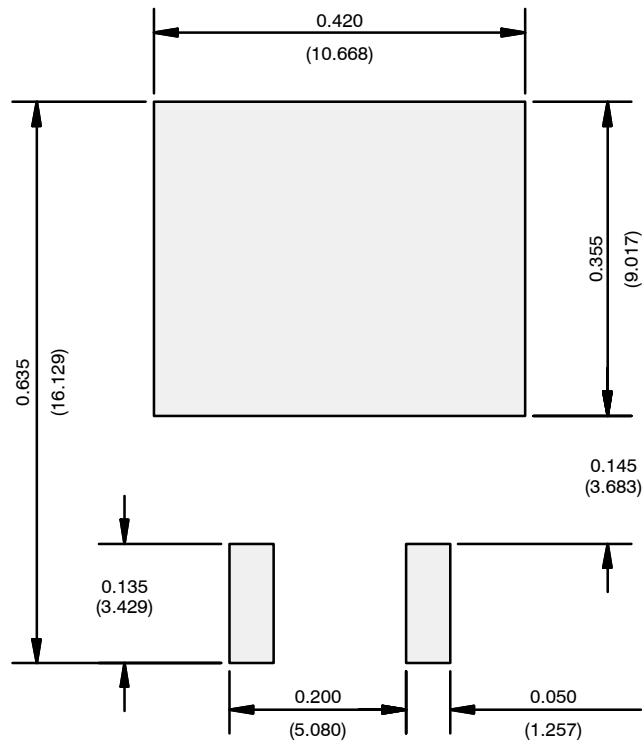


VERSION 2: FACILITY CODE = N



DIM.	MIN.	MAX.
A	4.36	4.56
A1	0	0.25
b	0.70	0.90
b1	0.51	0.89
b2	1.20	1.46
b3	1.17	1.37
c	0.38	0.694
c1	0.38	0.534
c2	1.19	1.34
D	8.60	9.00
D1	6.9	7.5
E	10.15	10.55
E1	8.1	8.7
e	2.54 BSC	
H	15.0	15.6
L	1.9	2.5
L1	-	1.65
L2	-	1.78
L3	0.25 typ.	
L4	4.78	5.28
J1	2.56	2.96
ECN: S24-1080-Rev. L, 28-Oct-2024		
DWG: 5843		

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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