

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: SQJ456EP-T1_GE3
Manufacturer: Vishay Siliconix
Package: Please confirm with sales
Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/vishay-siliconix/sqj456ep-t1-ge3.html>

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New & Original Components

Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

Secure sourcing support for OEM / EMS projects

Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

Automotive N-Channel 100 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

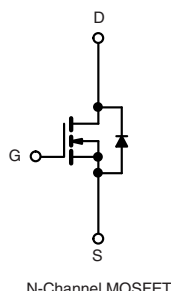
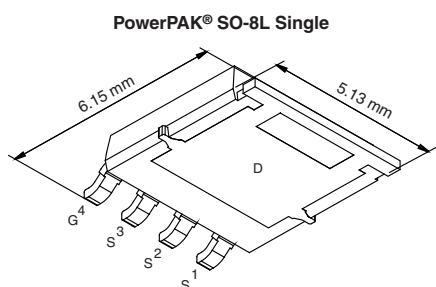
V_{DS} (V)	100
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.026
$R_{DS(on)}$ (Ω) at $V_{GS} = 6$ V	0.030
I_D (A)	32
Configuration	Single

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- AEC-Q101 Qualified^d
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE



ORDERING INFORMATION

Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ456EP-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C = 25$ °C ^a	32
		$T_C = 125$ °C	21
Continuous Source Current (Diode Conduction) ^a	I_S	32	A
Pulsed Drain Current ^b	I_{DM}	128	
Single Pulse Avalanche Current	I_{AS}	30	
Single Pulse Avalanche Energy	E_{AS}	45	
Maximum Power Dissipation ^b	P_D	$T_C = 25$ °C	83
		$T_C = 125$ °C	27
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature) ^{e, f}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	65	°C/W
Junction-to-Case (Drain)	R_{thJC}	1.8	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		100	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.5	3.0	3.5	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 100 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 100 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 100 V, T _J = 175 °C	-	-	150	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	30	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 9.3 A	-	0.021	0.026	Ω
		V _{GS} = 6 V	I _D = 8.8 A	-	0.024	0.030	
		V _{GS} = 10 V	I _D = 9.3 A, T _J = 125 °C	-	0.040	0.049	
		V _{GS} = 10 V	I _D = 9.3 A, T _J = 175 °C	-	0.051	0.063	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 9.3 A		-	36	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	2673	3342	pF
Output Capacitance	C _{oss}			-	292	365	
Reverse Transfer Capacitance	C _{rss}			-	106	133	
Total Gate Charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 15 V, I _D = 6 A	-	42	63	nC
Gate-Source Charge ^c	Q _{gs}			-	10	-	
Gate-Drain Charge ^c	Q _{gd}			-	7.6	-	
Gate Resistance	R _g	f = 1 MHz		0.31	1.72	3.12	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 6 Ω		-	14	21	ns
Rise Time ^c	t _r			-	12	18	
Turn-Off Delay Time ^c	t _{d(off)}			-	35	53	
Fall Time ^c	t _f			-	8	12	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	128	A
Forward Voltage	V _{SD}	I _F = 4.3 A, V _{GS} = 0		-	0.75	1.2	V

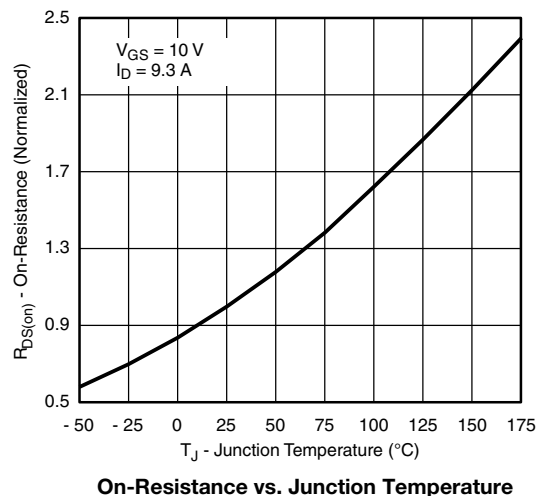
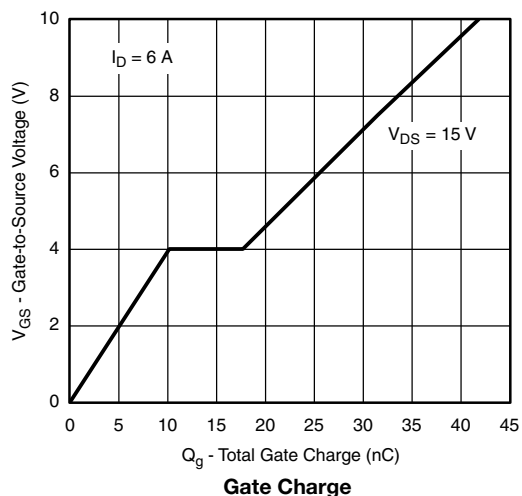
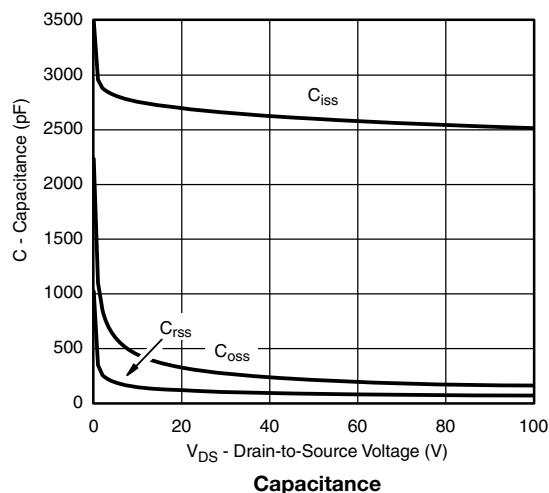
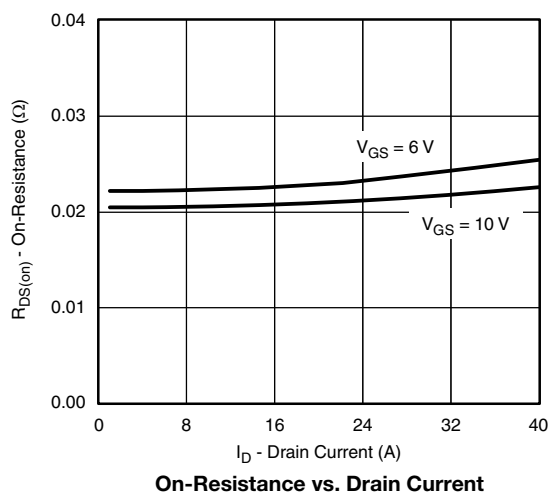
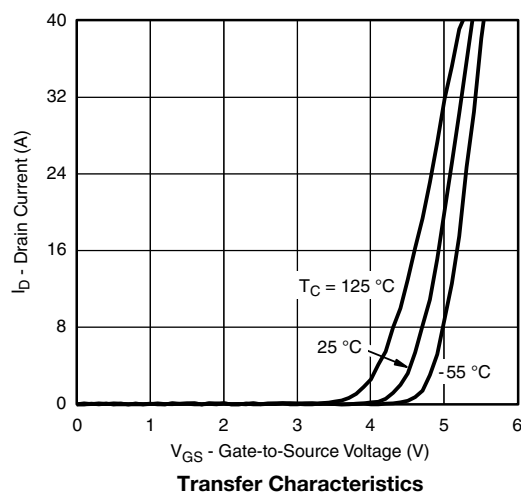
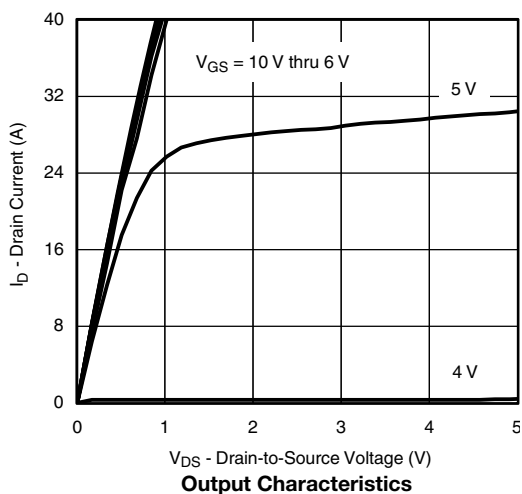
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

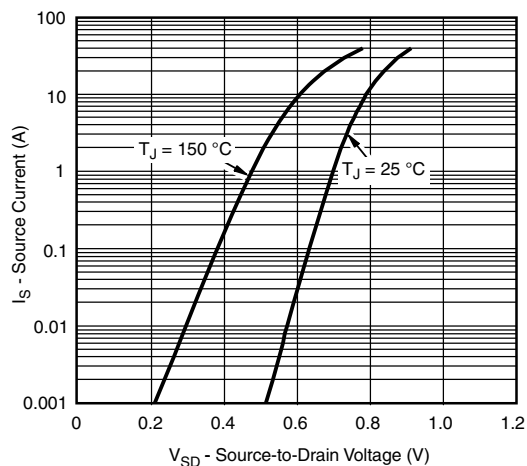


TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

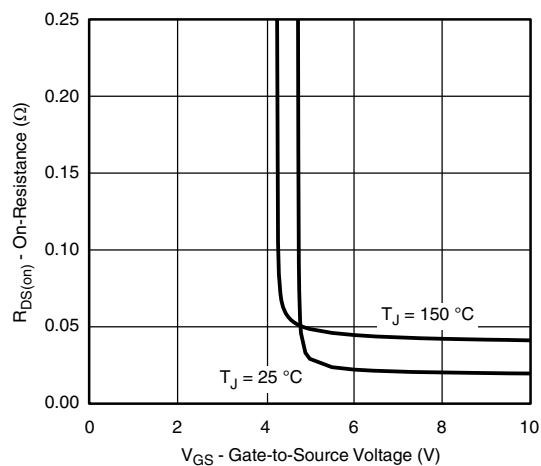




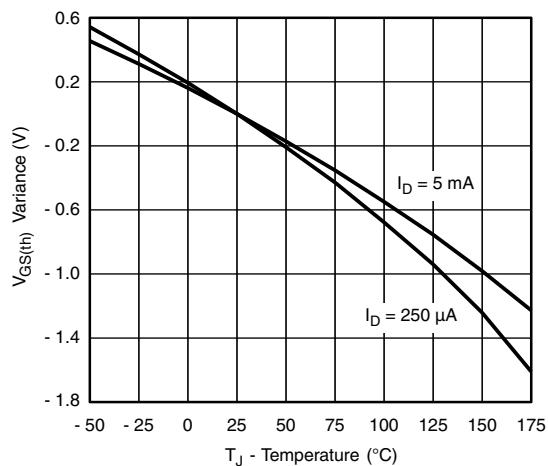
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



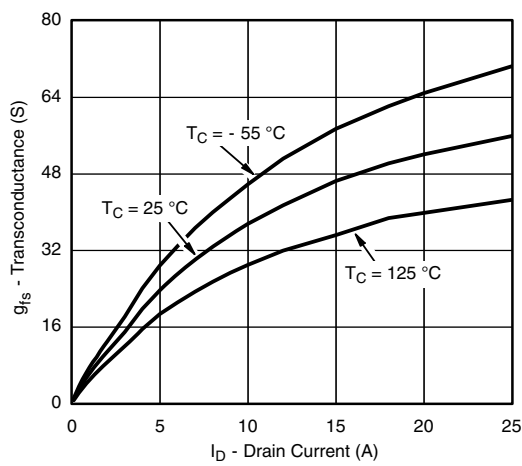
Source Drain Diode Forward Voltage



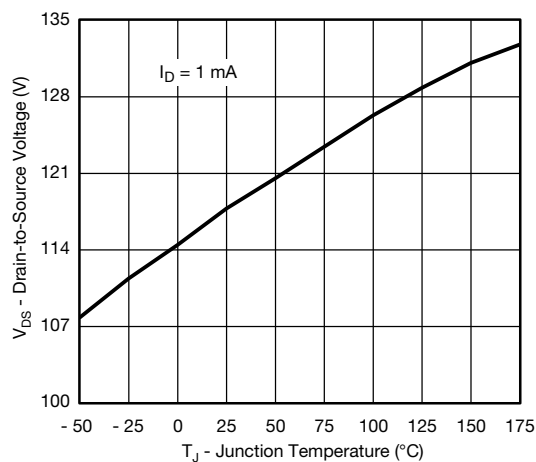
On-Resistance vs. Gate-to Source Voltage



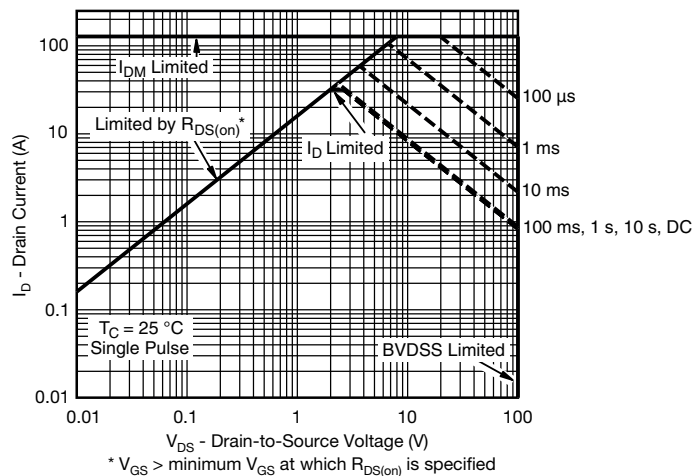
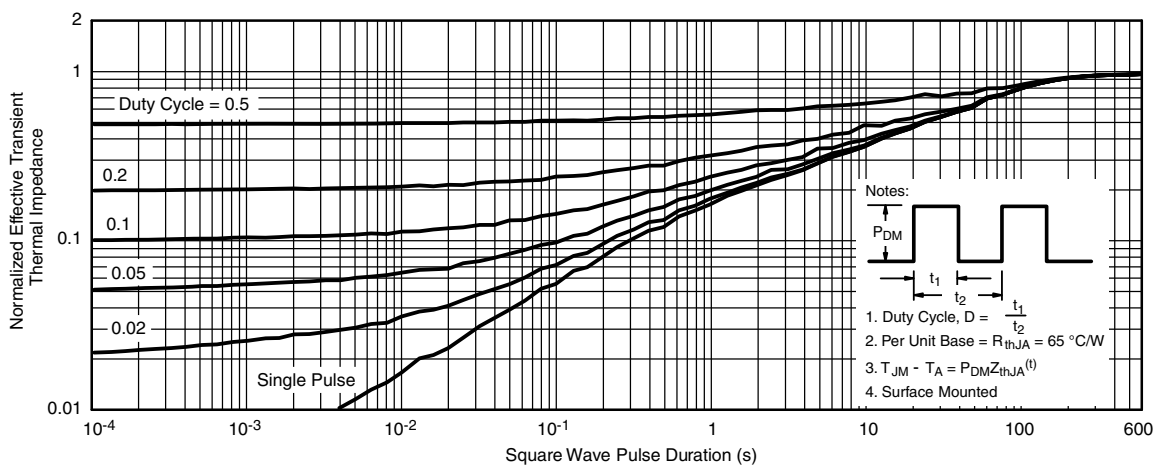
Threshold Voltage

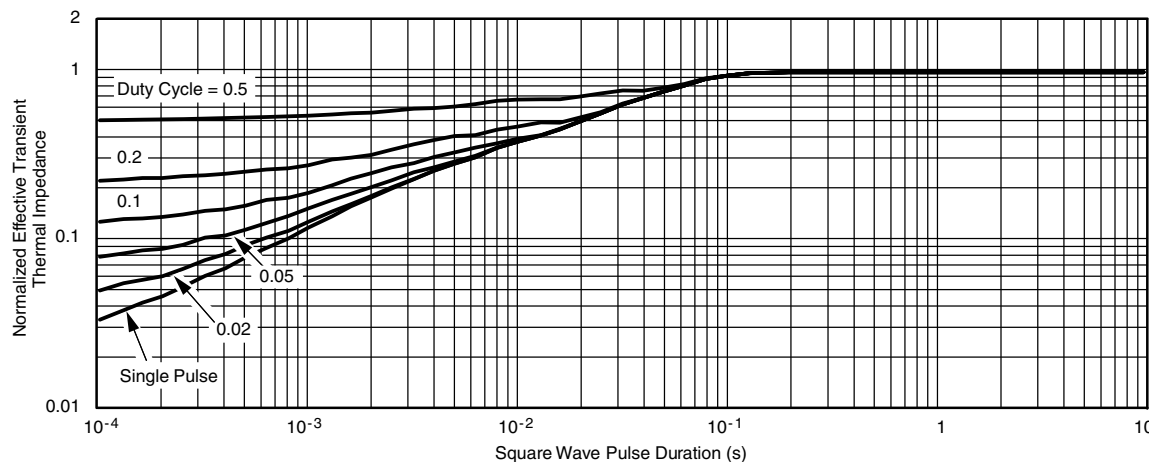


Transconductance



Drain Source Breakdown vs. Junction Temperature

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Safe Operating Area

Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)


Normalized Thermal Transient Impedance, Junction-to-Case

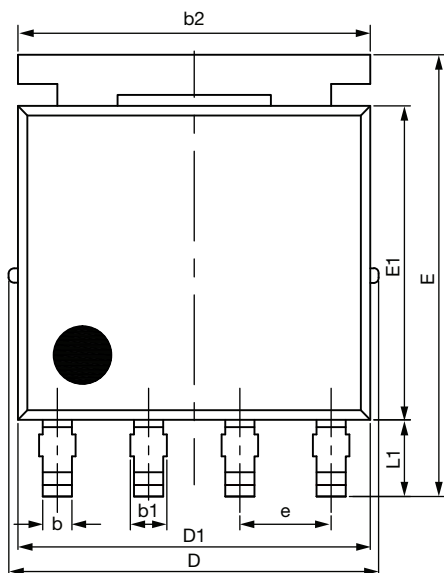
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)
 are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

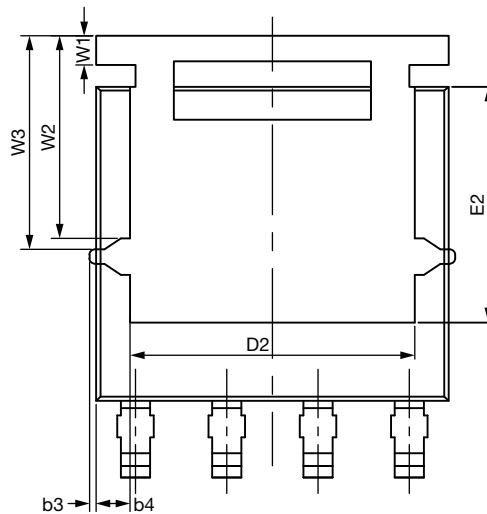
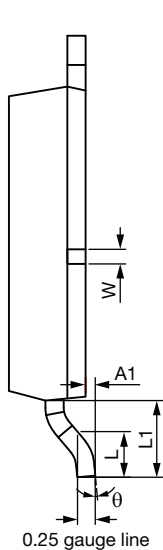
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65279.



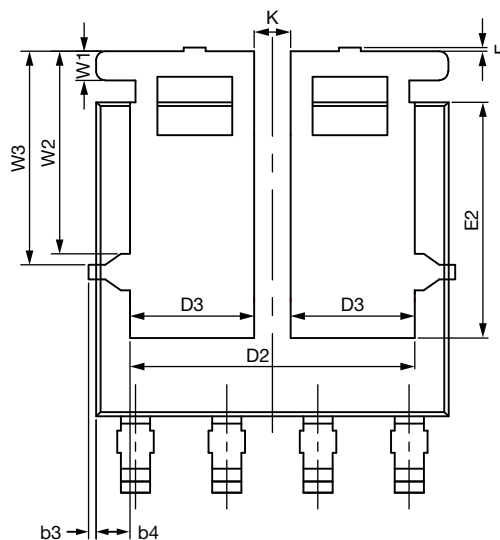
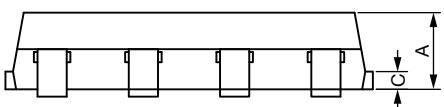
PowerPAK® SO-8L Case Outline 1



Topside view



Backside view (single)



Backside view (dual)



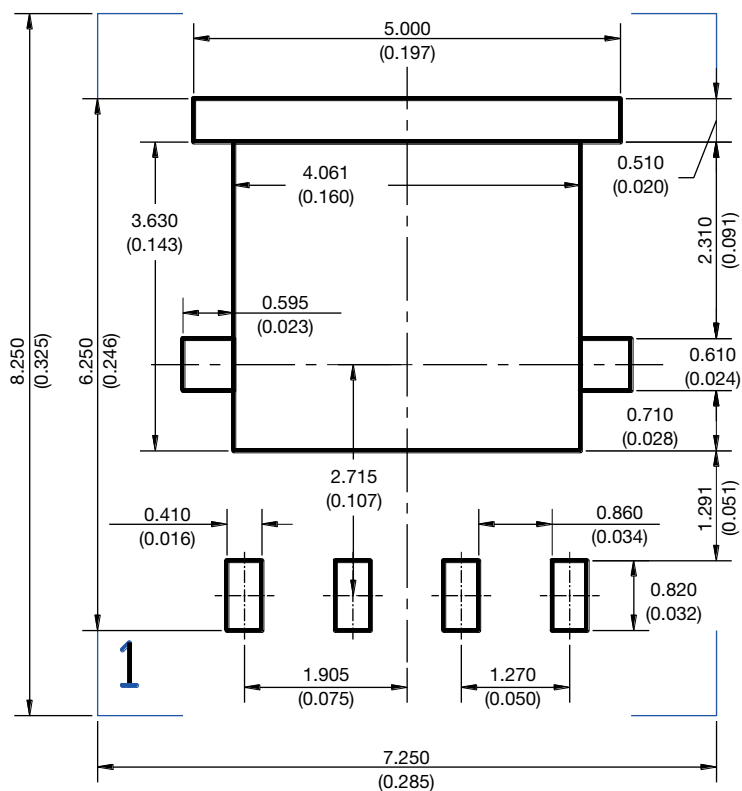
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	3.18	3.28	3.38	0.125	0.129	0.133
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°
ECN: S19-0643-Rev. E, 05-Aug-2019 DWG: 5976						

Note

- Millimeters will govern



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads
Dimensions in mm (inches)



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