

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	SQD50N04-5M6_GE3
Manufacturer:	Vishay Siliconix
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/vishay-siliconix/sqd50n04-5m6-ge3.html>

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Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

Secure sourcing support for OEM / EMS projects

Note:

This PDF includes an ANTREX product reference cover page.

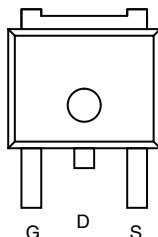
The original manufacturer datasheet follows from the next page.

Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.0056
I_D (A)	50
Configuration	Single

TO-252



Drain Connected to Tab

Top View

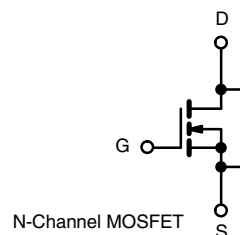
FEATURES

- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- AEC-Q101 Qualified
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE
GRADE



RoHS
COMPLIANT
HALOGEN
FREE



N-Channel MOSFET

ORDERING INFORMATION

Package	TO-252
Lead (Pb)-free and Halogen-free	SQD50N04-5m6-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	50	A
		45	
Continuous Source Current (Diode Conduction) ^a	I_S	50	
Pulsed Drain Current ^b	I_{DM}	200	
Single Pulse Avalanche Current	I_{AS}	40	
Single Pulse Avalanche Energy	E_{AS}	80	mJ
Maximum Power Dissipation ^b	P_D	71	W
		23	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	50	°C/W
Junction-to-Case (Drain)	R_{thJC}	2.1	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR-4 material).



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		40	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.5	-	3.5	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	150	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	50	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 20 A	-	0.0046	0.0056	Ω
		V _{GS} = 10 V	I _D = 20 A, T _J = 125 °C	-	-	0.0100	
		V _{GS} = 10 V	I _D = 20 A, T _J = 175 °C	-	-	0.0120	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 15 A		-	80	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	3040	4000	pF
Output Capacitance	C _{oss}			-	370	475	
Reverse Transfer Capacitance	C _{rss}			-	160	210	
Total Gate Charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 20 V, I _D = 50 A	-	55	85	nC
Gate-Source Charge ^c	Q _{gs}			-	11	-	
Gate-Drain Charge ^c	Q _{gd}			-	16	-	
Gate Resistance	R _g	f = 1 MHz		0.5	3	4.5	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 20 V, R _L = 0.4 Ω I _D ≅ 50 A, V _{GEN} = 10 V, R _g = 1 Ω		-	9	16	ns
Rise Time ^c	t _r			-	19	30	
Turn-Off Delay Time ^c	t _{d(off)}			-	13	21	
Fall Time ^c	t _f			-	5	10	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	200	A
Forward Voltage	V _{SD}	I _F = 30 A, V _{GS} = 0 V		-	0.85	1.5	V

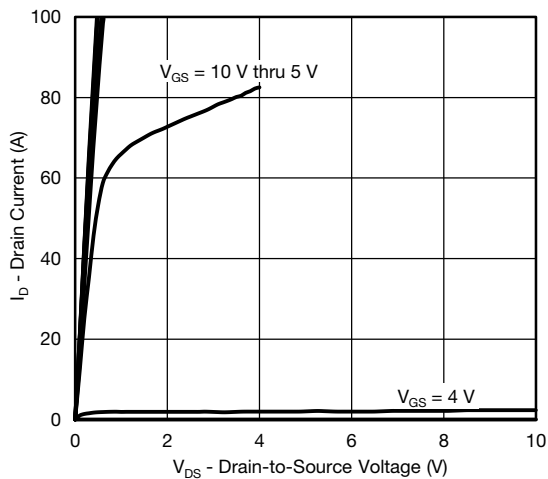
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

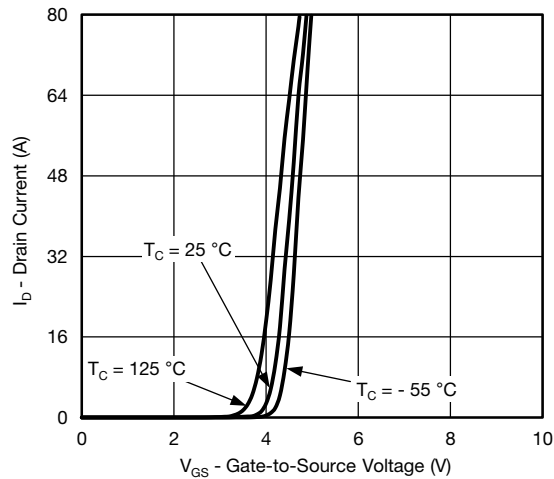
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



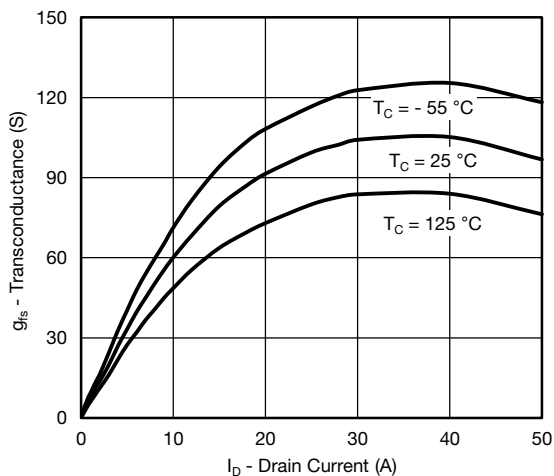
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



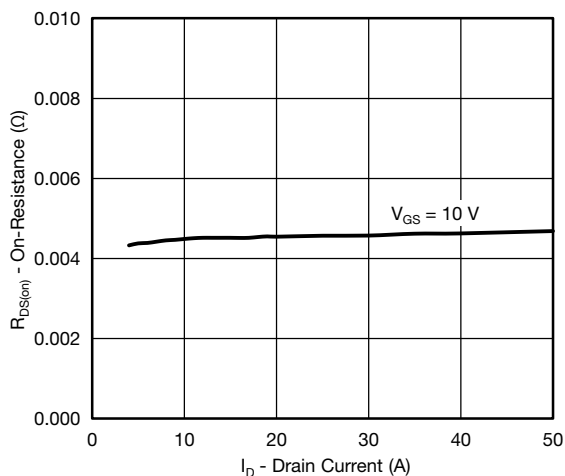
Output Characteristics



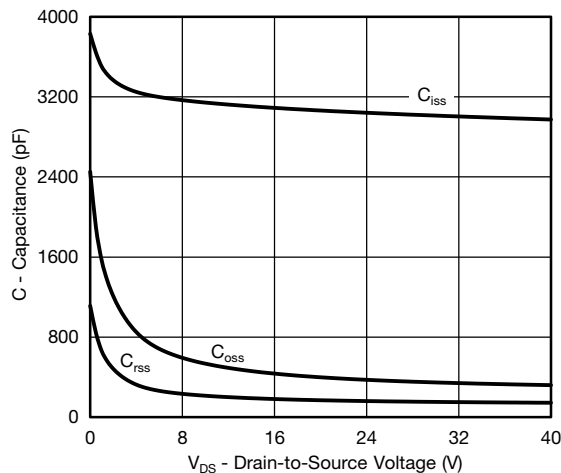
Transfer Characteristics



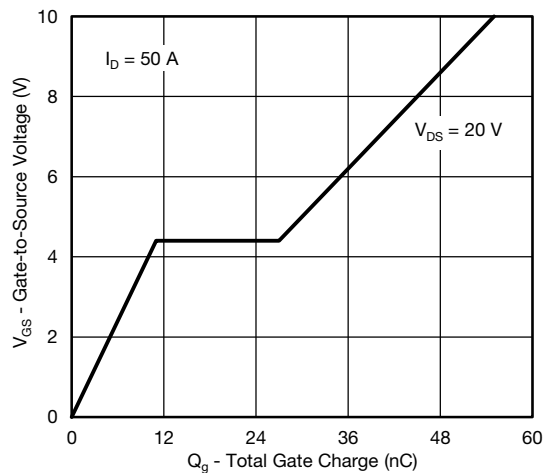
Transconductance



On-Resistance vs. Drain Current



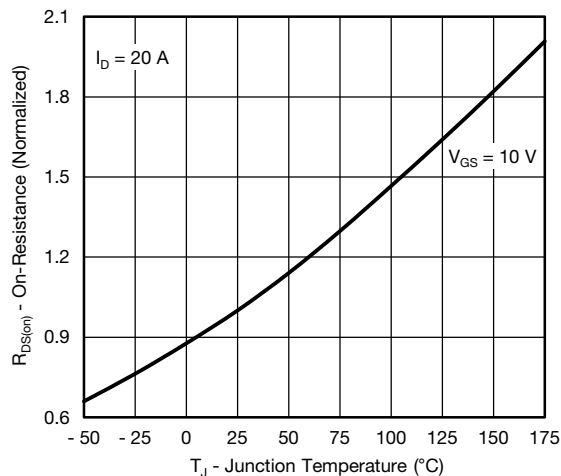
Capacitance



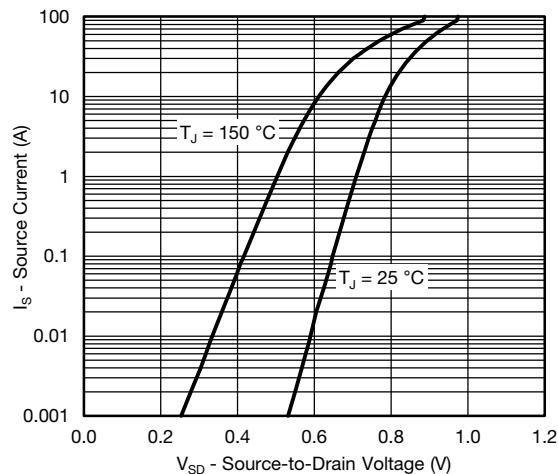
Gate Charge



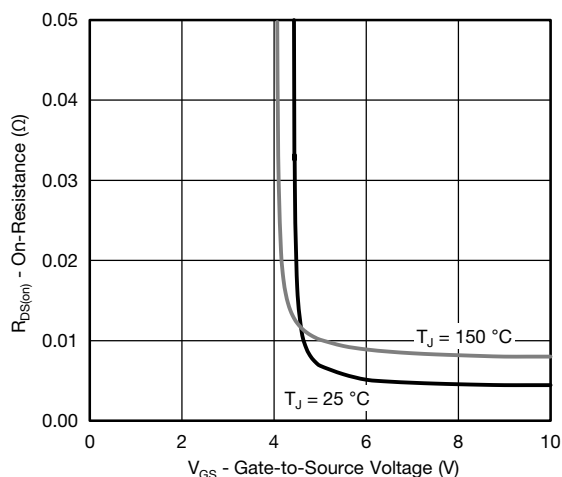
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



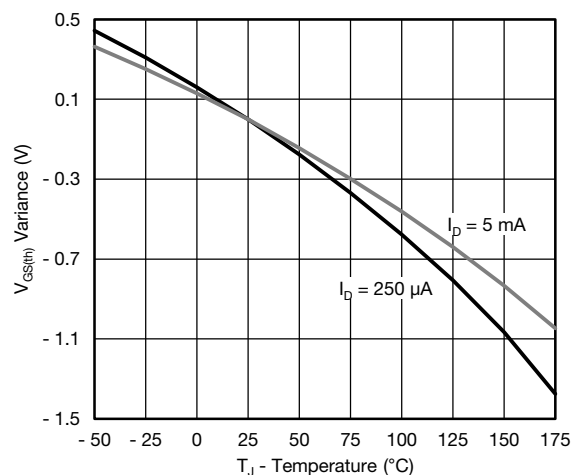
On-Resistance vs. Junction Temperature



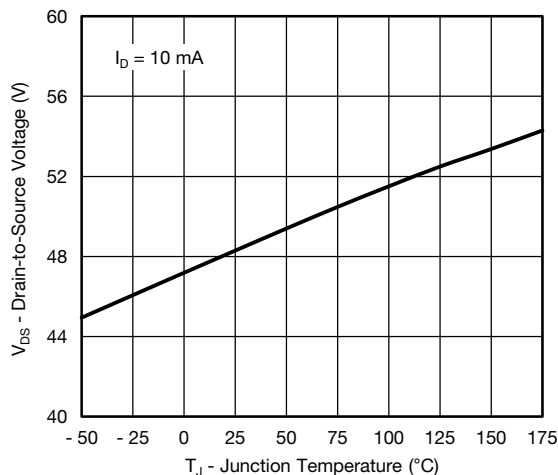
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



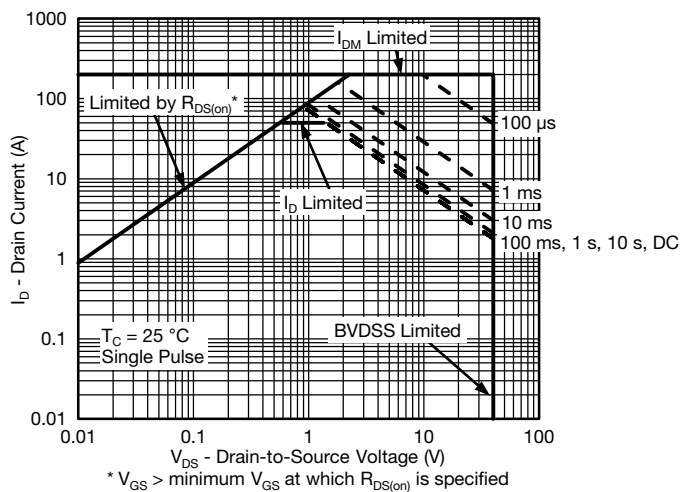
Threshold Voltage



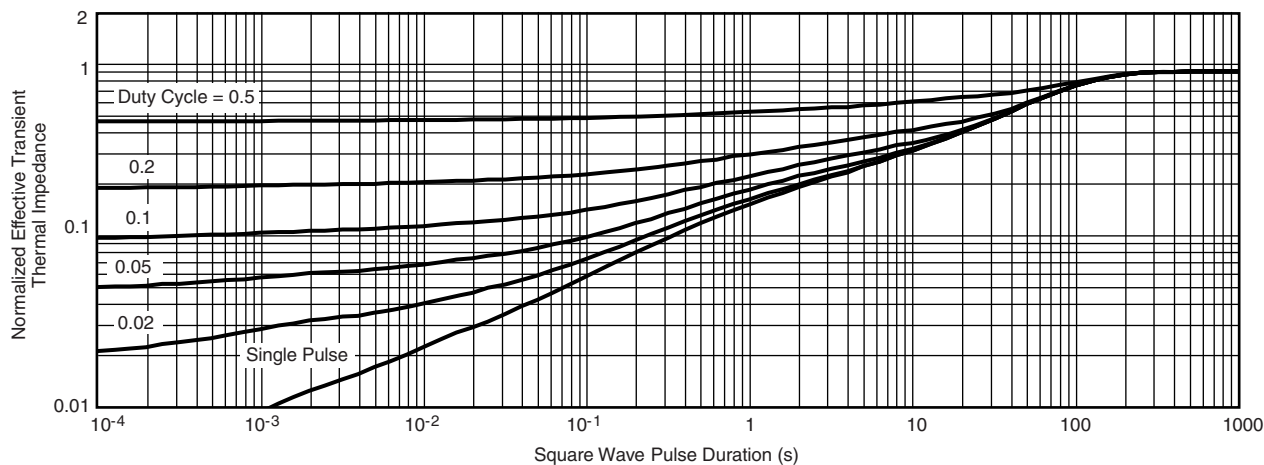
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



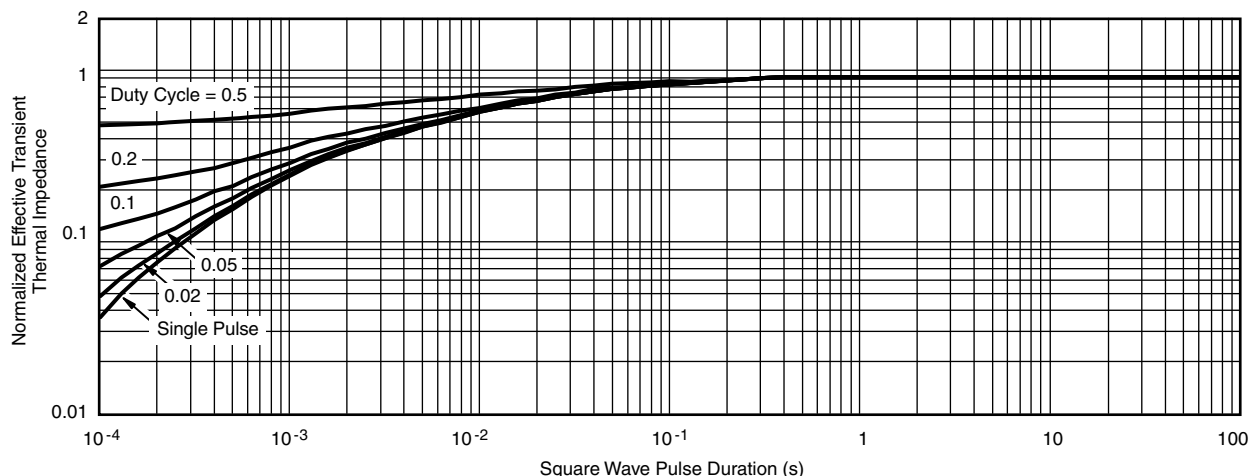
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



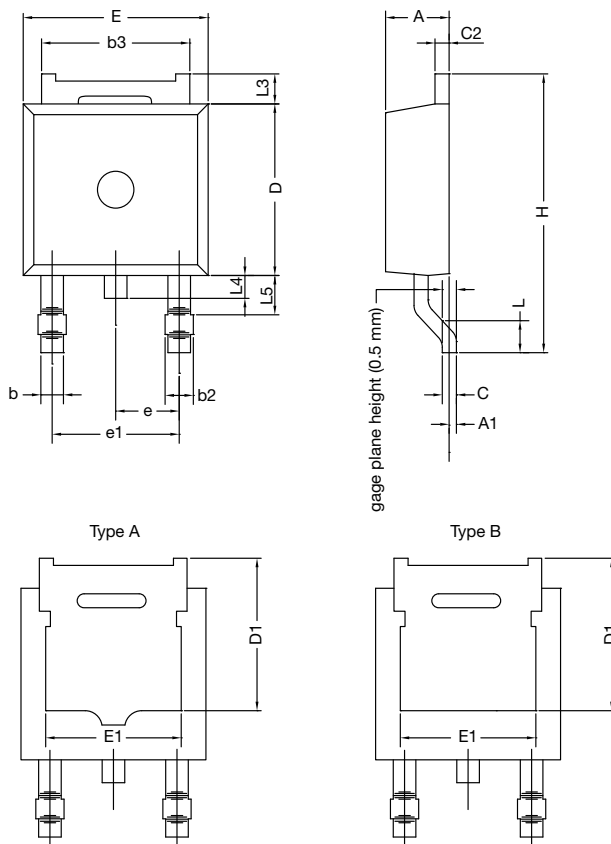
Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62666.

TO-252AA Case Outline



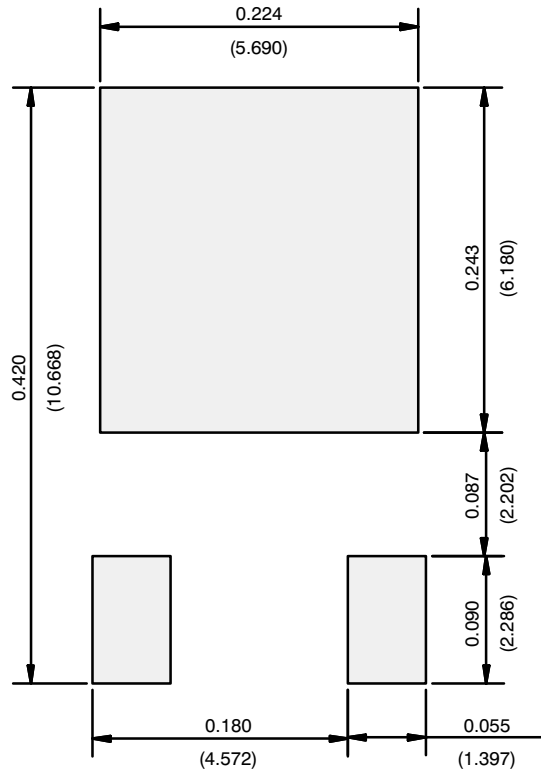
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T25-0122-Rev. C, 12-May-2025
DWG: 6019

Notes

- Dimension L3 is for reference only
- Dimension D1 and E1 on type A and B is the same

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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