

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: SQD15N06-42L_GE3

Manufacturer: Vishay Siliconix

Package: Please confirm with sales

Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/vishay-siliconix/sqd15n06-42l-ge3.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

Automotive N-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY ^d

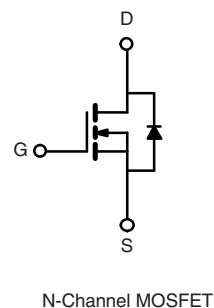
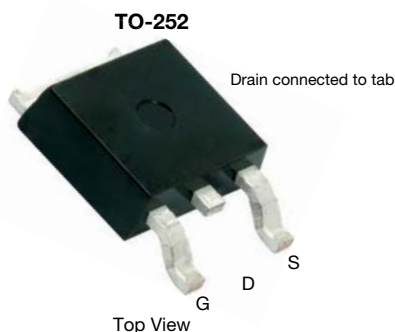
V _{DS} (V)	60
R _{DS(on)} (Ω) at V _{GS} = 10 V	0.042
R _{DS(on)} (Ω) at V _{GS} = 4.5 V	0.060
I _D (A)	15
Configuration	Single
Package	TO-252

FEATURES

- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- AEC-Q101 qualified
- Package with low thermal resistance
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V _{DS}	60	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current	T _C = 25 °C ^a	I _D	15	A
	T _C = 125 °C		10	
Continuous Source Current (Diode Conduction) ^a		I _S	15	
Pulsed Drain Current ^b		I _{DM}	50	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	18	
Single Pulse Avalanche Energy		E _{AS}	16.2	mJ
Maximum Power Dissipation ^b	T _C = 25 °C	P _D	37	W
	T _C = 125 °C		11	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R _{thJA}	50	°C/W
Junction-to-Case (Drain)	R _{thJC}	4	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		60	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.5	2	2.5	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 60 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 60 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 60 V, T _J = 175 °C	-	-	150	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	30	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A	-	0.036	0.042	Ω
		V _{GS} = 10 V	I _D = 10 A, T _J = 125 °C	-	-	0.075	
		V _{GS} = 10 V	I _D = 10 A, T _J = 175 °C	-	-	0.090	
		V _{GS} = 4.5 V	I _D = 10 A, T _J = 125 °C	-	0.092	-	
		V _{GS} = 4.5 V	I _D = 10 A, T _J = 175 °C	-	0.110	-	
		V _{GS} = 4.5 V	I _D = 10 A	-	0.048	0.060	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 6 A		-	11	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	425	535	pF
Output Capacitance	C _{oss}			-	95	120	
Reverse Transfer Capacitance	C _{rss}			-	40	50	
Total Gate Charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 30 V, I _D = 15 A	-	9.5	15	nC
Gate-Source Charge ^c	Q _{gs}			-	1.7	-	
Gate-Drain Charge ^c	Q _{gd}			-	2.5	-	
Gate Resistance	R _g	f = 1 MHz		1.2	2.5	5.4	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 30 V, R _L = 2 Ω I _D ≡ 15 A, V _{GEN} = 10 V, R _g = 1 Ω		-	5	8	ns
Rise Time ^c	t _r			-	10	15	
Turn-Off Delay Time ^c	t _{d(off)}			-	13	20	
Fall Time ^c	t _f			-	8	12	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	50	A
Forward Voltage	V _{SD}	I _F = 10 A, V _{GS} = 0 V		-	0.9	1.2	V
Reverse Recovery Time	t _{rr}	I _F = 15 A, dI/dt = 100 A/μs		-	29	60	ns

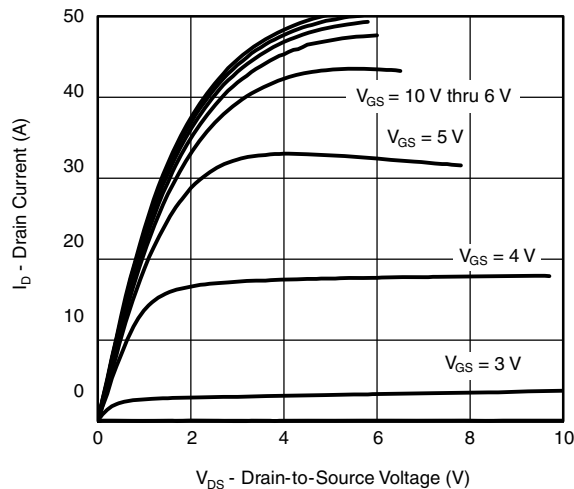
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

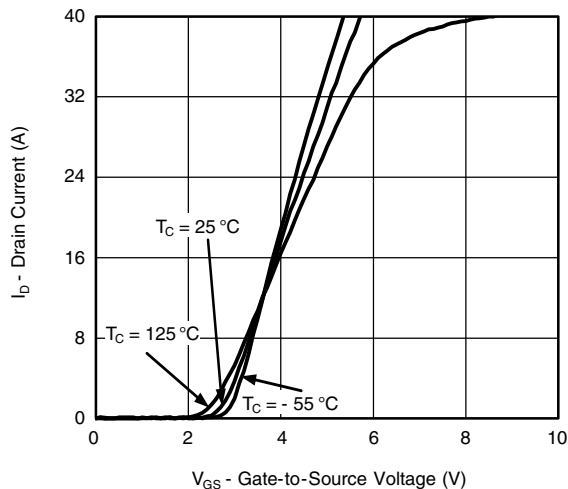
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



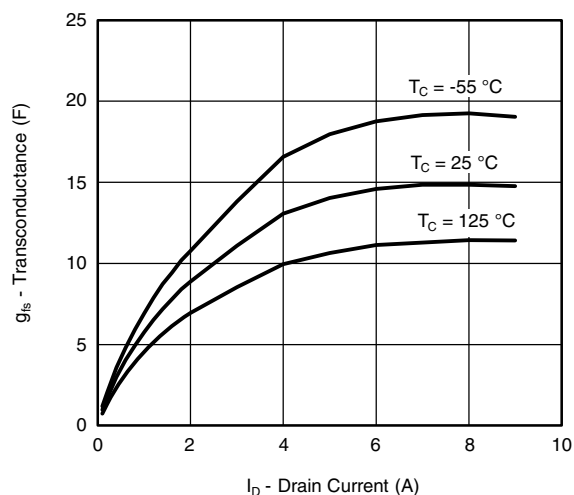
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



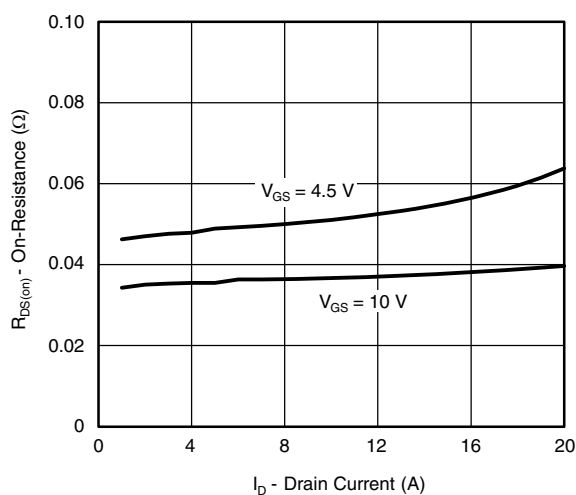
Output Characteristics



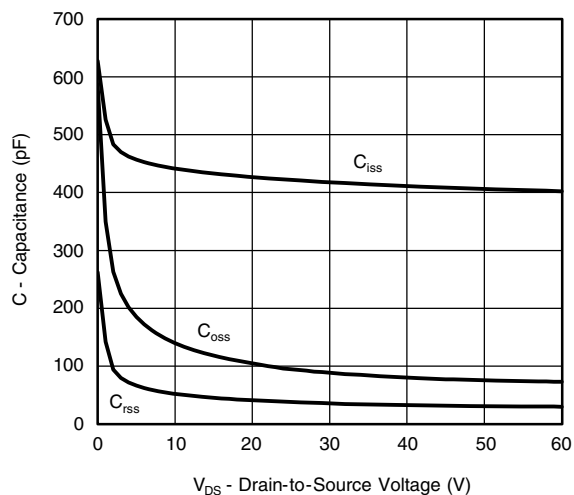
Transfer Characteristics



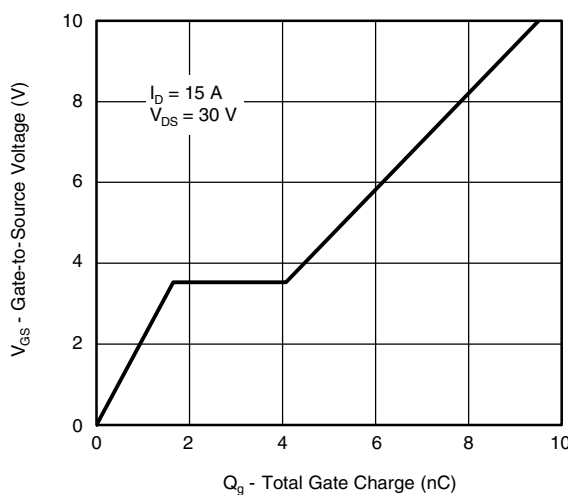
Transconductance



On-Resistance vs. Drain Current



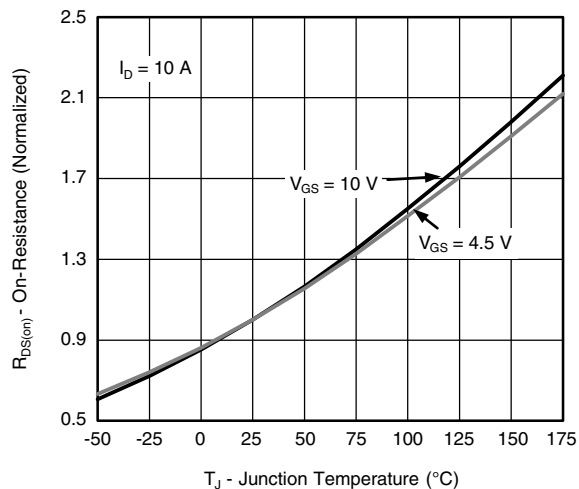
Capacitance



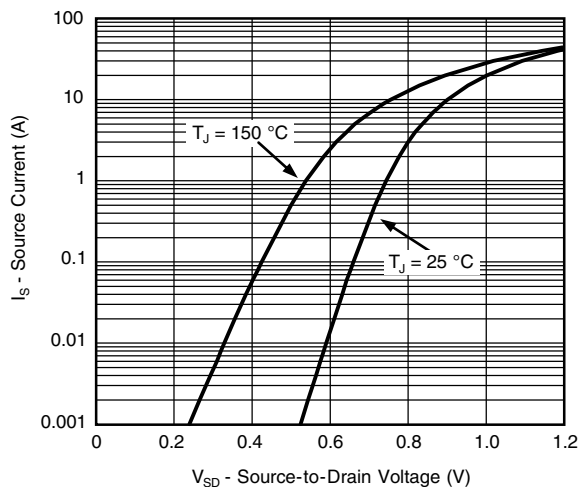
Gate Charge



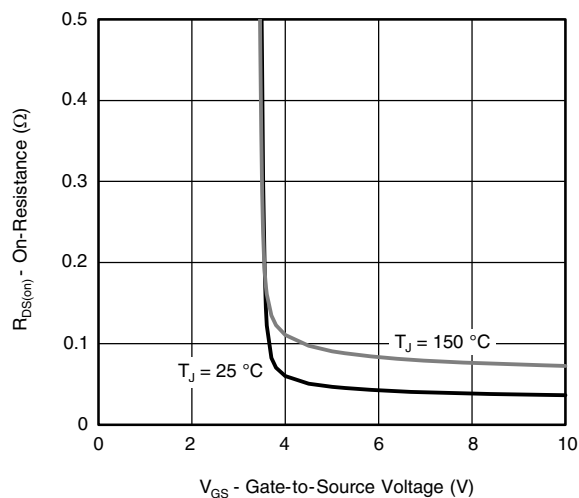
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



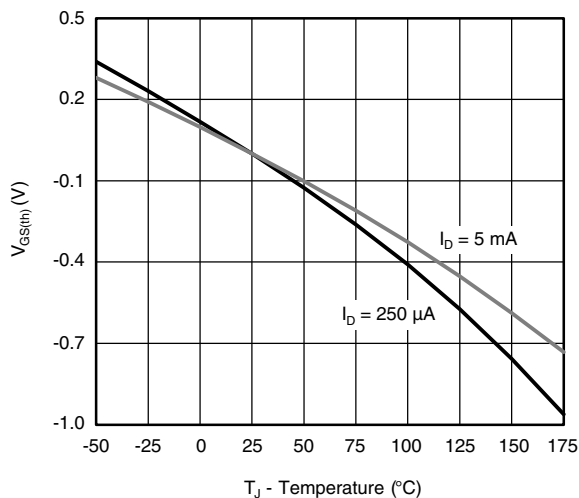
On-Resistance vs. Junction Temperature



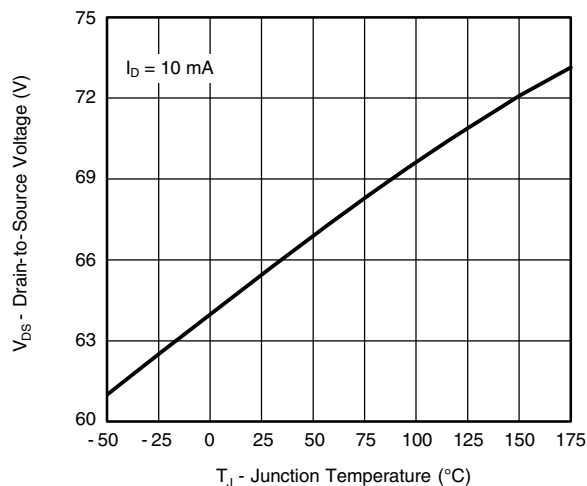
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



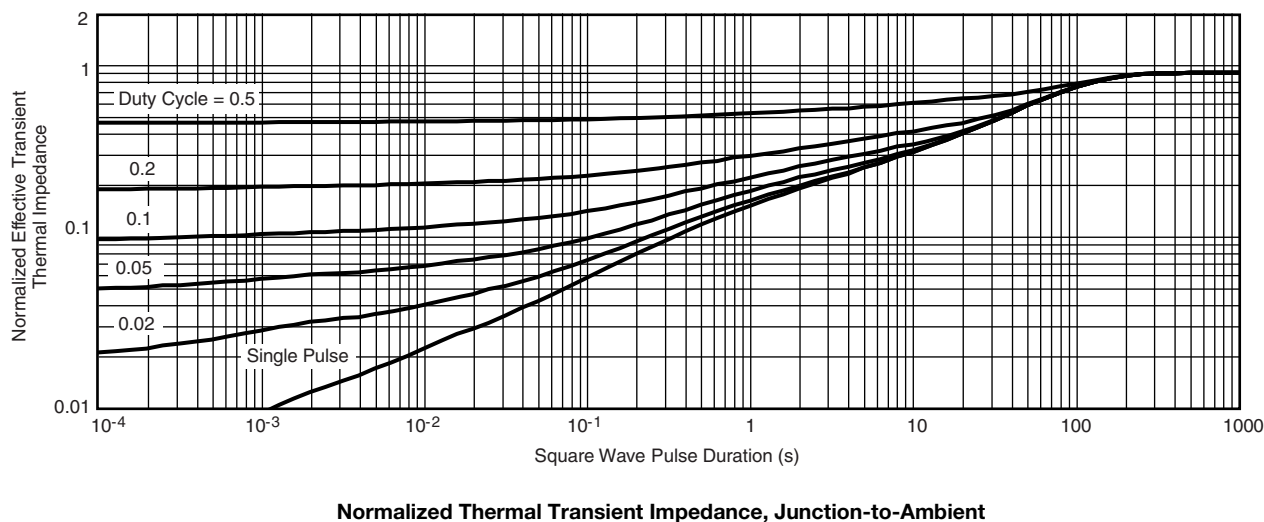
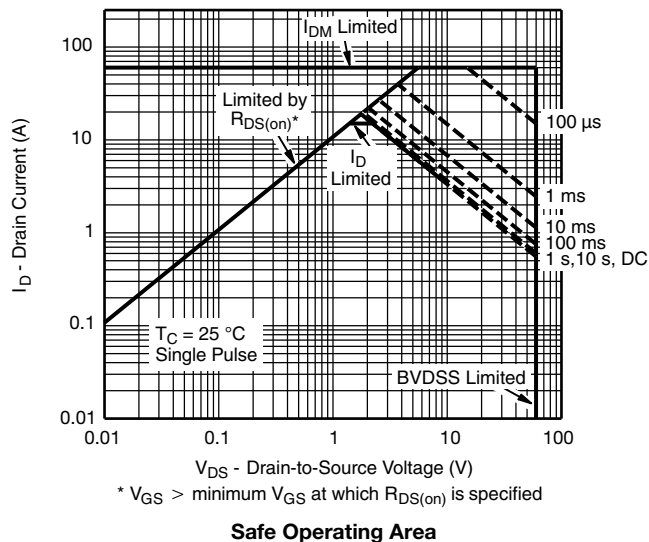
Threshold Voltage



On-Resistance vs. Junction Temperature

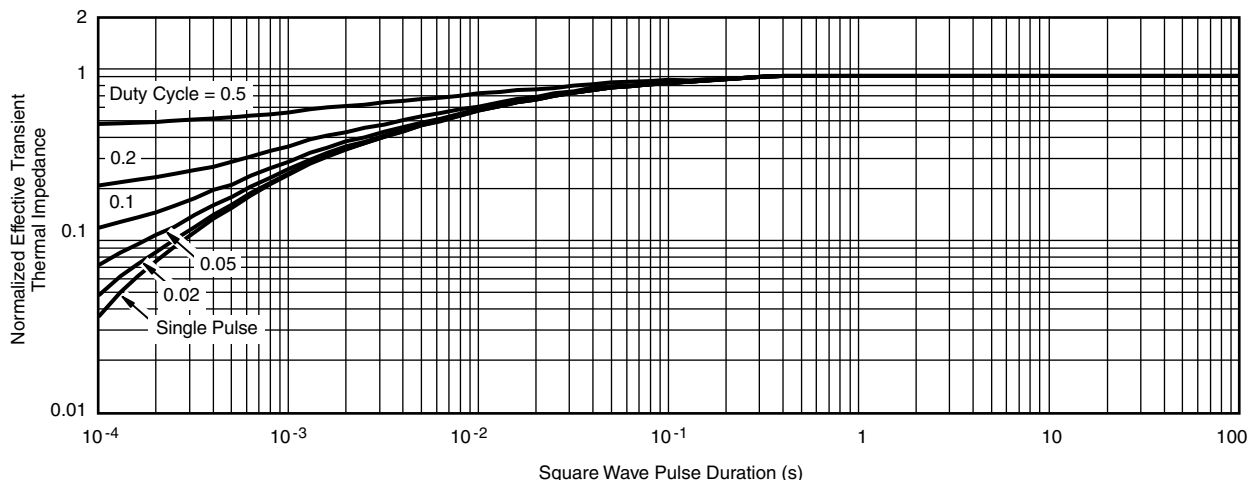


THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)





THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68880.

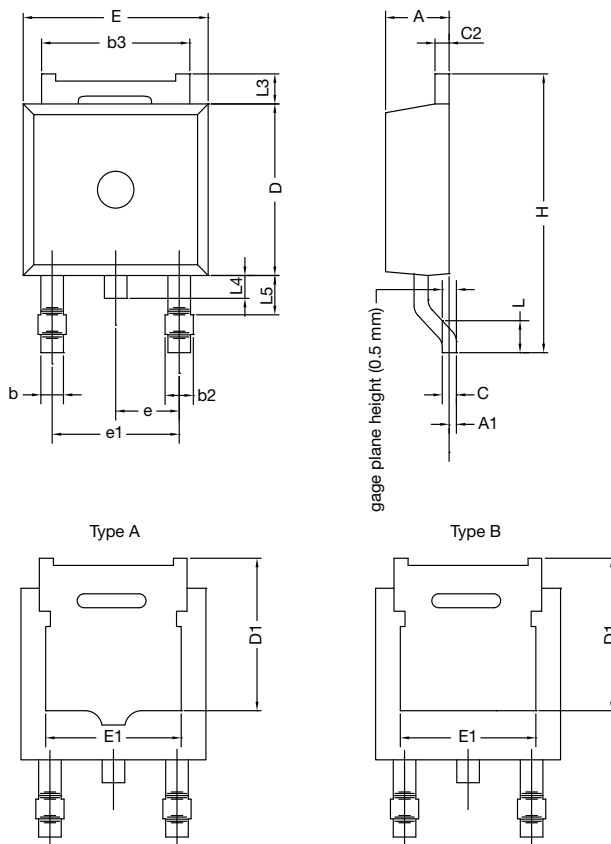


REVISION HISTORY ^a		
REVISION	DATE	DESCRIPTION OF CHANGE
G	04-Aug-15	• Revised R _g minimum limit

Note

a. As of April 2014

TO-252AA Case Outline



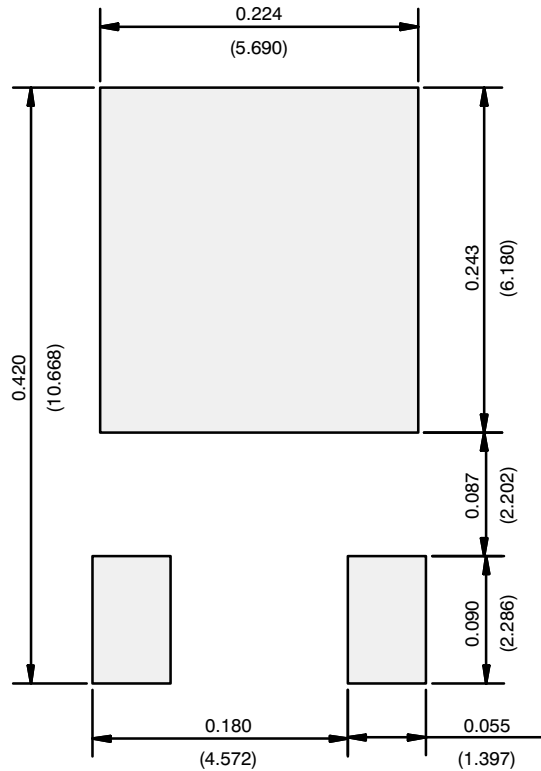
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T25-0122-Rev. C, 12-May-2025
DWG: 6019

Notes

- Dimension L3 is for reference only
- Dimension D1 and E1 on type A and B is the same

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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