

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: SQD10N30-330H_4GE3

Manufacturer: Vishay Siliconix

Package: Please confirm with sales

Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/vishay-siliconix/sqd10n30-330h-4ge3.html>

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New & Original Components

Supplier verification and packaging condition review

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

Automotive N-Channel 300 V (D-S) 175 °C MOSFET

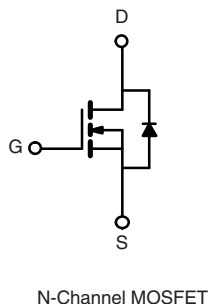
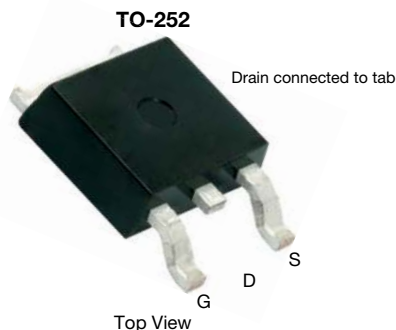


RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY	
V_{DS} (V)	300
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.330
I_D (A)	10
Configuration	Single

FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- AEC-Q101 qualified ^d
- 100 % R_g tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



ORDERING INFORMATION	
Package	TO-252
Lead (Pb)-free and Halogen-free	SQD10N30-330H-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	300	V
Gate-Source Voltage		V_{GS}	± 30	
Continuous Drain Current	$T_C = 25$ °C	I_D	10	A
	$T_C = 125$ °C		5	
Continuous Source Current (Diode Conduction) ^a		I_S	50	
Pulsed Drain Current ^b		I_{DM}	16	
Single Pulse Avalanche Current ^e	L = 0.05 mH	I_{AS}	12.65	
Single Pulse Avalanche Energy ^e		E_{AS}	4	mJ
Maximum Power Dissipation ^b	$T_C = 25$ °C	P_D	107	W
	$T_C = 125$ °C		35	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount ^c	R_{thJA}	50	°C/W
Junction-to-Case (Drain)		R_{thJC}	1.4	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.
- 1.5 k Ω resistance in series with the gate.



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		300	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.4	3.8	4.4	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 300 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 300 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 300 V, T _J = 175 °C	-	-	250	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	10	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 14 A	-	0.275	0.330	Ω
		V _{GS} = 10 V	I _D = 14 A, T _J = 125 °C	-	-	0.733	
		V _{GS} = 10 V	I _D = 14 A, T _J = 175 °C	-	-	1.000	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 14 A		-	26	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	1749	2190	pF
Output Capacitance	C _{oss}			-	112	140	
Reverse Transfer Capacitance	C _{rss}			-	44	55	
Total Gate Charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 150 V, I _D = 7 A	-	31	47	nC
Gate-Source Charge ^c	Q _{gs}			-	8	-	
Gate-Drain Charge ^c	Q _{gd}			-	9.6	-	
Gate Resistance	R _g	f = 1 MHz		0.4	0.8	3	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 150 V, R _L = 21 Ω I _D ≅ 7 A, V _{GEN} = 10 V, R _g = 1 Ω		-	10	15	ns
Rise Time ^c	t _r			-	18	28	
Turn-Off Delay Time ^c	t _{d(off)}			-	20	30	
Fall Time ^c	t _f			-	8	12	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	16	A
Forward Voltage	V _{SD}	I _F = 25 A, V _{GS} = 0 V		-	0.9	1.5	V

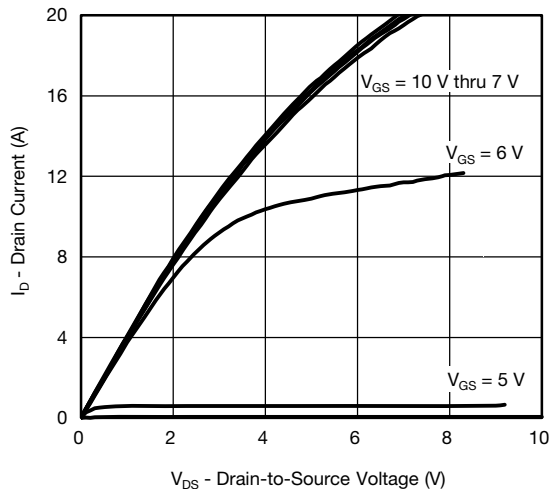
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

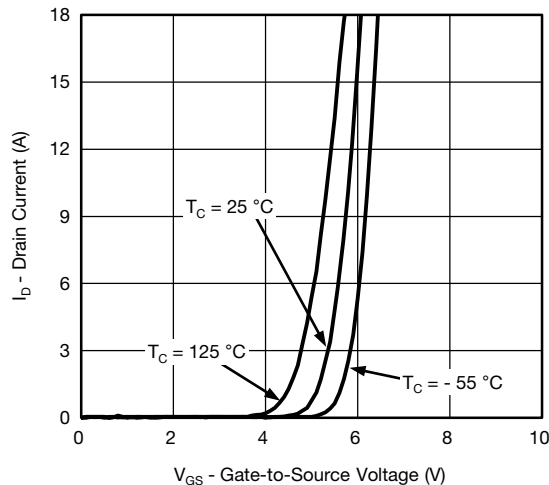
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



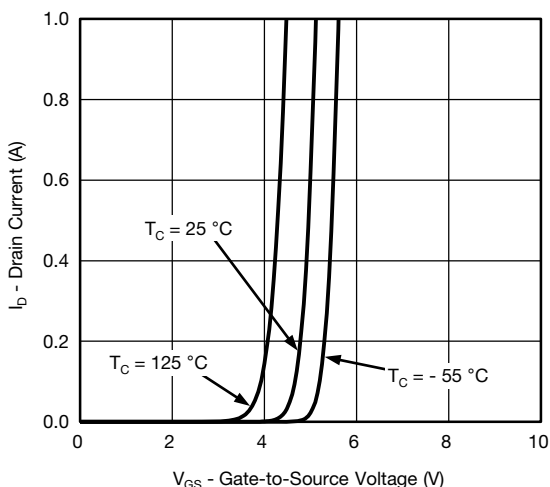
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



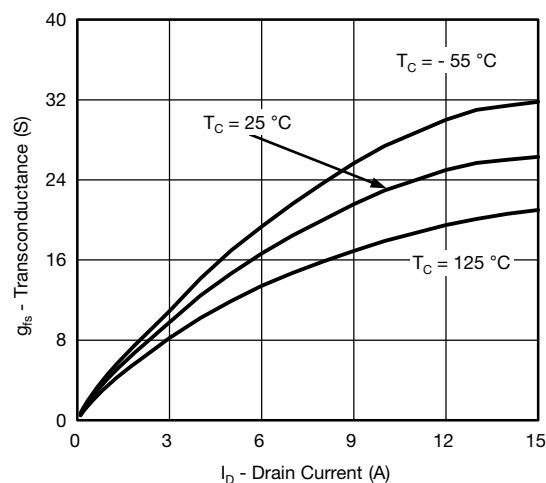
Output Characteristics



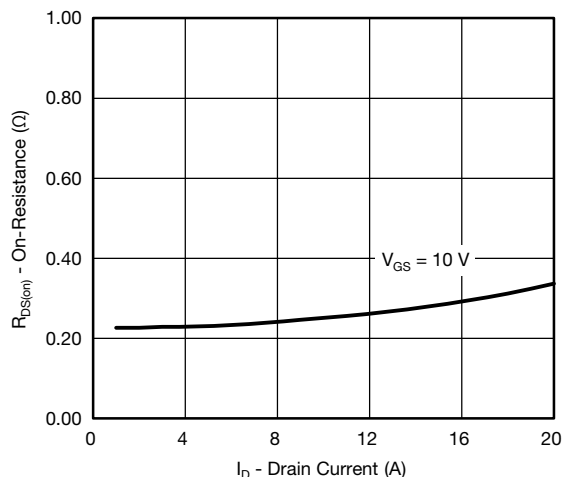
Transfer Characteristics



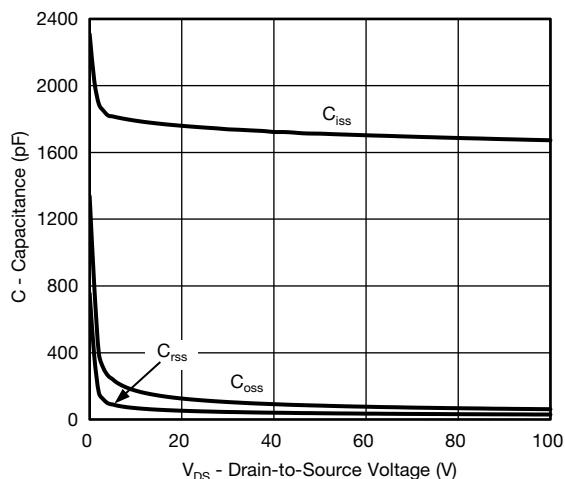
Transfer Characteristics



Transconductance



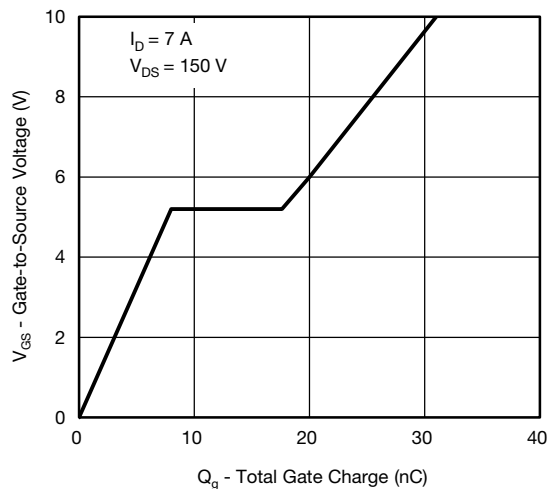
On-Resistance vs. Drain Current



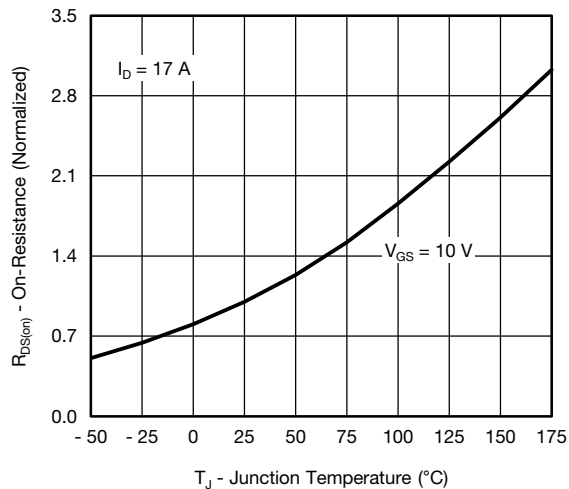
Capacitance



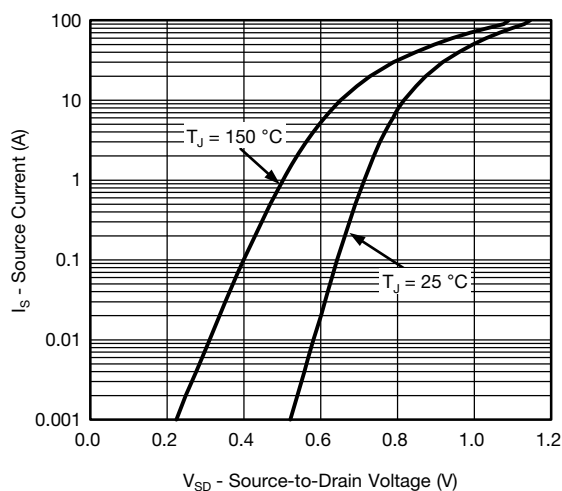
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



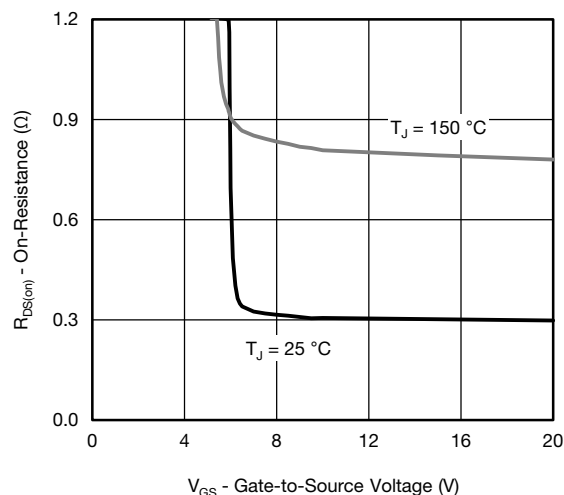
Gate Charge



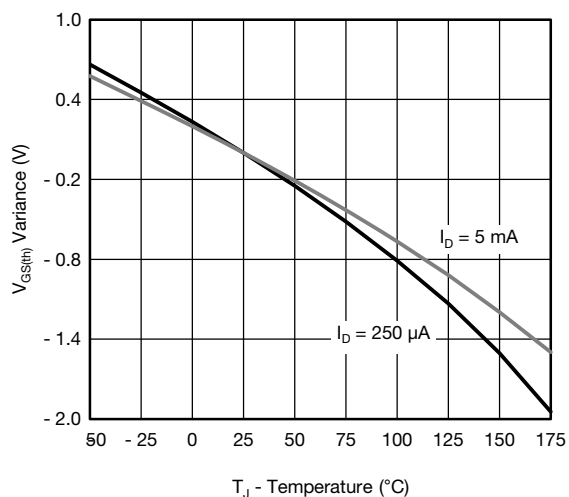
On-Resistance vs. Junction Temperature



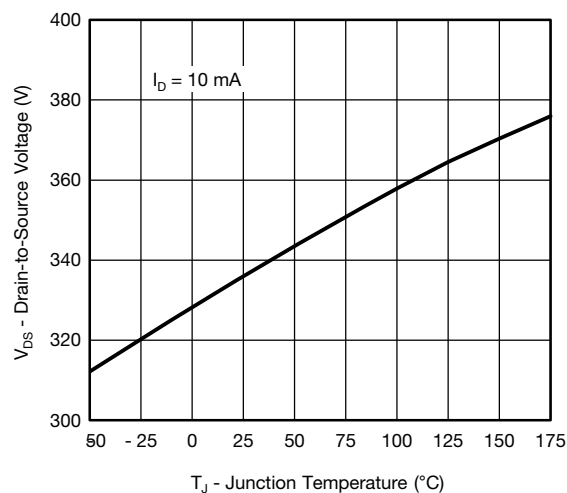
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



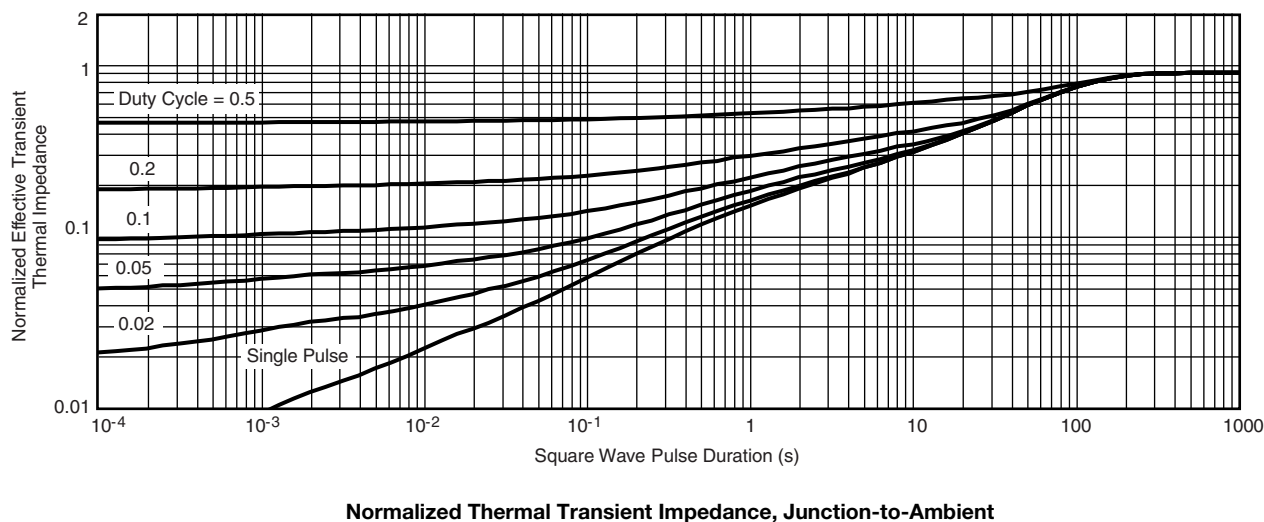
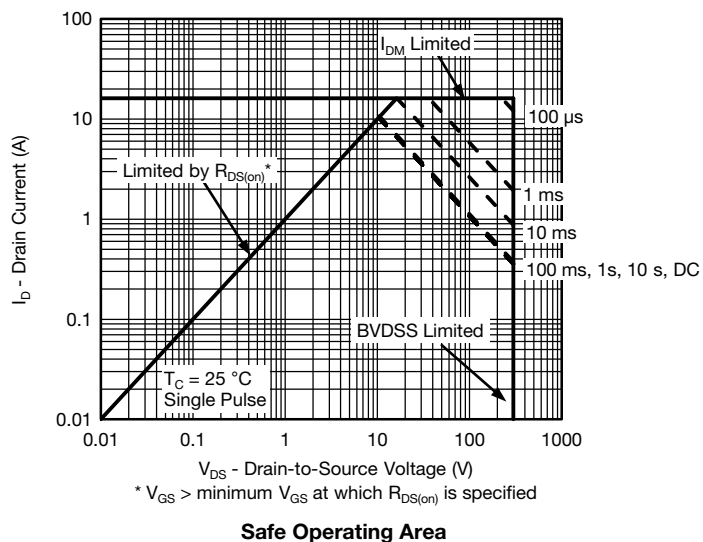
Threshold Voltage



Drain Source Breakdown vs. Junction Temperature

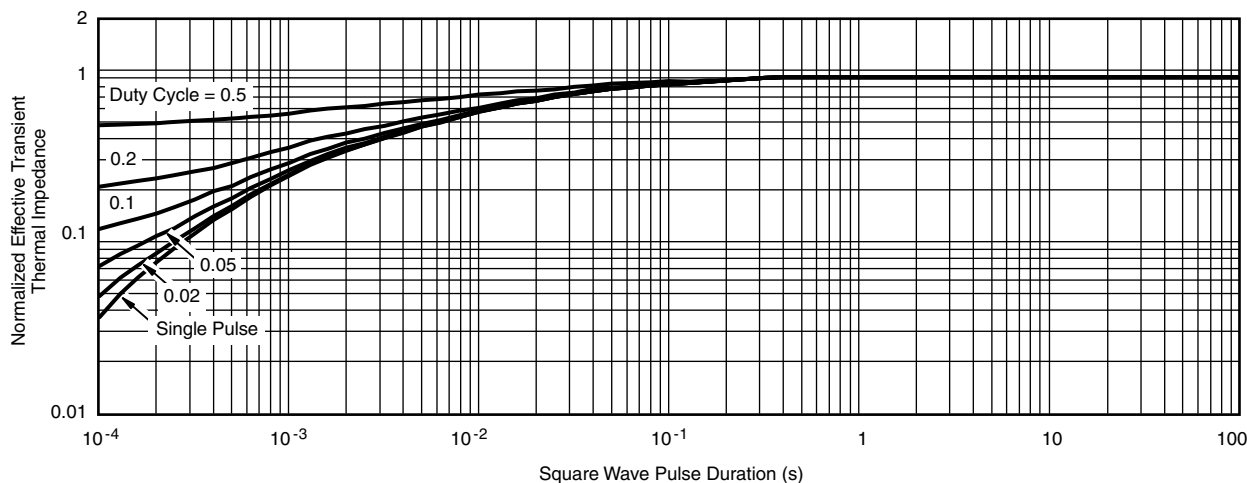


THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)





THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67070.

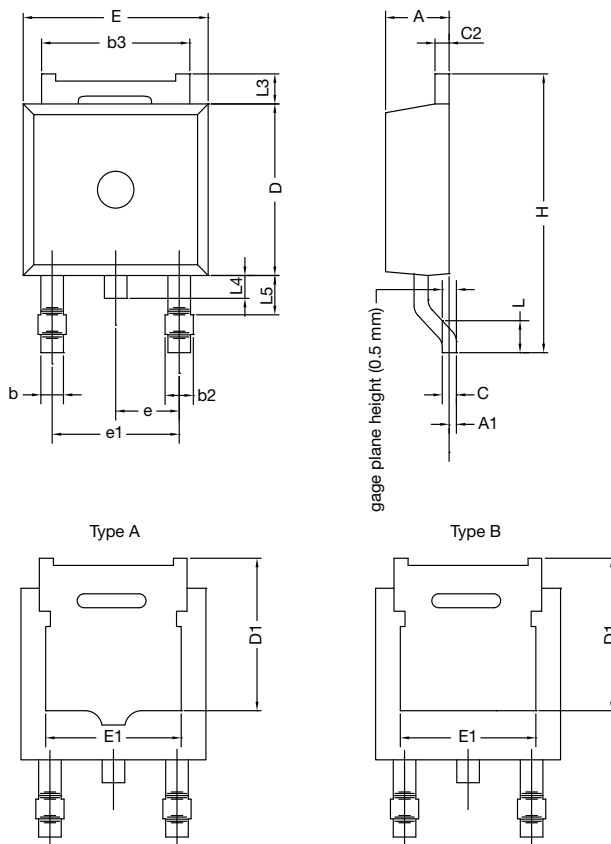


REVISION HISTORY ^a		
REVISION	DATE	DESCRIPTION OF CHANGE
B	26-Feb-2015	• UIS changed
C	04-May-2015	• R_g , C_{iss} and t_r updated

Note

a. As of April 2014

TO-252AA Case Outline



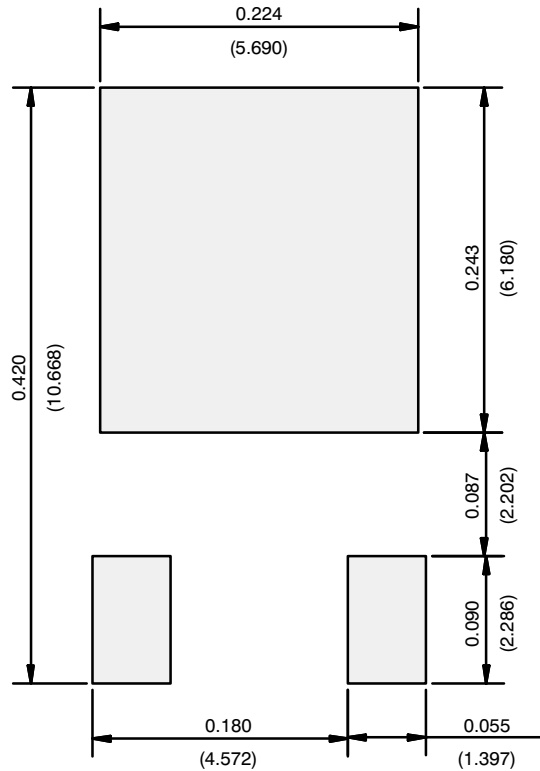
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T25-0122-Rev. C, 12-May-2025
DWG: 6019

Notes

- Dimension L3 is for reference only
- Dimension D1 and E1 on type A and B is the same

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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