

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: SQ4532AEY-T1_BE3

Manufacturer: Vishay Siliconix

Package: Please confirm with sales

Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/vishay-siliconix/sq4532aey-t1-be3.html>

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Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

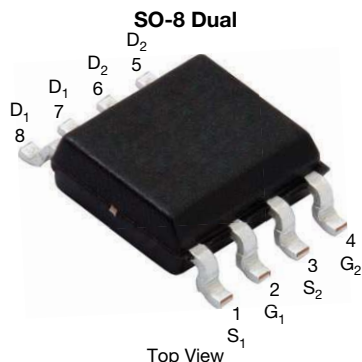
Secure sourcing support for OEM / EMS projects

Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

Automotive N-and P-Channel 30 V (D-S) 175 °C MOSFET

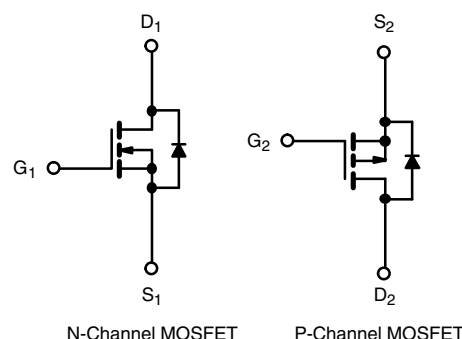


Marking Code: Q4532A

PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
V_{DS} (V)	30	-30
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 10$ V	0.031	0.070
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 4.5$ V	0.042	0.190
I_D (A)	7.3	-5.3
Configuration	N- and p-pair	

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified ^c
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free and halogen-free	SQ4532AEY (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-source voltage			V _{DS}	30	-30	V
Gate-source voltage			V _{GS}	± 20		
Continuous drain current	T _C = 25 °C		I _D	7.3	-5.3	A
	T _C = 125 °C			4.2	-3	
Continuous source current (diode conduction)			I _S	4.2	-3	
Pulsed drain current ^a			I _{DM}	29	-21	
Single pulse avalanche current	L = 0.1 mH		I _{AS}	10	-9	mJ
Single pulse avalanche energy			E _{AS}	5	4	
Maximum power dissipation ^a	T _C = 25 °C		P _D	3.3	3.3	W
	T _C = 125 °C			1.1	1.1	
Operating junction and storage temperature range			T _J , T _{sta}	-55 to +175		°C

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Junction-to-ambient	R_{thJA}	110	105	°C/W
Junction-to-foot (drain)	R_{thJF}	45	45	

Notes

- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- Parametric verification ongoing



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
Static								
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		N-Ch	30	-	-	V
		V _{GS} = 0, I _D = -250 μA		P-Ch	-30	-	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		N-Ch	1.5	2	2.5	
		V _{DS} = V _{GS} , I _D = -250 μA		P-Ch	-1.5	-2	-2.5	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		N-Ch	-	-	± 100	nA
				P-Ch	-	-	± 100	
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 30 V	N-Ch	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = -30 V	P-Ch	-	-	-1	
		V _{GS} = 0 V	V _{DS} = 30 V, T _J = 125 °C	N-Ch	-	-	50	
		V _{GS} = 0 V	V _{DS} = -30 V, T _J = 125 °C	P-Ch	-	-	-50	
		V _{GS} = 0 V	V _{DS} = 30 V, T _J = 175 °C	N-Ch	-	-	150	
		V _{GS} = 0 V	V _{DS} = -30 V, T _J = 175 °C	P-Ch	-	-	-150	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} = 5 V	N-Ch	15	-	-	A
		V _{GS} = -10 V	V _{DS} = -5 V	P-Ch	-15	-	-	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 4.9 A	N-Ch	-	0.021	0.031	Ω
		V _{GS} = -10 V	I _D = -3.5 A	P-Ch	-	0.056	0.070	
		V _{GS} = 10 V	I _D = 4.9 A, T _J = 125 °C	N-Ch	-	-	0.064	
		V _{GS} = -10 V	I _D = -3.5 A, T _J = 125 °C	P-Ch	-	-	0.100	
		V _{GS} = 10 V	I _D = 4.9 A, T _J = 175 °C	N-Ch	-	-	0.082	
		V _{GS} = -10 V	I _D = -3.5 A, T _J = 175 °C	P-Ch	-	-	0.117	
		V _{GS} = 4.5 V	I _D = 4.1 A	N-Ch	-	0.033	0.042	
		V _{GS} = -4.5 V	I _D = -2.5 A	P-Ch	-	0.157	0.190	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 4.9 A		N-Ch	-	22	-	S
		V _{DS} = -15 V, I _D = -3.5 A		P-Ch	-	5.5	-	
Dynamic ^b								
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 15 V, f = 1 MHz	N-Ch	-	357	535	pF
		V _{GS} = 0 V	V _{DS} = -15 V, f = 1 MHz	P-Ch	-	352	528	
Output capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 15 V, f = 1 MHz	N-Ch	-	82	123	pF
		V _{GS} = 0 V	V _{DS} = -15 V, f = 1 MHz	P-Ch	-	95	142	
Reverse transfer capacitance	C _{rss}	V _{GS} = 0 V	V _{DS} = 15 V, f = 1 MHz	N-Ch	-	36	53	pF
		V _{GS} = 0 V	V _{DS} = -15 V, f = 1 MHz	P-Ch	-	59	88	
Total gate charge	Q _g	V _{GS} = 10 V	V _{DS} = 15 V, I _D = 3.9 A	N-Ch	-	5.9	7.8	nC
		V _{GS} = -10 V	V _{DS} = -15 V, I _D = -2.5 A	P-Ch	-	7.9	10.2	
Gate-source charge	Q _{gs}	V _{GS} = 10 V	V _{DS} = 15 V, I _D = 3.9 A	N-Ch	-	1	-	nC
		V _{GS} = -10 V	V _{DS} = -15 V, I _D = -2.5 A	P-Ch	-	1.1	-	
Gate-drain charge ^c	Q _{gd}	V _{GS} = 10 V	V _{DS} = 15 V, I _D = 3.9 A	N-Ch	-	1.9	-	nC
		V _{GS} = -10 V	V _{DS} = -15 V, I _D = -2.5 A	P-Ch	-	2.7	-	
Gate resistance	R _g	f = 1 MHz		N-Ch	1.7	3.4	5.1	Ω
				P-Ch	2.8	5.8	8.6	



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω I _D ≡ 1 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch	-	7	10	ns
		V _{DD} = -15 V, R _L = 15 Ω I _D ≡ -1 A, V _{GEN} = -10 V, R _g = 1 Ω	P-Ch	-	6	9	
Rise time	t _r	V _{DD} = 15 V, R _L = 15 Ω I _D ≡ 1 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch	-	17	21	
		V _{DD} = -15 V, R _L = 15 Ω I _D ≡ -1 A, V _{GEN} = -10 V, R _g = 1 Ω	P-Ch	-	17	21	
Turn-off delay time	t _{d(off)}	V _{DD} = 15 V, R _L = 15 Ω I _D ≡ 1 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch	-	10	14	
		V _{DD} = -15 V, R _L = 15 Ω I _D ≡ -1 A, V _{GEN} = -10 V, R _g = 1 Ω	P-Ch	-	19	24	
Fall time	t _f	V _{DD} = 15 V, R _L = 15 Ω I _D ≡ 1 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch	-	19	24	
		V _{DD} = -15 V, R _L = 15 Ω I _D ≡ -1 A, V _{GEN} = -10 V, R _g = 1 Ω	P-Ch	-	16	20	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I _{SM}		N-Ch	-	-	29	A
			P-Ch	-	-	-21	
Forward voltage	V _{SD}	I _S = 2 A	N-Ch	-	0.8	1.2	V
		I _S = -1.5 A	P-Ch	-	-0.8	-1.2	

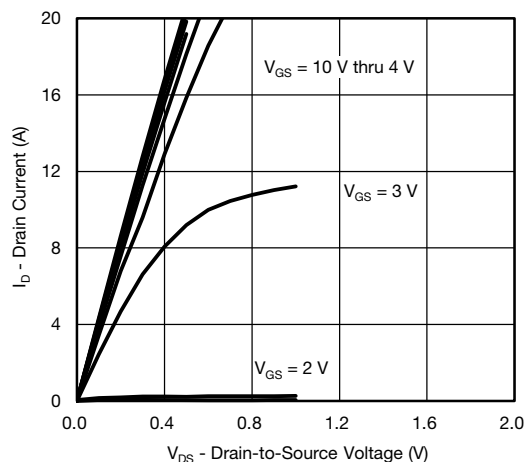
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

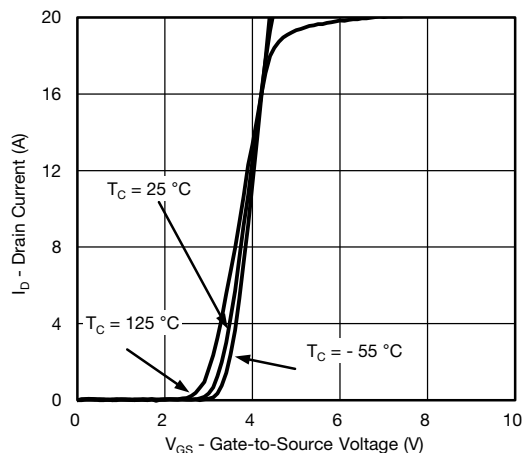
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



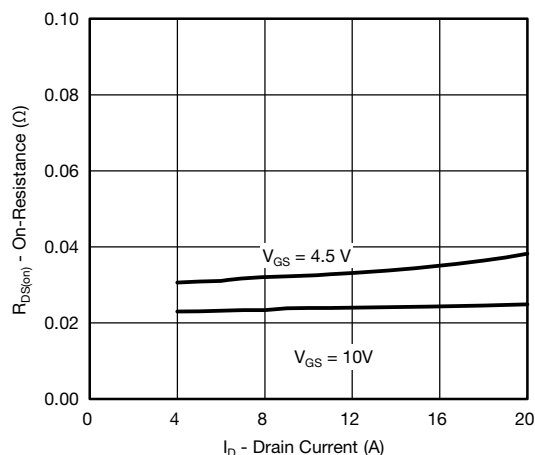
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



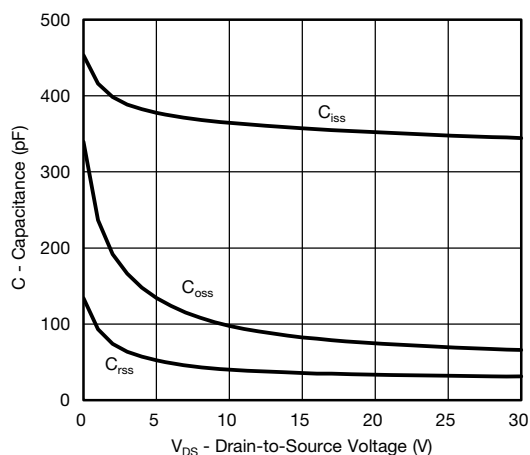
Output Characteristics



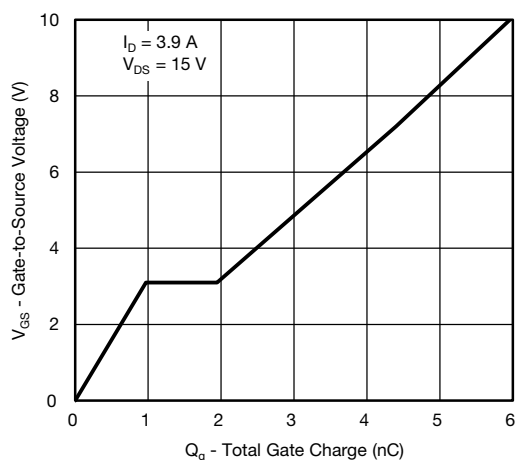
Transfer Characteristics



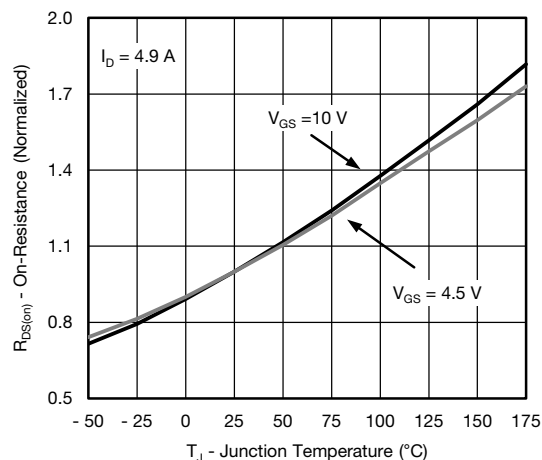
On-Resistance vs. Drain Current



Capacitance



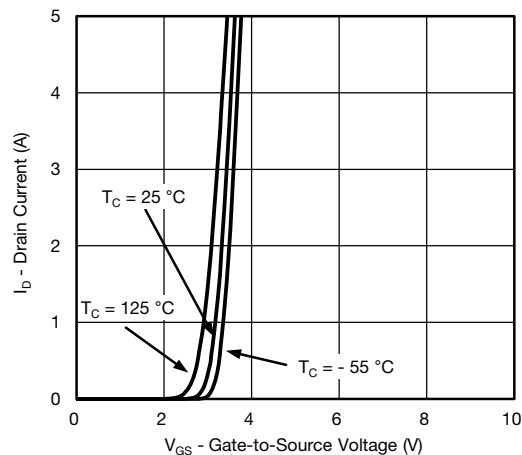
Gate Charge



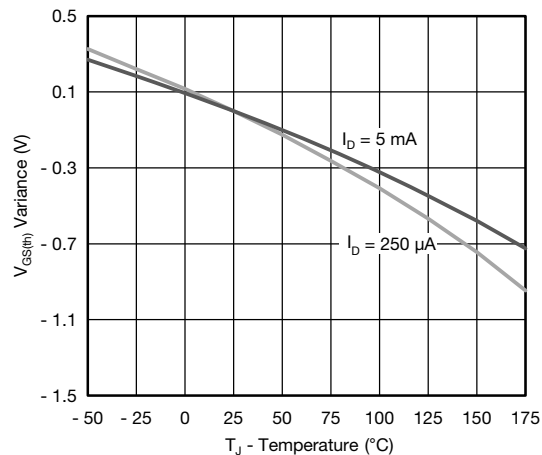
On-Resistance vs. Junction Temperature



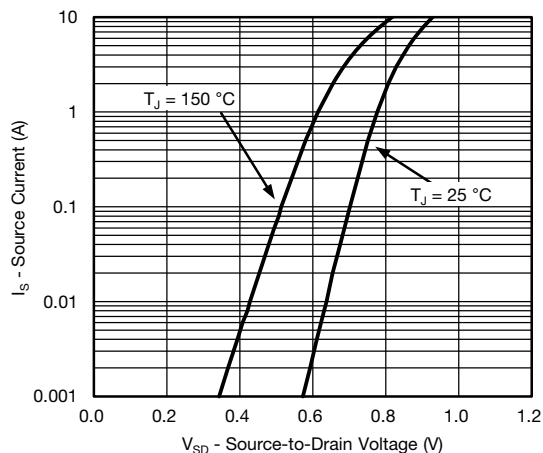
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



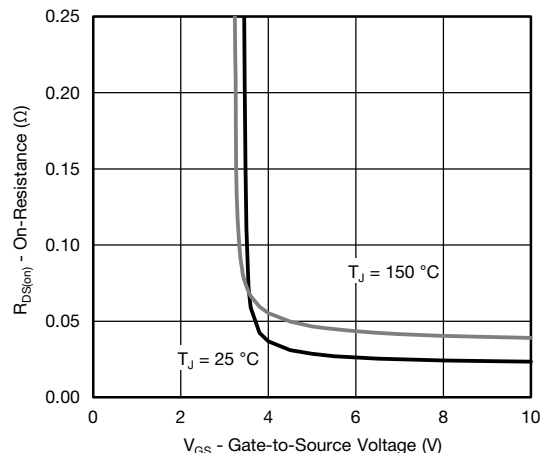
Transfer Characteristics



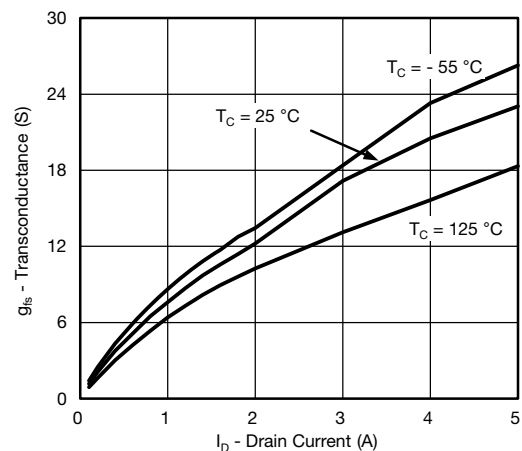
Threshold Voltage



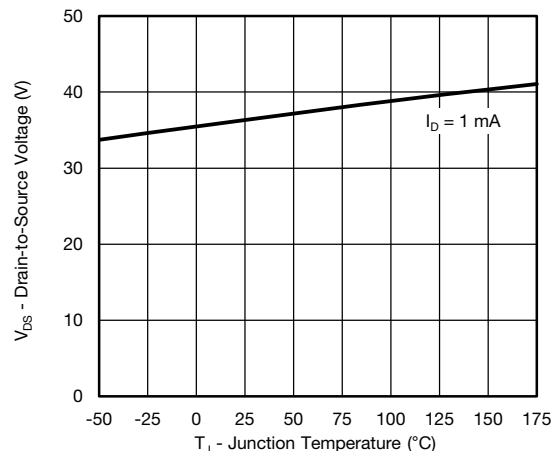
Source Drain Diode Forward Voltage



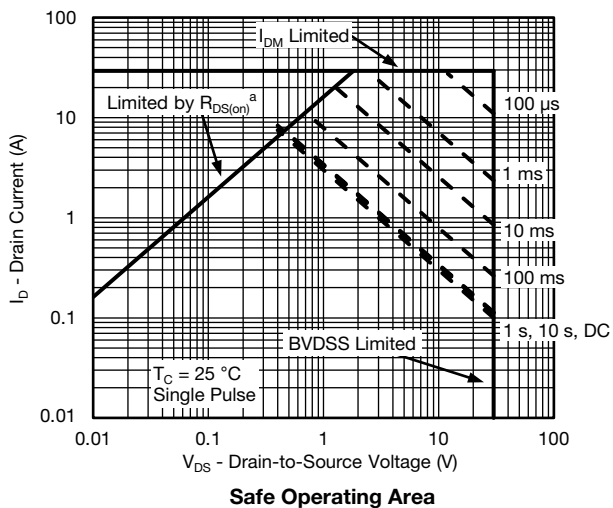
On-Resistance vs. Gate-to-Source Voltage



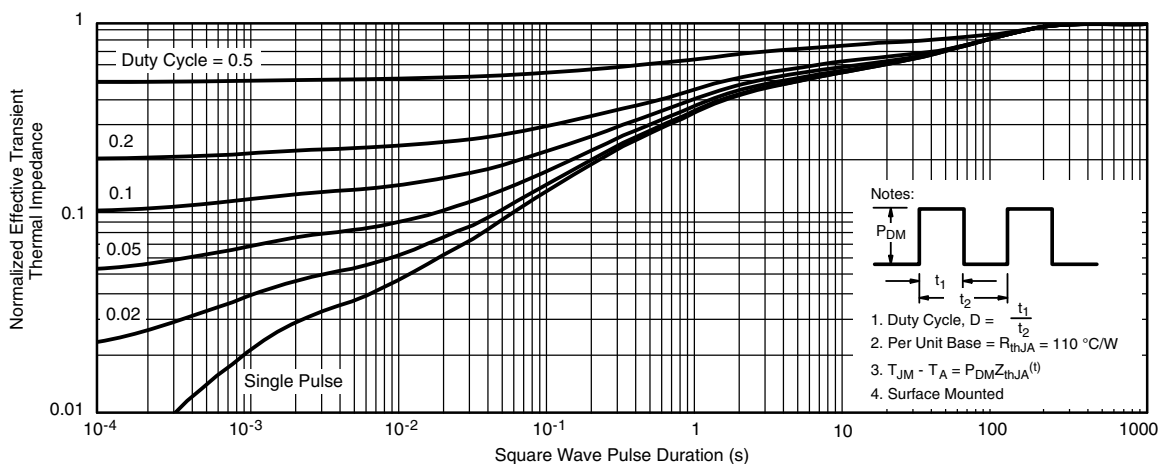
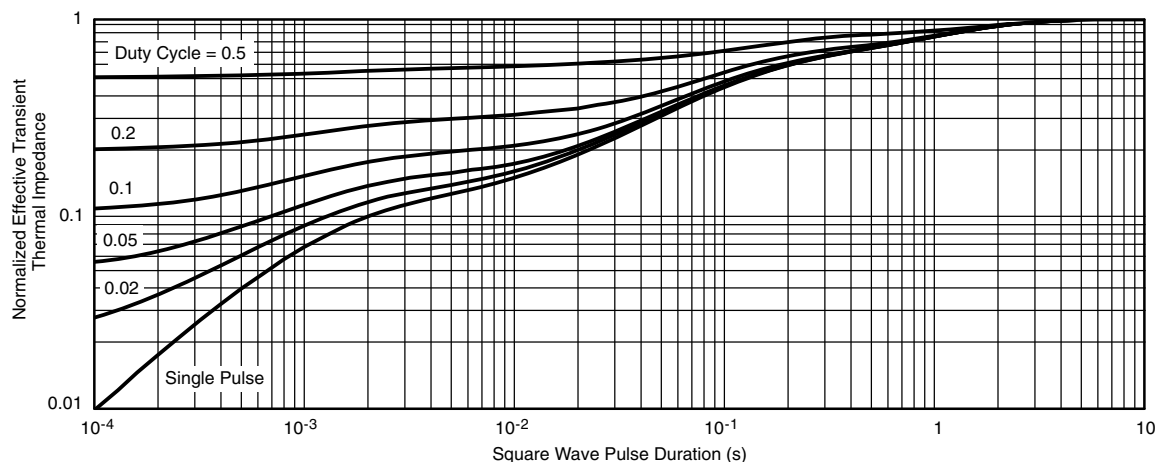
Transconductance



Drain Source Breakdown vs. Junction Temperature

N-CHANNEL THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Note

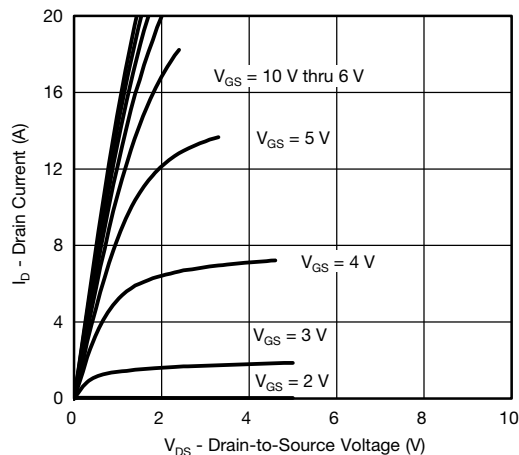
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

N-CHANNEL THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Foot
Note

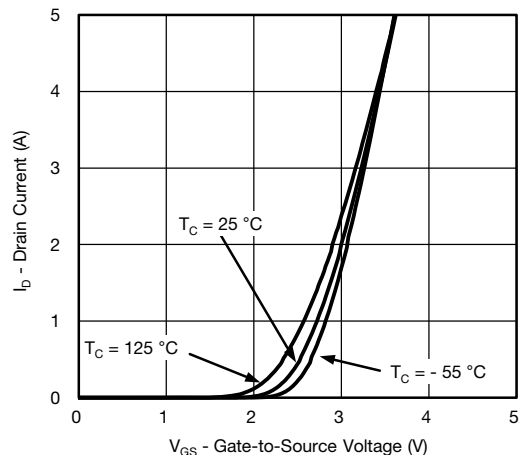
- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)
 are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.



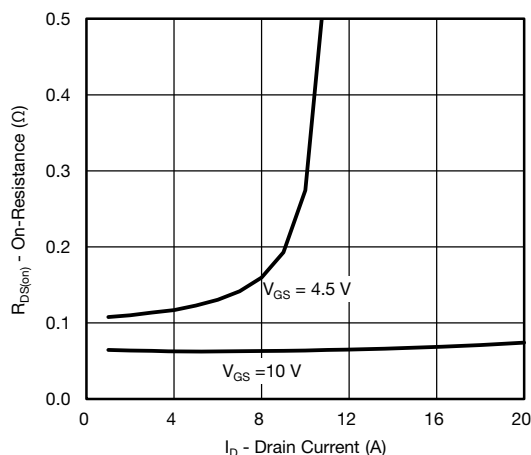
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



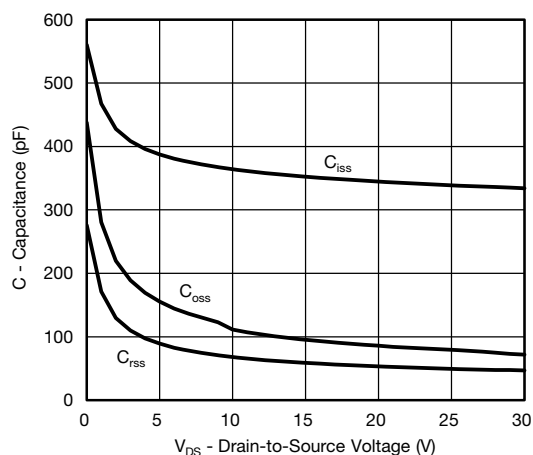
Output Characteristics



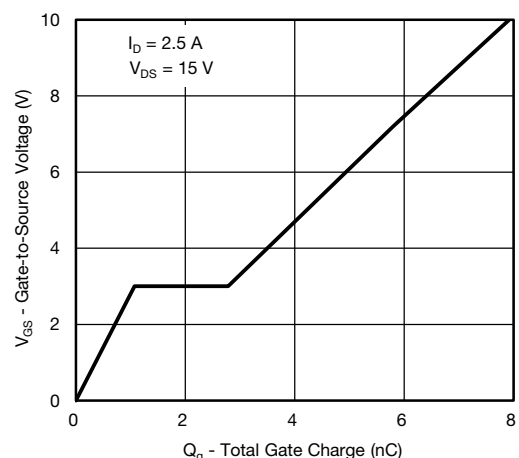
Transfer Characteristics



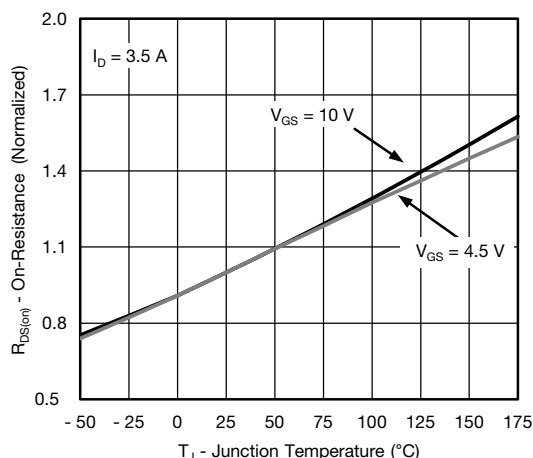
On-Resistance vs. Drain Current



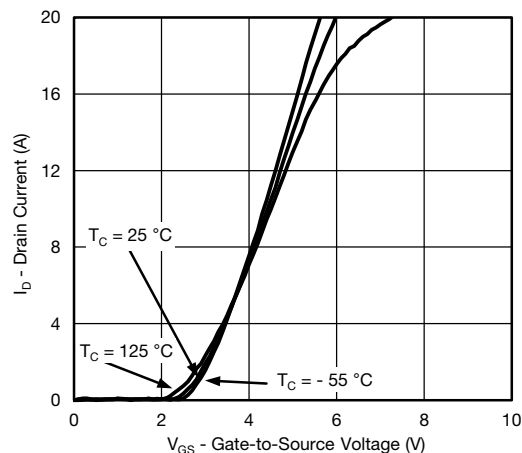
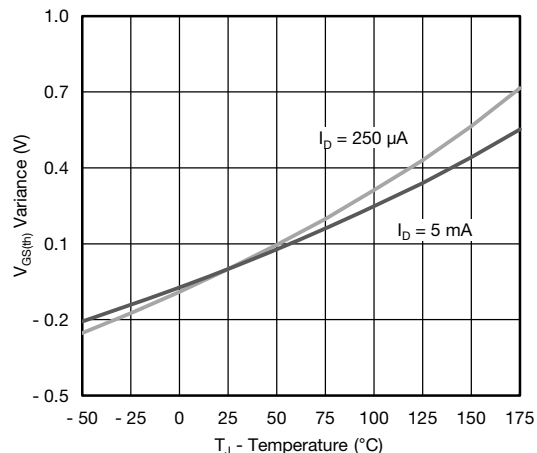
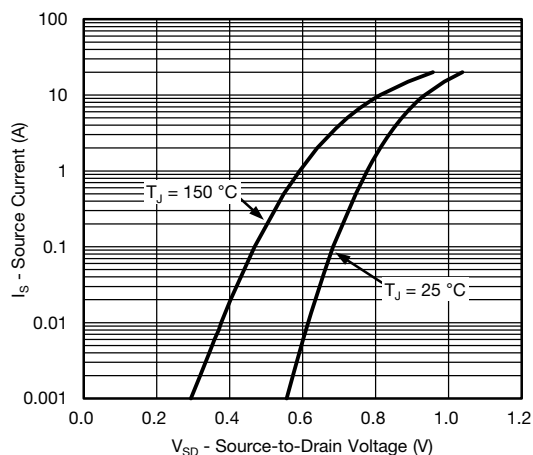
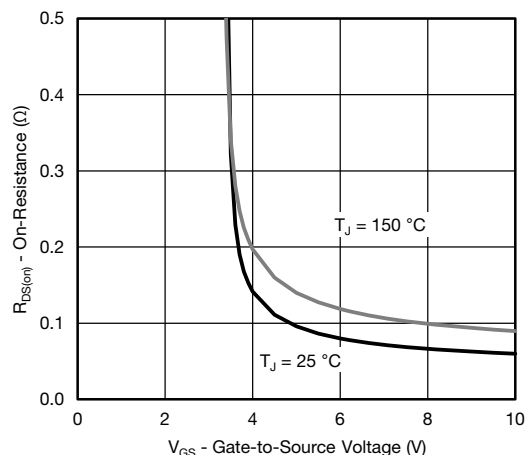
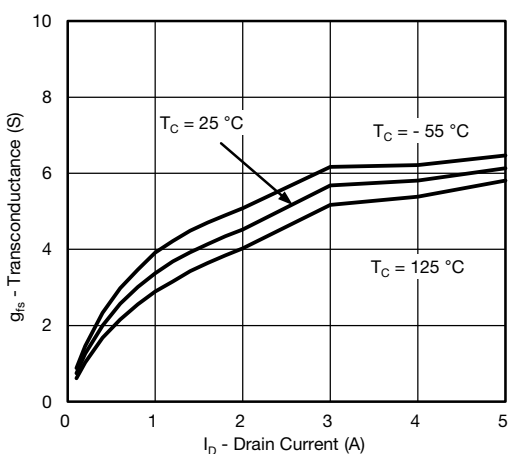
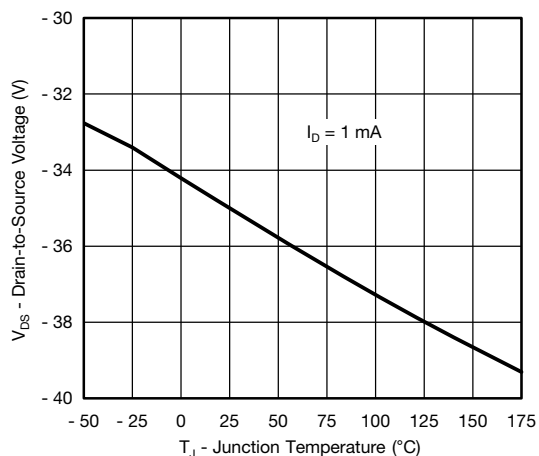
Capacitance



Gate Charge

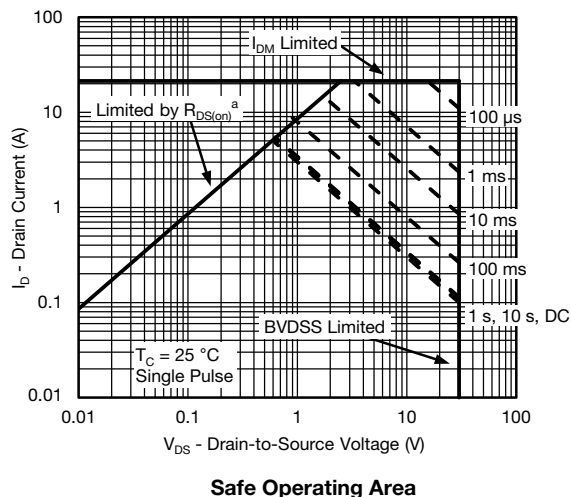


On-Resistance vs. Junction Temperature

P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Transfer Characteristics

Threshold Voltage

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Transconductance

Drain Source Breakdown vs. Junction Temperature

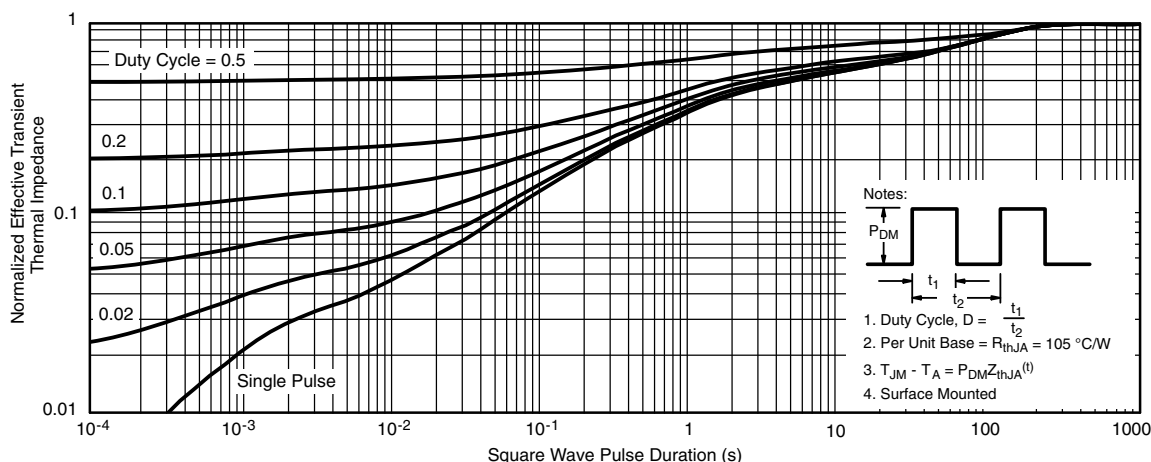
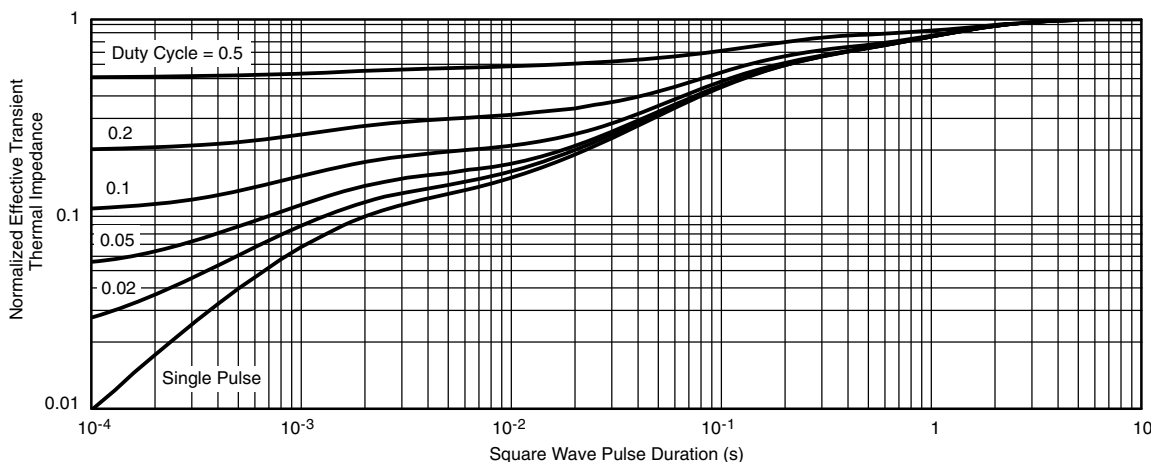


P-CHANNEL THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

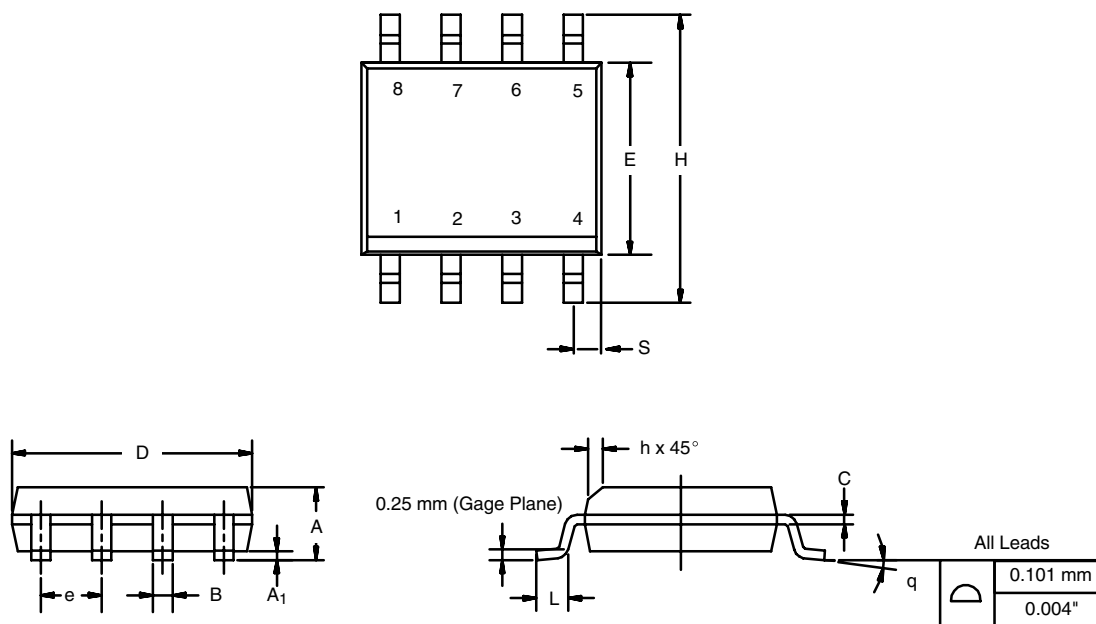
**P-CHANNEL THERMAL RATINGS** ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot****Note**

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
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- are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62981.

SOIC (NARROW): 8-LEAD

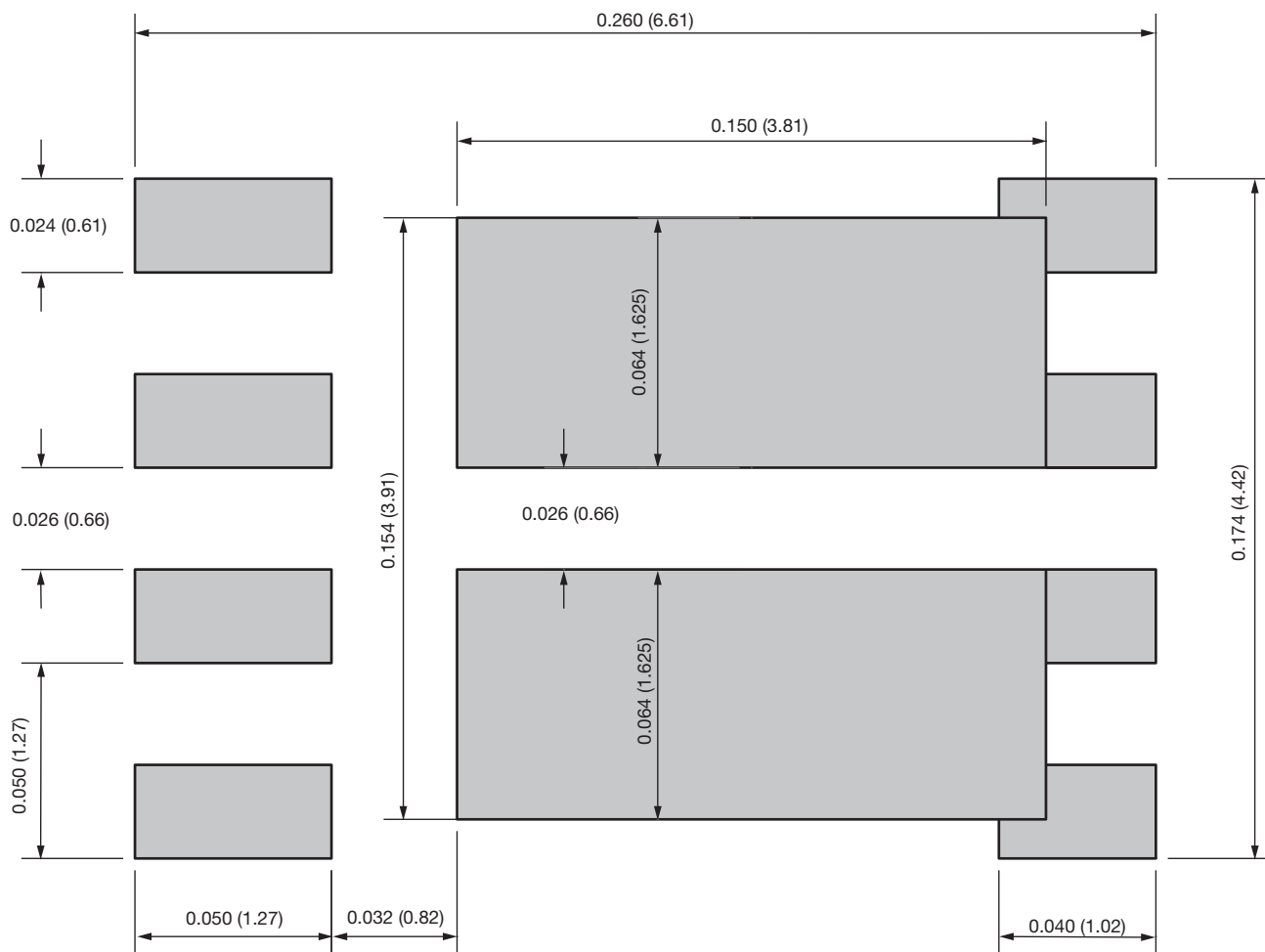
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				



Recommended Land Pattern PowerPAK® SO-8 Dual

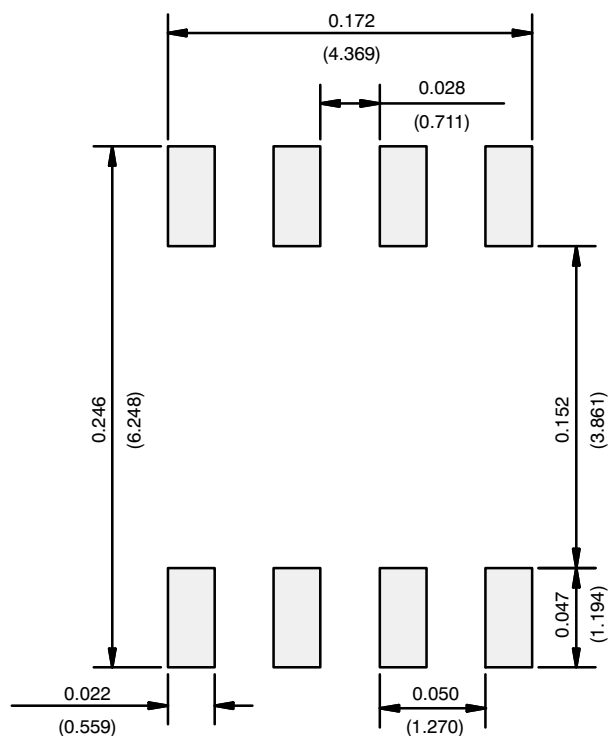


Note

- Dimensions in inches (millimeters)

ECN: S24-0458-Rev. A, 06-May-2024
DWG: 3026

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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