

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: SQ4284EY-T1_GE3

Manufacturer: Vishay Siliconix

Package: Please confirm with sales

Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/vishay-siliconix/sq4284ey-t1-ge3.html>

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Contact Information

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Website: <https://antrexco.com>

Quality & Trust

New & Original Components

Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

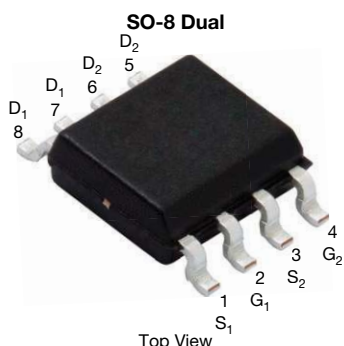
Secure sourcing support for OEM / EMS projects

Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFET

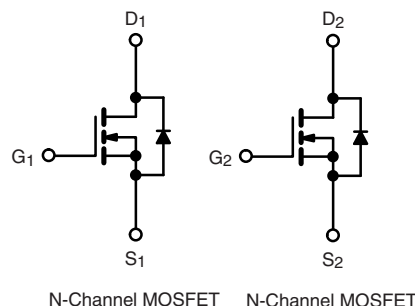


FEATURES

- TrenchFET® Power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE



PRODUCT SUMMARY	
V _{DS} (V)	40
R _{DS(on)} (Ω) at V _{GS} = 10 V	0.0135
R _{DS(on)} (Ω) at V _{GS} = 4.5 V	0.0148
I _D (A)	8
Configuration	Dual

ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free and halogen-free	SQ4284EY (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	40	V
Gate-source voltage		V _{GS}	± 20	
Continuous drain current	T _C = 25 °C ^a	I _D	8	A
	T _C = 125 °C		7.4	
Continuous source current (diode conduction)		I _S	3.5	
Pulsed drain current ^a		I _{DM}	32	
Single pulse avalanche current	L = 0.1 mH	I _{AS}	48	
Single pulse avalanche energy		E _{AS}	115	mJ
Maximum power dissipation ^a	T _C = 25 °C	P _D	3.9	W
	T _C = 125 °C		1.3	
Operating junction and storage temperature range		T _J , T _{stg}	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB Mount ^b	R _{thJA}	120	°C/W
Junction-to-foot (drain)		R _{thJF}	38	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. When mounted on 1" square PCB (FR-4 material)

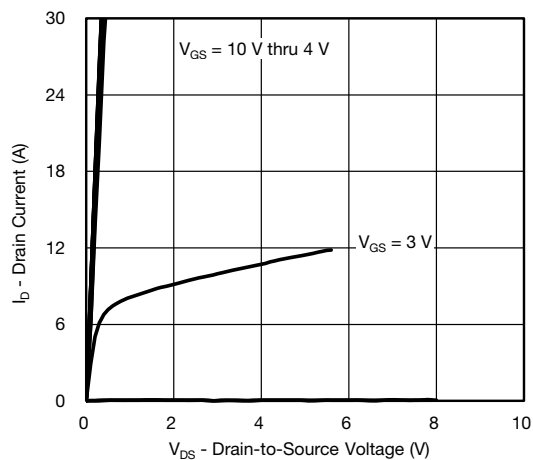
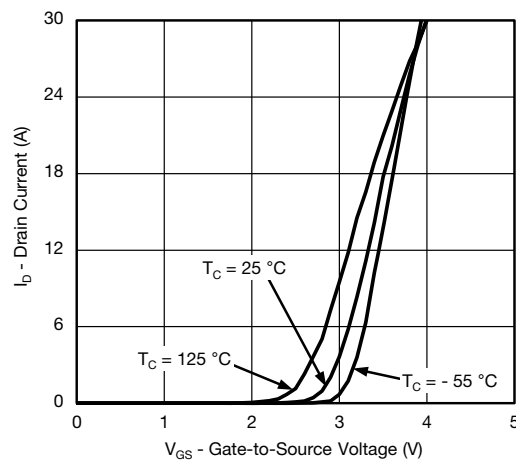
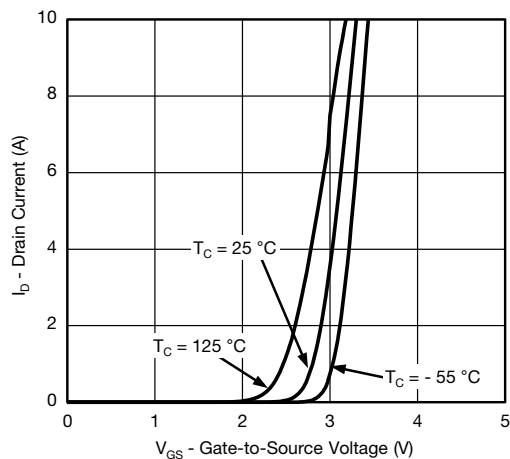
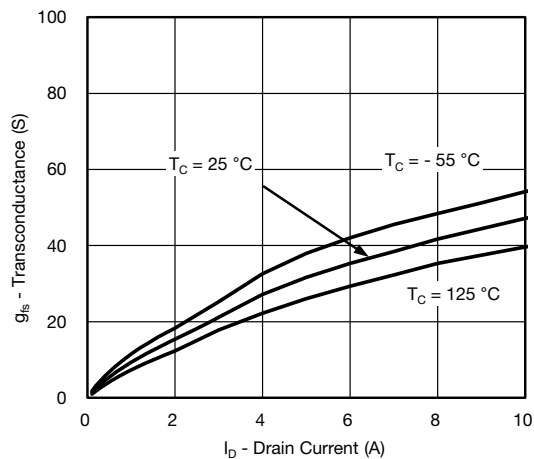
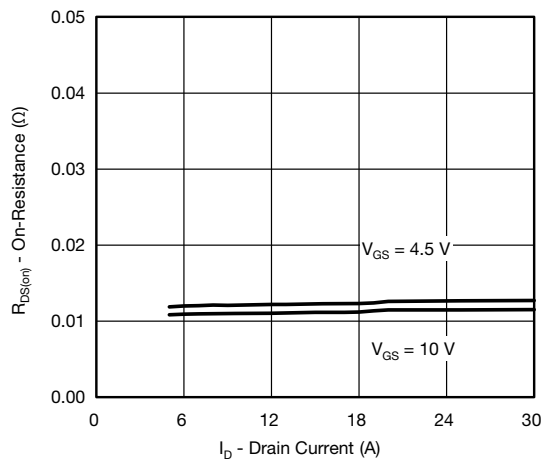
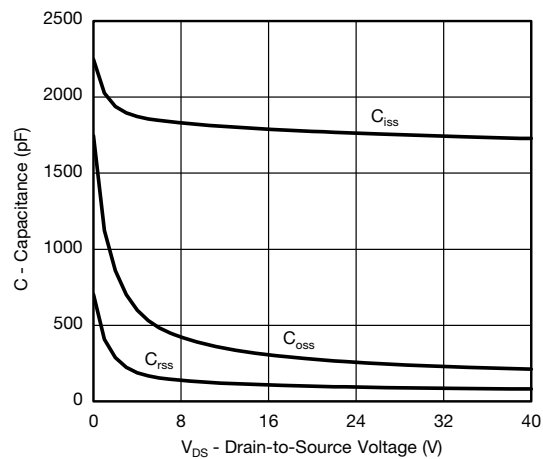


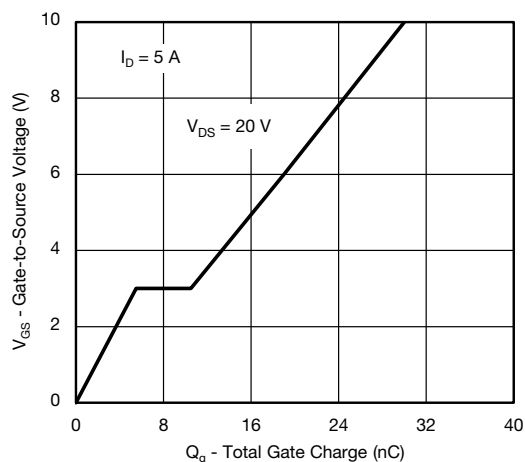
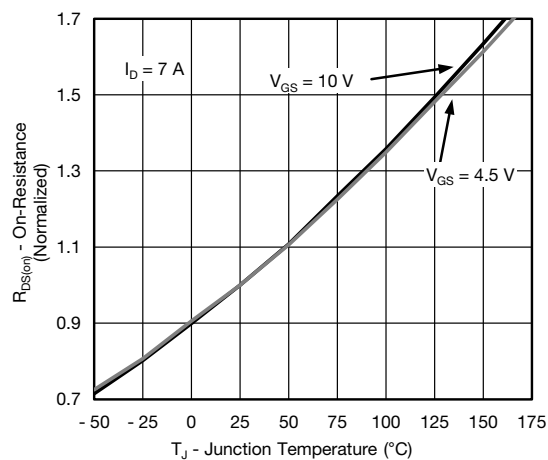
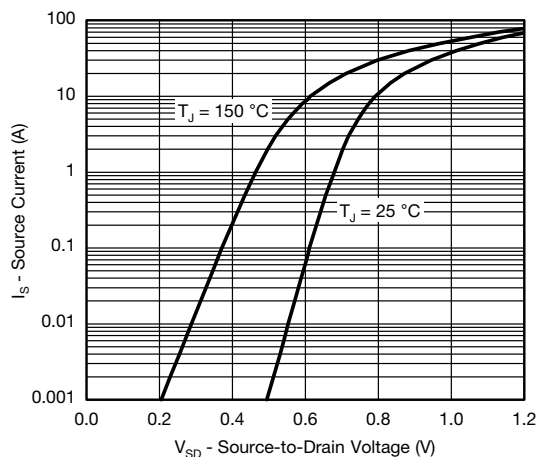
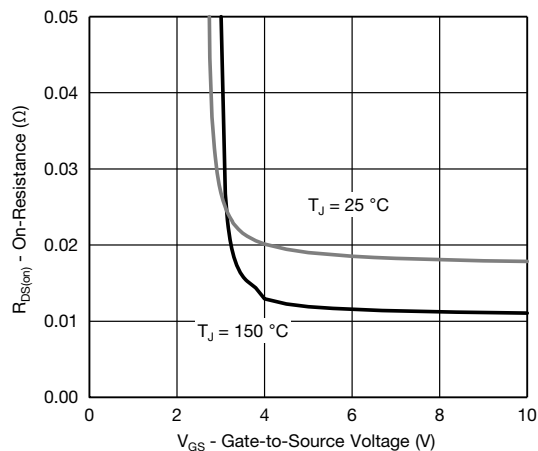
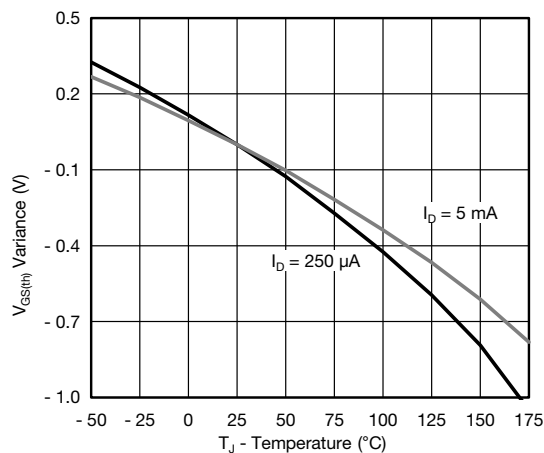
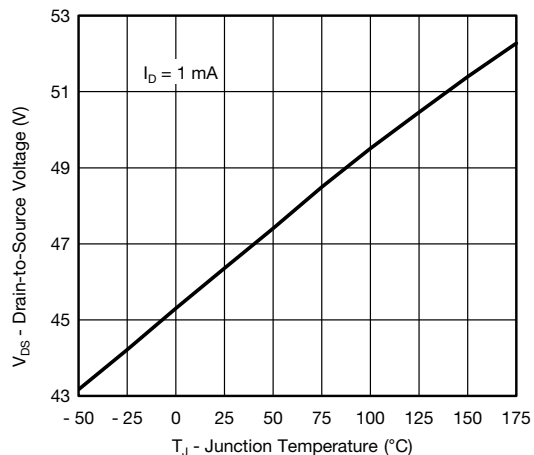
SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		40	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.5	2.0	2.5	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	150	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	25	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 7 A	-	0.0112	0.0135	Ω
		V _{GS} = 10 V	I _D = 7 A, T _J = 125 °C	-	-	0.0198	
		V _{GS} = 10 V	I _D = 7 A, T _J = 175 °C	-	-	0.0235	
		V _{GS} = 4.5 V	I _D = 5 A	-	0.0123	0.0148	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 7 A		-	30	-	S
Dynamic ^b							
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	1760	2200	pF
Output capacitance	C _{oss}			-	252	315	
Reverse transfer capacitance	C _{rss}			-	93	116	
Total gate charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 20 V, I _D = 5 A	-	30	45	nC
Gate-source charge ^c	Q _{gs}			-	5.5	-	
Gate-drain charge ^c	Q _{gd}			-	5	-	
Gate resistance	R _g	f = 1 MHz		2.2	4.53	6.8	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 20 V, R _L = 4 Ω I _D ≥ 5 A, V _{GEN} = 10 V, R _g = 1 Ω		-	10	15	ns
Rise Time ^c	t _r			-	40	60	
Turn-Off Delay Time ^c	t _{d(off)}			-	32	48	
Fall time ^c	t _f			-	11	17	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I _{SM}			-	-	32	A
Forward voltage	V _{SD}	I _F = 7 A, V _{GS} = 0 V		-	0.76	1.2	V

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

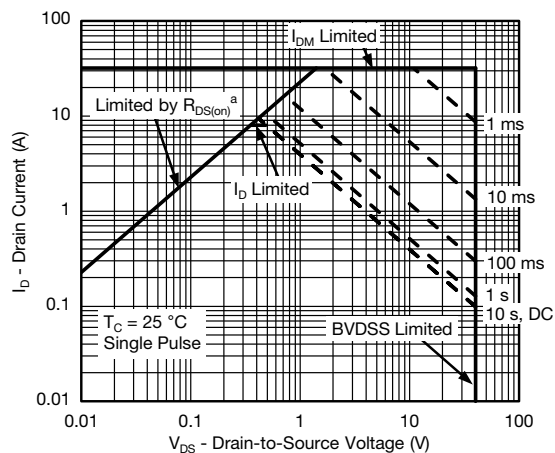
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Gate Charge

On-Resistance vs. Junction Temperature

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Drain Source Breakdown vs. Junction Temperature

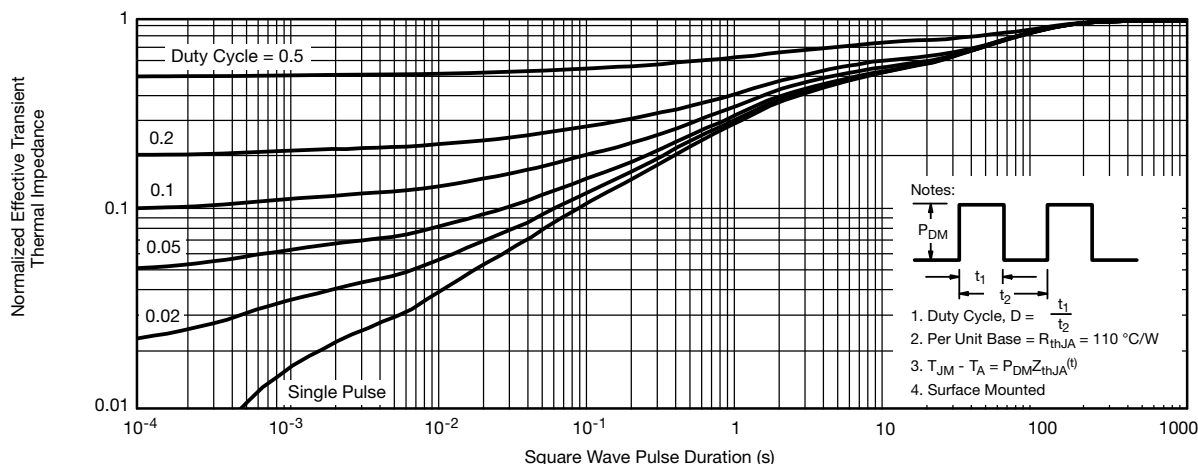
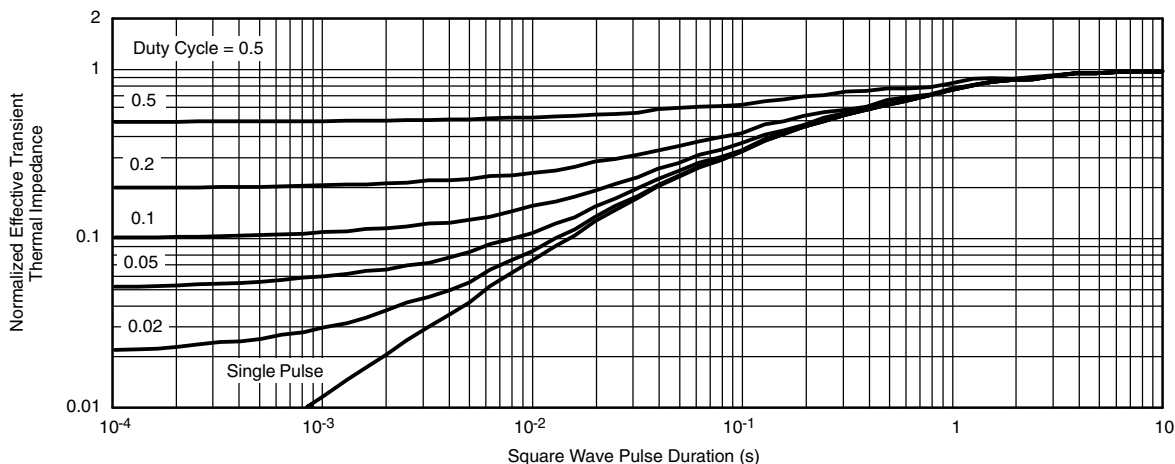


THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

**THERMAL RATINGS** ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot****Note**

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Foot ($25\text{ }^{\circ}\text{C}$)
- are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67334.

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012

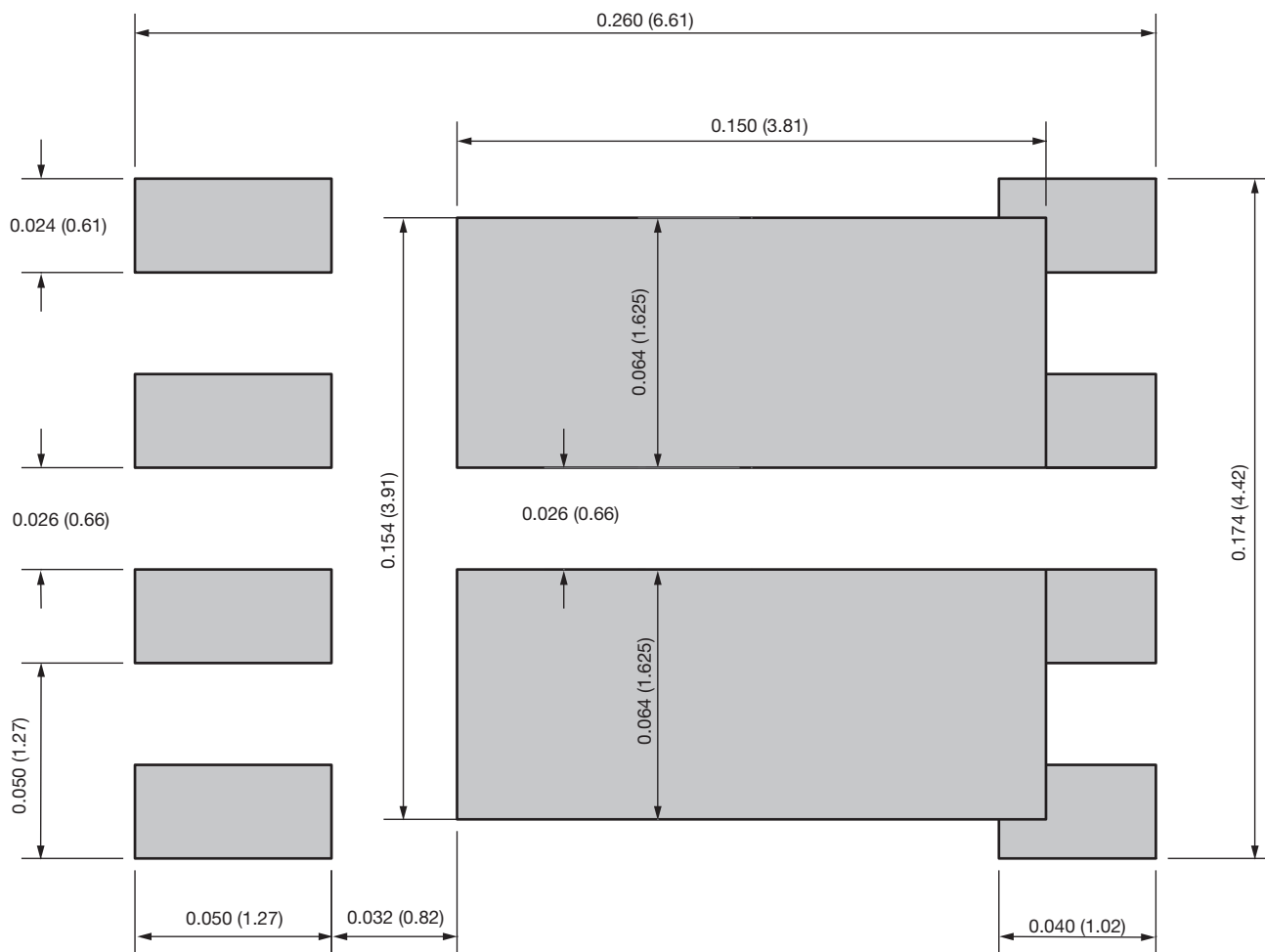


DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

ECN: C-06527-Rev. I, 11-Sep-06
DWG: 5498



Recommended Land Pattern PowerPAK® SO-8 Dual

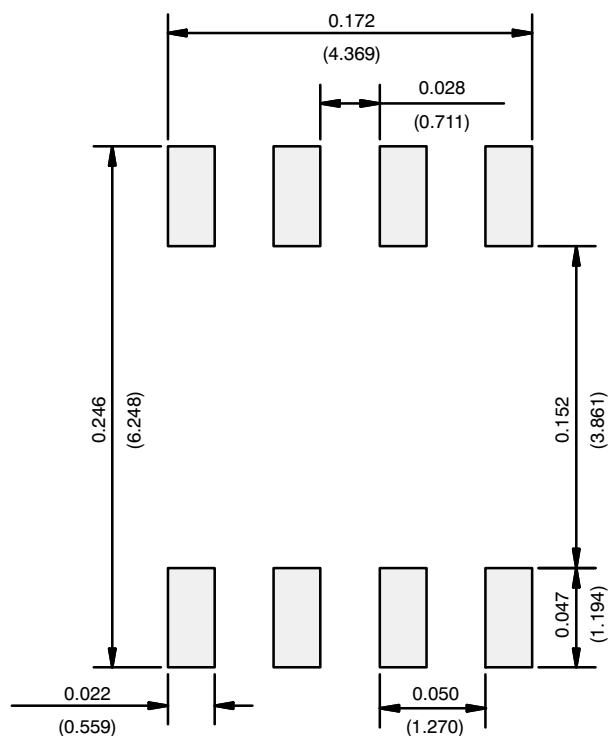


Note

- Dimensions in inches (millimeters)

ECN: S24-0458-Rev. A, 06-May-2024
DWG: 3026

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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