

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	IRF644NSTRL
Manufacturer:	Vishay Siliconix
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/vishay-siliconix/irf644nstrl.html>

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Contact Information

Email: info@antrexco.com

WhatsApp: +86-186-8066-5326

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Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

Secure sourcing support for OEM / EMS projects

Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	250 V	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.240
Q_g (Max.) (nC)	54	
Q_{gs} (nC)	9.2	
Q_{gd} (nC)	26	
Configuration	Single	

FEATURES

- Advanced Process Technology
- Dynamic dV/dt Rating
- 175 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available



Available

RoHS*
COMPLIANT

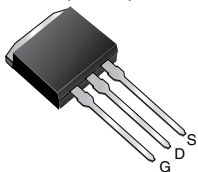
DESCRIPTION

Fifth generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

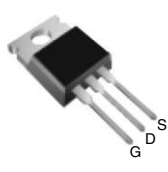
The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

The D²PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

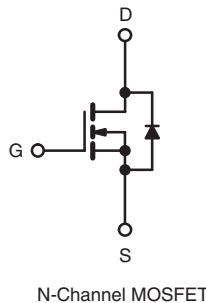
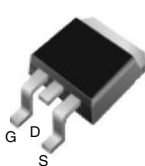
I²PAK (TO-262)



TO-220



D²PAK (TO-263)



N-Channel MOSFET

ORDERING INFORMATION

Package	TO-220	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free	IRF644NPbF	IRF644NSPbF	IRF644NSTRLPbF ^a	IRF644NSTRRPbF ^a	IRF644NLPbF
	SiHF644N-E3	SiHF644NS-E3	SiHF644NSTL-E3 ^a	SiHF644NSTR-E3 ^a	SiHF644NL-E3
SnPb	IRF644N	IRF644NS	IRF644NSTRL ^a	IRF644NSTR ^a	IRF644NL
	SiHF644N	SiHF644NS	SiHF644NSTL ^a	SiHF644NSTR ^a	SiHF644NL

Note

a. See device orientation.

* Pb containing terminations are not RoHS compliant, exemptions may apply

ABSOLUTE MAXIMUM RATINGS T _C = 25 °C, unless otherwise noted						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V _{DS}	250	V	
Gate-Source Voltage			V _{GS}	± 20		
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	14	A	
		T _C = 100 °C		9.9		
Pulsed Drain Current ^a			I _{DM}	56		
Linear Derating Factor				1.0	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	180 ^e	mJ	
Avalanche Current			I _{AR}	8.4	A	
Repetitive Avalanche Energy			E _{AR}	15	mJ	
Maximum Power Dissipation		T _C = 25 °C		P _D	150	W
Peak Diode Recovery dV/dt ^c			dV/dt	7.9	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature)		for 10 s		300 ^d		
Mounting Torque	6-32 or M3 screw			10	lbf · in	
				1.1	N · m	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 5.0\text{ }\mu\text{H}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 8.4\text{ A}$ (see fig. 12).
- $I_{SD} \leq 8.4\text{ A}$, $dI/dt \leq 378\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^{\circ}\text{C}$.
- 1.6 mm from case.
- This is a calculated value limited to $T_J = 175\text{ }^{\circ}\text{C}$.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient ^c	R_{thJA}	-	62	$^{\circ}\text{C}/\text{W}$
Case-to-Sink, Flat, Greased Surface ^c	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	
Maximum Junction-to-Ambient (PCB Mount) ^d	R_{thJA}	-	40	

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	250	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$	-	0.33	-	V/ $^{\circ}\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 250\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 200\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 150\text{ }^{\circ}\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 8.4\text{ A}^b$	-	-	0.240	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 8.4\text{ A}^b$	8.8	-	-	S



SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5		-	1060	-	pF
Output Capacitance	C_{oss}			-	140	-	
Reverse Transfer Capacitance	C_{rss}			-	38	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 8.4\text{ A}$, $V_{DS} = 200\text{ V}$, see fig. 6 and 13 ^b	-	-	54	nC
Gate-Source Charge	Q_{gs}			-	-	9.2	
Gate-Drain Charge	Q_{gd}			-	-	26	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 125\text{ V}$, $I_D = 8.4\text{ A}$, $R_G = 6.2\text{ }\Omega$, $V_{GS} = 10\text{ V}$, see fig. 10 ^b		-	10	-	ns
Rise Time	t_r			-	21	-	
Turn-Off Delay Time	$t_{d(off)}$			-	30	-	
Fall Time	t_f			-	17	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	14	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	56	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 14\text{ A}$, $V_{GS} = 0\text{ V}$ ^b		-	-	1.3	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = 14\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$ ^b		-	165	250	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	1.0	1.6	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
c. This is only applied to TO-220 package.
d. When mounted on 1" square PCB (fr-4 or G-10 material).

TYPICAL CHARACTERISTICS $25\text{ }^{\circ}\text{C}$, unless otherwise noted

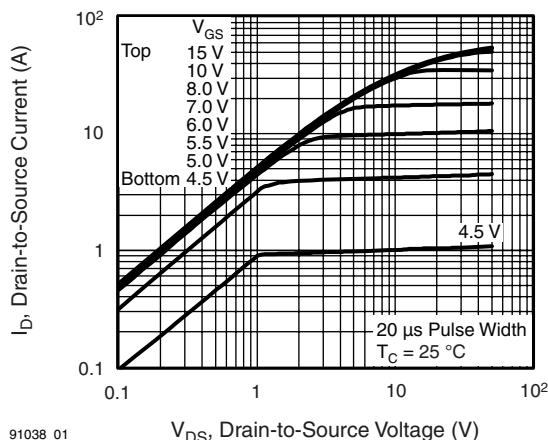


Fig. 1 - Typical Output Characteristics

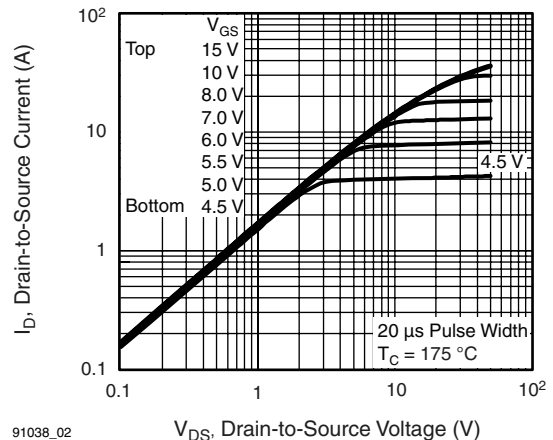


Fig. 2 - Typical Output Characteristics

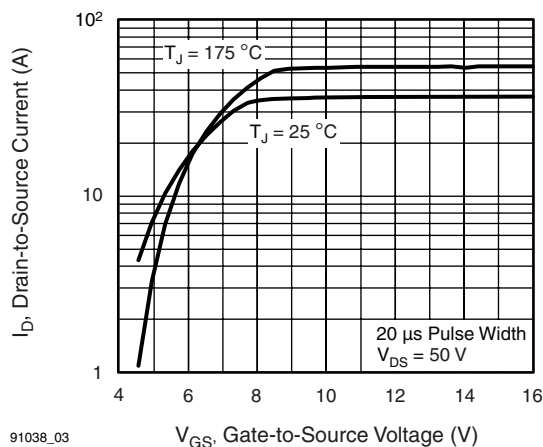


Fig. 3 - Typical Transfer Characteristics

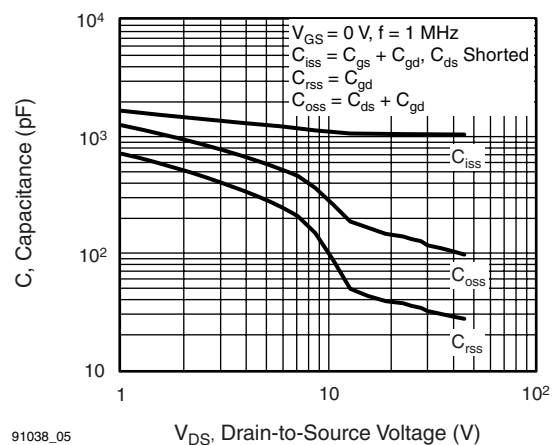


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

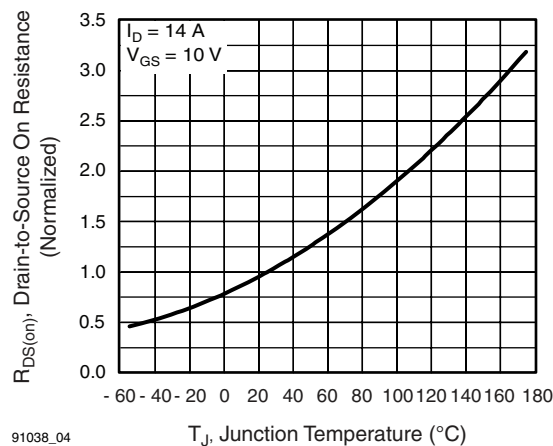


Fig. 4 - Normalized On-Resistance vs. Temperature

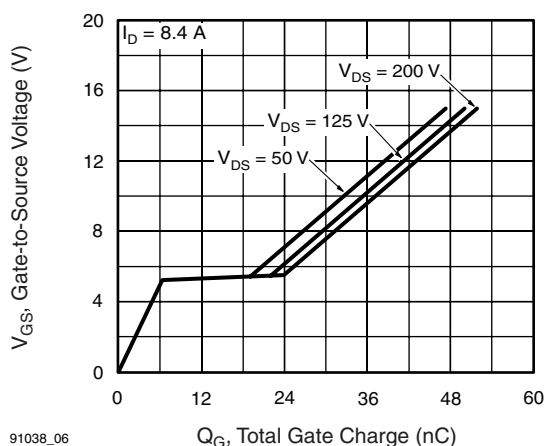


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

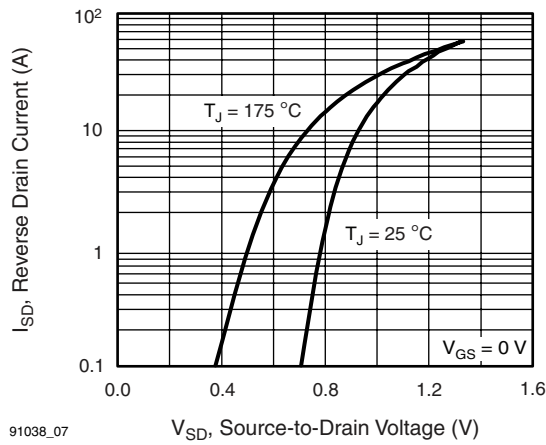


Fig. 7 - Typical Source-Drain Diode Forward Voltage

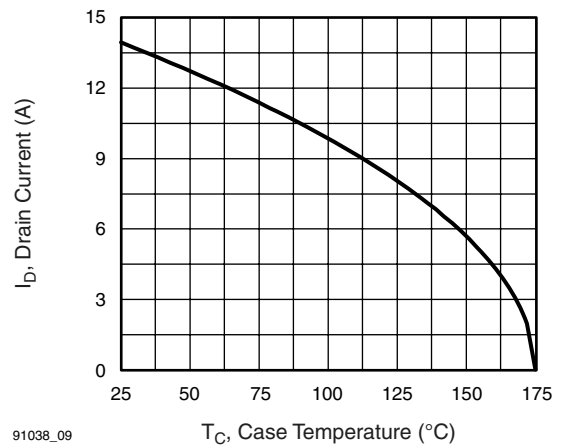


Fig. 9 - Maximum Drain Current vs. Case Temperature

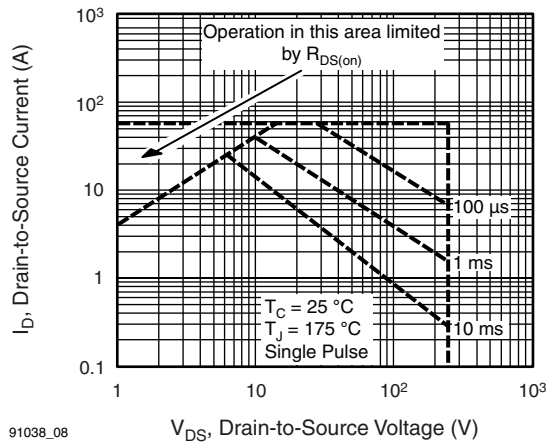


Fig. 8 - Maximum Safe Operating Area

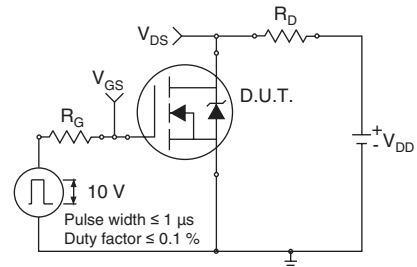


Fig. 10a - Switching Time Test Circuit

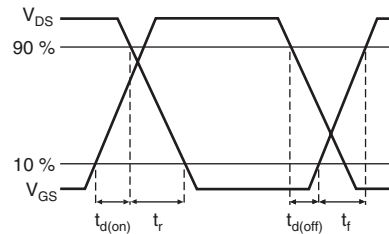


Fig. 10b - Switching Time Waveforms

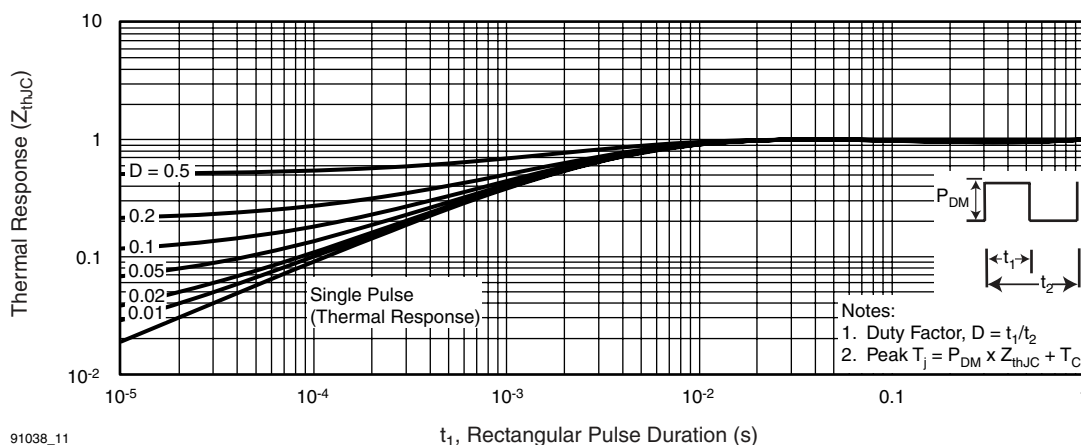


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

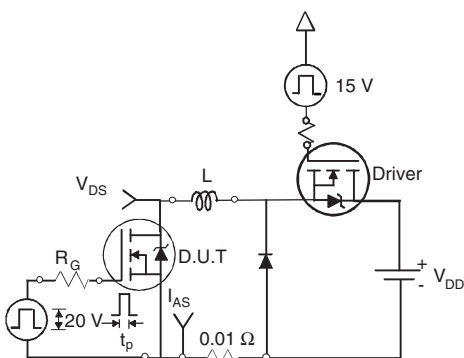


Fig. 12a - Unclamped Inductive Test Circuit

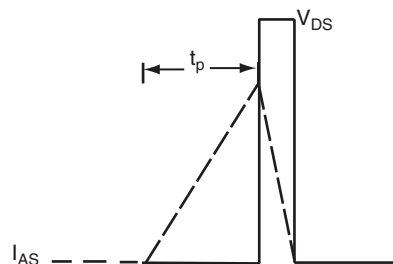


Fig. 12b - Unclamped Inductive Waveforms

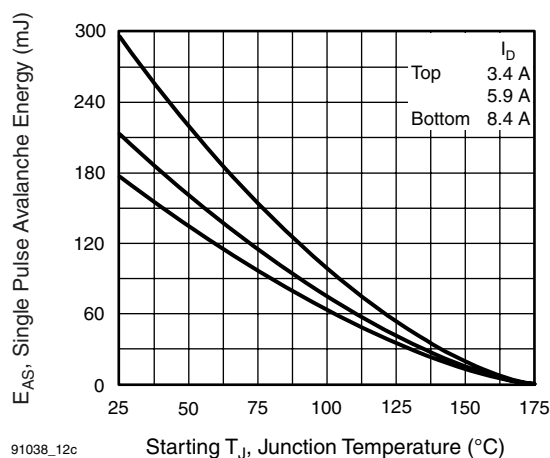


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

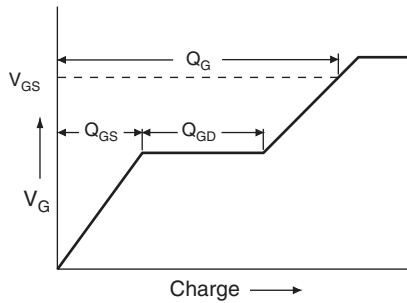


Fig. 13a - Basic Gate Charge Waveform

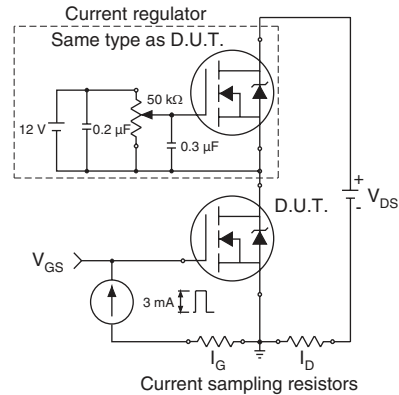
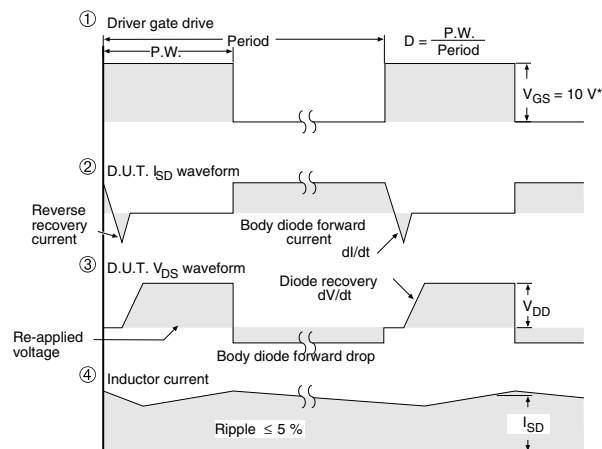
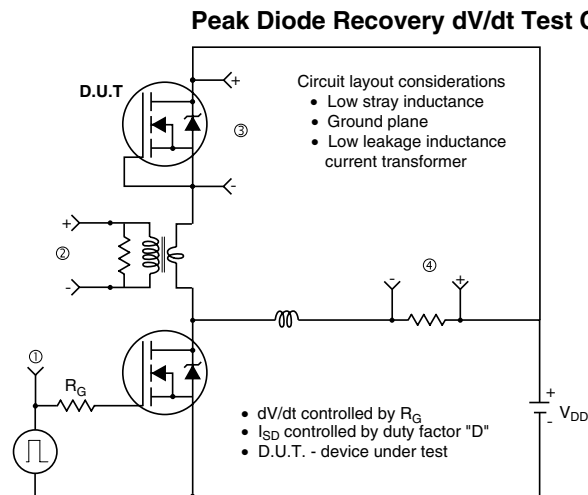


Fig. 13b - Gate Charge Test Circuit



* $V_{GS} = 5V$ for logic level devices and $3V$ drive devices

Fig. 14 - For N-Channel

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