

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: VS-ENM040M60P
Manufacturer: Vishay General Semiconductor - Diodes Division
Package: -
Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/vishay-general-semiconductor-diodes-division-vs-enm040m60p.html>

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Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



EMIPAK 1B PressFit Power Module

800 V Half Controlled Single Phase Bridge, 20 A

600 V PFC and Half Bridge MOSFET, 40 A



EMIPAK 1B
(package example)

PRIMARY CHARACTERISTICS	
HALF CONTROLLED SINGLE PHASE BRIDGE	
I_O at $T_{SINK} = 115\text{ }^{\circ}\text{C}$	20 A
D1, D2	
V_{RRM}	800 V
V_{FM} typical at 20 A	1.10 V
SCR1, SCR2	
V_{RRM}/V_{DRM}	800 V
V_{TM} typical at 20 A	1.29 V
QB1 - QB2 - QB3 MOSFET	
V_{DSS}	600 V
$R_{DS(on)}$ typical at $I_C = 40\text{ A}$	37 m Ω
I_D at $T_{SINK} = 39\text{ }^{\circ}\text{C}$	40 A
D3 SILICON CARBIDE CLAMP DIODE	
V_{RRM}	600 V
V_{FM} typical at 30 A	1.72 V
I_F at $T_C = 46\text{ }^{\circ}\text{C}$	30 A
Type	Modules - MOSFET
Package	EMIPAK 1B
Circuit configuration	Half controlled input bridge plus MOSFET boost PFC leg and MOSFET half bridge inverter

FEATURES

- E series power MOSFET with fast body diode
- MOAT and SiC diode technology
- Thyristor phase control
- Exposed Al_2O_3 substrate with low thermal resistance
- Low input capacitance
- Low switching and conduction losses
- Ultra low gate charge Q_g
- Low internal inductances
- Qualified using AQG324 guideline as reference
- PressFit pins locking technology
PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT

DESCRIPTION

The EMIPAK 1B package is easy to use thanks to the PressFit pins. The exposed substrate provides improved thermal performance.

The optimized layout also helps to minimize stray parameters, allowing for better EMI performance.

PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and international patents.



ABSOLUTE MAXIMUM RATINGS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Operating junction temperature	T_J		150	$^{\circ}\text{C}$
Storage temperature range	T_{Stg}		-40 to +150	
RMS isolation voltage	V_{ISOL}	$T_J = 25\text{ }^{\circ}\text{C}$, all terminals shorted, $f = 50\text{ Hz}$, $t = 1\text{ s}$	3500	V
HALF CONTROLLED SINGLE PHASE BRIDGE				
Maximum DC output current of bridge	I_O	$T_{\text{SINK}} = 25\text{ }^{\circ}\text{C}$	44	A
		$T_{\text{SINK}} = 80\text{ }^{\circ}\text{C}$	31	
One-cycle non-repetitive on-state peak or forward current	$I_{\text{FSM}}/I_{\text{TSM}}$	10 ms sine or 6 ms rectangular pulse, $T_J = 150\text{ }^{\circ}\text{C}$, no voltage reapplied	273	
Maximum I^2t for fusing	I^2t	10 ms sine pulse, no voltage reapplied	374	A^2s
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	$t = 0.1\text{ ms}$ to 10 ms , no voltage reapplied	3740	$\text{A}^2\sqrt{\text{s}}$
Value of threshold voltage	$V_{\text{F(TO)}}$	$T_J = 150\text{ }^{\circ}\text{C}$	1.04	V
Slope resistance	r_t	$T_J = 150\text{ }^{\circ}\text{C}$	38.9	$\text{m}\Omega$
Repetitive peak reverse diode	V_{RRM}		800	V
Repetitive peak direct and reverse thyristor	$V_{\text{RRM}}/V_{\text{DRM}}$		800	V
Maximum critical rate of rise of off-state voltage - thyristor	dV/dt	$V_{\text{DRM}} = 80\%$ of rated voltage, $T_J = 125\text{ }^{\circ}\text{C}$	500	$\text{V}/\mu\text{s}$
Maximum non-repetitive rate of rise of turned on current - thyristor	dI/dt	$T_J = 125\text{ }^{\circ}\text{C}$	150	$\text{A}/\mu\text{s}$
QB1 - QB2 - QB3 MOSFET				
Drain to source voltage	V_{DSS}		600	V
Gate to source voltage	V_{GS}		± 30	
Pulsed drain current	I_{DM}	$V_{\text{GS}} = 10\text{ V}$	135	A
Continuous drain current	I_D	$T_{\text{SINK}} = 25\text{ }^{\circ}\text{C}$	42	A
		$T_{\text{SINK}} = 80\text{ }^{\circ}\text{C}$	32	
Power dissipation	P_D	$T_{\text{SINK}} = 25\text{ }^{\circ}\text{C}$	174	W
		$T_{\text{SINK}} = 80\text{ }^{\circ}\text{C}$	97	
Single pulse avalanche energy	E_{AS}	$L = 10\text{ mH}$, $I_{\text{AS}} = 23\text{ A}$, $T_J = 25\text{ }^{\circ}\text{C}$	2645	mJ
Pulsed source current (body diode)	I_{SM}		135	A
D3 SILICON CARBIDE CLAMP DIODE				
Cathode to anode voltage	V_{RRM}		600	V
Single pulse forward current	I_{FSM}	10 ms sine or 6 ms rectangular pulse, $T_J = 25\text{ }^{\circ}\text{C}$	234	A
Diode continuous forward current	I_F	$T_{\text{SINK}} = 25\text{ }^{\circ}\text{C}$	33	A
		$T_{\text{SINK}} = 80\text{ }^{\circ}\text{C}$	23	
Power dissipation	P_D	$T_{\text{SINK}} = 25\text{ }^{\circ}\text{C}$	96	W
		$T_{\text{SINK}} = 80\text{ }^{\circ}\text{C}$	54	



ELECTRICAL SPECIFICATIONS (T _J = 25 °C unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
INPUT SINGLE PHASE BRIDGE						
D1, D2						
Forward voltage drop	V _{FM}	I _F = 20 A	-	1.10	1.32	V
		I _F = 20 A, T _J = 150°C	-	1.02	-	
Breakdown voltage	V _{BR}	I _R = 500 μA	800	-	-	V
Reverse leakage current	I _{RM}	V _R = 800 V	-	0.7	100	μA
		V _R = 800 V, T _J = 150 °C	-	0.7	-	mA
SCR1, SCR2						
Peak on state voltage	V _{TM}	I _{TM} = 20 A	-	1.29	1.70	V
		I _{TM} = 20 A, T _J = 150 °C	-	1.24	-	
Breakdown voltage	V _{RRM} /V _{DRM}	I _R = 500 μA	800	-	-	V
Reverse and direct leakage current	I _{RM} /I _{DM}	V _R = 800 V	-	1.0	100	μA
		V _R = 800 V, T _J = 150°C	-	4.5	-	mA
QB1 - QB2 - QB3 MOSFET						
Drain to source breakdown voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 250 μA	600	-	-	mΩ
Drain to source on resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 40 A	-	37	48	
		V _{GS} = 10 V, I _D = 40 A, T _J = 150 °C	-	87	-	
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.8	2.7	4.4	V
Temperature coefficient of threshold voltage	ΔV _{GS(th)} /ΔT _J	V _{DS} = V _{GS} , I _D = 250 μA (25 °C to 125 °C)	-	-11.4	-	mV/°C
Forward transconductance	g _{fs}	V _{DS} = 20 V, I _D = 40 A	-	48	-	S
Transfer characteristics	V _{GS}	V _{DS} = 20 V, I _D = 40 A	-	5.3	-	V
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 600 V	-	0.7	10	μA
		V _{GS} = 0 V, V _{DS} = 600 V, T _J = 150 °C	-	1.1	-	mA
Gate to source leakage current	I _{GSS}	V _{GS} = ± 20 V, V _{DS} = 0 V	-	-	± 150	nA
QB1 - QB2 - QB3 MOSFET BODY DIODE						
Source-to-drain voltage drop	V _{SD}	I _{SD} = 40 A, V _{GS} = 0 V	-	0.92	1.32	V
D3 SILICON CARBIDE CLAMP DIODE						
Forward voltage drop	V _{FM}	I _F = 30 A	-	1.72	1.98	V
		I _F = 30 A, T _J = 150 °C	-	2.37	-	
Breakdown voltage	V _{BR}	I _R = 1.5 mA	600	-	-	V
Reverse leakage current	I _{RM}	V _R = 600 V	-	0.6	300	μA
		V _R = 600 V, T _J = 150 °C	-	4.2	-	

TRIGGERING ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
SCR1, SCR2				
Maximum peak gate power	P_{GM}		8.0	W
Maximum average gate power	$P_{G(AV)}$		2.0	W
Maximum peak gate current	I_{GM}		1.5	A
Maximum peak negative gate voltage	V_{GM}		10	V
Maximum gate voltage required to trigger	V_{GT}	$T_J = 25\text{ }^{\circ}\text{C}$, anode supply = 6 V resistive load	2.0	V
		$T_J = 125\text{ }^{\circ}\text{C}$, anode supply = 6 V resistive load	0.75	
Maximum gate current required to trigger	I_{GT}	$T_J = 25\text{ }^{\circ}\text{C}$, anode supply = 6 V resistive load	45	mA
		$T_J = 125\text{ }^{\circ}\text{C}$, anode supply = 6 V resistive load	14	
Maximum gate voltage that will not trigger	V_{GD}	$T_J = 125\text{ }^{\circ}\text{C}$, 100 % V_{DRM} applied	0.2	V
Maximum gate current that will not trigger	I_{GD}	$T_J = 125\text{ }^{\circ}\text{C}$, 100 % V_{DRM} applied	1.0	mA



SWITCHING ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
SCR1, SCR2				
Typical turn-on time	t_{gt}	$T_J = 25\text{ }^{\circ}\text{C}$	0.9	μs
Typical reverse recovery time	t_{rr}	$T_J = 125\text{ }^{\circ}\text{C}$	4	
Typical turn-off time	t_g	$T_J = 125\text{ }^{\circ}\text{C}$	110	

SWITCHING CHARACTERISTICS (T _J = 25 °C unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
QB1 MOSFET with D3 CLAMP DIODE						
Total gate charge (turn-on)	Q _g	I _D = 32 A, V _{DS} = 480 V, V _{GS} = 10 V	-	240	-	nC
Gate to source charge (turn-on)	Q _{gs}		-	58	-	
Gate to drain charge (turn-on)	Q _{gd}		-	96	-	
Turn-on switching loss	E _{ON}	I _D = 40 A, V _{DD} = 450 V, V _{GS} = +10 V / -10 V, R _g = 10 Ω, L = 500 μH	-	0.53	-	mJ
Turn-on delay time	t _{d(on)}		-	43	-	ns
Rise time	t _r		-	26	-	
Turn-off switching loss	E _{OFF}		-	0.19	-	mJ
Turn-off delay time	t _{d(off)}		-	160	-	ns
Fall time	t _f		-	18	-	
Turn-on switching loss	E _{ON}	I _D = 40 A, V _{DD} = 450 V, V _{GS} = +10 V / -10 V, R _g = 10 Ω, L = 500 μH, T _J = 125 °C	-	0.63	-	mJ
Turn-on delay time	t _{d(on)}		-	39	-	ns
Rise time	t _r		-	29	-	
Turn-off switching loss	E _{OFF}		-	0.23	-	mJ
Turn-off delay time	t _{d(off)}		-	162	-	ns
Fall time	t _f		-	19	-	
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz	-	7500	-	pF
Output capacitance	C _{oss}		-	378	-	
Reverse transfer capacitance	C _{rss}		-	5	-	
Reverse bias safe operating area	RBSOA	T _J = 150 °C, I _D = 100 A, V _{DD} = 400 V, V _P = 600 V, R _g = 10 Ω, V _{GS} = +10 V / 0 V				
QB2 - QB3 MOSFET						
Total gate charge (turn-on)	Q _g	I _D = 32 A, V _{DS} = 480 V, V _{GS} = 10 V	-	240	-	nC
Gate-source charge	Q _{gs}		-	58	-	
Gate-drain charge	Q _{gd}		-	96	-	
Turn-off switching loss	E _{OFF}	I _D = 40 A, V _{DD} = 450 V, V _{GS} = +10 V / -10 V, R _g = 10 Ω, L = 500 μH	-	0.17	-	mJ
Turn-off delay time	t _{d(off)}		-	157	-	ns
Fall time	t _f		-	18	-	
Turn-off switching loss	E _{OFF}	I _D = 40 A, V _{DD} = 450 V, V _{GS} = +10 V / -10 V, R _g = 10 Ω, L = 500 μH, T _J = 125 °C	-	0.19	-	mJ
Turn-off delay time	t _{d(off)}		-	164	-	ns
Fall time	t _f		-	19	-	
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz	-	7500	-	pF
Output capacitance	C _{oss}		-	378	-	
Reverse transfer capacitance	C _{rss}		-	5	-	
Reverse bias safe operating area	RBSOA	T _J = 150 °C, I _D = 150 A, V _{DD} = 400 V, V _P = 600 V, R _g = 10 Ω, V _{GS} = +10 V / 0 V				
QB1 - QB2 - QB3 MOSFET BODY DIODE						
Diode reverse recovery time	t _{rr}	V _R = 200 V, T _J = 25 °C, I _S = 40 A, dI/dt = 100 A/μs	-	211	-	ns
Diode reverse recovery current	I _{rr}		-	17	-	A
Diode reverse recovery charge	Q _{rr}		-	1775	-	nC
D3 SILICON CARBIDE CLAMP DIODE						
Total capacitive charge	Q _C	V _R = 600 V, I _F = 30 A, dI/dt = 500 A/μs	-	75	-	nC

**INTERNAL NTC - THERMISTOR SPECIFICATIONS**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUE	UNITS
Resistance	R25	$T_C = 25\text{ }^{\circ}\text{C}$	5000	Ω
	R100	$T_C = 100\text{ }^{\circ}\text{C}$	$493 \pm 5\%$	
B-value	$B_{25/50}$	$R_2 = R_{25} \exp. [B_{25/50}(1/T_2 - 1/(298.15\text{K}))]$	$3375 \pm 5\%$	K
Maximum operating temperature			220	$^{\circ}\text{C}$
Dissipation constant			2	mW/ $^{\circ}\text{C}$
Thermal time constant			8	s

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
INPUT SINGLE PHASE BRIDGE - Junction to sink thermal resistance (per diode) ⁽¹⁾	R_{thJS}	-	1.28	-	$^{\circ}\text{C}/\text{W}$
INPUT SINGLE PHASE BRIDGE - Junction to sink thermal resistance (per thyristor) ⁽¹⁾		-	1.11	-	
QB1 - QB2 - QB3 MOSFET - Junction to sink thermal resistance (per switch) ⁽¹⁾		-	0.64	-	
D3 SILICON CARBIDE CLAMP DIODE - Junction to sink thermal resistance (per diode) ⁽¹⁾		-	1.07	-	
Case to sink thermal resistance (per module) ⁽¹⁾		-	0.1	-	
Mounting torque (M4)		2	-	3	Nm
Weight		-	28	-	g

Note

⁽¹⁾ Mounting surface flat, smooth, and greased, $\lambda_{\text{grease}} = 0.67\text{ W/mK}$

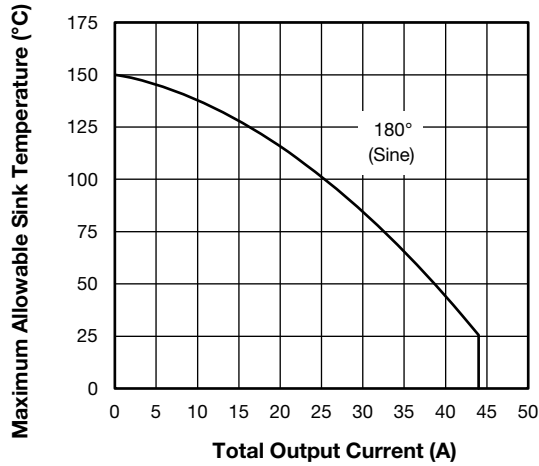


Fig. 1 - Current Rating Characteristics

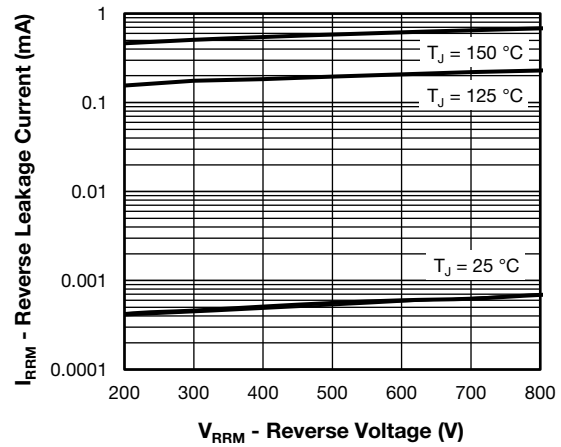


Fig. 4 - Typical D1 - D2 Reverse Current vs. Reverse Voltage

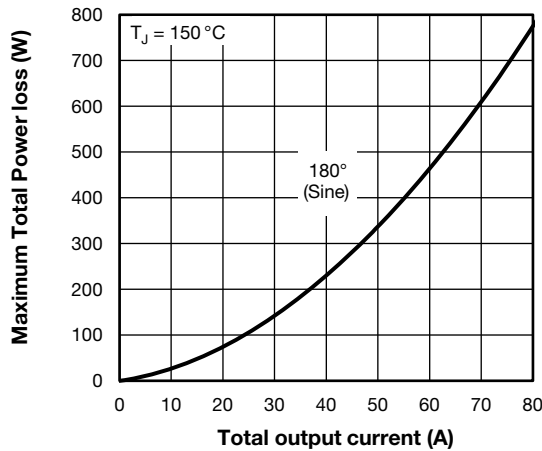


Fig. 2 - Total Power Loss Characteristics

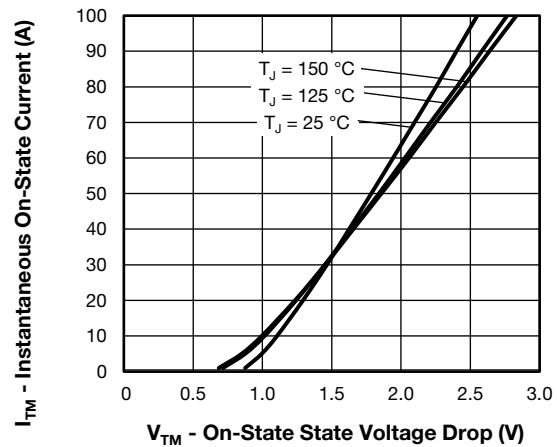


Fig. 5 - Typical Scr1 - Scr2 On-State Voltage Drop vs. Instantaneous On-State Current

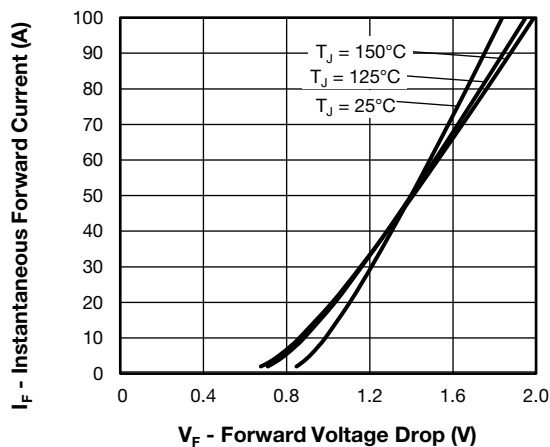


Fig. 3 - Typical D1 - D2 Forward Voltage Drop vs. Instantaneous Forward Current

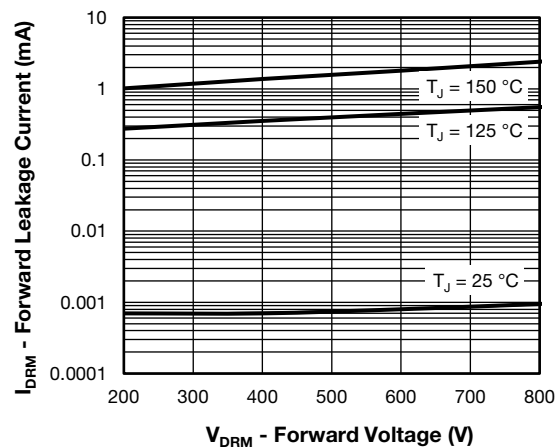


Fig. 6 - Typical Scr1 - Scr2 Forward Leakage Current vs. Direct Blocking Voltage

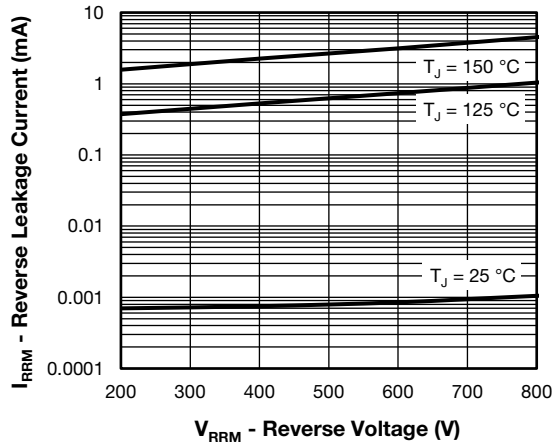


Fig. 7 - Typical Scr1 - Scr2 Reverse Leakage Current vs. Reverse Blocking Voltage

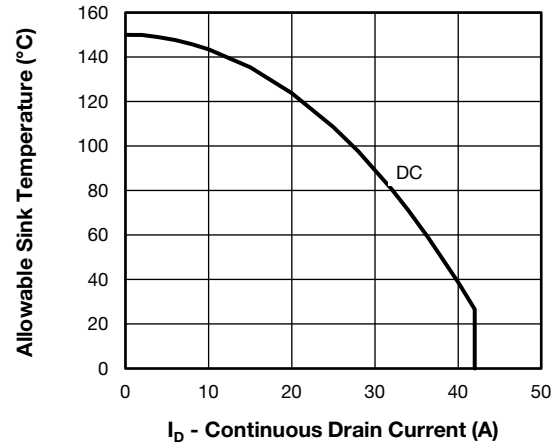


Fig. 10 - Maximum QB1 - QB3 Continuous Drain Current vs. Sink Temperature

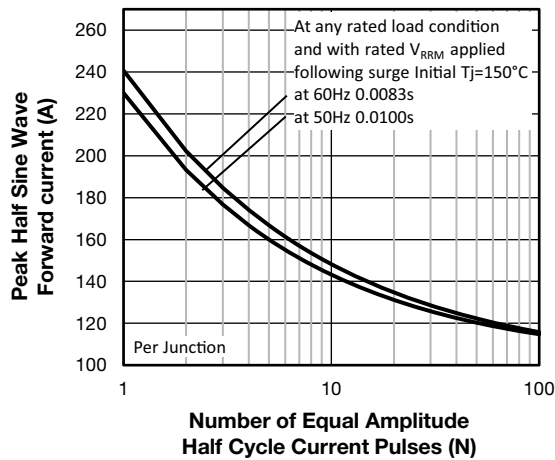


Fig. 8 - Maximum Non-Repetitive Surge Current vs. Number of Current Pulses

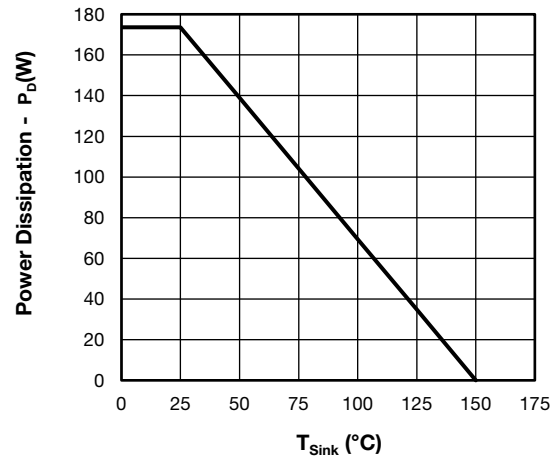


Fig. 11 - QB1 - QB3 Power Dissipation Curve

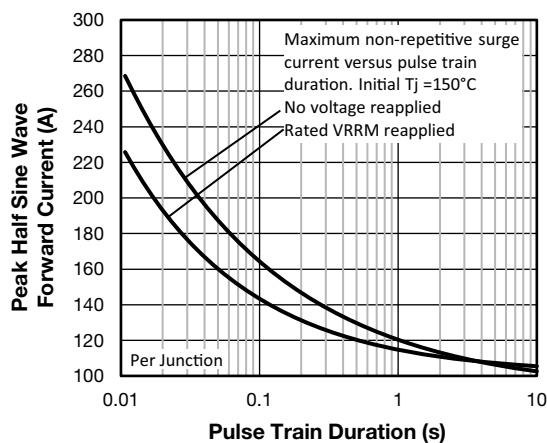
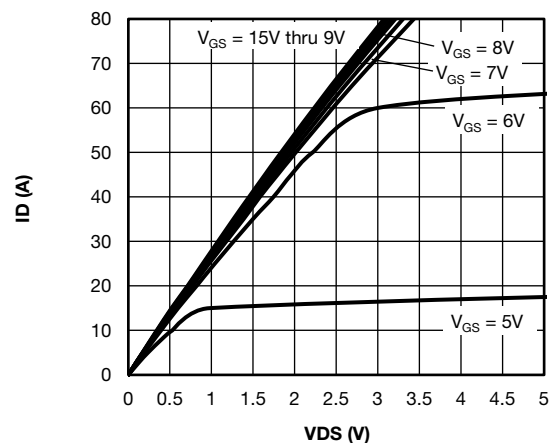


Fig. 9 - Maximum Non-Repetitive Surge Current vs. Pulse Train Duration

Fig. 12 - Typical QB1 - QB3 Drain to Source Current Output Characteristics at $T_J = 25\text{ °C}$

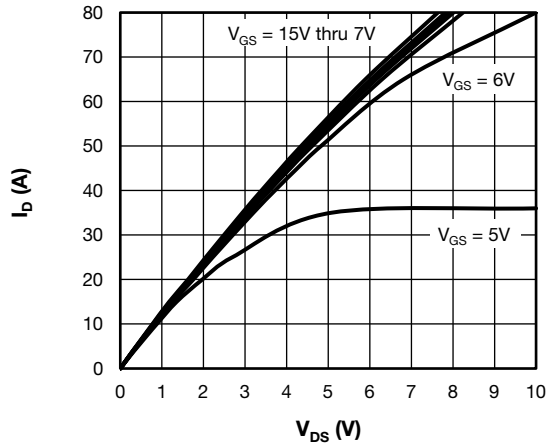


Fig. 13 - Typical QB1 - QB3
Drain to Source Current Output Characteristics at $T_J = 150\text{ }^{\circ}\text{C}$

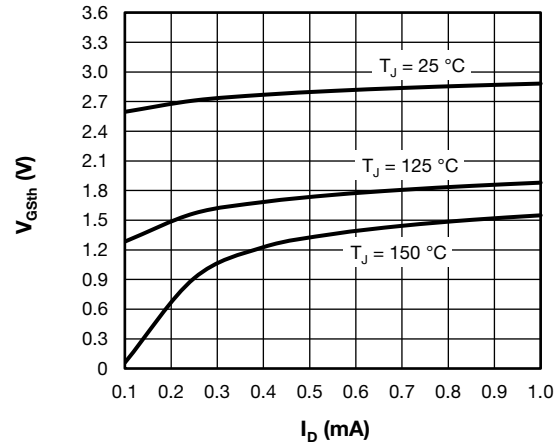


Fig. 16 - Typical QB1-QB3
Gate Threshold Voltage Characteristics

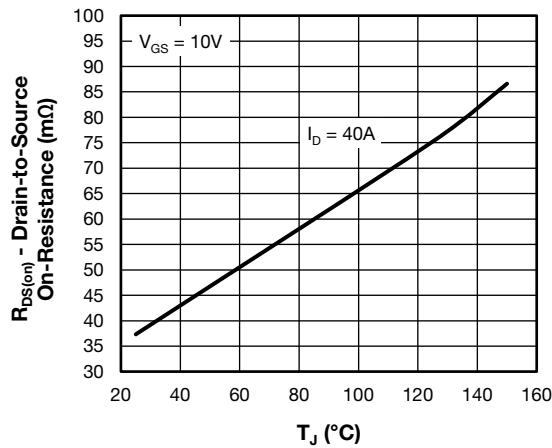


Fig. 14 - Typical QB1 - QB3
Drain-to-Source On-Resistance vs. Temperature

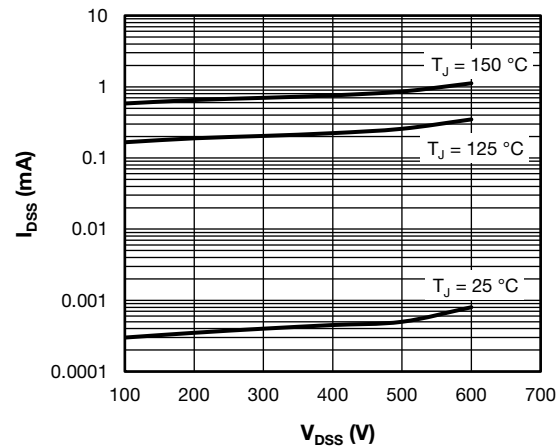


Fig. 17 - Typical QB1 - QB3
Zero Gate Voltage Drain Current

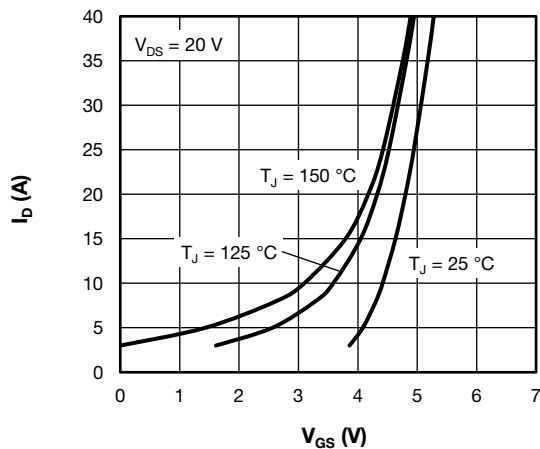


Fig. 15 - Typical QB1 - QB3
Transfer Characteristics

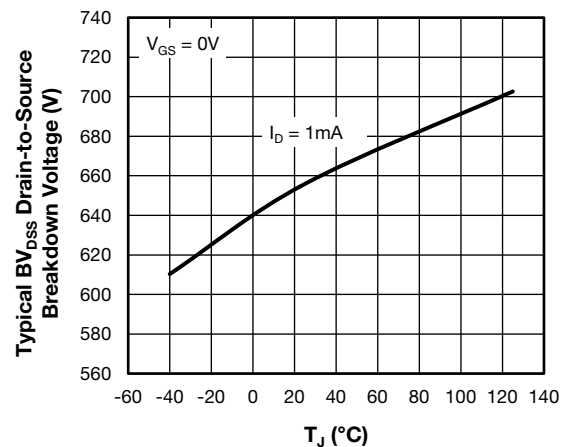


Fig. 18 - Typical QB1 - QB3
Drain to Source Breakdown Voltage vs. Temperature

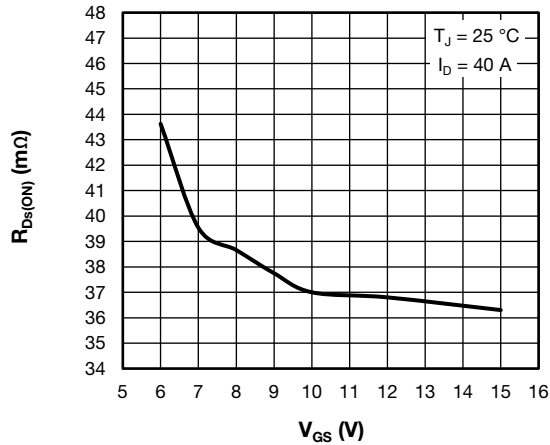


Fig. 19 - Typical QB1 - QB3
Drain - State Resistance vs. Gate-to-Source Voltage

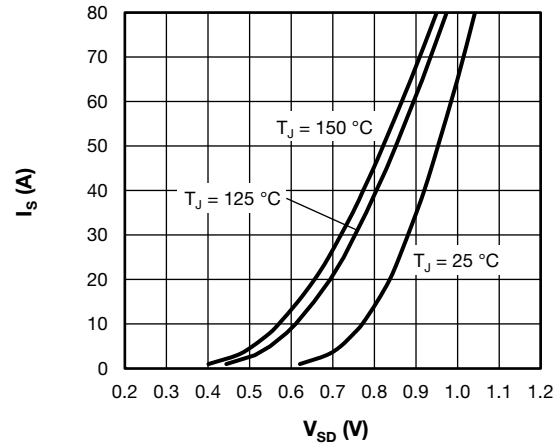


Fig. 22 - Typical QB1 - QB3
Body Diode Source-to-Drain Current Characteristics

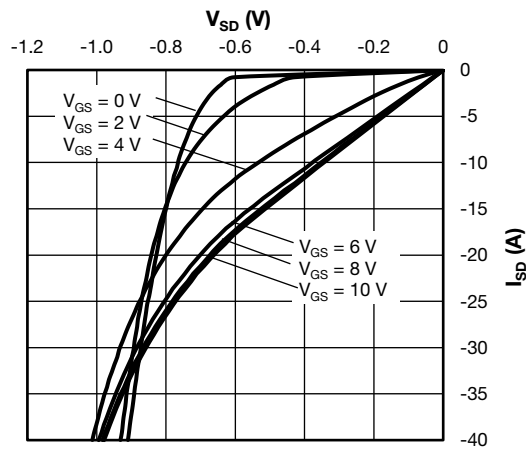


Fig. 20 - Typical QB1 - QB3
Source-to-Drain Current Characteristics at $T_J = 125\text{ °C}$

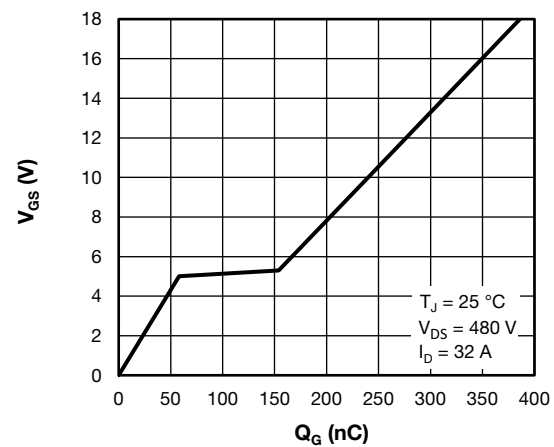


Fig. 23 - Typical QB1 - QB3
Gate charge vs. Gate-to-Source Voltage

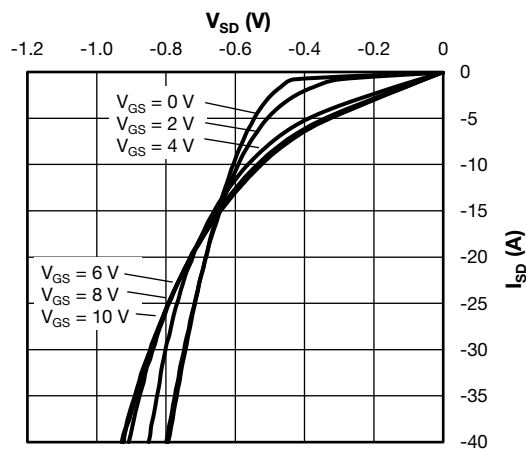


Fig. 21 - Typical QB1 - QB3
Source-to-Drain Current Characteristics at $T_J = 125\text{ °C}$

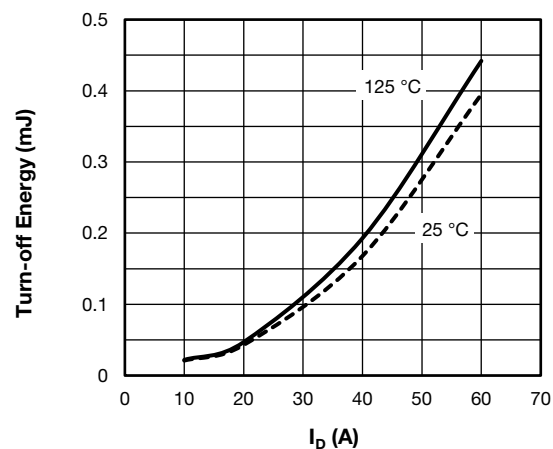


Fig. 24 - Typical QB2 - QB3 Turn-off Energy Loss vs. I_D
 $V_{DD} = 450\text{ V}$, $R_g = 10\text{ }\Omega$, $V_{GS} = \pm 10\text{ V}$, $L = 500\text{ }\mu\text{H}$

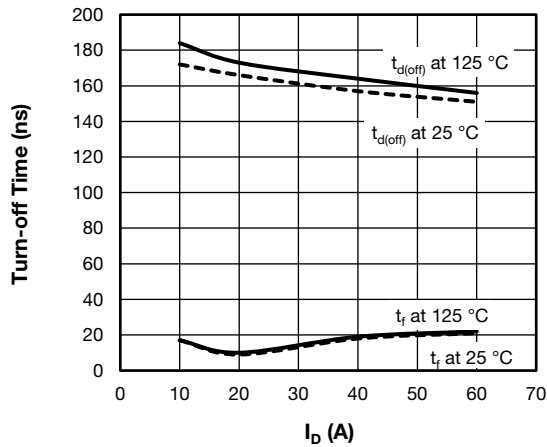


Fig. 25 - Typical QB2-QB3 Turn-off Switching Time vs I_D
 $V_{DD} = 450 \text{ V}$, $R_g = 10 \text{ } \Omega$, $V_{GS} = \pm 10 \text{ V}$, $L = 500 \text{ } \mu\text{H}$

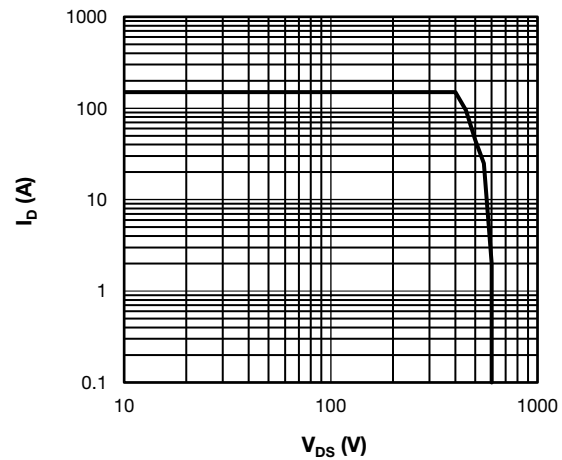


Fig. 28 - QB2 - QB3 MOSFET Reverse BIAS SOA
 $T_J = 150 \text{ } ^\circ\text{C}$, $V_{GS} = 10 \text{ V}$

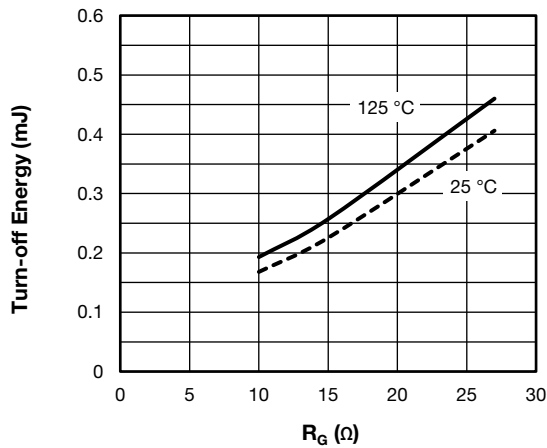


Fig. 26 - Typical QB2-QB3 Turn-off Energy Loss vs R_g
 $V_{DD} = 450 \text{ V}$, $I_D = 40 \text{ A}$, $V_{GS} = \pm 10 \text{ V}$, $L = 500 \text{ } \mu\text{H}$

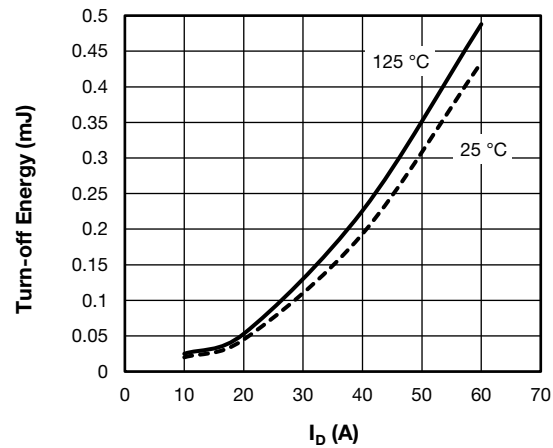


Fig. 29 - Typical QB1 Turn-off Energy Loss vs. I_D
 $V_{DD} = 450 \text{ V}$, $R_g = 10 \text{ } \Omega$, $V_{GS} = \pm 10 \text{ V}$, $L = 500 \text{ } \mu\text{H}$

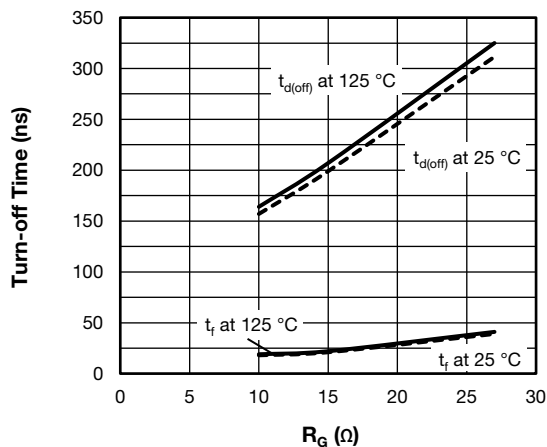


Fig. 27 - Typical QB2-QB3 Turn-off Switching Time vs R_g
 $V_{DD} = 450 \text{ V}$, $I_D = 40 \text{ A}$, $V_{GS} = \pm 10 \text{ V}$, $L = 500 \text{ } \mu\text{H}$

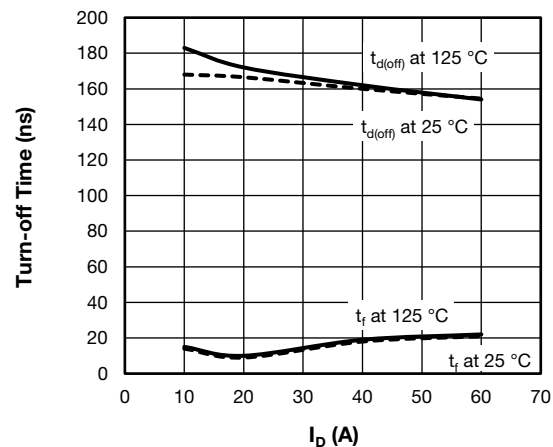


Fig. 30 - Typical QB1 Turn-off Switching Time vs. I_D
 $V_{DD} = 450 \text{ V}$, $R_g = 10 \text{ } \Omega$, $V_{GS} = \pm 10 \text{ V}$, $L = 500 \text{ } \mu\text{H}$

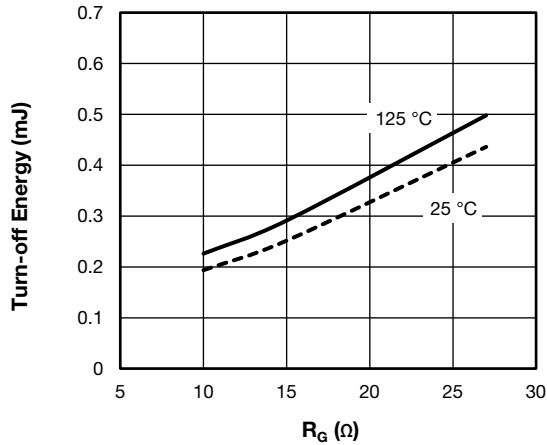


Fig. 31 - Typical QB1 Turn-off Energy Loss vs. R_g
 $V_{DD} = 450\text{ V}$, $I_D = 40\text{ A}$, $V_{GS} = \pm 10\text{ V}$, $L = 500\text{ }\mu\text{H}$

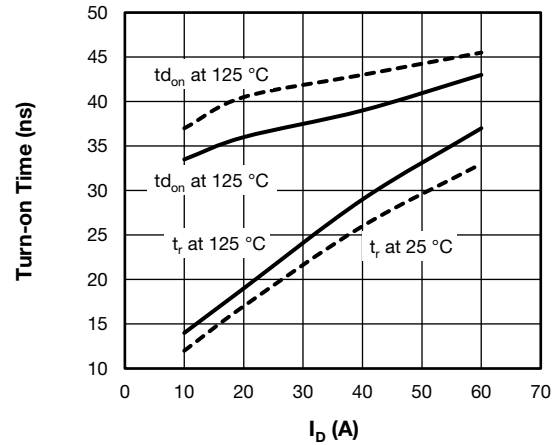


Fig. 34 - Typical QB1 Turn-on Switching Time vs. I_D
 $V_{DD} = 450\text{ V}$, $R_g = 10\text{ }\Omega$, $V_{GS} = \pm 10\text{ V}$, $L = 500\text{ }\mu\text{H}$

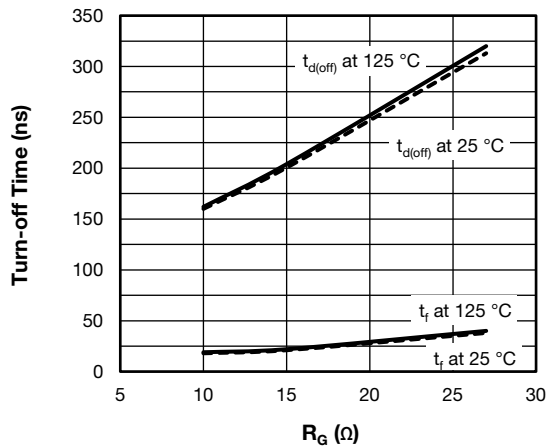


Fig. 32 - Typical QB1 Turn-off Switching Time vs. R_g
 $V_{DD} = 450\text{ V}$, $I_D = 40\text{ A}$, $V_{GS} = \pm 10\text{ V}$, $L = 500\text{ }\mu\text{H}$

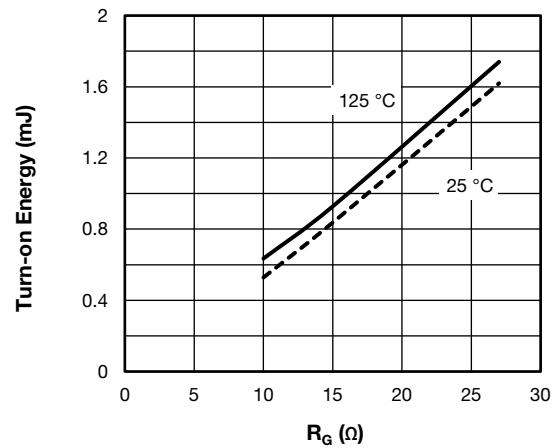


Fig. 35 - Typical QB1 Turn-on Energy Loss vs. R_g
 $V_{DD} = 450\text{ V}$, $I_D = 40\text{ A}$, $V_{GS} = \pm 10\text{ V}$, $L = 500\text{ }\mu\text{H}$

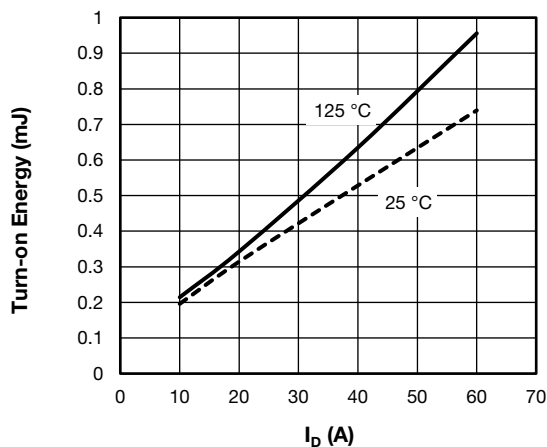


Fig. 33 - Typical QB1 Turn-on Energy Loss vs. I_D
 $V_{DD} = 450\text{ V}$, $R_g = 10\text{ }\Omega$, $V_{GS} = \pm 10\text{ V}$, $L = 500\text{ }\mu\text{H}$

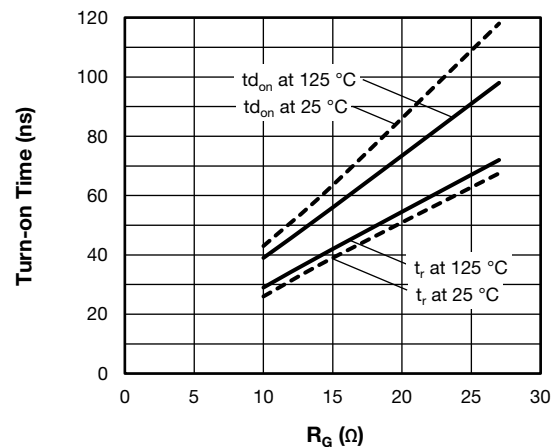


Fig. 36 - Typical QB1 Turn-on Switching Time vs. R_g
 $V_{DD} = 450\text{ V}$, $I_D = 40\text{ A}$, $V_{GS} = \pm 10\text{ V}$, $L = 500\text{ }\mu\text{H}$

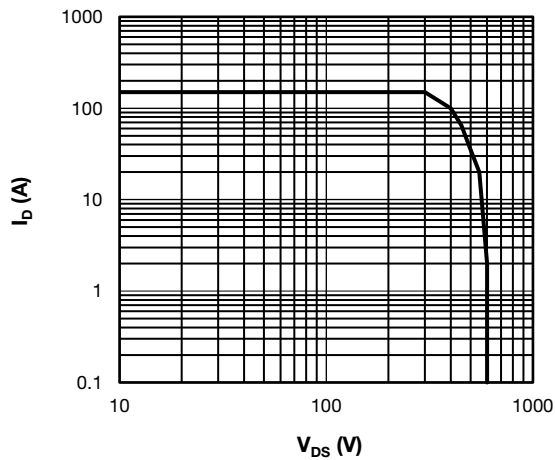


Fig. 37 - QB1 MOSFET Reverse BIAS SOA
 $T_J = 150\text{ °C}$, $V_{GS} = 10\text{ V}$

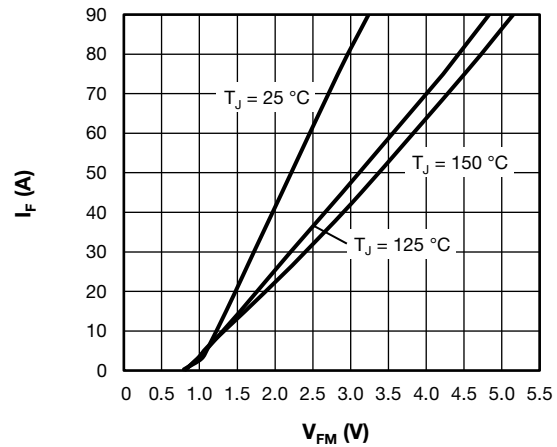


Fig. 39 - Typical D3 Diode Forward Characteristics

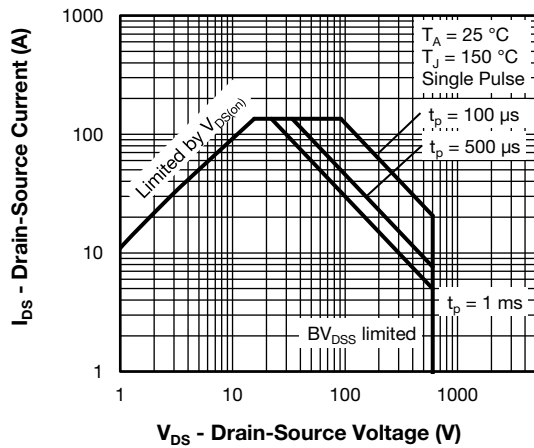


Fig. 38 - QB1 - QB3 Safe Operating Area

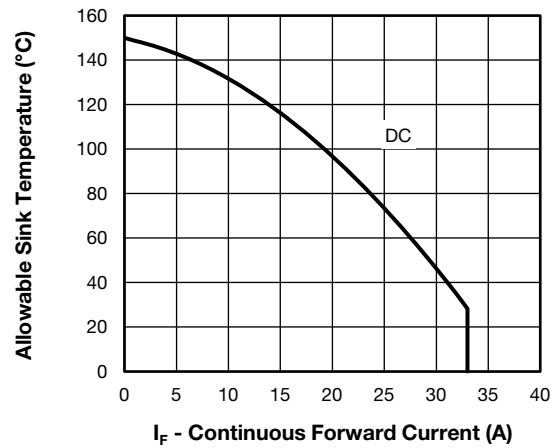


Fig. 40 - Maximum D3 Diode Continuous Forward Current vs. Sink Temperature

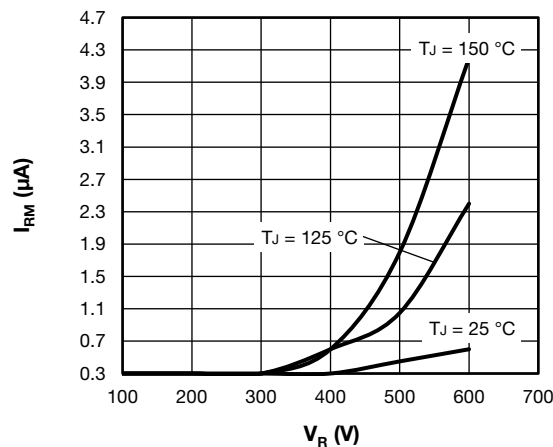
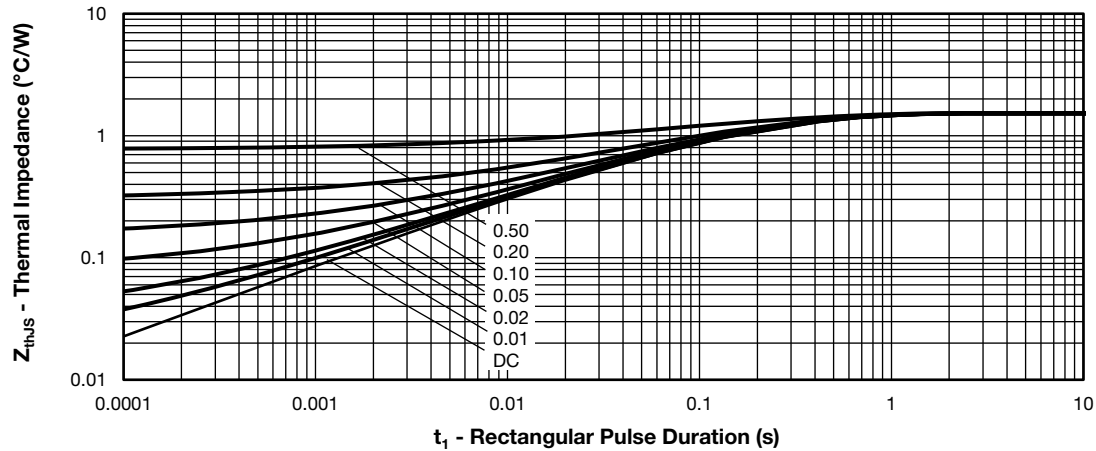
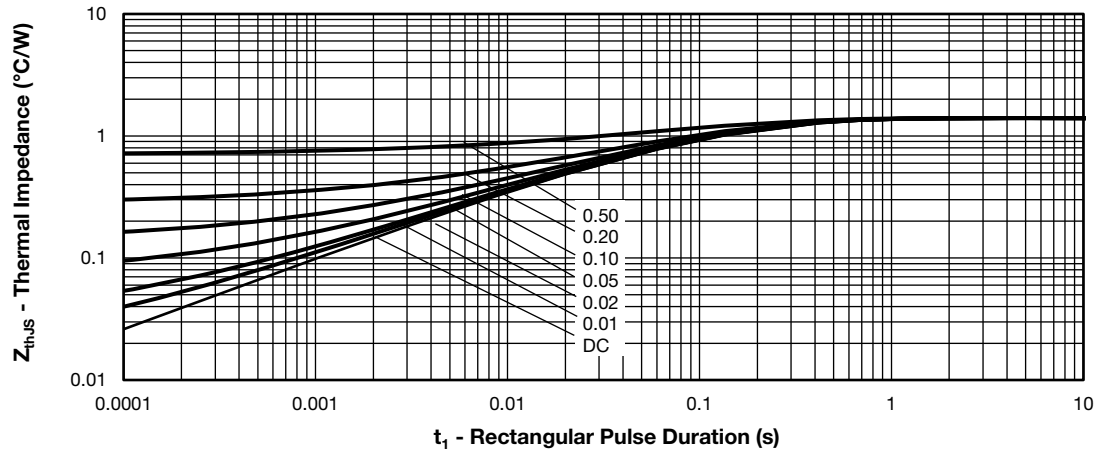
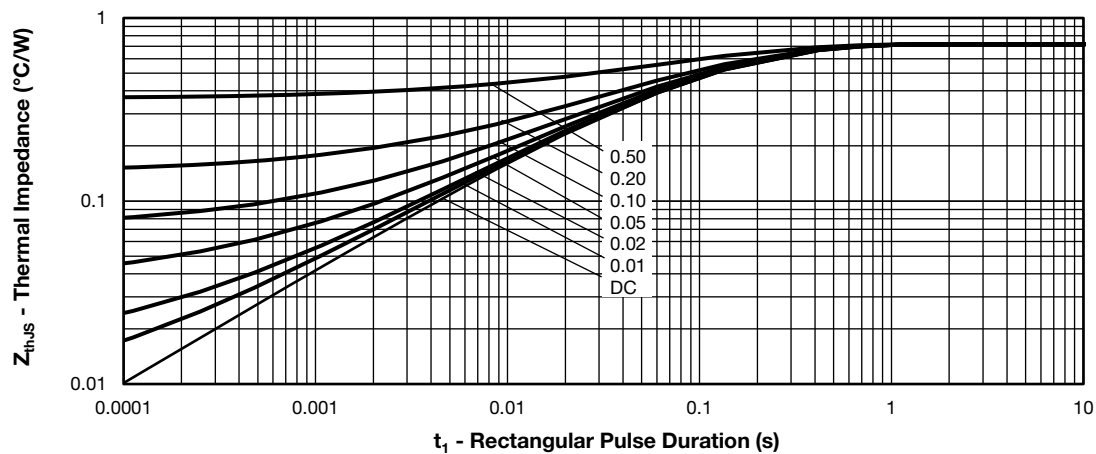
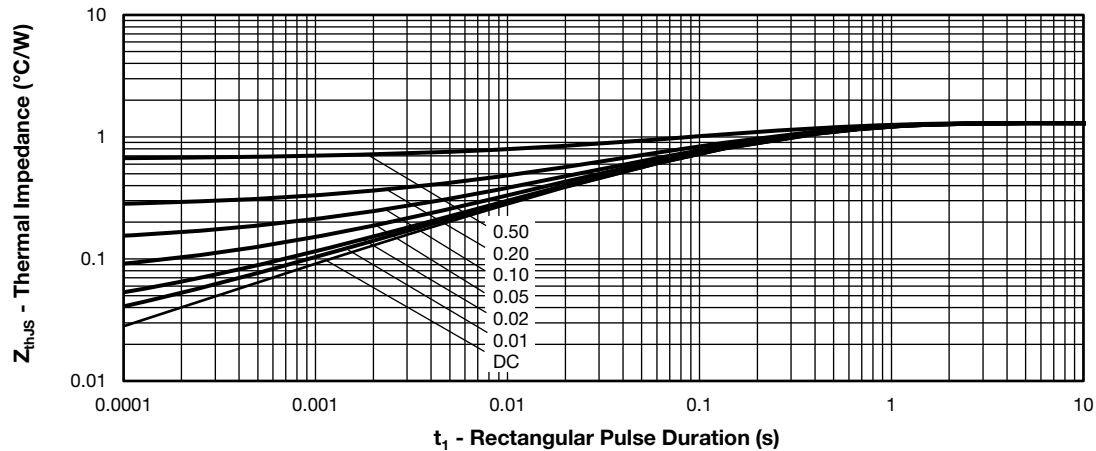


Fig. 41 - Typical D3 Diode Reverse Leakage Current

Fig. 42 - Maximum D1 - D2 Z_{thJS} Thermal Impedance CharacteristicFig. 43 - Maximum Scr1 - Scr2 Z_{thJS} Thermal Impedance CharacteristicFig. 44 - Maximum QB1 - QB3 Z_{thJS} Thermal Impedance Characteristic

Fig. 45 - Maximum D3 Z_{thJS} Thermal Impedance Characteristics

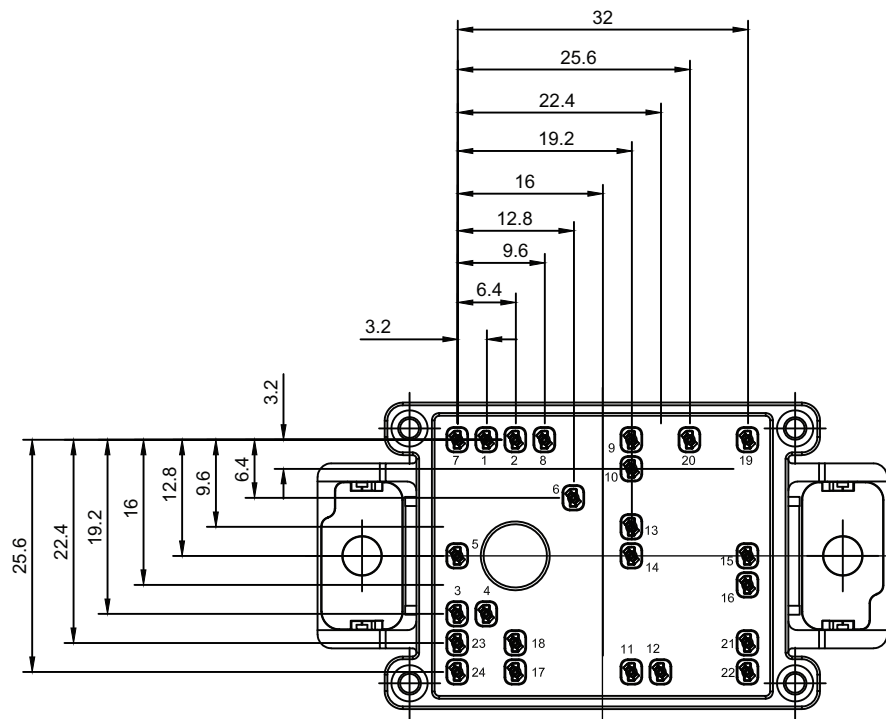
ORDERING INFORMATION TABLE

Device code	VS-	EN	M	040	M	60	P
	1	2	3	4	5	6	7
1	Vishay Semiconductors product						
2	Package indicator (EN = EMIPAK 1B)						
3	Circuit configuration (M = Half controlled input bridge plus MOSFET boost PFC leg and MOSFET half bridge inverter)						
4	Current rating (040 = 40 A)						
5	Switch die technology (M = SiC diodes + Power MOSFET + MOAT)						
6	Voltage rating (60 = 600 V)						
7	Diode technology (P = SiC diodes + MOAT + SCR)						

CIRCUIT CONFIGURATION		
CIRCUIT	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Half controlled input bridge plus MOSFET boost PFC leg and MOSFET half bridge inverter	M	



PACKAGE

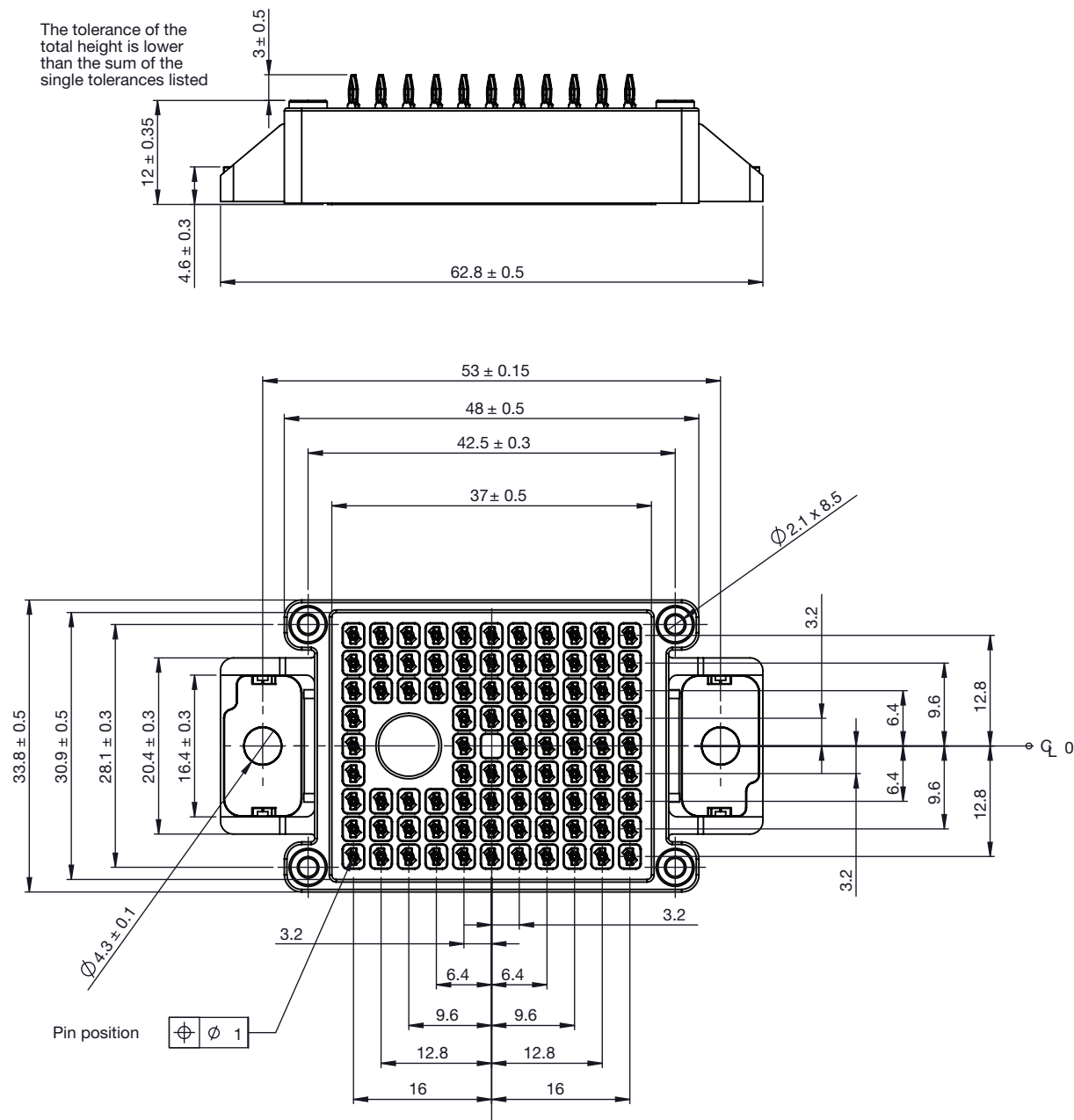


LINKS TO RELATED DOCUMENTS

Dimensions	www.vishay.com/doc?95558
Application Note	www.vishay.com/doc?95580

EMIPAK 1B

DIMENSIONS in millimeters





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