

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

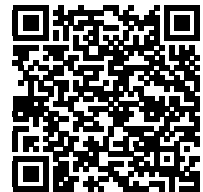
Part Number:	TK5P53D(T6RSS-Q)
Manufacturer:	Toshiba Semiconductor and Storage
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/toshiba-semiconductor-and-storage-tk5p53d-t6rss-q.html>

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Contact Information

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New & Original Components

Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

Secure sourcing support for OEM / EMS projects

Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

TK5P53D

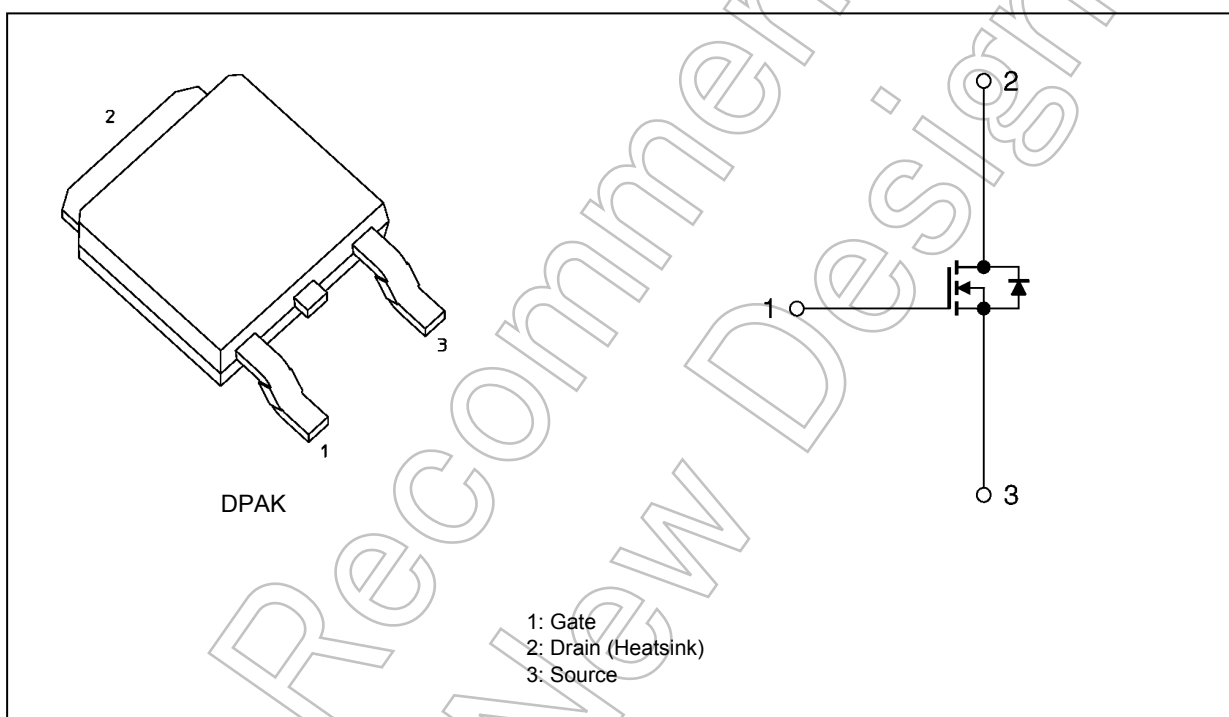
1. Applications

- Switching Voltage Regulators

2. Features

- (1) Low drain-source on-resistance : $R_{DS(ON)} = 1.2 \Omega$ (typ.)
- (2) High forward transfer admittance : $|Y_{fs}| = 2.8 \text{ S}$ (typ.)
- (3) Low leakage current : $I_{DSS} = 10 \mu\text{A}$ (max) ($V_{DS} = 525 \text{ V}$)
- (4) Enhancement mode : $V_{th} = 2.4 \text{ to } 4.4 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$)

3. Packaging and Internal Circuit



Start of commercial production
2009-12

4. Absolute Maximum Ratings (Note) ($T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	525	V
Gate-source voltage	V_{GS}	± 30	
Drain current (DC) (Note 1)	I_D	5	A
Drain current (pulsed) (Note 1)	I_{DP}	20	
Power dissipation ($T_c = 25\text{ }^{\circ}\text{C}$)	P_D	80	W
Single-pulse avalanche energy (Note 2)	E_{AS}	142	mJ
Avalanche current (Note 3)	I_{AR}	5	A
Repetitive avalanche energy (Note 3)	E_{AR}	8	mJ
Reverse drain current (DC) (Note 1)	I_{DR}	5	A
Reverse drain current (pulsed) (Note 1)	I_{DRP}	20	
Channel temperature	T_{ch}	150	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	1.56	$^{\circ}\text{C}/\text{W}$
Channel-to-ambient thermal resistance	$R_{th(ch-a)}$	125	

Note 1: Ensure that the channel temperature does not exceed $150\text{ }^{\circ}\text{C}$.

Note 2: $V_{DD} = 90\text{ V}$, $T_{ch} = 25\text{ }^{\circ}\text{C}$ (initial), $L = 9.72\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AR} = 5\text{ A}$

Note 3: Repetitive rating; pulse width limited by maximum channel temperature.

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

6. Electrical Characteristics

6.1. Static Characteristics ($T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 30\text{ V}$, $V_{DS} = 0\text{ V}$	—	—	± 1	μA
Drain cut-off current	I_{DSS}	$V_{DS} = 525\text{ V}$, $V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}$, $V_{GS} = 0\text{ V}$	525	—	—	V
Gate threshold voltage	V_{th}	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ mA}$	2.4	—	4.4	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}$, $I_D = 2.5\text{ A}$	—	1.2	1.5	Ω
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 10\text{ V}$, $I_D = 2.5\text{ A}$	0.7	2.8	—	S

6.2. Dynamic Characteristics ($T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	—	540	—	pF
Reverse transfer capacitance	C_{rss}		—	3	—	
Output capacitance	C_{oss}		—	60	—	
Switching time (rise time)	t_r	See Fig.6.2.1	—	18	—	ns
Switching time (turn-on time)	t_{on}		—	40	—	
Switching time (fall time)	t_f		—	8	—	
Switching time (turn-off time)	t_{off}		—	55	—	

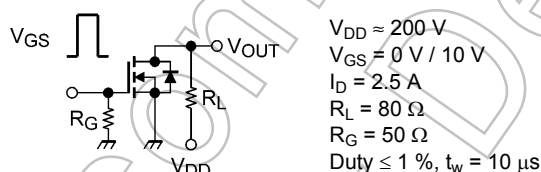


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics ($T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 400\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 5\text{ A}$	—	11	—	nC
Gate-source charge	Q_{gs}		—	6	—	
Gate-drain charge	Q_{gd}		—	5	—	

6.4. Source-Drain Characteristics ($T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	V_{DSF}	$I_{DR} = 5\text{ A}$, $V_{GS} = 0\text{ V}$	—	—	-1.7	V
Reverse recovery time	t_{rr}	$I_{DR} = 5\text{ A}$, $V_{GS} = 0\text{ V}$, $-di/dt = 100\text{ A}/\mu\text{s}$	—	1000	—	ns
Reverse recovery charge	Q_{rr}		—	6	—	μC

7. Marking

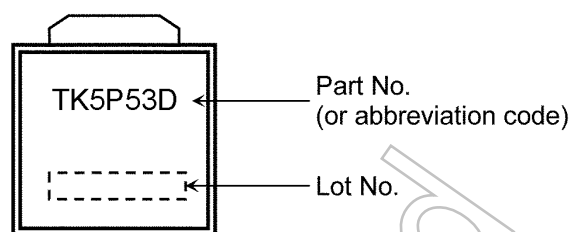


Fig. 7.1 Marking

Not Recommended
for New Design

8. Characteristics Curves (Note)

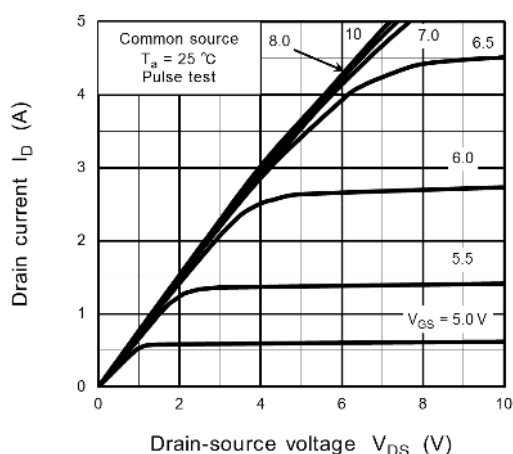


Fig. 8.1 $I_D - V_{DS}$

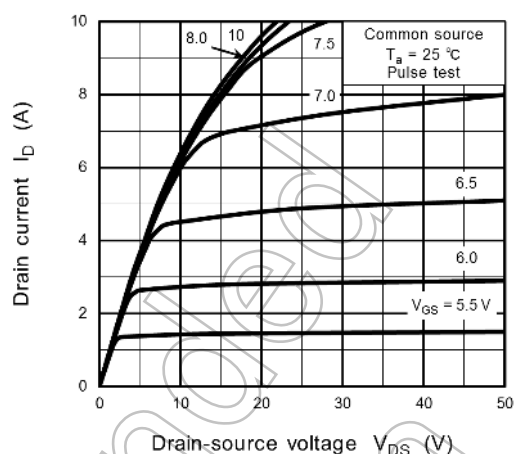


Fig. 8.2 $I_D - V_{DS}$

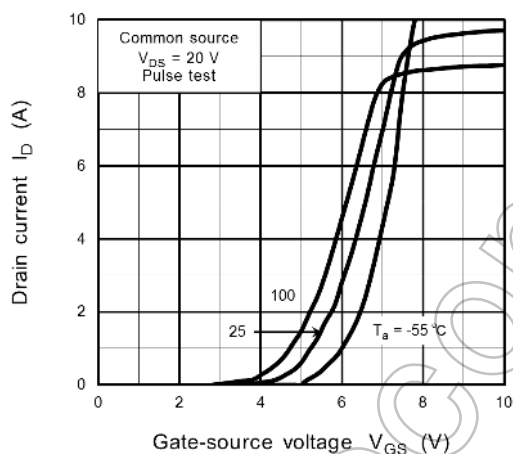


Fig. 8.3 $I_D - V_{GS}$

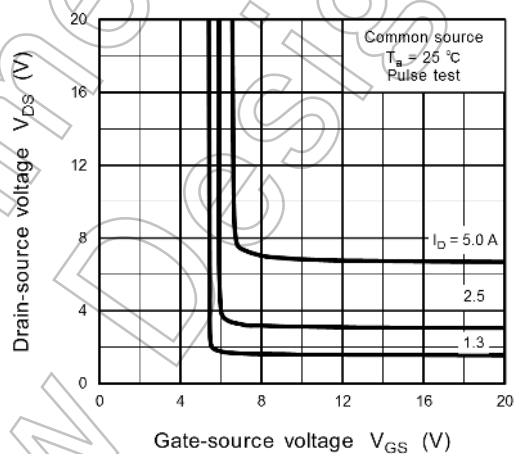


Fig. 8.4 $V_{DS} - V_{GS}$

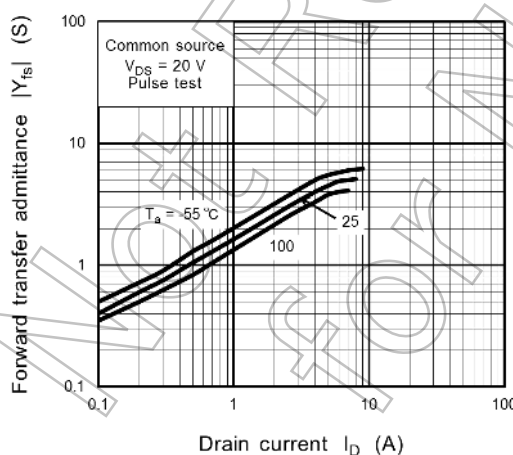


Fig. 8.5 $|Y_{fs}| - I_D$

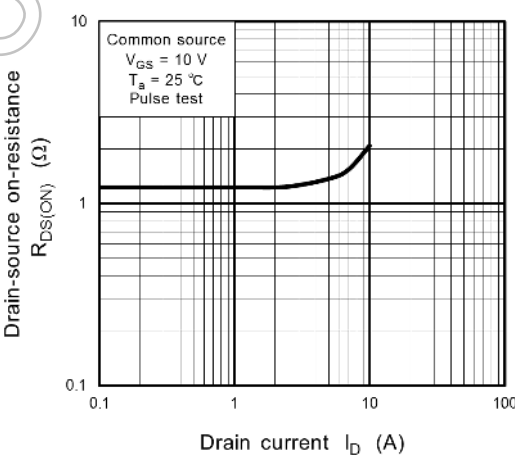


Fig. 8.6 $R_{DS(ON)} - I_D$

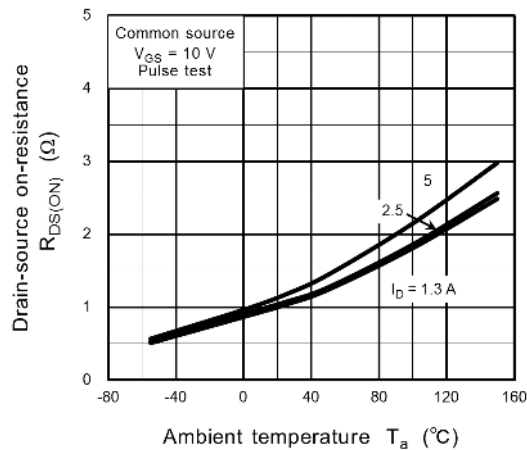


Fig. 8.7 $R_{DS(ON)} - T_a$

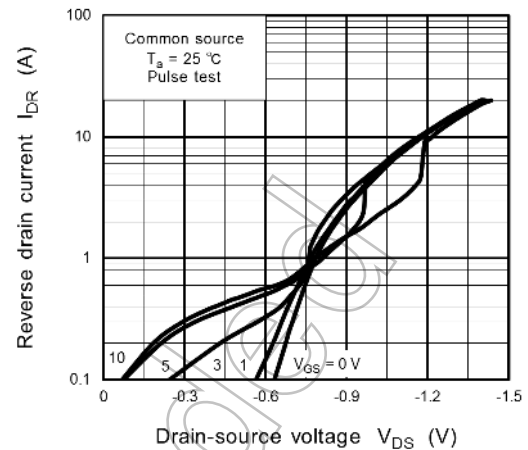


Fig. 8.8 $I_{DR} - V_{DS}$

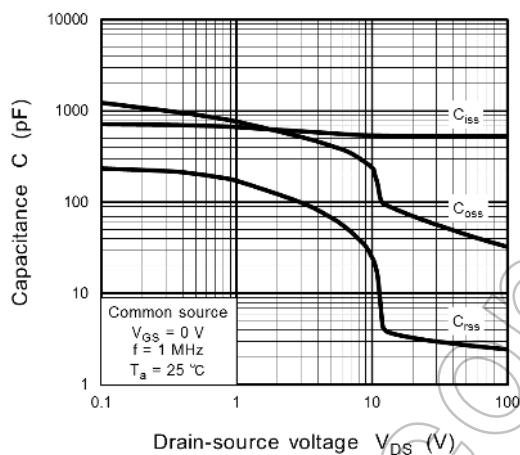


Fig. 8.9 $C - V_{DS}$

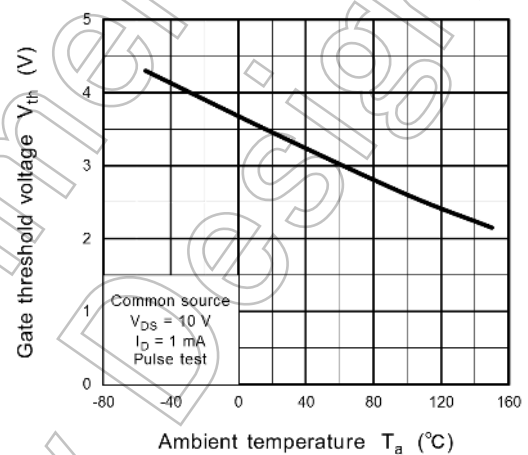
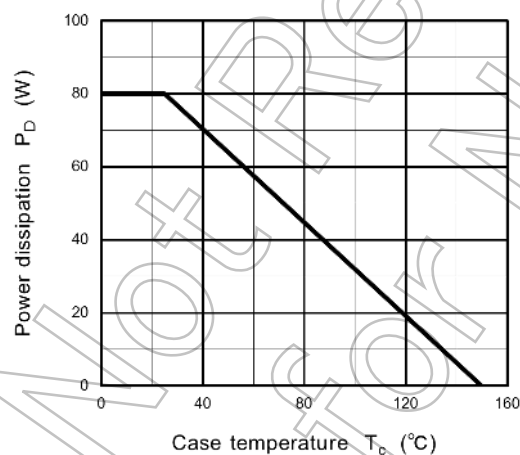


Fig. 8.10 $V_{th} - T_a$



**Fig. 8.11 $P_D - T_c$
(Guaranteed Maximum)**

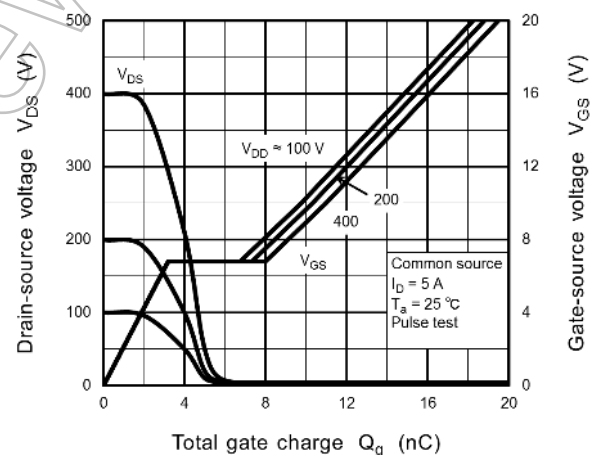
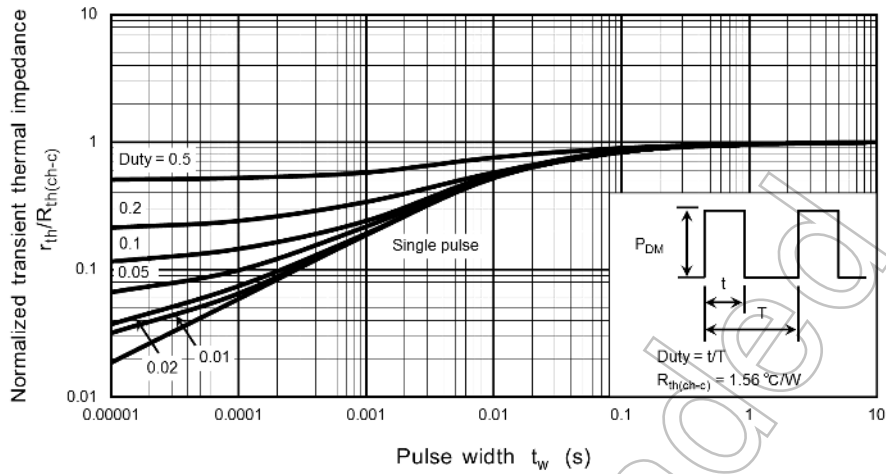
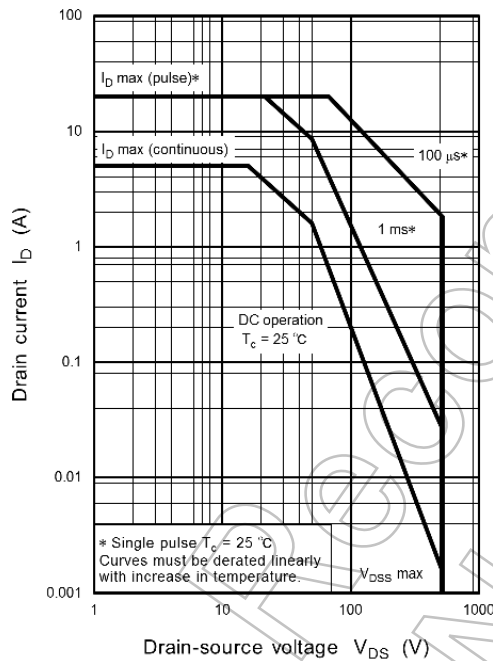


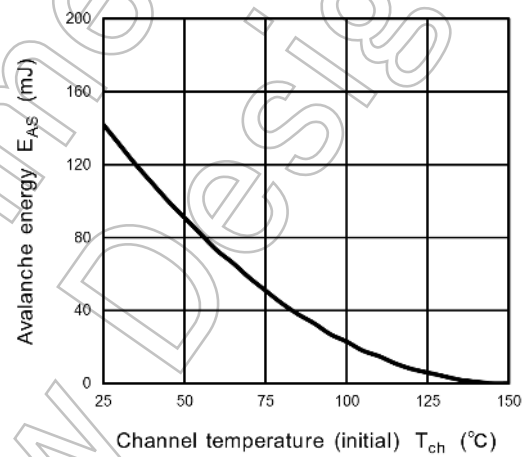
Fig. 8.12 Dynamic Input/Output Characteristics



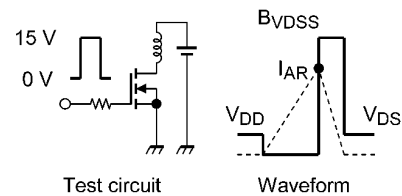
**Fig. 8.13 $r_{th}/R_{th(ch-c)} - t_w$
(Guaranteed Maximum)**



**Fig. 8.14 Safe Operating Area
(Guaranteed Maximum)**



**Fig. 8.15 $E_{AS} - T_{ch}$
(Guaranteed Maximum)**



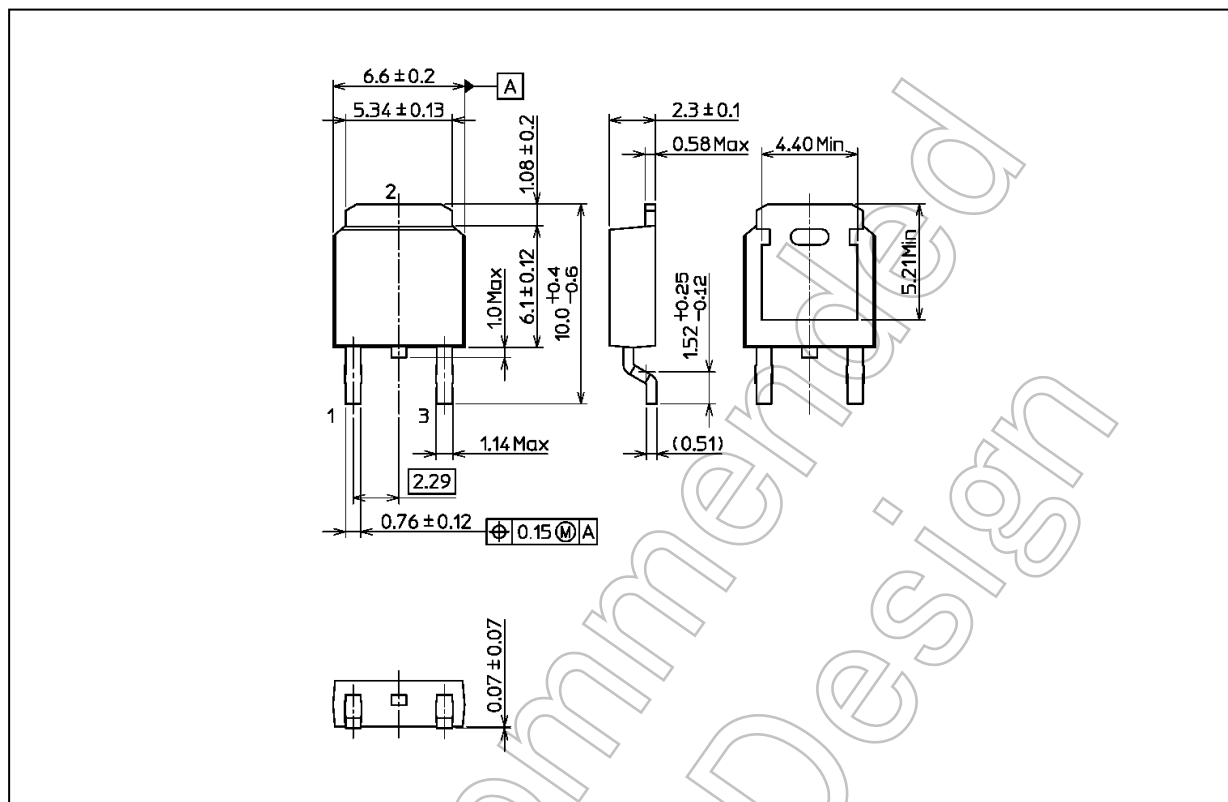
$$R_G = 25 \, \Omega, V_{DD} = 90 \, V \quad E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

Fig. 8.16 Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



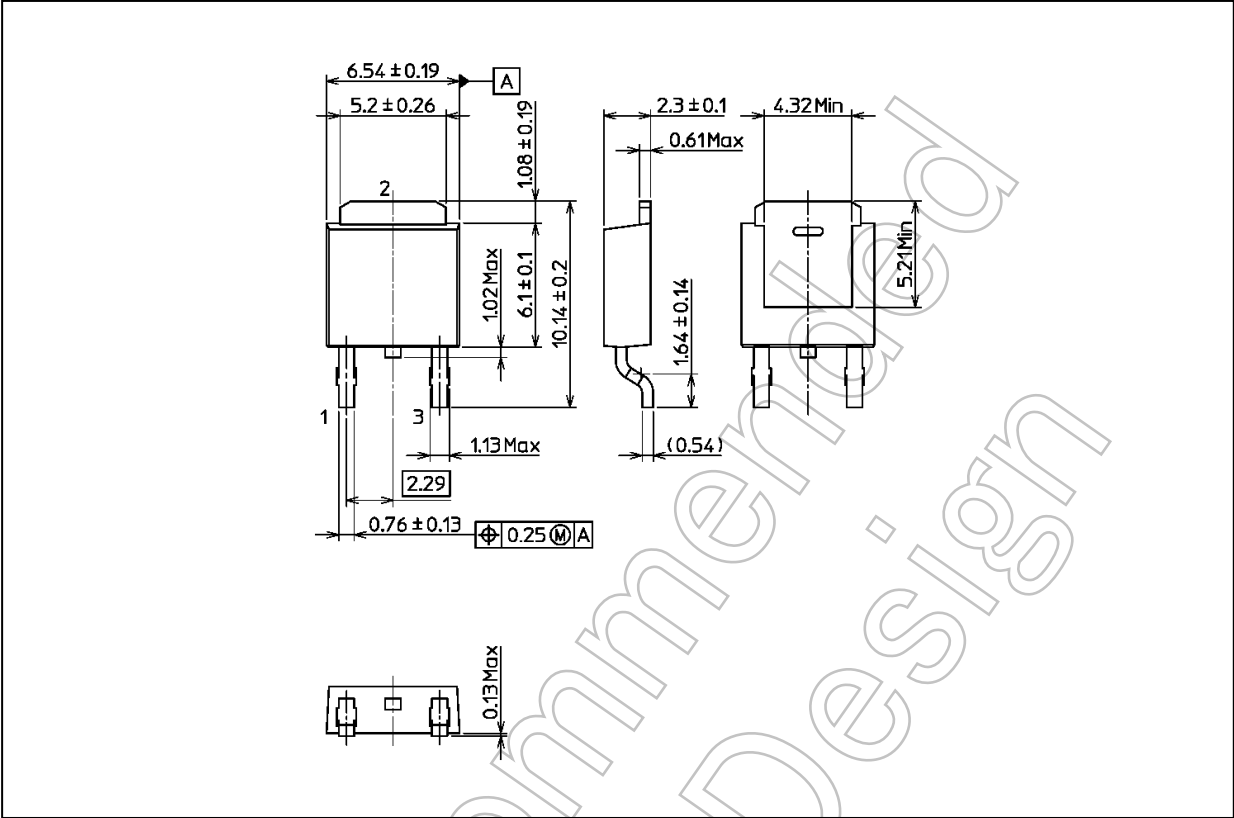
Both products are compliant with the JEDEC: TO-252 Package specification. Please contact the Toshiba sales representative for further details.

Weight: 0.36 g (typ.)

Package Name(s)
JEDEC: TO-252
TOSHIBA: 2-7K1S
Nickname: DPAK

Package Dimensions

Unit: mm



Both products are compliant with the JEDEC: TO-252 Package specification. Please contact the Toshiba sales representative for further details.

Weight: 0.389 g (typ.)

Package Name(s)
JEDEC: TO-252
TOSHIBA: 2-7N1S
Nickname: DPAK

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