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Electronic Components Sourcing Information

Product Reference Information

Part Number: TPS16415DRCR

Manufacturer: Texas Instruments

Package: 10-VSON (3x3)

Availability: Please confirm with sales

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

TPS1641x 40V, 1.8A Power and Current Limiting eFuse With IN to OUT Short Detection

1 Features

- Operating voltage range (IN):
  - 4.5V to 40V (power limit devices)
  - 2.7V to 40V (current limit devices)
- Withstands negative voltages up to –1V at output
- Ultra-low ON-resistance: R_{ON} = 152mΩ (typical)
- 2W to 64W power limiting
- 0.03A to 1.8A current limiting
- IN to OUT short detection and indication on $\overline{\text{FLT}}$ pin
- $\overline{\text{FLT}}$ output for diagnostics and driving external PFET
- ±5% accurate power limit at 15W (power limit devices)
- ±6% accurate current limit at 1A (current limit devices)
- Configurable overvoltage protection
- Configurable overcurrent protection (I_{OCP})
- Configurable blanking time for transient currents
- Overvoltage protection up to 60V with external FET
- Adjustable output slew rate control (dVdt) for inrush current protection
- Enable and shutdown control
- Output load current monitoring on IOCP pin
- Overtemperature protection (OTP) with thermal shutdown
- Small footprint: QFN 3 × 3mm, 0.5mm pitch
- UL 2367 recognition
  - File No. E169910
  - R_{ILM} ≥ 5.1kΩ
- IEC 62368-1 CB certified

2 Applications

- Refrigerator and freezer
- Oven
- Dishwasher
- HVAC valve and actuator control
- Ventilators
- Anesthesia delivery systems

3 Description

The TPS1641x family are integrated eFuse devices with accurate power limit or current limit. The device family provides robust protection with integrated overcurrent protection, overvoltage protection, IN to OUT short detection, and overtemperature protection.

TPS16410, TPS16411, TPS16414, and TPS16415 devices provide ± 5% power limiting at 15W for loads and also provide configurable blanking time for transient overload or overcurrent events. Use TPS16410, TPS16411, TPS16414, and TPS16415 in low-power circuits (LPCs) for 15W power limiting as per IEC60335 and UL60730 standards. TPS1641x devices provide protection from adjacent pin short and pin short to GND faults.

Applications such as backplane power protection in PLC and DCS modules configure the current limit with a resistor on the ILIM pin. TPS16412, TPS16413, TPS16416, and TPS16417 devices provide ± 6% current limiting at 1A for loads and also provide output slew rate control with dVdT pin to charge large capacitive loads at power up.

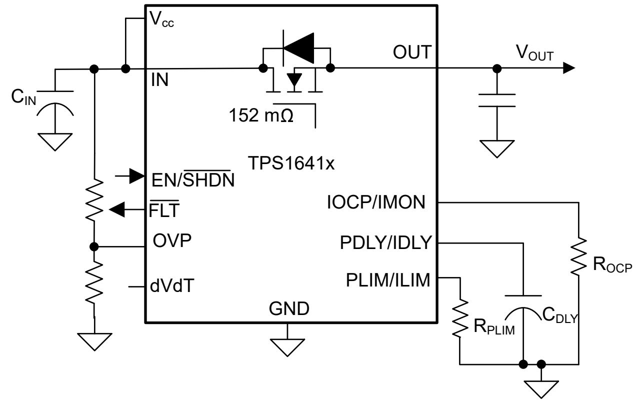
TPS1641x features IN to OUT short detection and indicate IN to OUT short on the $\overline{\text{FLT}}$ pin. The $\overline{\text{FLT}}$ pin either provides to MCU as digital input or to drive an external PFET.

The devices are characterized for operation over a junction temperature range from –40°C to +125°C.

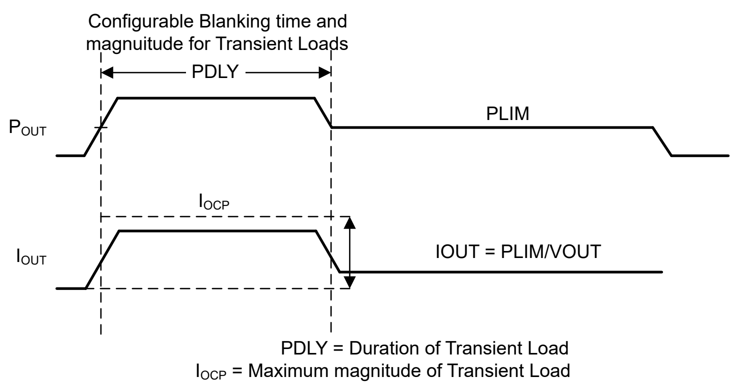
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS1641x	VSON (10)	3.00mm × 3.00mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic



Configurable Blanking Time for Transient Loads

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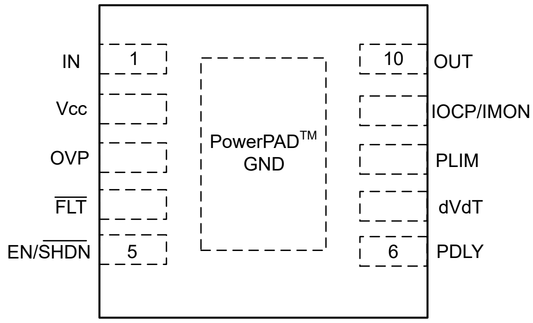
4 Device Comparison Table

Part Number	Power or Current Limit	Fault Behavior	IN-OUT Short Detection
TPS16410	Power limit	Auto-retry	Y
TPS16411	Power limit	Latch-off	Y
TPS16412	Current limit	Auto-retry	Y
TPS16413	Current limit	Latch-off	Y
TPS16414	Power limit	Auto-retry	N
TPS16415	Power limit	Latch-off	N
TPS16416	Current limit	Auto-retry	N
TPS16417	Current limit	Latch-off	N

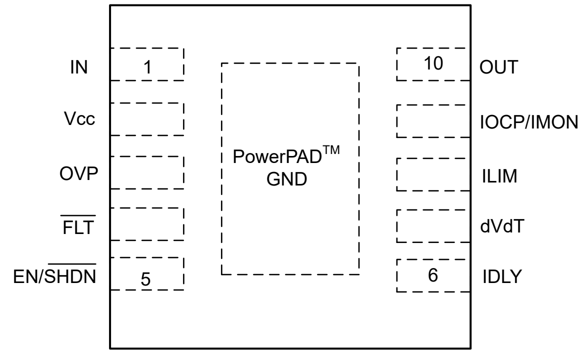
See Section 7.3.9 for recommended device variants.

5 Pin Configuration and Functions



TPS16410, TPS16411,
TPS16414, TPS16415

Figure 5-1. TPS16410, TPS16411, TPS16414 and TPS16415 10-Pin DRC VSON Package (Top View)



TPS16412, TPS16413,
TPS16416, TPS16417

Figure 5-2. TPS16412, TPS16413, TPS16416 and TPS16417 10-Pin DRC VSON Package (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN	1	P	Power input for internal FET.
V_{cc}	2	P	Supply input for internal circuits of the device.
OVP	3	I	Overvoltage protection input. Connect this pin to GND for disabling OVP.
$\overline{\text{FLT}}$	4	O	Active low fault output. See Section 7.3.11 for different $\overline{\text{FLT}}$ pin indications.
EN/$\overline{\text{SHDN}}$	5	I	Enable or shutdown input.
PDLY	6	I/O	TPS16410, TPS16411: Input for blanking time for power limiting. Connect a capacitor to set PDLY blanking time.
IDLY			TPS16412, TPS16413: Input for blanking time for current limiting. Connect a capacitor to set IDLY blanking time.
dVdT	7	I/O	Output slew control input. Connect a capacitor to set the output slew rate. If not used, this pin can be left open.
PLIM	8	I/O	TPS16410, TPS16411: Power limit input. Connect a resistor to set PLIM setpoint.
ILIM			TPS16412, TPS16413: Current limit input. Connect a resistor to set ILIM setpoint.
IOCP/IMON	9	I/O	Overcurrent protection input and current monitoring output for output current. Output current can be sensed by reading voltage on this pin. Connect a resistor to set IOCP set-point and for reading output current.
OUT	10	P	Power output from internal FET.
PowerPAD/GND	—	G	GND connection for the device. PowerPAD™ must connect to GND of input power supply. Connect PowerPAD to GND plane on PCB using multiple vias for enhanced thermal performance.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{cc}, $\overline{FLT}$	Input Voltage	–0.3	67	V
OVP	Input Voltage	–0.3	62	V
IN, IN-OUT, IOCP	Input Voltage	–0.3	42	V
OUT	Input Voltage	–1	42	V
EN/$\overline{SHDN}$, PDLY/IDLY	Input Voltage	–0.3	5.5	V
dVdT, PLIM/ILIM	Input Voltage	–0.3	5.5	V
I_{IOCP}, I_{PDLY}, I_{PLIM}, I_{dVdT}, I_{ILIM}	Source Current	Internally Limited		
T_J	Junction temperature	–40	150	°C
	Transient Junction Temperature	–40	T_{TSD}	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±1500	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	V_{IN}		60	V
$\overline{FLT}$	Input Voltage	0		60	V
IN	Input Voltage (TPS16410, TPS16411, TPS16414, TPS16415)	4.5		40	V
IN	Input Voltage (TPS16412, TPS16413, TPS16416, TPS16417)	2.7		40	V
OUT	Input Voltage	0		40	V
EN/$\overline{SHDN}$, OVP	Input Voltage	0		5.5	V
PDLY/IDLY	External capacitor	0.012		10	µF
dVdT	External capacitor	0.01		5	µF
IOCP	External resistor	6.34		80.6	kΩ
PLIM	External resistor	12.4		412	kΩ
ILIM	External resistor	5.1		348	kΩ

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS1641 DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	15.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

–40°C ≤ T_A = T_J ≤ +125°C, V_{IN} = 3V to 40V (TPS16412, TPS16413, TPS16416, TPS16417), V_{IN} = 4.5V to 40V (TPS16410, TPS16411, TPS16414, TPS16415), Vcc = V_{IN}, R_{ILIM} = 5.49kΩ R_{PLIM} = 255kΩ R_{IOCP} = 7.32kΩ , $\overline{FLT}$ = Open, C_{OUT} = 100nF, C_{IN} = 10nF C_{dVdT} = Open, PDLY/IDLY = Open. , EN/$\overline{SHDN}$ = Open
(All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING INPUT AND SUPPLY VOLTAGE						
V_{cc}	Operating Supply voltage		V_{IN}		60	V
V_{IN}	Operating Input voltage	TPS16410, TPS16411, TPS16414 ,TPS16415	4.5		40	V
V_{IN}	Operating Input voltage	TPS16412, TPS16413, TPS16416, TPS16417	2.7		40	V
I_Q	Operating Supply current (Vcc)	EN/$\overline{SHDN}$ = 2V, V_{cc} = 40V, V_{IN} = Open, R_{ILIM} or R_{PLIM} = Open		1.2	2.1	mA
I_{QSD}	Shutdown Supply current (Vcc)	EN/$\overline{SHDN}$ = GND, V_{cc} = 40V, V_{IN} = Open, R_{ILIM} or R_{PLIM} = Open, R_{IOCP} = Open		14	36	µA
I_{INLKG}	IN Leakage Current in ON State	EN/$\overline{SHDN}$ = 2V, V_{IN} = V_{cc} = 40V, Open, R_{ILIM} or R_{PLIM} = Open		0.025	0.52	mA
$I_{INLKG-SD}$	IN Leakage Current in Shutdown	EN/$\overline{SHDN}$ = GND,V_{IN} = V_{cc} = 40V, R_{ILIM} or R_{PLIM} = Open, R_{IOCP} = Open		0.7	2.8	µA
OVER-VOLTAGE PROTECTION (OVP) INPUT						
V_{OVPR}	OVP rising threshold		1.48	1.53	1.58	V
V_{OVPF}	OVP falling threshold		1.34	1.40	1.46	V
I_{OVP}	OVP leakage current	0V ≤ V_{OVP} ≤ 4V	–350	–265	–200	nA
EN/SHDN INPUT						
V_{ENR}	Enable rising threshold				1.2	V
V_{ENF}	Enable falling threshold		0.59			V
I_{EN}	Enable leakage current	0V ≤ V_{EN} ≤ 4V	–10			µA
$V_{EN-Open}$	Open circuit Enable Voltage	I_{EN} = 0.1 µA, V_{CC} ≥ 5V		4.9		V
OUTPUT POWER LIMITING (PLIM)						

6.5 Electrical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, V_{IN} = 3V to 40V (TPS16412, TPS16413, TPS16416, TPS16417), V_{IN} = 4.5V to 40V (TPS16410, TPS16411, TPS16414, TPS16415), Vcc = V_{IN}, R_{ILIM} = 5.49kΩ R_{PLIM} = 255kΩ R_{IOCP} = 7.32kΩ , $\overline{FLT}$ = Open, C_{OUT} = 100nF, C_{IN} = 10nF C_{dVdT} = Open, PDLY/IDLY = Open. , EN/$\overline{SHDN}$ = Open
(All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{OUT}	Output Power Limit	R_{PLIM} = 26.7kΩ	3	3.66	4.5	W
P_{OUT}	Output Power Limit	R_{PLIM} = 95.3kΩ, –40°C ≤ T_A ≤ +85°C	12.94	13.69	14.44	W
P_{OUT}	Output Power Limit	R_{PLIM} = 255kΩ, –40°C ≤ T_A ≤ +85°C	34	37	39.8	W
OUTPUT CURRENT LIMITING (ILIM)						
I_{OUT}	Output Current Limit	R_{ILIM} = 332kΩ	0.024	0.032	0.039	A
I_{OUT}	Output Current Limit	R_{ILIM} = 10kΩ, –40°C ≤ T_A ≤ +85°C	0.918	0.987	1.035	A
I_{OUT}	Output Current Limit	R_{ILIM} = 5.49kΩ, –40°C ≤ T_A ≤ +85°C	1.671	1.77	1.881	A
POWER OUTPUT (OUT)						
R_{ON}	IN to OUT On resistance	–40°C ≤ T_J ≤ 125°C	96	153	260	mΩ
R_{ON}	IN to OUT On resistance	0°C ≤ T_J ≤ 85°C		153	215	mΩ
R_{ON}	IN to OUT On resistance	T_J = 25°C		153	160	mΩ
$I_{LKG-OUT}$	Output Leakage current in OFF state	V_{IN} = 40V, V_{OUT} = 0V, EN = Low	–15	–1.2		µA
CURRENT MONITORING OUTPUT (IMON)						
G_{IMON}	Gain : I_{MON}/I_{OUT}	I_{OUT} = 0.05 to 1.8A	45	50	55	µA/A
OS_{IMON}	I_{MON} Offset current	I_{OUT} = 0.3 to 0.8A	–0.8	0.05	0.8	µA
OVER CURRENT PROTECTION (IOCP) AND SHORT CIRCUIT PROTECTION (ISCP)						
I_{OCP}	Over current protection set-point	R_{IOCP} = 7.32kΩ	2.11	2.23	2.35	A
I_{OCP}	Over current protection set-point	R_{IOCP} = 16.2kΩ	0.95	1.01	1.07	A
$I_{Fasttrip}$	Fast Trip protection threshold			1.9 × I_{OCP}		A
I_{SCP}	Short circuit protection threshold			6.7		A
$I_{LIM-Internal}$	Internal Current Limit	TPS16410, TPS16411, TPS16414, TPS16415		0.81 × I_{OCP}		A
THERMAL PROTECTION and SHUTDOWN (TTSD)						
T_{TSD}	Thermal shutdown temperature			155		°C
$T_{TSD-hyst}$	Thermal shutdown temperature hysteresis			12		°C
Output slew rate control (dVdT)						
I_{dVdT}	dVdT charging current		1.78	2	2.23	µA
G_{dVdT}	dVdT Gain			50		V/V
FLT Output (FLTb) (Open Drain Output)						
R_{FLTb}	Fault pin pull down resistance			73		Ω
$I_{FLTb-LKG}$	Fault pin leakage current	$\overline{FLT}$ is High, $V_{\overline{FLT}}$ ≤ 25V	–1	0.005	1	µA
IN to OUT Short Detection (TPS16410, TPS16411, TPS16412, TPS16413)						
R_{short}	Resistance for IN to OUT short detection				30	mΩ

6.6 Timing Requirements

–40°C ≤ T_A = T_J ≤ +125°C, V_{IN} = 3V to 40V (TPS16412, TPS16413), V_{IN} = 4.5V to 40V (TPS16410, TPS16411), V_{CC} = V_{IN}, V_{EN} = 2V, R_{ILIM} = 5.49kΩ R_{PLIM} = 255kΩ R_{IOCP} = 7.32kΩ , FLT = Open, C_{OUT} = 100nF, C_{IN} = 10nF C_{dVdT} = Open, PDLY = Open.
(All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Enable/SHDN and Vcc Input						
t_{ON_DLY}	Turn on delay with V_{CC}	V_{EN} = V_{ENR} + 0.1V , R_{LOAD} = Open		500		µs
$t_{EN\_ON\_DLY}$	Enable on delay	Fast turn-on with Enable when device is not in shutdown, V_{EN} = V_{ENR} + 0.1V , R_{LOAD} = Open		270		µs
$t_{EN\_OFF\_DLY}$	Enable off delay	V_{EN} < V_{ENF} to V_{OUT} = 0.9 × V_{IN}, , R_{LOAD} = 100		1.2		µs
t_{LOW_SHDN}	Min low pulse for entering shutdown	R_{LOAD} = 100	24			ms
OVP Input						
$t_{OVP\_ENTRY\_DLY}$	OVP entry delay	V_{OVP} = V_{OVPR} + 25mV to $\overline{FLT}$ Low		0.75		µs
$t_{OVP\_EXIT\_DLY}$	OVP exit delay	V_{OVP} = V_{OVPF} - 25mV to to $\overline{FLT}$ High		0.6		µs
Over Current Protection and Short-circuit protection						
$t_{FASTTRIP\_DLY}$	Fast Trip protection delay	$I_{FASTTRIP}$ < I_{OUT} < I_{SCP} to FET OFF		5.65		µs
t_{SCP_DLY}	Short-Circuit protection delay	I_{OUT} = I_{SCP} + 500mA to FET OFF		280		ns
Power Limiting						
t_{PDLY}	Blanking time before power limiting	I_{OUT} < I_{OCP}, P_{OUT} = 1.2 × PLIM, CDLY = 12nF		6.5		ms
$t_{PLIM-RES}$	Power Limit response time	I_{OUT} < I_{OCP}, I_{OUT} = 1.2 × ILIM, CDLY = OPEN		215		µs
$t_{PLIM-DUR}$	PowerLimit Duration			2 × t_{PDLY}		s
Current Limiting						
t_{IDLY}	Blanking time before current limiting	I_{OUT} < I_{OCP}, I_{OUT} = 1.2 × ILIM, CDLY = 12nF		6.5		ms
$t_{ILIM-RES}$	Current Limit response time	I_{OUT} < I_{OCP}, I_{OUT} = 1.2 × ILIM, CDLY = OPEN		280		µs
$t_{ILIM-DUR}$	Current Limit Duration			2 × t_{PDLY}		s
Auto-Retry and Thermal Shutdown						
t_{RETRY}	Retry Delay			8 × t_{PDLY}		s
Output Ramp Control (dVdT)						
t_{dVdT}	Output Ramp Time	C_{dVdT} = Open, V_{IN} = V_{CC} = 24V		105		µs
IN to OUT Short (TPS16410, TPS16411, TPS16412, TPS16413) and FLT Output						
$t_{IN\_OUT\_Short\_Detect}$	IN to OUT short detection time when FET is ON	IN-OUT Short to FLT Low		135		ms
$t_{IN\_OUT\_Short\_Detect}$	IN to OUT short detection time when FET is OFF	IN-OUT Short to FLT Low		20		ms

6.7 Typical Characteristics

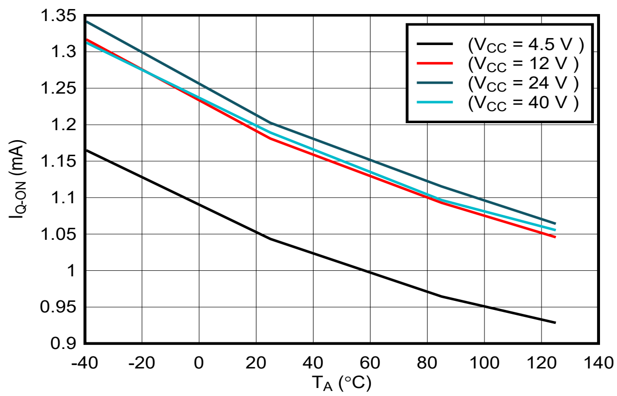


Figure 6-1. $I_{Q\text{-}ON}$ vs Temperature

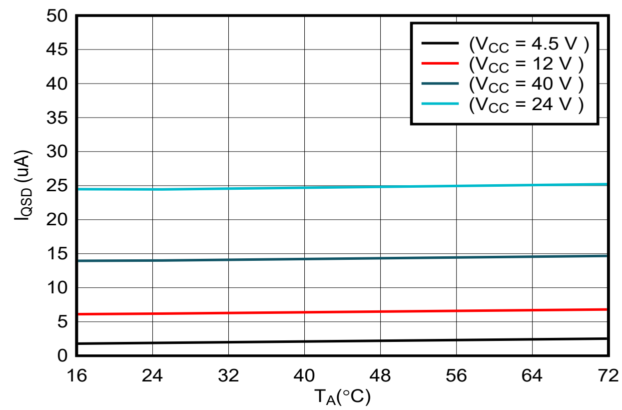


Figure 6-2. I_{QSD} vs Temperature

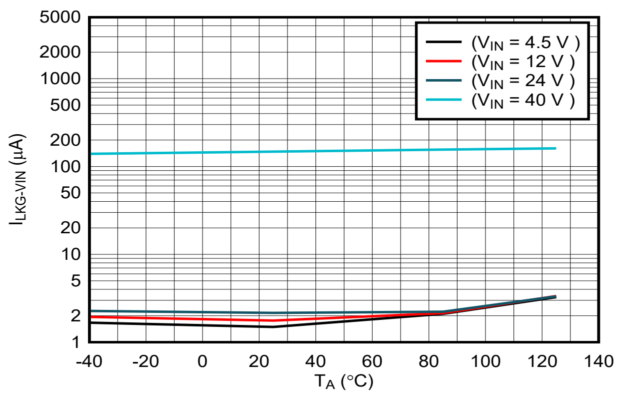


Figure 6-3. $I_{LKG\text{-}VIN}$ vs Temperature

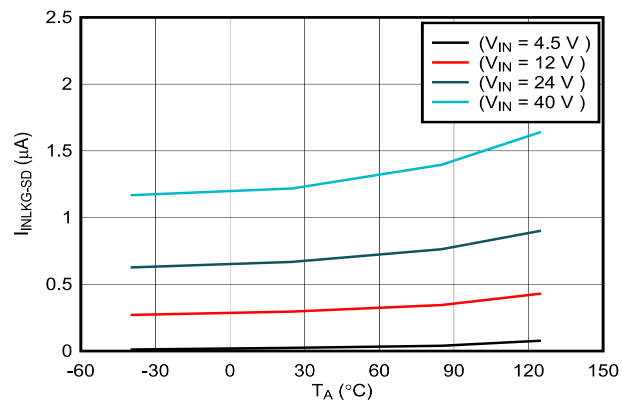


Figure 6-4. $I_{LKG\text{-}VIN\text{-}SD}$ vs Temperature

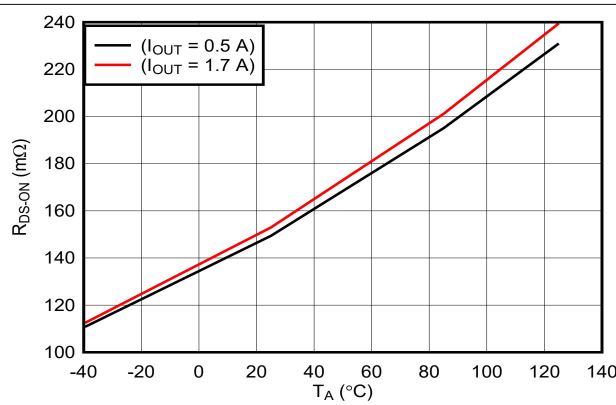


Figure 6-5. $R_{DS\text{-}ON}$ vs Temperature

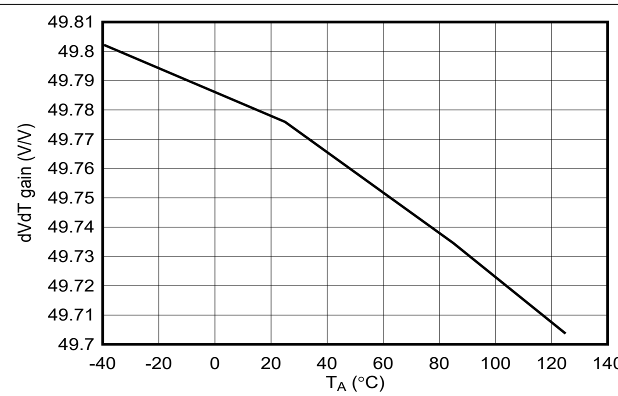


Figure 6-6. G_{dVdT} vs Temperature

6.7 Typical Characteristics (continued)

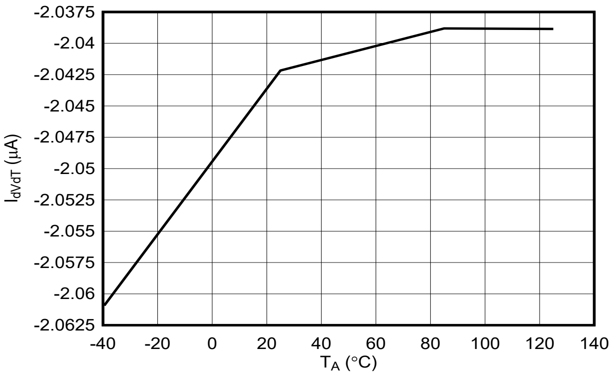


Figure 6-7. I_{dVdT} vs Temperature

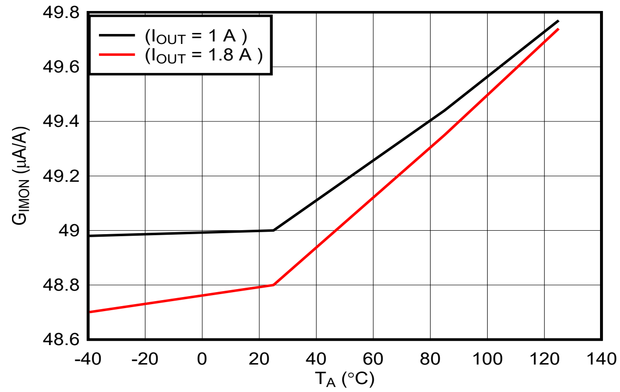


Figure 6-8. G_{IMON} vs Temperature

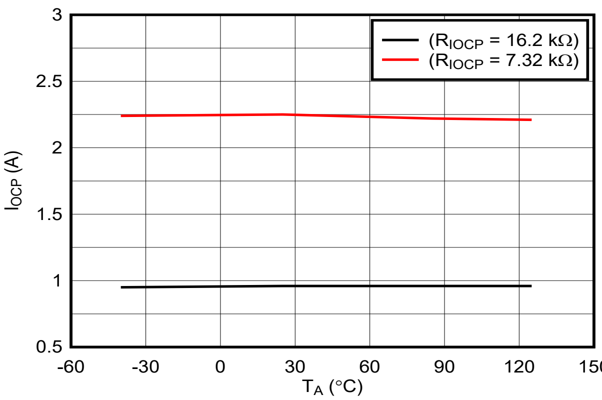


Figure 6-9. I_{OCP} vs Temperature

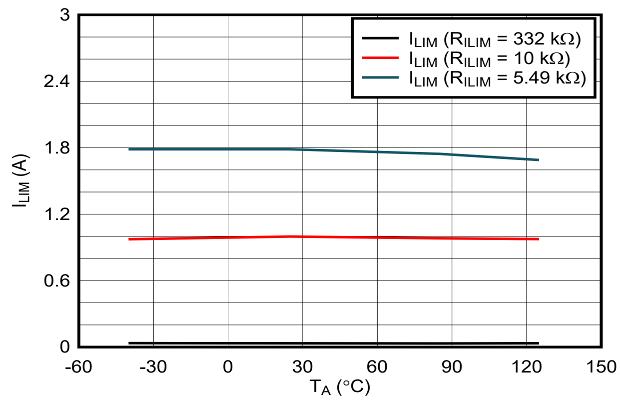


Figure 6-10. Output Current Limit vs Temperature for TPS16412 and TPS16413

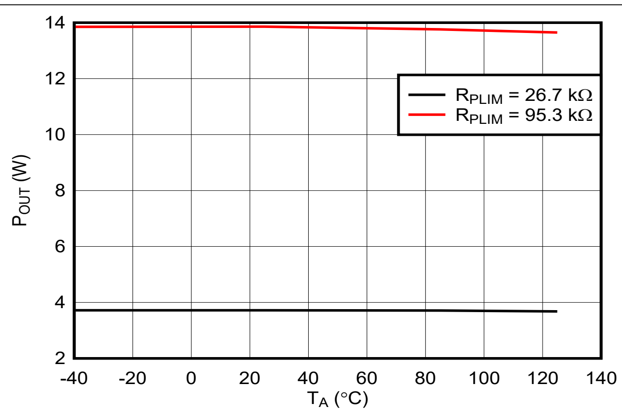


Figure 6-11. Output Power Limit vs Temperature for TPS16410 and TPS16411 with V_{IN} = 12V

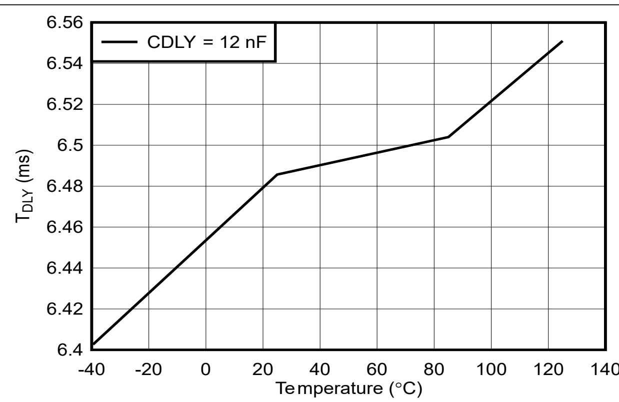


Figure 6-12. TDLY vs Temperature

6.7 Typical Characteristics (continued)

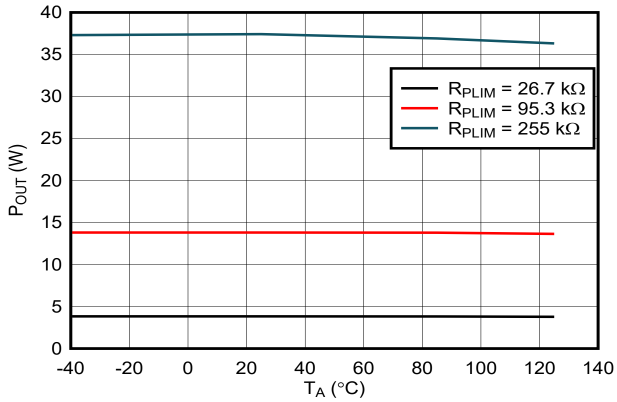


Figure 6-13. Output Power Limit vs Temperature for TPS16410 and TPS16411 with V_{IN} = 24V

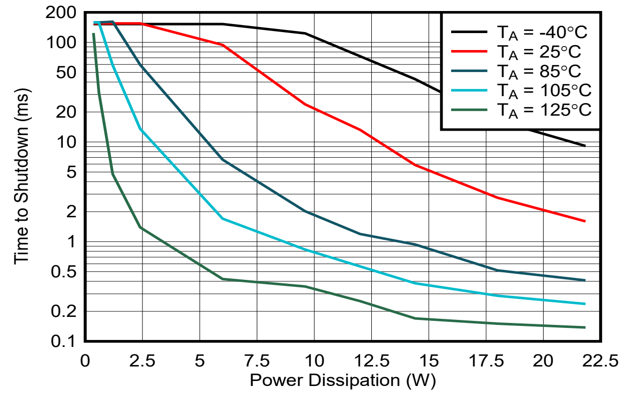


Figure 6-14. Thermal Shutdown Time vs Power Dissipation with V_{IN} = 12V

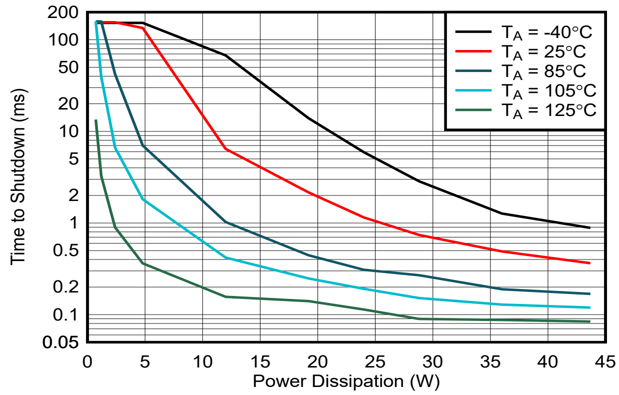


Figure 6-15. Thermal Shutdown Time vs Power Dissipation with V_{IN} = 24V

7 Detailed Description

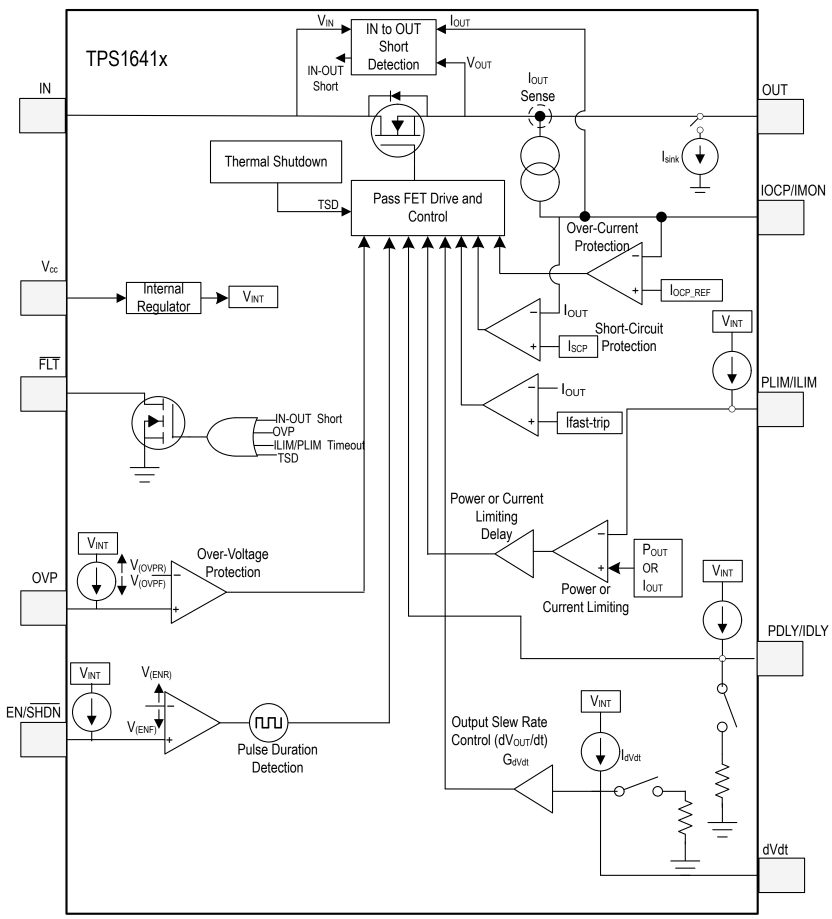
7.1 Overview

The TPS1641x is an integrated eFuse with accurate power limit or current limit. The device integrates an NFET with R_{ON} of 152mΩ. TPS16410, TPS16411, TPS16414 and TPS16415 provide power limiting whereas the TPS16412, TPS16413, TPS16416, and TPS16417 provide current limiting. The TPS16410, TPS16411, TPS16414 and TPS16415 can provide 15W accurate power limiting for low-power circuit (LPCs) as per IEC60335 and UL60730 standards. TPS16410, TPS16411, TPS16412 and TPS16413 also provide IN to OUT short detection and its indication on $\overline{\text{FLT}}$ output. IN to OUT short detection eliminates the need of additional eFuse or power limiting circuit in case of IN to OUT short test for IEC60335, UL60730, and similar standards. Use $\overline{\text{FLT}}$ as an input for MCU or to drive an external PFET. TPS1641x devices also provide protection from adjacent pin short and pin short to GND faults.

The TPS1641x device also provide configurable blanking time (IDLY or PDLY) and overcurrent protection (IOCP) for transient loads. Load such as motors need higher current for start-up. Blanking time is useful for providing higher current for start-up of loads such as motors.

TPS1641x devices have overvoltage protection (OVP), overtemperature protection, and adjustable output slew rate control (dvdt). Vcc and $\overline{\text{FLT}}$ are rated up to 60V and can provide protection up to 60V with an external PFET.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Shutdown Input (EN/$\overline{\text{SHDN}}$)

The TPS1641x devices include a enable and shutdown input. Keeping EN/SHDN low for a duration more than t_{Low_SHDN} brings the device into low power shutdown mode, internal blocks of device are turned off, and the quiescent current of the device is reduced to I_{QSD} from V_{cc} supply.

While keeping EN/SHDN low for a duration less than t_{Low_SHDN}, the device turns off the internal FET only and FET can quickly turn back on. The device turns off the internal FET with a delay of $t_{EN\_OFF\_dly}$ as the enable pin is brought low. Quickly enable the internal FET with a delay of $t_{EN\_ON\_dly}$ when the device is not in shutdown. See the *Section 6.5* for V_{ENR} and V_{ENF} thresholds and the *Section 6.6* for t_{Low_SHDN}, $t_{EN\_OFF\_dly}$, and $t_{EN\_ON\_dly}$ timings. A PWM signal with low period less than t_{Low_SHDN} can be provided on EN/SHDN pin of the device for fast turn-on and turn-off of internal FET. Figure 7-1 illustrates the EN/$\overline{\text{SHDN}}$ input in the TPS1641x devices. Figure 7-2 shows the start-up of the device with enable input.

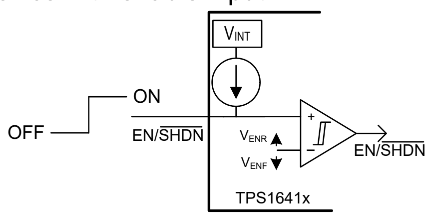
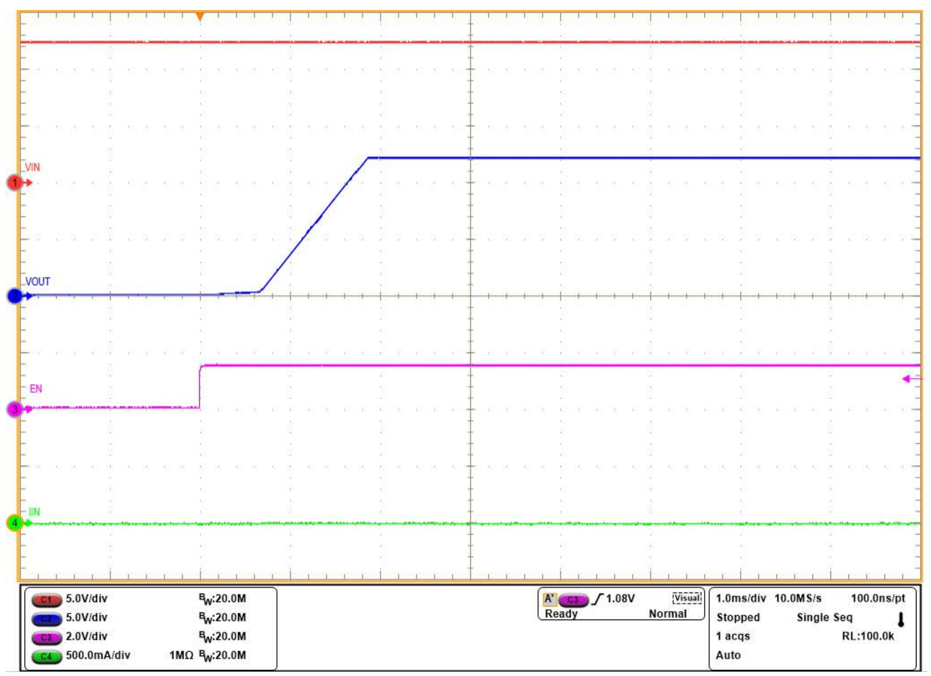


Figure 7-1. EN/$\overline{\text{SHDN}}$ in TPS1641x Devices



V_{IN} = 12V

Figure 7-2. Turn-On with Enable

7.3.2 Overvoltage Protection (OVP)

The TPS1641x implements overvoltage protection to protect the load from input overvoltage conditions. A resistor divider can be connected from the IN pin of device to configure the overvoltage protection setpoint. The device turns off the internal FET and asserts the $\overline{\text{FLT}}$ pin as the voltage at OVP pin goes above V_{OVPR}, and as the OVP pin voltage falls below V_{OVPF}, the internal FET is turned ON and $\overline{\text{FLT}}$ pin is de-asserted. See the

Section 6.5 table for V_{OVPF} and V_{OVPR} and *Section 6.6* for $t_{OVP\_entry\_dly}$ and $t_{OVP\_exit\_dly}$ timings for overvoltage protection input. Figure 7-3 illustrates the OVP input in TPS1641x devices. Figure 7-4 shows the overvoltage response.

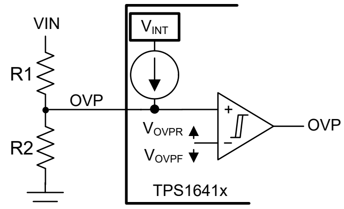


Figure 7-3. OVP Input in TPS1641x

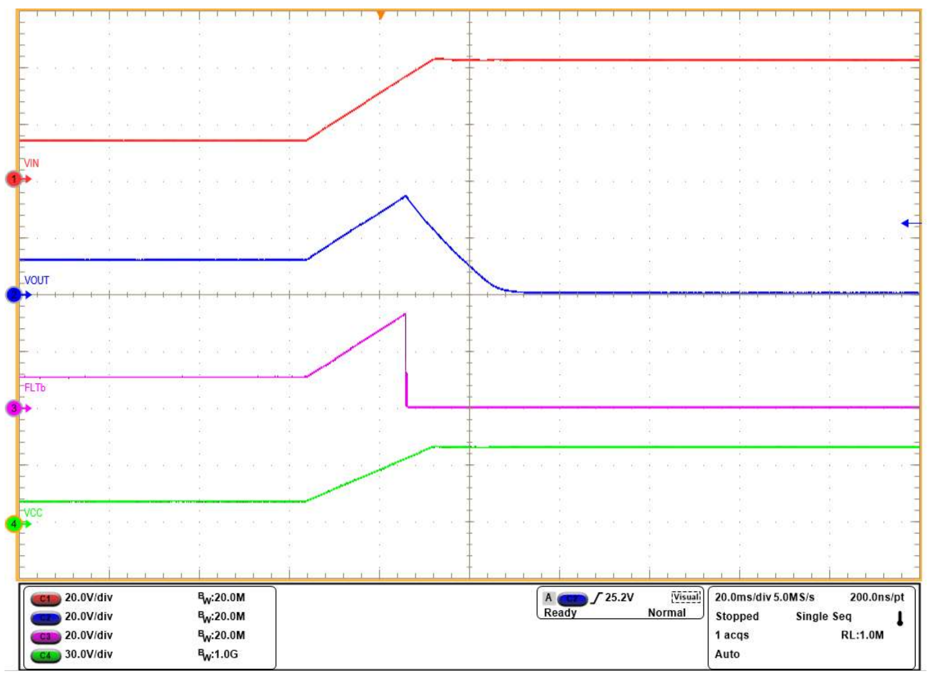


Figure 7-4. Overvoltage Protection Response for IN Voltage 12V to 40V

V_{cc} and $\overline{FLT}$ pins of the device are rated up to 60V, and the $\overline{FLT}$ pin can be used to drive an external PFET transistor and provide protection from 60V overvoltage at input as shown in Figure 7-5.

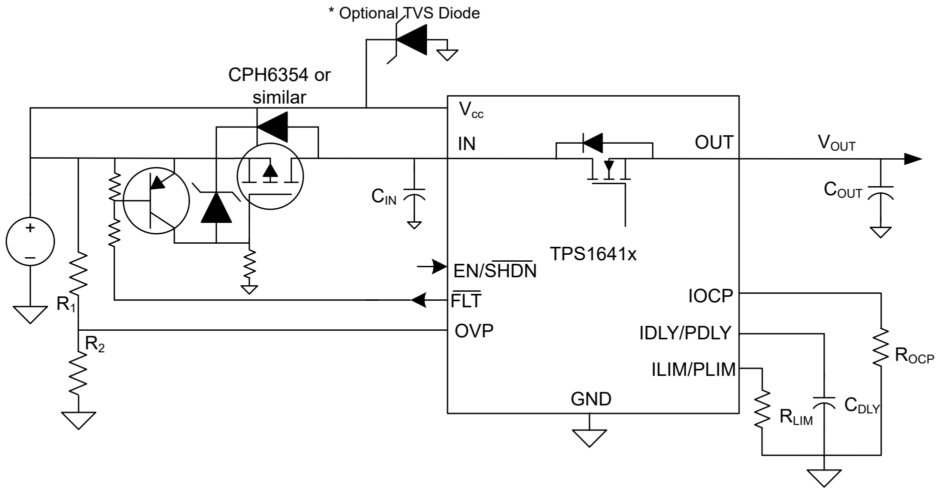


Figure 7-5. Overvoltage (up to 60V) Protection with External PFET

To disable the overvoltage input, connect OVP to GND. If the OVP pin is left open, the device turns off the internal FET.

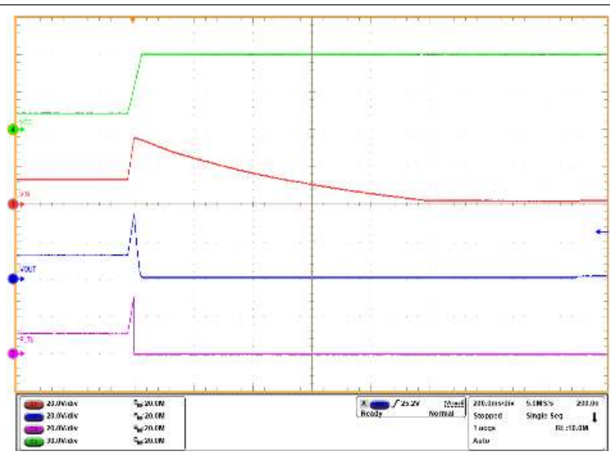


Figure 7-6. Overvoltage Response with External PFET for IN Voltage from 12V to 60V

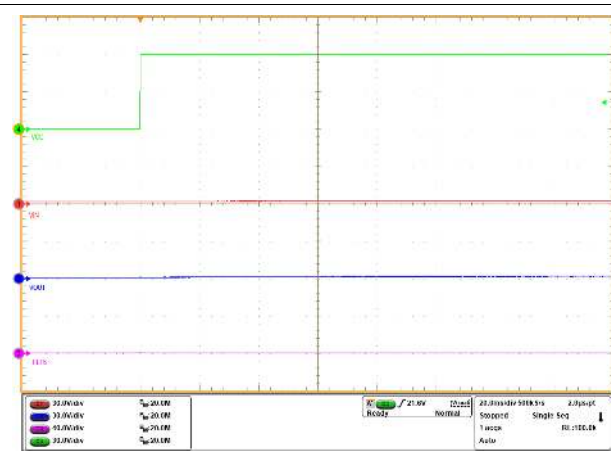


Figure 7-7. Hot Plugin with External PFET for 60V Input

7.3.3 Output Slew Rate and Inrush Current Control (dVdt)

During hot plug events or while trying to charge a large output capacitance, there can be a large inrush current. If the inrush current is not managed properly, it can damage the input connectors and cause the system power supply to droop leading to unexpected restarts elsewhere in the system. The inrush current during turn-on is directly proportional to the load capacitance and rising slew rate. Equation 1 can be used to find the output slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given output capacitance (C_{OUT}).

$$SR = \frac{I_{INRUSH}}{C_{OUT}} \tag{1}$$

A capacitance can be added to the dVdt pin to control the rising slew rate and lower the inrush current during turn-on. Calculate the required C_{dVdt} capacitance to produce a given slew rate using Equation 2.

$$C_{dVdt} = \frac{I_{dVdt} \times G_{dVdt}}{SR} \tag{2}$$

The fastest output slew rate is achieved by leaving the dVdt pin open. If dVdt pin is connected to GND, the device does not power up the output. Figure 7-8 shows the output slew rate control in the TPS1641x devices. Figure 7-9 shows the output slew rate control response of the device.

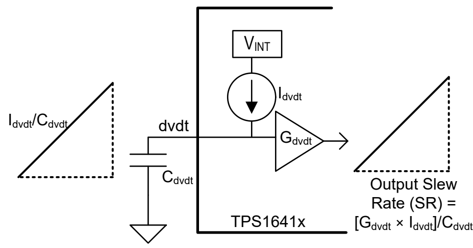


Figure 7-8. Output Slew Rate Control in the TPS1641x

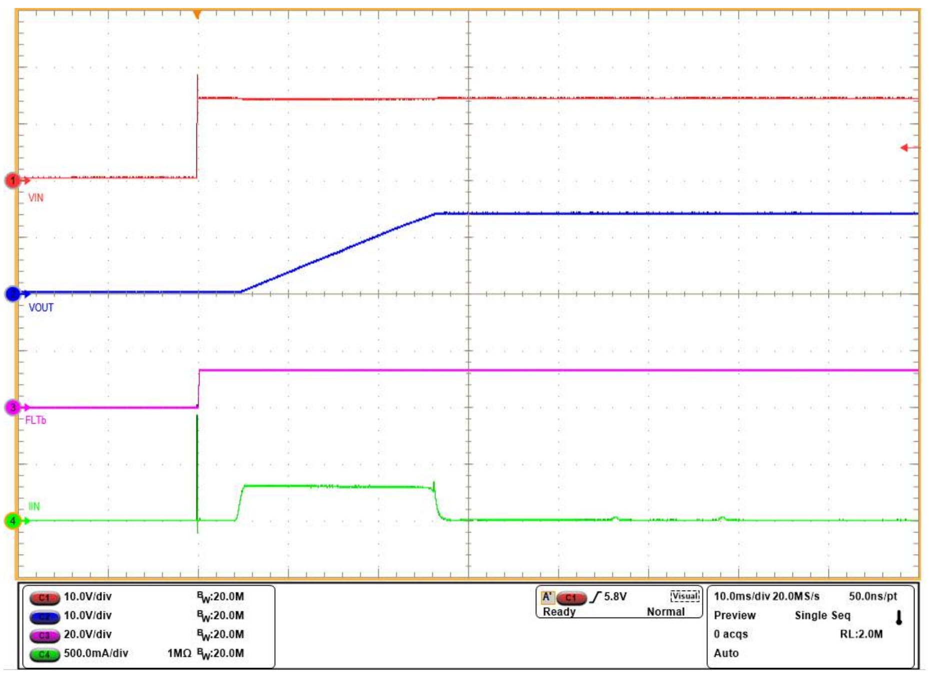


Figure 7-9. Output Slew Rate Control with V_{IN} = 12V, C_{dVdt} = 150nF, and C_{OUT} = 470µF

7.3.4 Active Current Limiting (ILIM) With the TPS16412, TPS16413, TPS16416, and TPS16417

The TPS16412, TPS16413, TPS16416, and TPS16417 devices respond to output overcurrent or overload conditions by actively limiting the current. The devices first provide a blanking time configured by capacitance on the IDLY pin. During this blanking time, the device can provide a current up to I_{OCP} value. After the end of this blanking time, the devices limit current to ILIM value. ILIM can be set by connecting resistor on ILIM pin. Calculate R_{ILIM} using Equation 3.

$$I_{LIM} = \frac{0.984A}{R_{ILIM}} \times 10k\Omega \tag{3}$$

If the output current exceeds I_{OCP}, the device goes into current limiting. During current limiting, if the output current goes below ILIM (I_{OUT} < ILIM), the device resets the IDLY timer and restarts IDLY timer when I_{OUT} > ILIM. Figure 7-10 shows the current limiting behavior for $I_{OUT} < I_{OCP}$ and for $I_{OCP} \le I_{OUT} < I_{fast\text{-}trip}$.

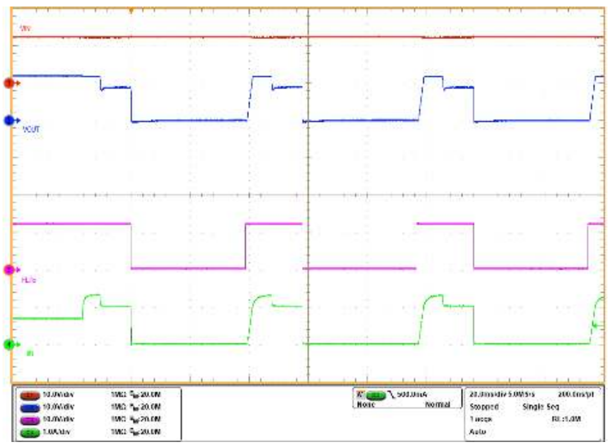


Figure 7-10. Current Limiting for $I_{OUT} < I_{OCP}$

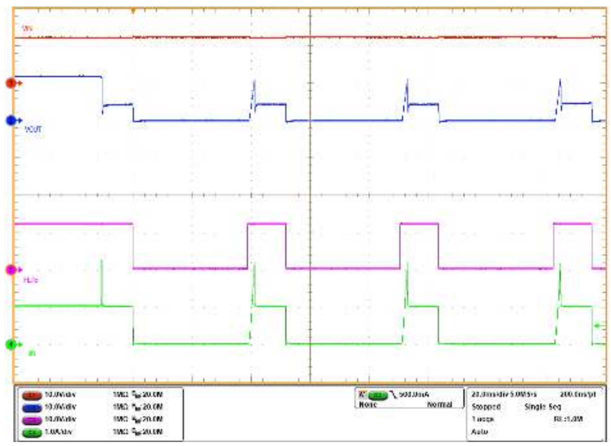


Figure 7-11. $I_{OCP} \le I_{OUT} < I_{fast\text{-}trip}$

During the current limiting, the device dissipates a power of (V_{IN} – V_{OUT}) × I_{OUT} and the device gets heated up. If the junction temperature of device reaches thermal shutdown temperature (T_{TSD}), the device turns off the internal FET. If the device does not go into thermal shutdown, the internal FET is turned off after a duration of $t_{ILIM\text{-}DUR}$. After the internal FET is turned off, the TPS16412 and TPS16416 auto-retry while the TPS16413 and TPS16417 latch off. If ILIM pin is connected to GND or left open, the device turns-off the internal FET. If the IDLY pin is left open or connected to GND, device provides $t_{ILIM\text{-}DUR}$ = 155ms unless the device enters thermal shutdown. Table 7-1 summarizes the device behavior for different output currents.

Table 7-1. Current Limiting and Overload Protection With TPS16412, TPS16413, TPS16416, and TPS16417

Output Current (I_{OUT})	Device Response
$I_{OUT} < I_{LIM}$	The device provides current up to I_{LIM}.
$I_{LIM} \le I_{OUT} < I_{OCP}$	The device provides current up to I_{OCP} for a duration of IDLY and then limits current to ILIM for a maximum duration of $t_{ILIM\text{-}DUR}$.
$I_{OCP} \le I_{OUT} < I_{fast\text{-}trip}$	The device limits current to ILIM for a maximum duration of $t_{ILIM\text{-}DUR}$.
$I_{fast\text{-}trip} \le I_{OUT} < I_{SCP}$	The device turns off the internal FET after a delay of $t_{fast\text{-}trip}$.
$I_{SCP} \le I_{OUT}$	The device turns off the internal FET after a delay of t_{SCP_dly}.

7.3.5 Active Power Limiting (PLIM) With the TPS16410, TPS16411, TPS16414, and TPS16415

The TPS16410, TPS16411, TPS16414, and TPS16415 devices respond to output overcurrent or overload conditions by actively limiting the output power. The devices first provide a blanking time configured by capacitance on PDLY pin. During this blanking time, the device can provide a current up to I_{OCP} value. After the end of this blanking time, the devices limit power to PLIM value. Set the power limit by connecting a resistor on the PLIM pin. During power limiting, if the output power goes below PLIM (P_{OUT} < PLIM), the device resets the PDLY timer and restarts the PDLY timer when P_{OUT} > PLIM. Use Equation 4 to calculate the value of resistor for power limiting. The device is rated for 1.8A continuous current, TI recommends to set PLIM < V_{IN} × 1.8A and PLIM < 0.9 × V_{OUT} × I_{OCP}

$$P_{LIM} = \frac{13.82W}{95.3k\Omega} \times R_{PLIM} \quad (4)$$

Figure 7-12 shows the power limiting in the TPS16410 and TPS16411 devices for $I_{OUT} < I_{OCP}$ and $I_{OCP} \le I_{OUT} < I_{fast\text{-}trip}$.

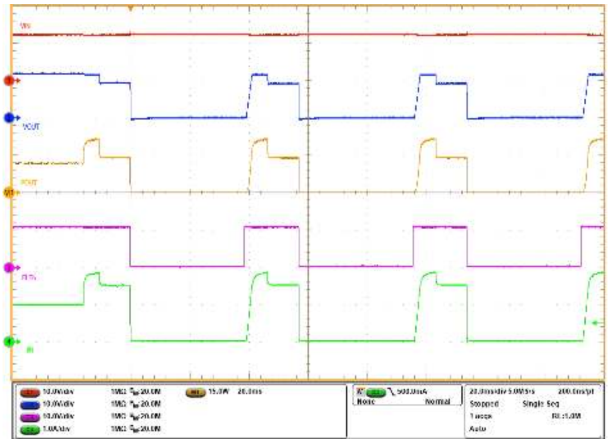


Figure 7-12. Power Limiting ($I_{OUT} < I_{OCP}$)

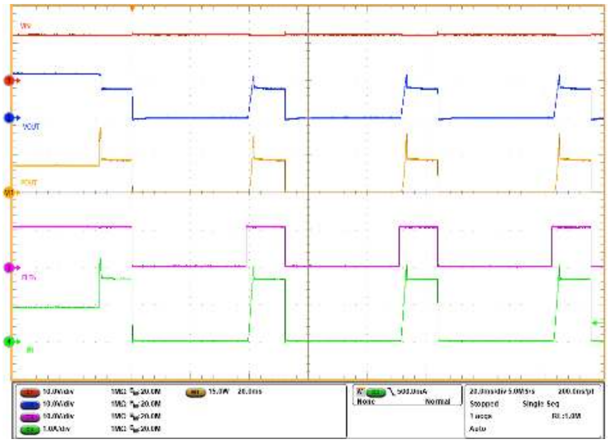


Figure 7-13. Power Limiting ($I_{OCP} \le I_{OUT} < I_{fast\text{-}trip}$)

During power limiting, the device dissipates a power of ($V_{IN} – V_{OUT}$) × I_{OUT} and the device gets heated up. If the junction temperature of device reaches thermal shutdown temperature (T_{TSD}), the device turns off the internal FET. If the device does not go into thermal shutdown, the internal FET is turned off after a duration of $t_{PLIM\text{-}DUR}$. After the internal FET is turned off, the TPS16410 and TPS16414 devices auto-retry while the TPS16411 and TPS16415 device latch off. If PLIM is connected to GND or left open, the device turns-off the internal FET. If the PDLY pin is left open or connected to GND, device provides $t_{PLIM\text{-}DUR}$ = 155ms unless the device enters thermal shutdown. Table 7-2 summarizes the device behavior for different output power and current.

Table 7-2. Power Limiting and Overload Response in TPS16410, TPS16411, TPS16414, and TPS16415 Devices

Output Power (P_{OUT}) or Output Current (I_{OUT})	Device Response
P_{OUT} < PLIM	The device provides power up to PLIM.
PLIM ≤ P_{OUT} and $I_{OUT} < I_{OCP}$	The device provides current up to IOCP for a duration of PDLY and then limits power to PLIM for a maximum duration of $t_{PLIM\text{-}DUR}$.
$I_{OCP} \le I_{OUT} < I_{fast\text{-}trip}$	The device limits current to PLIM for a maximum duration of $t_{PLIM\text{-}DUR}$.
$I_{fast\text{-}trip} \le I_{OUT} < I_{SCP}$	The device turns off the internal FET after a delay of $t_{fast\text{-}trip}$.
$I_{SCP} \le I_{OUT}$	The device turns off the internal FET after a delay of t_{SCP_dly}.

7.3.5.1 Internal Current Limit for the TPS16410 and TPS16411

In power limiting devices, there is an internal current limit. If during power up, the output current exceeds overcurrent protection setpoint (I_{OCP}), these devices limit current to 0.81 × I_{OCP}.

TPS16410, TPS16411, TPS16414, and TPS16415 devices also limit the output current if PLIM is set to more than (V_{OUT} × I_{OCP}) and I_{OUT} exceeds I_{OCP}.

7.3.6 Overcurrent Protection (I_{OCP}) and Blanking Time (IDLY or PDLY) for Transient Loads

In TPS1641x devices, configure the overcurrent protection set-point by connecting a resistor on I_{OCP} pin. Calculate the resistor value for overcurrent using Equation 5.

$$I_{OCP} = \frac{2.25A}{R_{IOCP}} \times 7.32k\Omega \quad (5)$$

If the IOCP pin is left open or connected to GND, the device turns off the internal FET.

The devices also provide blanking time for overload or overcurrent events. Configure this blanking time by connecting a capacitor on IDLY or PDLY. Calculate the blanking time using Equation 6.

If IDLY/PDLY pin is left open or connected to GND, device disables the blanking time and directly goes into power or current limiting.

$$\text{Blanking Time (IDLY or PDLY)} = \frac{6.5\text{ms}}{12\text{nF}} \times \text{CDLY} \quad (6)$$

7.3.7 Fast-Trip and Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When an output short-circuit is detected and output current reaches I_{SCP} level, the device turns off the internal FET after a delay of t_{SCP_dly}.

In case of fast input transients, the current through internal FET rises rapidly, but these transients can lead to false turn-off of internal FET due to excessive flow of current through internal FET. To prevent false tripping during these input transients, the device includes fast-trip comparator, which turns off the internal FET if the output current exceeds $I_{fast\text{-}trip}$ for a duration of $t_{fast\text{-}trip}$. Figure 7-14 shows the short-circuit response of the device.

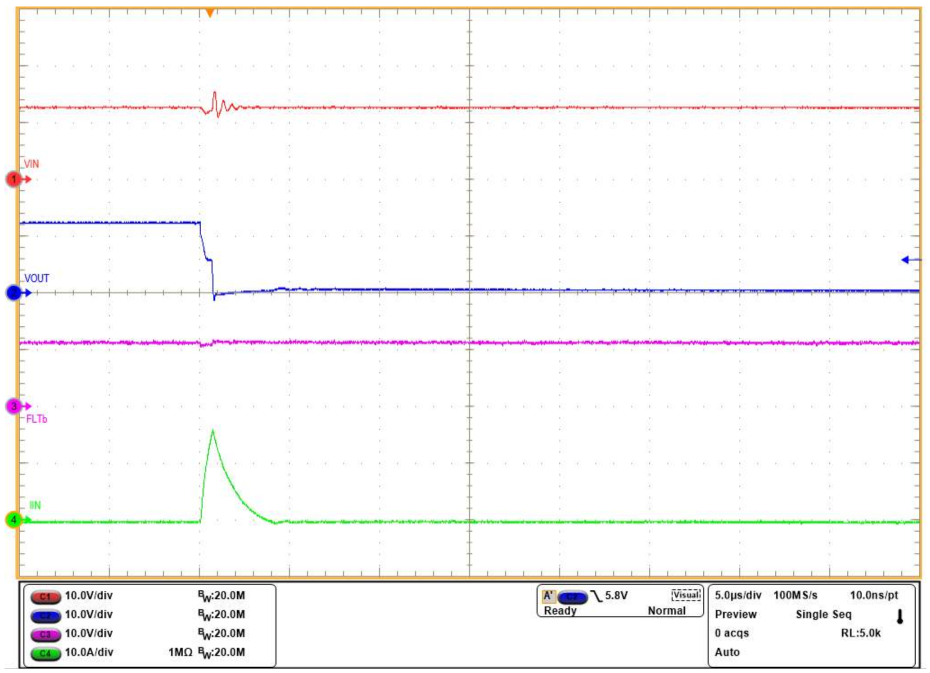


Figure 7-14. Short-Circuit Response with V_{IN} = 12V

7.3.8 Analog Load Current Monitor (IMON) on the IOCP Pin

The device allows the system to monitor the output load current accurately by providing an analog current on the IOCP/IMON pin, which is proportional to the current through the FET. The resistor on IOCP/IMON pin converts this current into voltage, use this voltage to monitor the output current. Calculate the output current from voltage at IOCP/IMON pin by using Equation 7.

$$I_{OUT} = \frac{V_{IOCP} - (OS_{IMON} \times R_{IOCP})}{G_{IMON} \times R_{IOCP}} \quad (7)$$

7.3.9 IN to OUT Short Detection (TPS16410, TPS16411, TPS16412, and TPS16413)

TPS16410, TPS16411, TPS16412, and TPS16413 devices include short detection across IN and OUT pins. If the device detects a resistance less than R_{short} across IN and OUT pins, the device asserts the $\overline{FLT}$ pin low. See the *Section 6.5* for R_{short} and *Section 6.6* for $t_{IN\_OUT\_Short\_Detect}$.

At start-up, the device keeps $\overline{\text{FLT}}$ low and the internal FET off. The device detects for short across IN to OUT before turning on the internal FET. If device does not detect any short across IN to OUT, the device de-asserts the $\overline{\text{FLT}}$ and enables the internal FET. After start-up, the device detects for short across IN to OUT at regular intervals and asserts the $\overline{\text{FLT}}$ pin after a delay of $t_{IN\_OUT\_Short\_Detect}$. After the device detects IN to OUT short, it latches off. To reset the latch, toggle EN/SHDN or recycle the Vcc supply. To reset the latch, keep EN/SHDN pin low for duration more than t_{Low_SHDN}. Figure 7-15 shows the response of device for IN to OUT short. In case of switching loads on output of device, see Table 7-3 for recommended device variants based on switching load frequency f_{SW} (in kHz) and ripple load current I_{Ripple} (in mAp-p).

Table 7-3. Recommended Device Variants

Switching Load Frequency	$(I_{Ripple} / f_{SW}) \geq 2$	$(I_{Ripple} / f_{SW}) < 2$
0 to 5Hz	TPS16410, TPS16411, TPS16412, TPS16413, TPS16414, TPS16415, TPS16416, or TPS16417	
> 5Hz	TPS16414, TPS16415, TPS16416, or TPS16417	TPS16410, TPS16411, TPS16412, TPS16413, TPS16414, TPS16415, TPS16416, or TPS16417

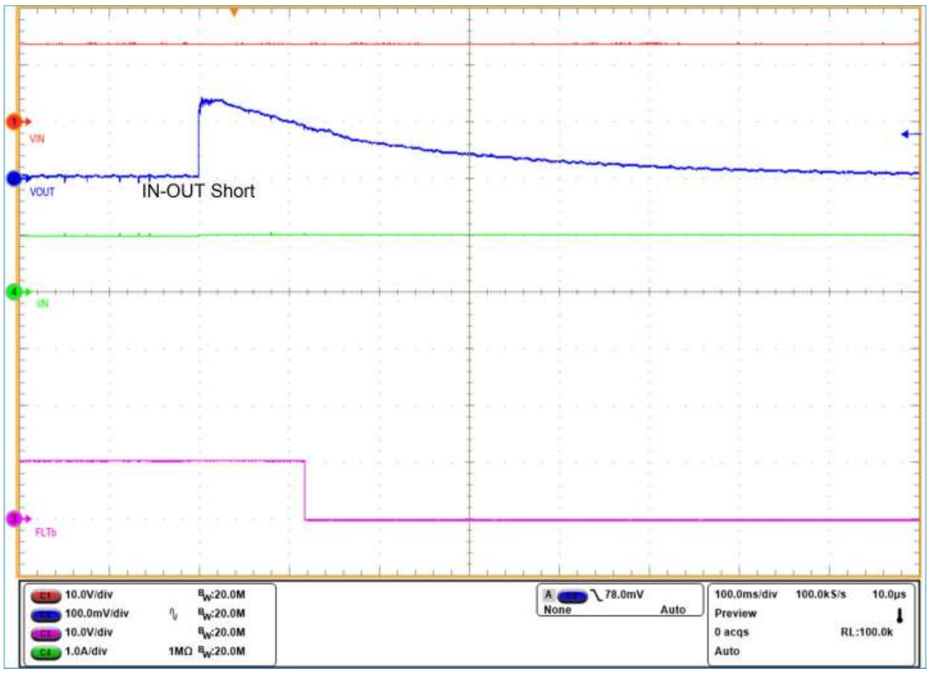


Figure 7-15. IN to OUT Short Detection for V_{IN} = 12V

7.3.10 Thermal Shutdown and Overtemperature Protection

During power or current limiting, there is a power dissipation $[(V_{IN} - V_{OUT}) \times I_{OUT}]$ in the internal FET of the device. Due to this power dissipation, the temperature (T_J) of device increases. When the device temperature increases above T_{TSD}, it shuts down. After the thermal shutdown, the TPS16411, TPS16413, TPS16415, and TPS16417 remain latched. To reset the latch, toggle EN/$\overline{\text{SHDN}}$ or recycle the Vcc supply. To reset the latch, keep EN/$\overline{\text{SHDN}}$ pin low for duration more than t_{Low_SHDN}.

After thermal shutdown, the TPS16410, TPS16412, TPS16414, and TPS16416 devices wait for temperature to go below $[T_{TSD} - T_{TSD\text{-}hyst}]$ and then the device restarts after a delay of t_{retry}.

7.3.11 Fault Response and Indication ($\overline{\text{FLT}}$)

$\overline{\text{FLT}}$ is an open-drain output to indicate the overvoltage, IN to OUT short, overtemperature, current limit, and power limit events. Table 7-4 summarizes the state of $\overline{\text{FLT}}$ pin under different events. To prevent excessive dissipation in device during adjacent pin short test ($\overline{\text{FLT}}$ to EN/$\overline{\text{SHDN}}$), pull up the $\overline{\text{FLT}}$ pin with a resistor ($R_{\overline{FLT}}$) such that sink current into $\overline{\text{FLT}}$ pin is less than 3mA. Figure 7-16 shows the connection diagram for $\overline{\text{FLT}}$ pin with a pullup resistor.

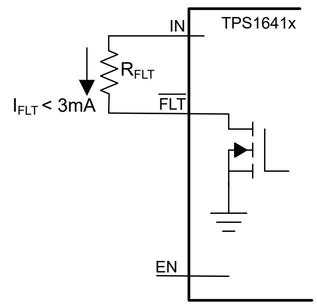


Figure 7-16. $\overline{FLT}$ Output in the TPS1641x

Table 7-4. $\overline{FLT}$ Pin Indication for Different Events

Event, Condition	$\overline{FLT}$ Pin	Retry Delay With IDLY/ PDLY = Open or GND for TPS16410, TPS16412, TPS16414, and TPS16416	Retry Delay With Capacitor on IDLY/PDLY pin for TPS16410, TPS16412, TPS16414, and TPS16416
Overvoltage protection (V_{OVP} > V_{OVPR})(1)	Low	NA	NA
IN to short detection (TPS16410, TPS16411, TPS16412, and TPS16413)	Low	No retry, latch off	No retry, latch off
Thermal shutdown (T_J > T_{TSD})	Low	620ms	8 × $t_{PDLY/IDLY}$
After current or power limiting timeout	Low	620ms	8 × $t_{PDLY/IDLY}$

(1) For overvoltage protection, device turns on the FET as V_{OVP} falls below V_{OVPF}

7.4 Device Functional Modes

The device can be brought into low power shutdown mode by bringing the EN/$\overline{SHDN}$ pin low. In low power shutdown mode, the internal blocks of devices are shut down and it takes I_{QSD} from V_{CC} supply. See the *Enable and Shutdown Input (EN/$\overline{SHDN}$)* section for details.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

TPS1641x devices include power limiting or current limiting for a low power circuit (as per IEC60335 and UL60730 standards) in appliances, HVAC actuators, and medical equipment. TPS1641x devices also have IN to OUT short detection for internal FET for IN-OUT short testing during IEC60335 or UL60730 certifications. The TPS16410 and TPS16411 have an accurate power limiting feature while the TPS16412 and TPS16413 have an accurate current limiting feature. For transient current required for start-up of motors or actuators, TPS1641x devices have a configurable overcurrent protection threshold (IOCP) and configurable blanking time (IDLY/PDLY). For start-up with big capacitance (< 1mF) on output, the TPS1641x include dVdT feature to control the output slew rate and limiting the inrush current during power up. Monitor the output current from the IOCP or IMON pin by sensing the voltage on this pin.

8.2 Typical Application: 15W Power Limiting for Low Power Circuits (LPCs)

Use the TPS16410 and TPS16411 for 15W power limiting for low-power circuits in IEC60335 and UL60730 standards. Use a resistor on the PLIM pin to configure the output power limit. Figure 8-1 provides a typical application circuit for 15W power limiting.

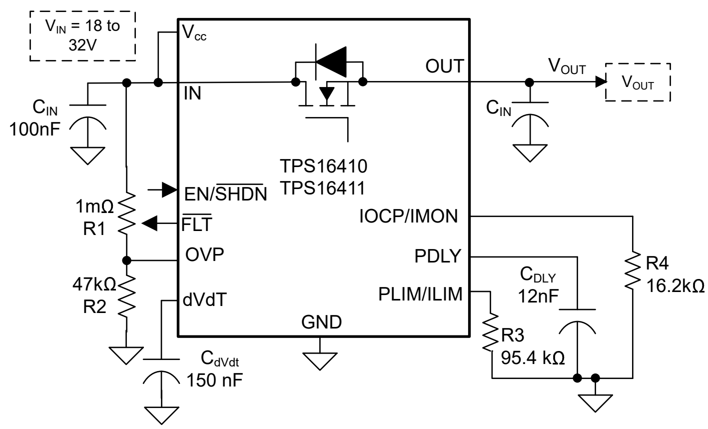


Figure 8-1. 15W Power Limiting for Low-Power Circuits

8.2.1 Design Requirements

Table 8-1. Design Parameters

Parameter	Value
V_{IN}	18V to 32V
P_{OUT}	≤ 15W
Overcurrent protection	1A
Output capacitance (C_{OUT})	470µF
I_{INRUSH}	≤ 350mA
Blanking time for transients (PDLY)	6.5ms

8.2.2 Detailed Design Procedure

8.2.2.1 Setting Overvoltage Setpoints

Set input overvoltage protection setpoints by connecting resistors (R1, R2) from the IN pin to OVP pin. Calculate the value of resistors using Equation 8 and Equation 9. To set the OVP rising setpoint to 32V, R1 = 1MΩ and R2 = 47kΩ are selected.

$$\mathrm{OVP\ Rising\ Setpoint} = \frac{V_{OVPR} \times (R1 + R2)}{R2} \tag{8}$$

$$\mathrm{OVP\ Falling\ Setpoint} = \frac{V_{OVPF} \times (R1 + R2)}{R2} \tag{9}$$

8.2.2.2 Setting the Output Overcurrent Setpoint (IOCP)

To set the output overcurrent setpoint, a resistor (R4) is required on the IOCP pin. To calculate the value of this resistor (R4), use Equation 5. For I_{OCP} = 1A, R4 is selected as 16.2kΩ.

8.2.2.3 Setting the Output Power Limit

For setting the output power limit, a resistor (R3) is required on the PLIM pin. To calculate the value of power limit, use Equation 4. To keep output power limit ≤ 15W, R3 is selected as 95.3kΩ.

8.2.2.4 Monitoring the Output Current

Monitor the output current on IOCP or IMON by reading the voltage on this pin. Calculate the output current using Equation 7.

8.2.2.5 Limiting the Inrush Current and Setting the Output Slew Rate

For charging the large capacitors on output, control the output slew rate by using a capacitor on dVdt pin. Estimate the value of inrush current by Equation 10. To keep the inrush current below 350mA, C_{dVdt} is selected as 150nF.

$$I_{INRUSH} = \frac{I_{dVdt} \times G_{dVdt} \times C_{OUT}}{C_{dVdt}} \tag{10}$$

8.2.3 Application Curves

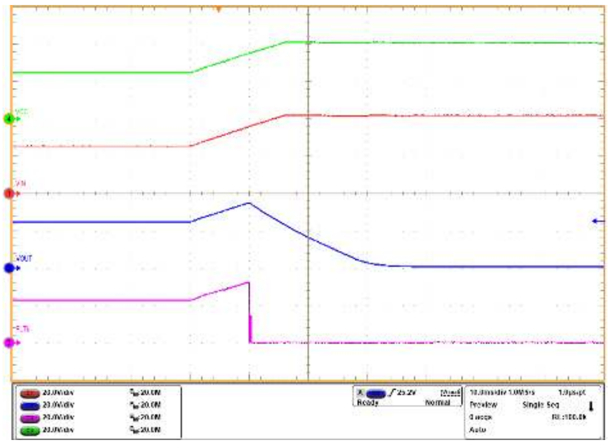


Figure 8-2. Overvoltage Protection up to 40V

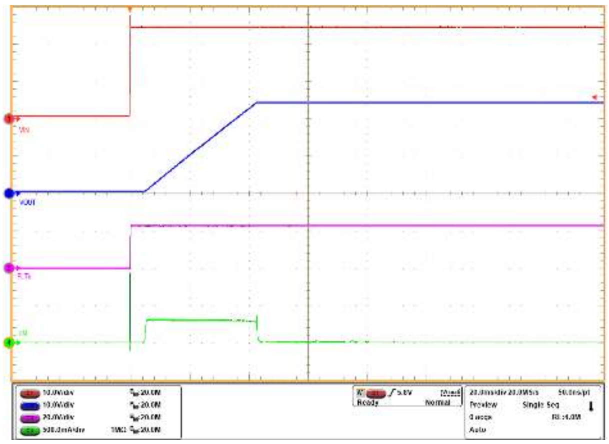


Figure 8-3. Inrush Current Control for Hot Plugin at Input

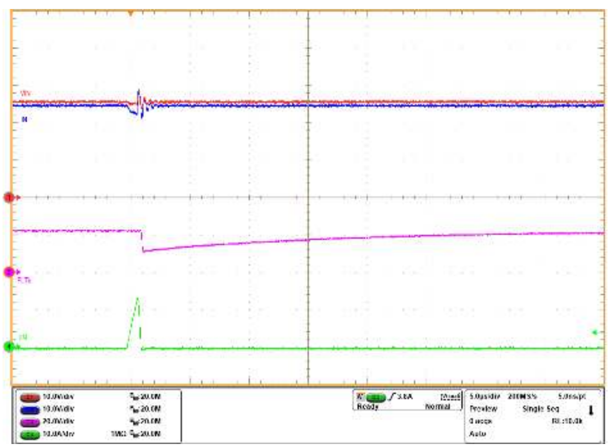


Figure 8-4. Output Short-Circuit Protection

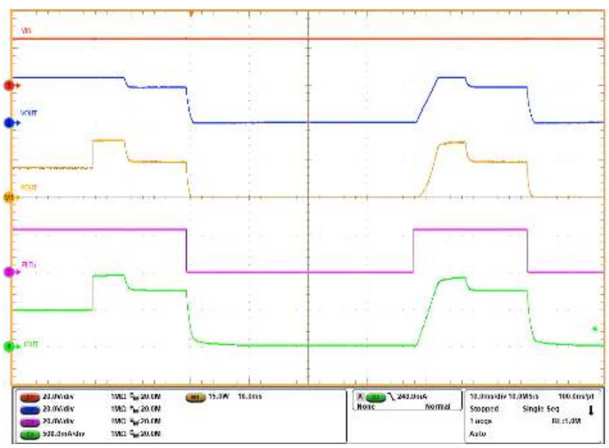


Figure 8-5. 15W Power Limiting with TPS16410 ($I_{OUT} < I_{OCP}$)

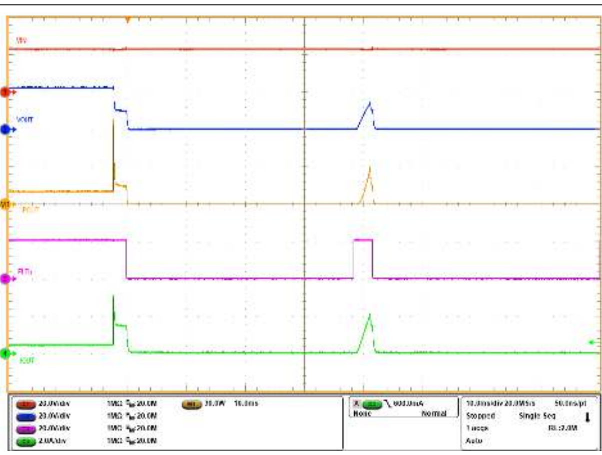


Figure 8-6. 15W Power Limiting with TPS16410 ($I_{OCP} \leq I_{OUT} < I_{fast\text{-}trip}$)

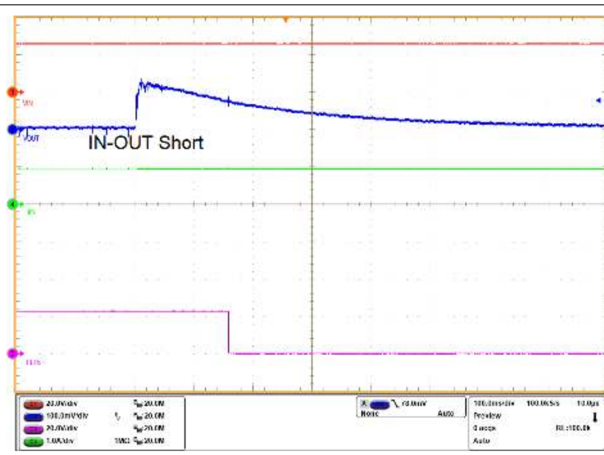


Figure 8-7. IN to OUT Short Detection with V_{IN} = 24V

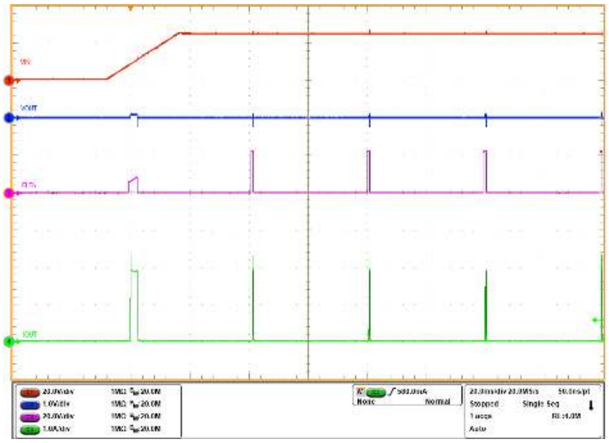


Figure 8-8. Power-Up Into Short

8.3 System Examples

8.3.1 Accurate Power or Current Limiting at the Output of DC/DC or Flyback Converter

For systems using a DC/DC converter or a flyback converter, use the device for accurate power or current limiting (± 5%) at the output. For additional protection, the device has a fault pin and it is asserted in case of overvoltage, overcurrent or overpower, IN-short detection and thermal shutdown events. Use the fault to turn-off the DC/DC converter or flyback converter providing the power to input of TPS1641 for the load. The device has separate Vcc pin for powering itself and it can remain on with Vcc supply. Figure 8-9 shows the application at the output of DC/DC or flyback converter.

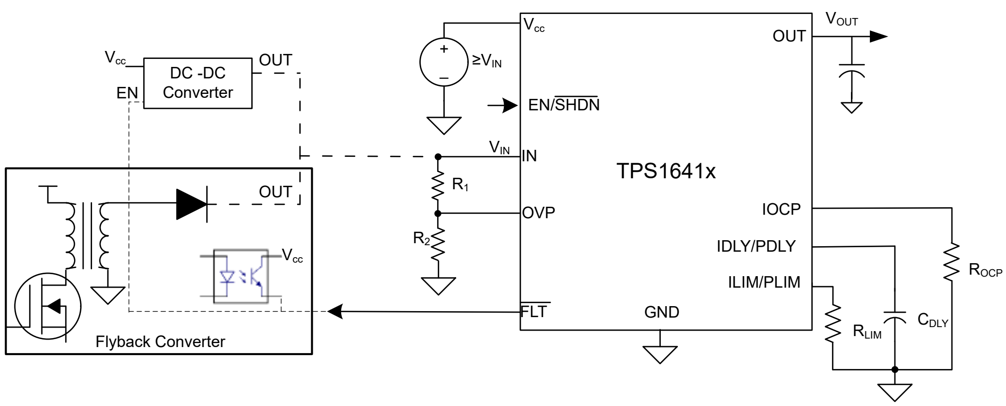


Figure 8-9. Accurate Power or Current Limiting at the Output of DC/DC or Flyback Converter

8.4 Best Design Practices

- Use C_{IN} ≥ 10nF for decoupling V_{cc} and IN pins.
- Do not leave the OVP, PLIM/ILIM, and IOCP/IMON pins open or floating.
- Connect the PowerPAD of the device to GND on the PCB.
- Do not connect the EN/$\overline{\text{SHDN}}$ pin to voltage more than 5V.

8.5 Power Supply Recommendations

- Use 4.5V ≤ V_{IN} ≤ 40V for the TPS16410 and TPS16411.
- Use 2.7V ≤ V_{IN} ≤ 40V for the TPS16412 and TPS16413.
- Use $V_{IN} \le V_{CC}$ ≤ 60V.
- Pull up $\overline{\text{FLT}}$ with voltage ≤ 60V. Use a pullup resistor to keep current into the $\overline{\text{FLT}}$ pin < 3mA.

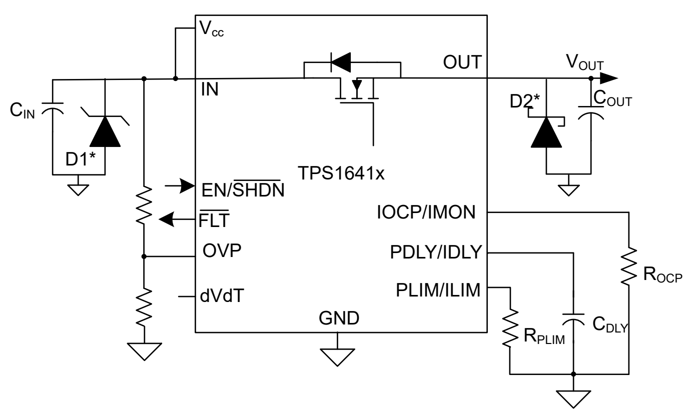
8.5.1 Transient Protection

In the case of a short-circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Figure 8-10 shows the transient protection circuit. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode (D2) from the OUT pin ground to absorb negative spikes. The OUT pin has an absolute maximum rating of –1V for negative transient spikes on output.
- Connect a low-ESR capacitor larger than 1µF at the OUT pin very close to the device.
- Use a low-value ceramic capacitor C_{IN} = 0.1µF to absorb the energy and dampen the transients. Estimate the approximate value of input capacitance using Equation 11.

$$V_{IN-SPIKE} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \qquad (11)$$

- Some applications require additional Transient Voltage Suppressor (TVS) to keep transients below the absolute maximum rating of the device. A TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input of the device. Use an appropriate TVS to clamp the transient voltage below the absolute maximum rating of the device.



TVS D1* and Schottky D2* are optional diodes for transient protection on the input and output.

Figure 8-10. Transient Protection with TPS1641x

8.6 Layout

8.6.1 Layout Guidelines

- Verify that the high current-carrying power-path connections are as short as possible and are sized to carry at least twice the full-load current.
- Tie the GND (PowerPAD) pin to the PCB ground plane at the terminal of the IC with the shortest possible trace. The PCB ground must be a copper plane or island on the board. TI recommends to have a separate ground plane island for the eFuse. This plane does not carry any high currents and serves as a quiet ground reference for all the critical analog signals of the eFuse. Connect the device ground plane to the system power ground plane using a star connection.
- The best placement of the decoupling capacitor (C_{IN}) is closest to the IN and GND pins of the device. Take care to minimize the loop area that the bypass-capacitor connection, the IN pin, and the GND pin of the IC form.
- Locate the following support components close to the connection pins:
  - R_{ILM} or R_{PLM}
  - R_{IOCP}
  - C_{DLY}
  - C_{dVdT}
  - Resistors for OVP
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for these components to the device must be as short as possible to reduce parasitic effects on the current limit, overcurrent blanking interval, and soft-start timing.
- Because the bias current on ILM pin directly controls the overcurrent protection behavior of the device, the PCB routing of this node must be kept away from any noisy (switching) signals.
- Physically place protection devices such as TVS, snubbers, capacitors, or diodes close to the device the protection device is intended to protect. Route these protection devices with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads. TI recommends to add a ceramic decoupling capacitor (C_{OUT}) of 1µF or greater between OUT and GND. These components must be physically close to the OUT pins. Take care to minimize the loop area that the Schottky diode and bypass-capacitor connection, the OUT pin, and the GND pin of the IC form.

8.6.2 Layout Example

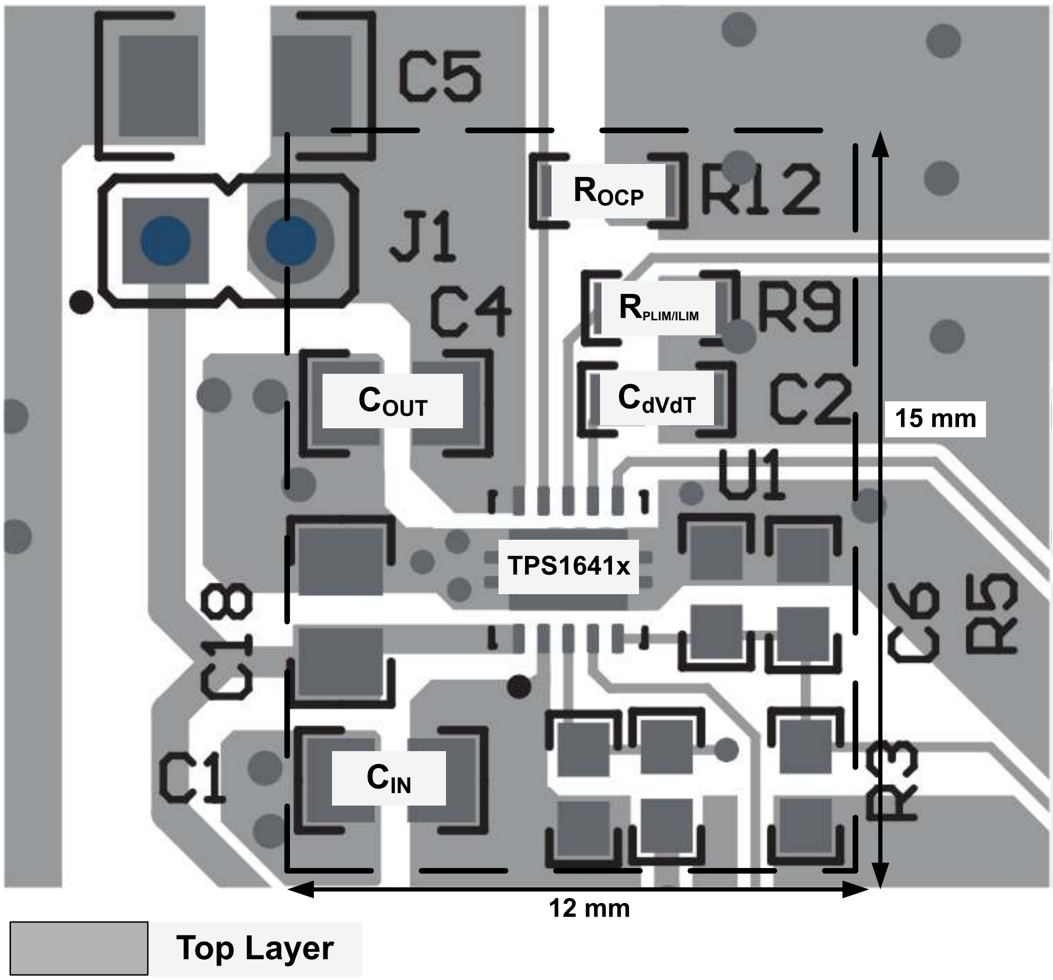


Figure 8-11. Layout Example

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2023) to Revision C (June 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added UL 2367 recognition status	1
• Added IEC 62368-1 CB certification	1

Changes from Revision A (December 2022) to Revision B (April 2023)	Page
• Added information for new device variants throughout the document	1
• Added recommendations for new device variants	20

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS16410DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16410
TPS16410DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16410
TPS16411DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16411
TPS16411DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16411
TPS16412DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16412
TPS16412DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16412
TPS16413DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16413
TPS16413DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16413
TPS16413DRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16413
TPS16413DRCRG4.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16413
TPS16414DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16414
TPS16414DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16414
TPS16415DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16415
TPS16415DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16415
TPS16416DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16416
TPS16416DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16416
TPS16417DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16417
TPS16417DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T16417

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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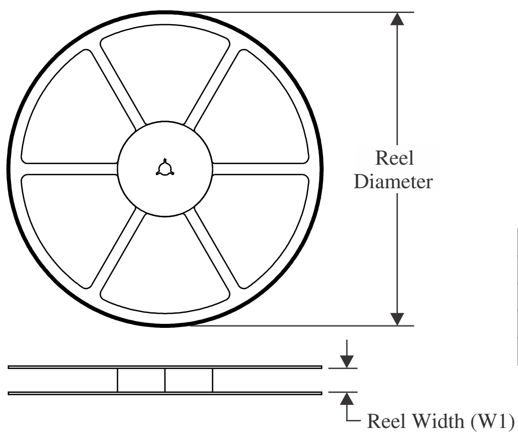
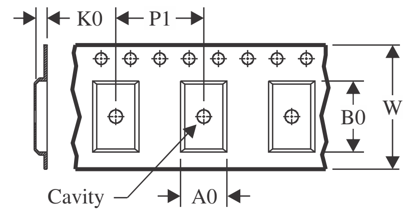
TAPE AND REEL INFORMATION

REEL DIMENSIONS

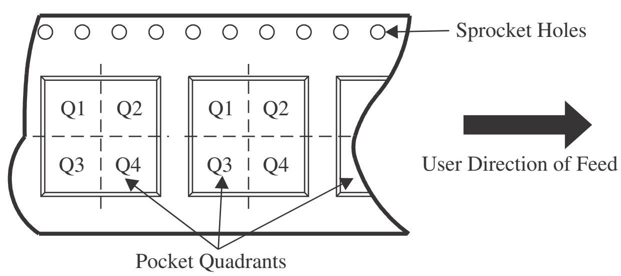


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

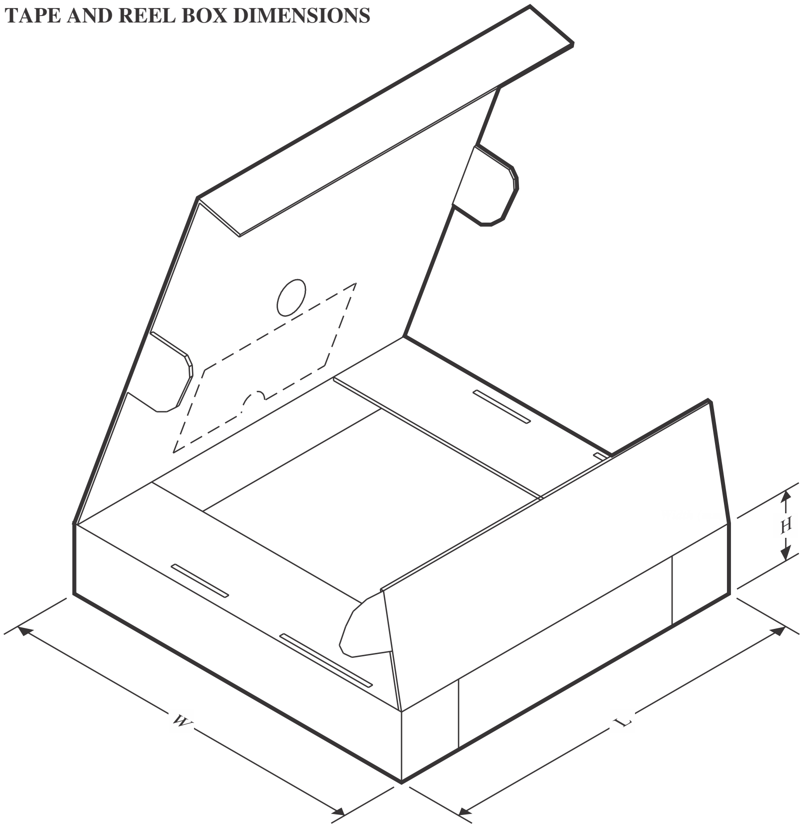
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS16410DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS16411DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS16412DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS16413DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS16413DRCRG4	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS16414DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS16415DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS16416DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS16417DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

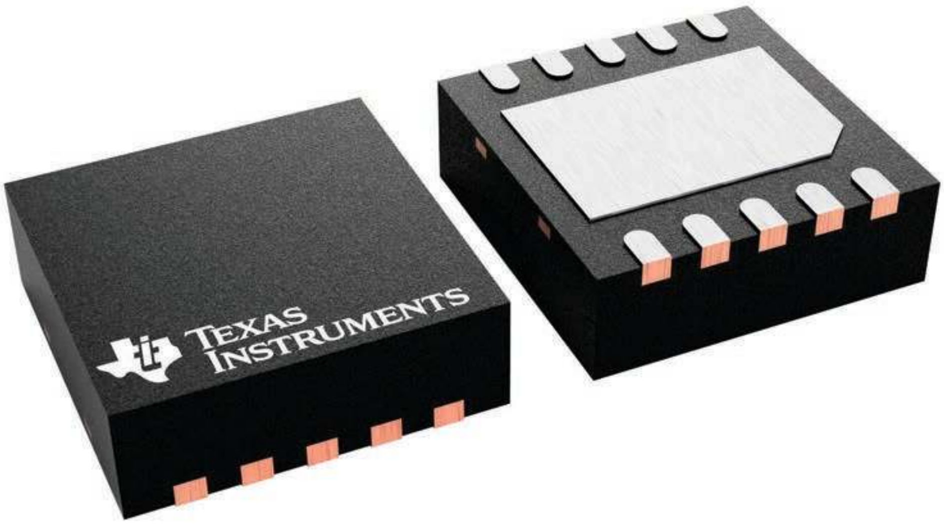
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS16410DRCR	VSON	DRC	10	3000	360.0	360.0	36.0
TPS16411DRCR	VSON	DRC	10	3000	360.0	360.0	36.0
TPS16412DRCR	VSON	DRC	10	3000	360.0	360.0	36.0
TPS16413DRCR	VSON	DRC	10	3000	360.0	360.0	36.0
TPS16413DRCRG4	VSON	DRC	10	3000	367.0	367.0	35.0
TPS16414DRCR	VSON	DRC	10	3000	360.0	360.0	36.0
TPS16415DRCR	VSON	DRC	10	3000	360.0	360.0	36.0
TPS16416DRCR	VSON	DRC	10	3000	360.0	360.0	36.0
TPS16417DRCR	VSON	DRC	10	3000	360.0	360.0	36.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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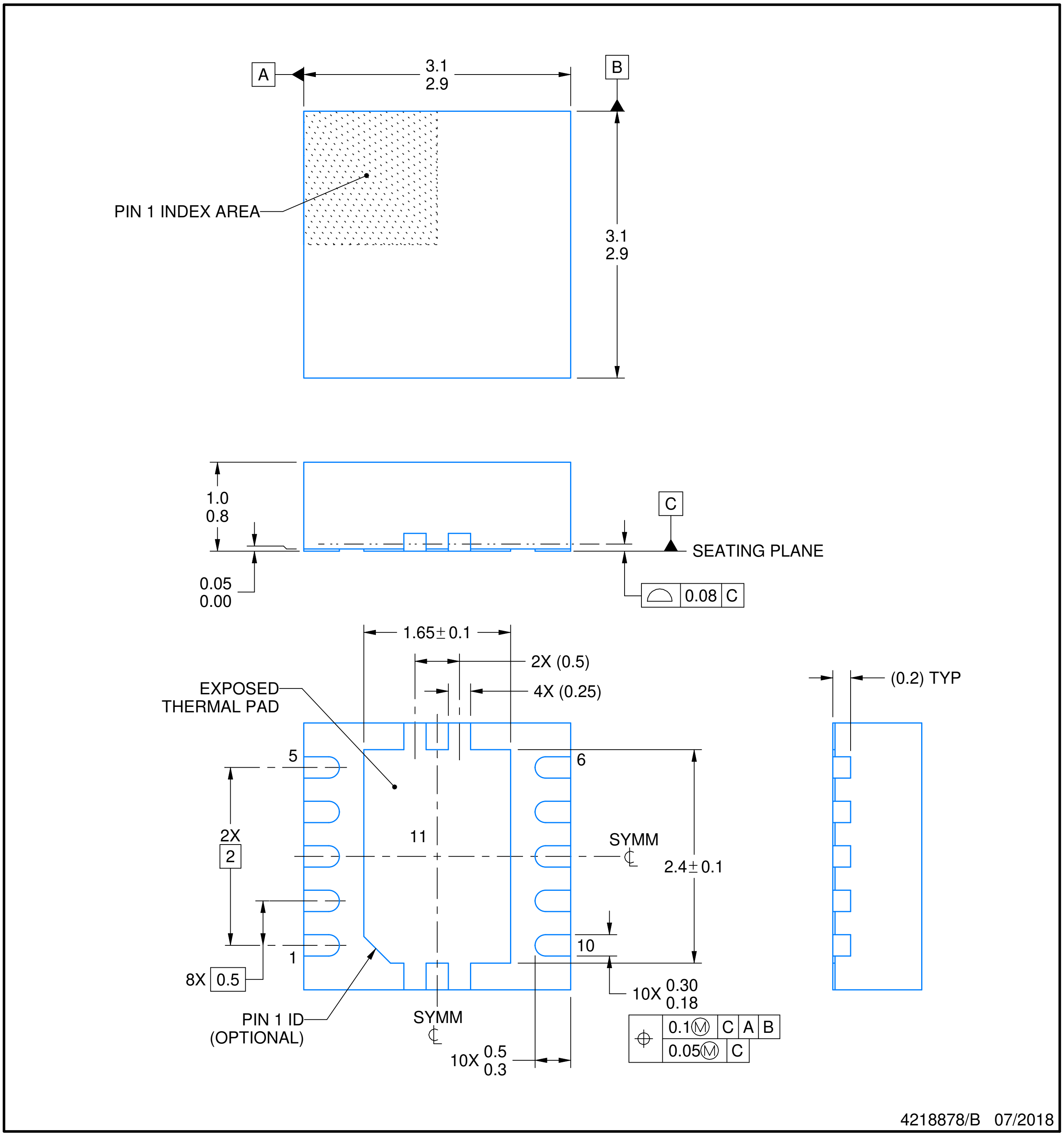
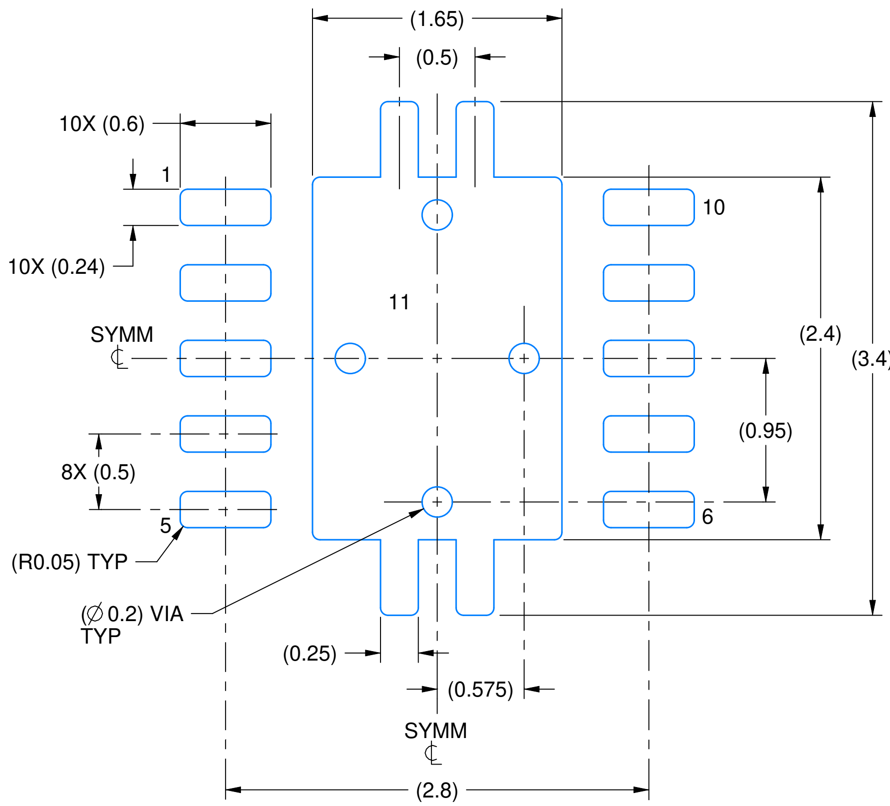
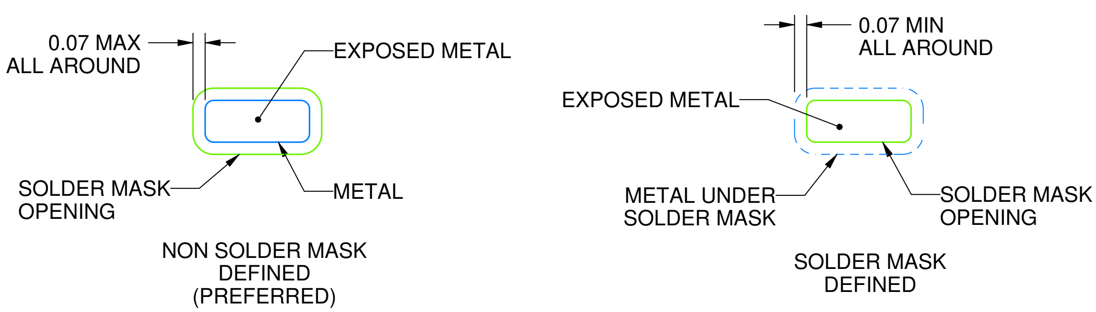


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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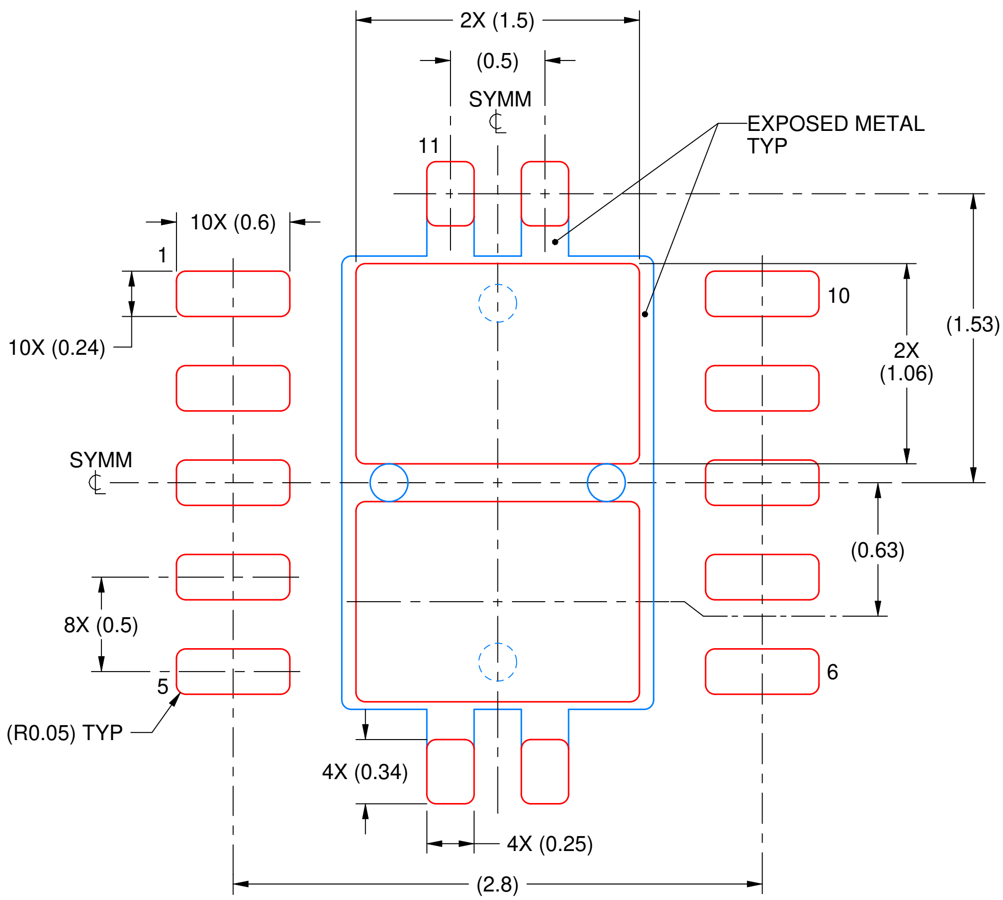
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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