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Product Reference Information

Part Number: DAC43401DSGRQ1

Manufacturer: Texas Instruments

Package: 8-WFDFN Exposed Pad

Availability: Please confirm with sales

Product Page:

https://antrexco.com/product/details/texas-instruments/dac43401dsgrq1.html

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

DACx3401-Q1 Automotive, 10-Bit and 8-Bit, Voltage-Output Smart DACs With Nonvolatile Memory and PMBus™ Compatible I²C Interface in Tiny 2 × 2 WSON

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- 1 LSB INL and DNL (10-bit and 8-bit)
- Wide operating range:
  - Power supply: 1.8 V to 5.5 V
- PMBus™ compatible I²C interface
  - Standard, fast, and fast mode plus
  - Four slave address options configured by A0 pin
  - 1.62-V V_{IH} with V_{DD} = 5.5 V
- User-programmable nonvolatile memory (NVM, EEPROM)
  - Save and recall all register settings
- Programmable waveform generation: Square, ramp, and sawtooth
- Pulse-width modulation (PWM) output using triangular waveform and FB pin
- Digital slew-rate control
- Internal reference
- Very-low power: 0.2 mA at 1.8 V
- Flexible startup: High impedance or 10K-GND
- Tiny package: 8-pin WSON (2 mm × 2 mm)

2 Applications

- Automotive USB charge
- Headlight
- Rear light

3 Description

The 10-bit DAC53401-Q1 and 8-bit DAC43401-Q1 (DACx3401-Q1) are a pin-compatible family of automotive, buffered, voltage-output, smart digital-to-analog converters (DACs). These devices consume very low power, and are available in a tiny 8-pin WSON package. The feature set, combined with the tiny package and low power, make the DACx3401-Q1 an excellent choice for applications such as LED and general-purpose bias point generation, power supply control, and PWM signal generation.

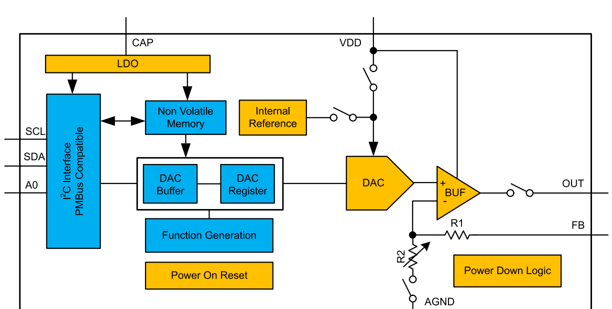
These devices have nonvolatile memory (NVM), an internal reference, and a PMBus-compatible I²C interface. The DACx3401-Q1 operates with either an internal reference or the power supply as a reference, and provides full-scale output of 1.8 V to 5.5 V. The devices communicate through the I²C interface. These devices support I²C standard mode, fast mode, and fast mode plus.

The DACx3401-Q1 are smart DAC devices because of their advanced integrated features. The force-sense output, PWM output, and NVM capabilities of these smart DACs enable system performance and control without the use of software.

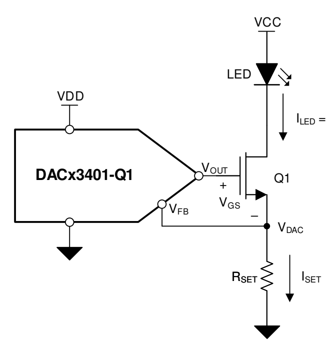
Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
DAC53401-Q1	WSON (8)	2.00 mm × 2.00 mm
DAC43401-Q1		

(1) For all available packages, see the package option addendum at the end of the data sheet.



Functional Block Diagram



LED Biasing With the DACx3401-Q1

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4 Revision History

DATE	REVISION	NOTES
October 2020	*	Initial release.

5 Device Comparison Table

DEVICE	RESOLUTION
DAC53401-Q1	10-bit
DAC43401-Q1	8-bit

6 Pin Configuration and Functions

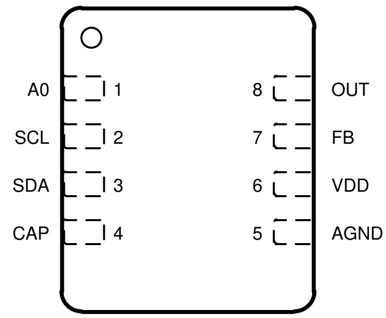


Figure 6-1. DSG Package, 8-Pin WSON, Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	1	Input	Four-state address input
AGND	5	Ground	Ground reference point for all circuitry on the device
CAP	4	Input	External capacitor for the internal LDO. Connect a capacitor (0.5 µF to 15 µF) between CAP and AGND.
FB	7	Input	Voltage feedback pin
OUT	8	Output	Analog output voltage from DAC
SCL	2	Input	Serial interface clock. This pin must be connected to the supply voltage with an external pullup resistor.
SDA	3	Input/output	Data are clocked into or out of the input register. This pin is a bidirectional, and must be connected to the supply voltage with an external pullup resistor.
VDD	6	Power	Analog supply voltage: 1.8 V to 5.5 V

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{DD}	Supply voltage, V_{DD} to A_{GND}	–0.3	6	V
	Digital input(s) to A_{GND}	–0.3	V_{DD} + 0.3	V
	CAP to A_{GND}	–0.3	1.65	V
	V_{FB} to A_{GND}	–0.3	V_{DD} + 0.3	V
	V_{OUT} to A_{GND}	–0.3	V_{DD} + 0.3	V
	Current into any pin	–10	10	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1] HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C5	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage to ground (A_{GND})	1.71		5.5	V
V_{IH}	Digital input high voltage, 1.7 V < V_{DD} ≤ 5.5 V	1.62			V
V_{IL}	Digital input low voltage			0.4	V
T_A	Ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		DACx3401-Q1	UNIT
		DSG (WSON)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1x, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution	DAC53401-Q1	10			Bits
	Resolution	DAC43401-Q1	8			Bits
INL	Relative accuracy[(1)]		–1		1	LSB
DNL	Differential nonlinearity[(1)]		–1		1	LSB
	Zero code error	Code 0d into DAC		6	12	mV
	Zero code error	Internal V_{REF}, gain = 4x, V_{DD} = 5.5 V		6	15	mV
	Zero code error temperature coefficient			±10		µV/°C
	Offset error[(4)]		–0.6	0.25	0.6	%FSR
	Offset error temperature coefficient[(4)]			±0.0003		%FSR/°C
	Gain error[(4)]		–0.5	0.25	0.5	%FSR
	Gain error temperature coefficient[(4)]			±0.0008		%FSR/°C
	Full scale error	1.8 V ≤ V_{DD} < 2.7 V, code 1023d into DAC, no headroom	–1	0.5	1	%FSR
	Full scale error	2.7 V ≤ V_{DD} ≤ 5.5 V, code 1023d into DAC, no headroom	–0.5	0.25	0.5	%FSR
	Full scale error temperature coefficient			±0.0008		%FSR/°C
OUTPUT CHARACTERISTICS						
	Output voltage	Reference tied to V_{DD}	0		5.5	V
C_L	Capacitive load[(2)]	R_L = Infinite, phase margin = 30°			1	nF
C_L	Capacitive load[(2)]	R_L = 5 kΩ, phase margin = 30°			2	nF
	Load regulation	DAC at midscale, –10 mA ≤ I_{OUT} ≤ 10 mA, V_{DD} = 5.5 V		0.4		mV/mA
	Short circuit current	V_{DD} = 1.8 V, full-scale output shorted to A_{GND} or zero-scale output shorted to V_{DD}		10		mA
	Short circuit current	V_{DD} = 2.7 V, full-scale output shorted to A_{GND} or zero-scale output shorted to V_{DD}		25		mA
	Short circuit current	V_{DD} = 5.5 V, full-scale output shorted to A_{GND} or zero-scale output shorted to V_{DD}		50		mA
	Output voltage headroom[(1)]	To V_{DD} (DAC output unloaded, internal reference = 1.21 V), V_{DD} ≥ 1.21 × gain + 0.2 V		0.2		V
	Output voltage headroom[(1)]	To V_{DD} (DAC output unloaded, reference tied to V_{DD})		0.8		%FSR
	Output voltage headroom[(1)]	To V_{DD} (I_{LOAD} = 10 mA at V_{DD} = 5.5 V, I_{LOAD} = 3 mA at V_{DD} = 2.7 V, I_{LOAD} = 1 mA at V_{DD} = 1.8 V), DAC code = full scale	10			%FSR
	V_{OUT} dc output impedance	DAC output enabled and DAC code = midscale		0.25		Ω
	V_{OUT} dc output impedance	DAC output enabled and DAC code = 4d		0.25		Ω
	V_{OUT} dc output impedance	DAC output enabled and DAC code = 1016d		0.26		Ω
Z_O	V_{FB} dc output impedance[(3)]	DAC output enabled, DAC reference tied to VDD (gain = 1x) or internal reference (gain = 1.5x or 2x)	160	200	240	kΩ
Z_O	V_{FB} dc output impedance[(3)]	DAC output enabled, internal V_{REF}, gain = 3x or 4x	192	240	288	kΩ

7.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1x, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	V_{OUT} + V_{FB} dc output leakage(2)	At startup, measured when DAC output is disabled and held at V_{DD} / 2 for V_{DD} = 5.5 V			5	nA
	Power supply rejection ratio (dc)	Internal V_{REF}, gain = 2x, DAC at midscale; V_{DD} = 5 V ±10%		0.25		mV/V
DYNAMIC PERFORMANCE						
t_{sett}	Output voltage settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V		8		µs
		1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V, internal V_{REF}, gain = 4x		12		
	Slew rate	V_{DD} = 5.5 V		1		V/µs
	Power-on glitch magnitude	At startup (DAC output disabled), R_L = 5 kΩ, C_L = 200 pF		75		mV
		At startup (DAC output disabled), R_L = 100 kΩ		200		
	Output enable glitch magnitude	DAC output disabled to enabled (DAC registers at zero scale, R_L = 100 kΩ		250		mV
V_n	Output noise voltage (peak to peak)	0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		34		μV_{PP}
		Internal V_{REF}, gain = 4x, 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		70		
	Output noise density	Measured at 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.2		µV/√Hz
		Internal $V_{REF,}$ gain = 4x,, measured at 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.7		
	Power supply rejection ratio (ac)(3)	Internal V_{REF}, gain = 4x, 200-mV 50 or 60 Hz sine wave superimposed on power supply voltage, DAC at midscale		–71		dB
	Code change glitch impulse	±1 LSB change around mid code (including feedthrough)		10		nV-s
	Code change glitch impulse magnitude	±1 LSB change around mid code (including feedthrough)		15		mV
VOLTAGE REFERENCE						
	Initial accuracy	T_A = 25°C		1.212		V
	Reference output temperature coefficient(2)				50	ppm/°C
EEPROM						
	Endurance	–40°C ≤ T_A ≤ +85°C		20000		Cycles
		T_A > 85°C		1000		
	Data retention(2)	T_A = 25°C		50		Years
	EEPROM programming write cycle time(2)		10		20	ms
DIGITAL INPUTS						
	Digital feedthrough	DAC output static at midscale, fast mode plus, SCL toggling		20		nV-s
	Pin capacitance	Per pin		10		pF

7.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1x, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
	Load capacitor - CAP pin[(2)]		0.5		15	µF
I_{DD}	Current flowing into VDD	Normal mode, DACs at full scale, digital pins static		0.5	0.8	mA
		DAC power-down, internal reference power down		80		µA

(1) Measured with DAC output unloaded. For external reference between end-point codes: 8d to 1016d for 10-bit resolution, 2d to 254d for 8-bit resolution. For internal reference V_{DD} ≥ 1.21 x gain + 0.2 V, between end-point codes: 8d to 1016d for 10-bit resolution, 2d to 254d for 8-bit resolution.
(2) Specified by design and characterization, not production tested.
(3) Specified with 200-mV headroom with respect to reference value when internal reference is used.
(4) Measured with DAC output unloaded. For 10-bit resolution, between end-point codes: 8d to 1016d and for 8-bit resolution, between end-point codes: 2d to 254d.

7.6 Timing Requirements: I²C Standard Mode

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.8 V ≤ $V_{pull-up}$ ≤ V_{DD} V (unless otherwise noted)

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			0.1	MHz
t_{BUF}	Bus free time between stop and start conditions	4.7			µs
t_{HDSTA}	Hold time after repeated start	4			µs
t_{SUSTA}	Repeated start setup time	4.7			µs
t_{SUSTO}	Stop condition setup time	4			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	250			ns
t_{LOW}	SCL clock low period	4700			ns
t_{HIGH}	SCL clock high period	4000			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			1000	ns

7.7 Timing Requirements: I²C Fast Mode

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.8 V ≤ $V_{pull-up}$ ≤ V_{DD} V (unless otherwise noted)

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			0.4	MHz
t_{BUF}	Bus free time between stop and start conditions	1.3			μs
t_{HDSTA}	Hold time after repeated start	0.6			μs
t_{SUSTA}	Repeated start setup time	0.6			μs
t_{SUSTO}	Stop condition setup time	0.6			μs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			300	ns

7.8 Timing Requirements: I²C Fast Mode Plus

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.8 V ≤ $V_{pull-up}$ ≤ V_{DD} V (unless otherwise noted)

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			1	MHz
t_{BUF}	Bus free time between stop and start conditions	0.5			μs
t_{HDSTA}	Hold time after repeated start	0.26			μs
t_{SUSTA}	Repeated start setup time	0.26			μs
t_{SUSTO}	Stop condition setup time	0.26			μs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	50			ns
t_{LOW}	SCL clock low period	0.5			μs
t_{HIGH}	SCL clock high period	0.26			μs
t_F	Clock and data fall time			120	ns
t_R	Clock and data rise time			120	ns

7.9 Typical Characteristics: V_{DD} = 1.8 V (Reference = V_{DD}) or V_{DD} = 2 V (Internal Reference)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)

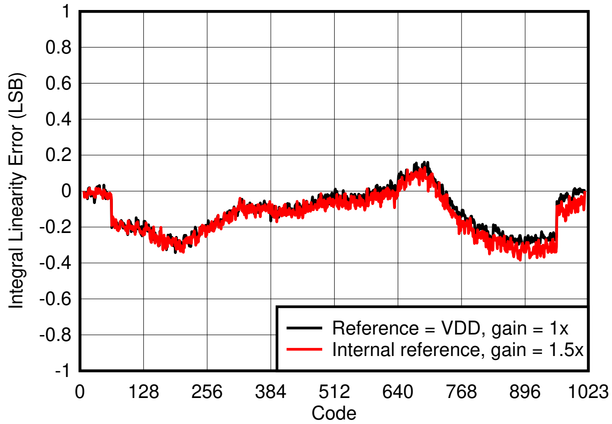


Figure 7-1. Integral Linearity Error vs Digital Input Code

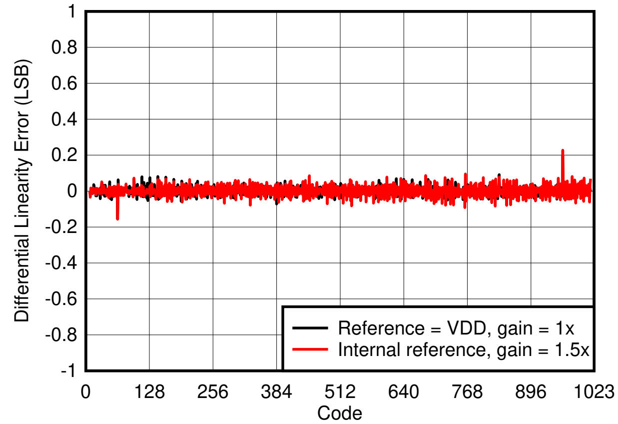


Figure 7-2. Differential Linearity Error vs Digital Input Code

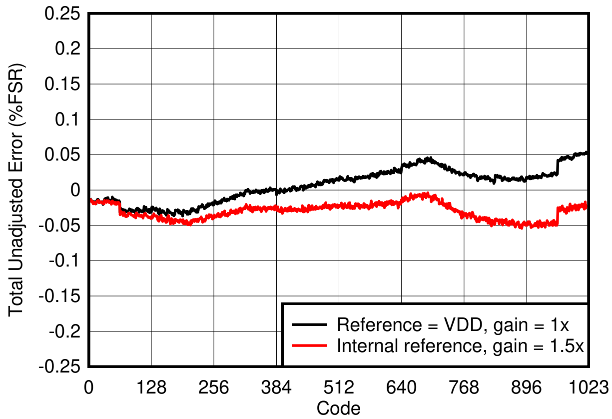


Figure 7-3. Total Unadjusted Error vs Digital Input Code

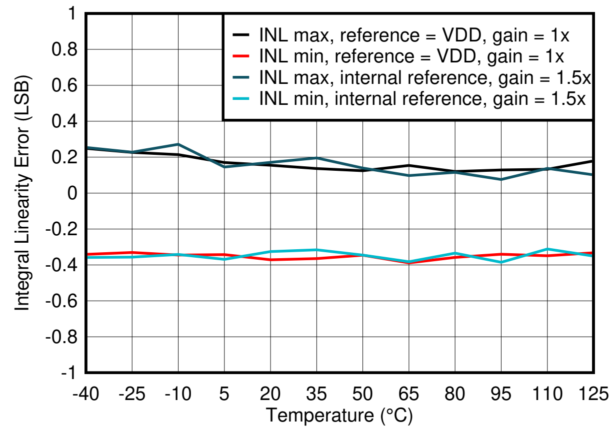


Figure 7-4. Integral Linearity Error vs Temperature

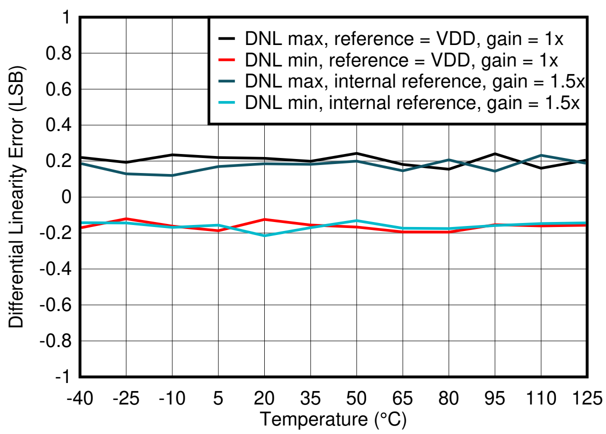


Figure 7-5. Differential Linearity Error vs Temperature

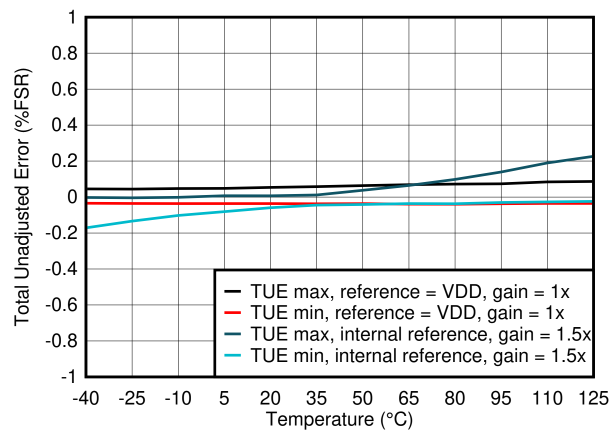
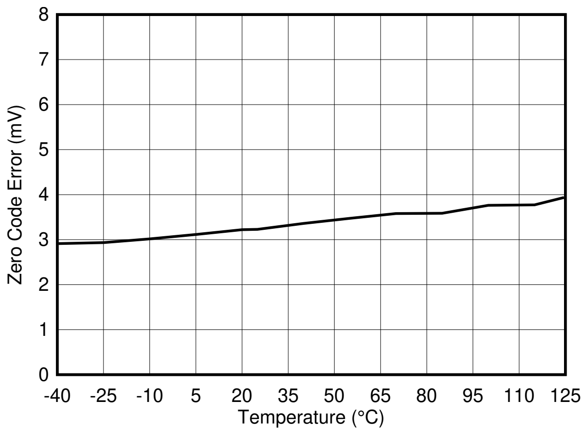


Figure 7-6. Total Unadjusted Error vs Temperature

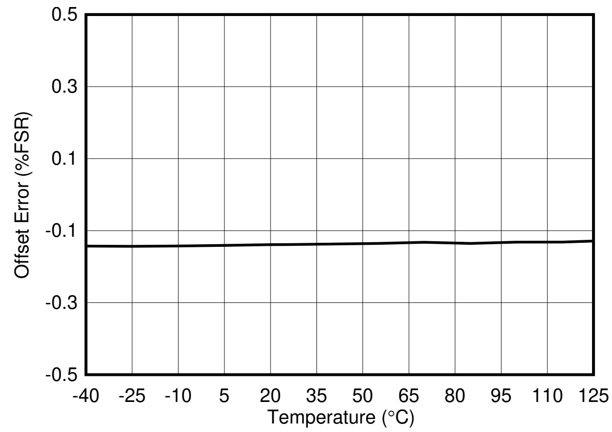
7.9 Typical Characteristics: V_{DD} = 1.8 V (Reference = V_{DD}) or V_{DD} = 2 V (Internal Reference) (continued)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)



Reference = V_{DD}

Figure 7-7. Zero Code Error vs Temperature



Reference = V_{DD}

Figure 7-8. Offset Error vs Temperature

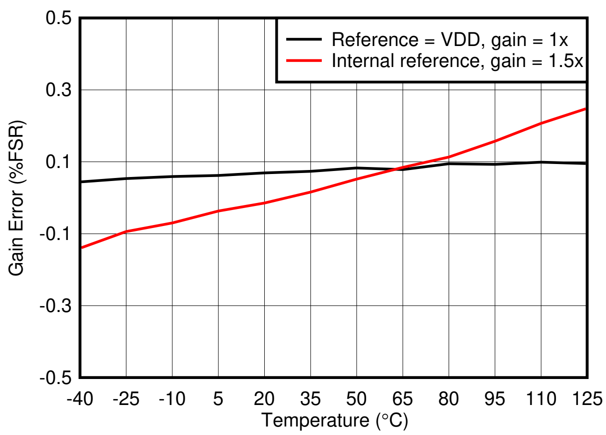


Figure 7-9. Gain Error vs Temperature

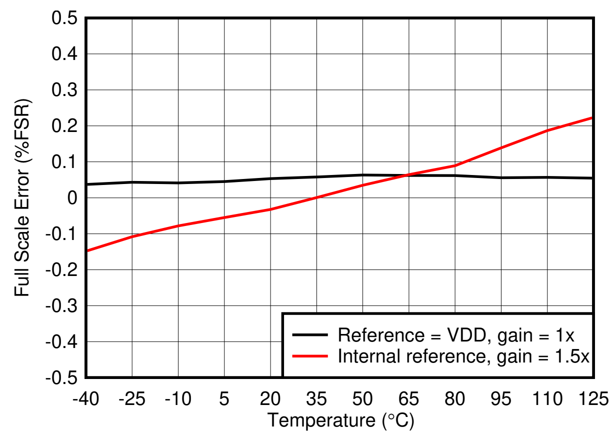


Figure 7-10. Full-Scale Error vs Temperature

7.10 Typical Characteristics: V_{DD} = 5.5 V (Reference = V_{DD}) or V_{DD} = 5 V (Internal Reference)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)

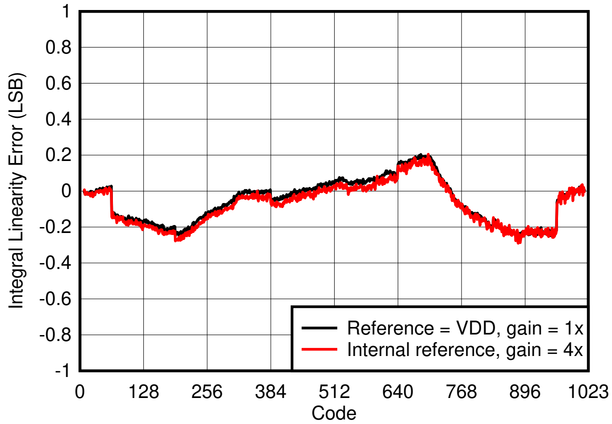


Figure 7-11. Integral Linearity Error vs Digital Input Code

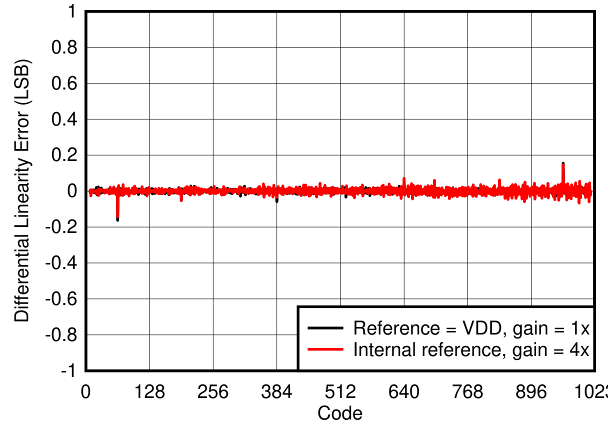


Figure 7-12. Differential Linearity Error vs Digital Input Code

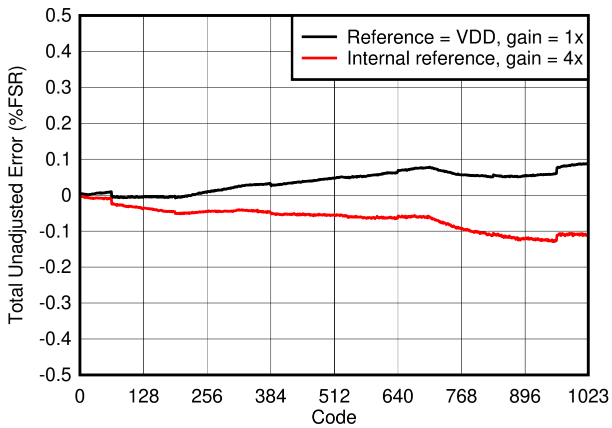


Figure 7-13. Total Unadjusted Error vs Digital Input Code

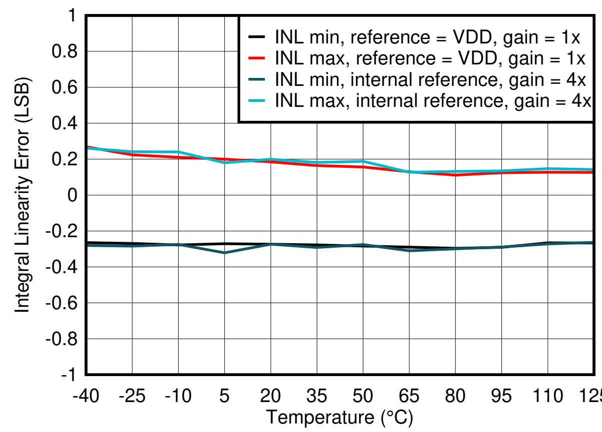


Figure 7-14. Integral Linearity Error vs Temperature

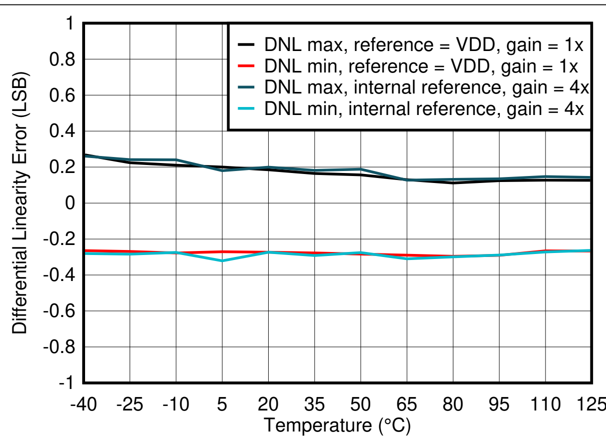


Figure 7-15. Differential Linearity Error vs Temperature

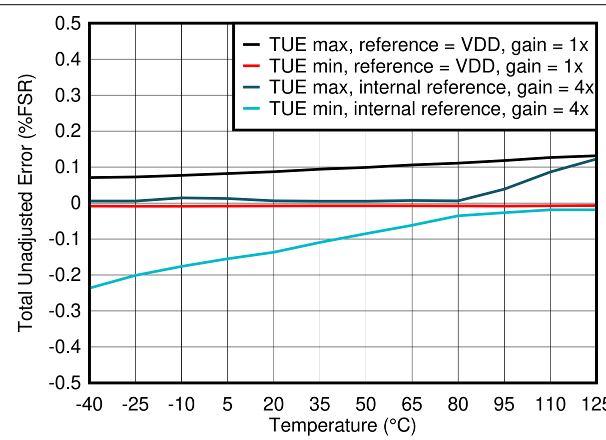
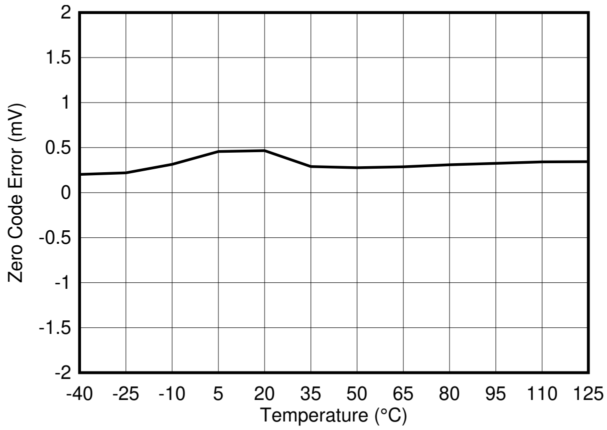


Figure 7-16. Total Unadjusted Error vs Temperature

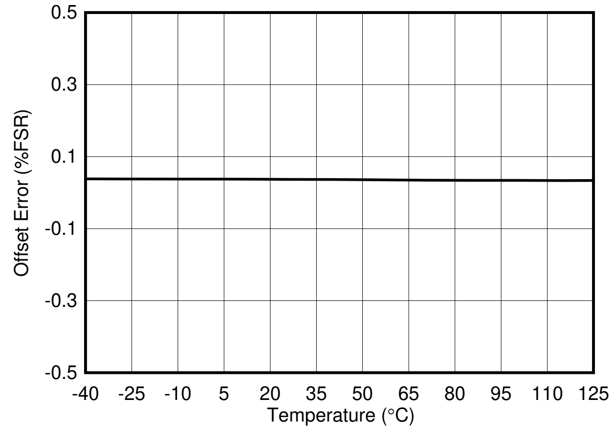
7.10 Typical Characteristics: V_{DD} = 5.5 V (Reference = V_{DD}) or V_{DD} = 5 V (Internal Reference) (continued)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)



Reference = V_{DD}

Figure 7-17. Zero Code Error vs Temperature



Reference = V_{DD}

Figure 7-18. Offset Error vs Temperature

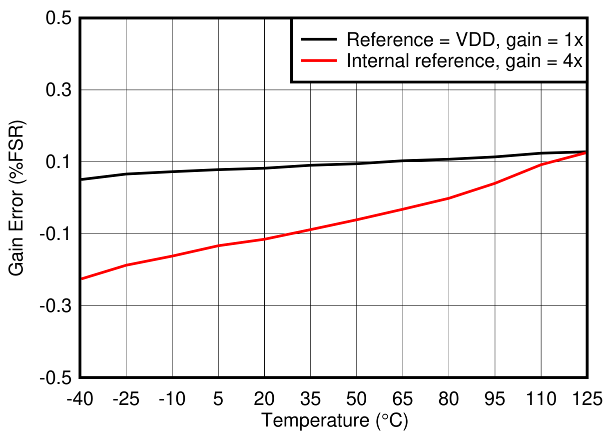


Figure 7-19. Gain Error vs Temperature

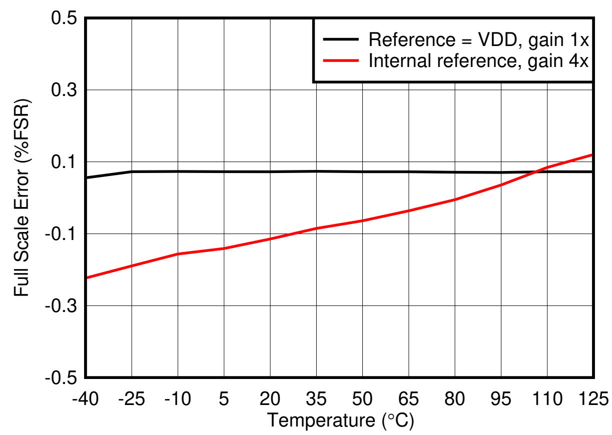
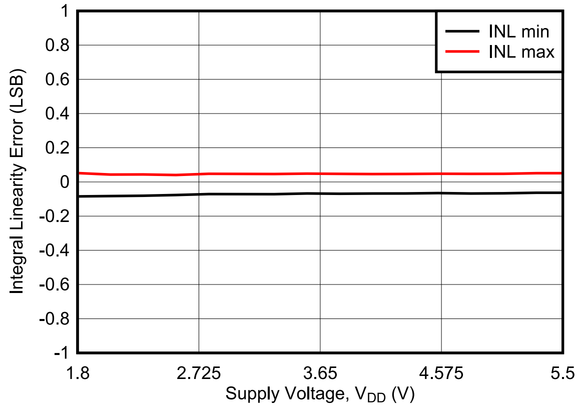


Figure 7-20. Full-Scale Error vs Temperature

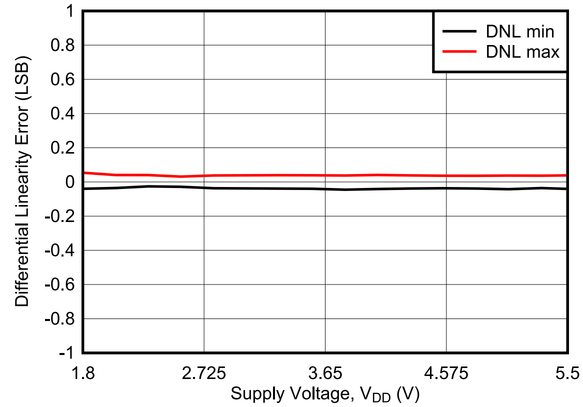
7.11 Typical Characteristics

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)



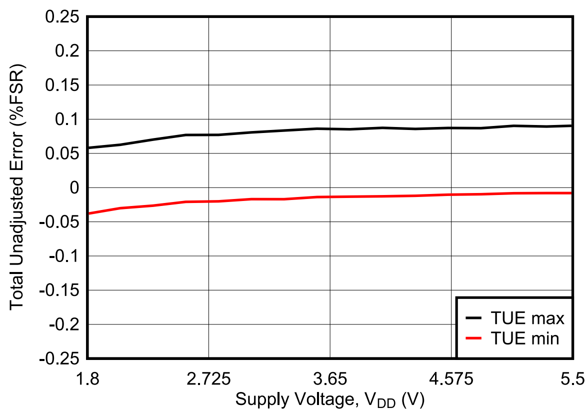
Reference = V_{DD}

Figure 7-21. Integral Linearity Error vs Supply Voltage



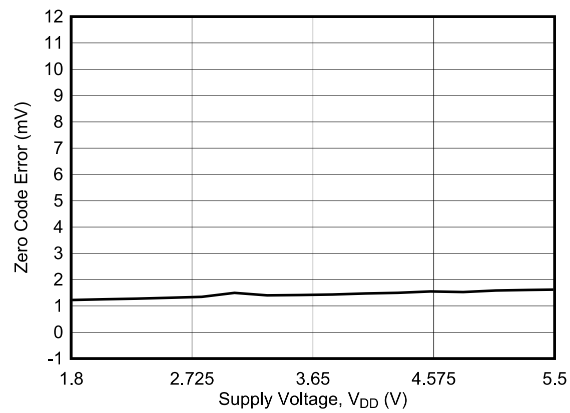
Reference = V_{DD}

Figure 7-22. Differential Linearity Error vs Supply Voltage



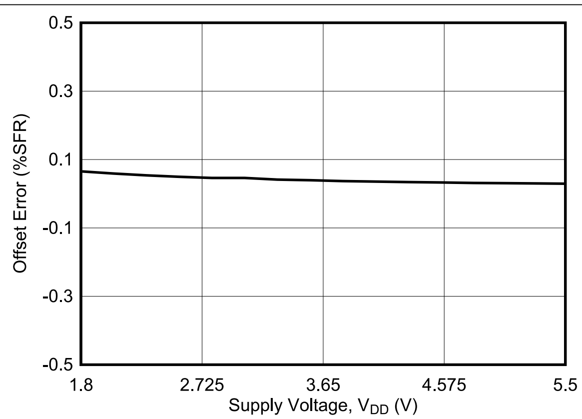
Reference = V_{DD}

Figure 7-23. Total Unadjusted Error vs Supply Voltage



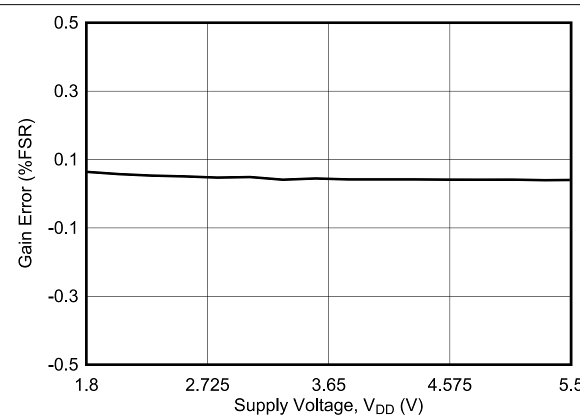
Reference = V_{DD}

Figure 7-24. Zero-Code Error vs Supply Voltage



Reference = V_{DD}

Figure 7-25. Offset Error vs Supply Voltage

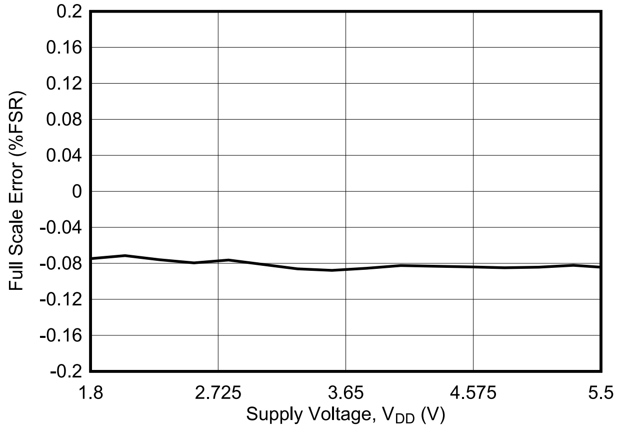


Reference = V_{DD}

Figure 7-26. Gain Error vs Supply Voltage

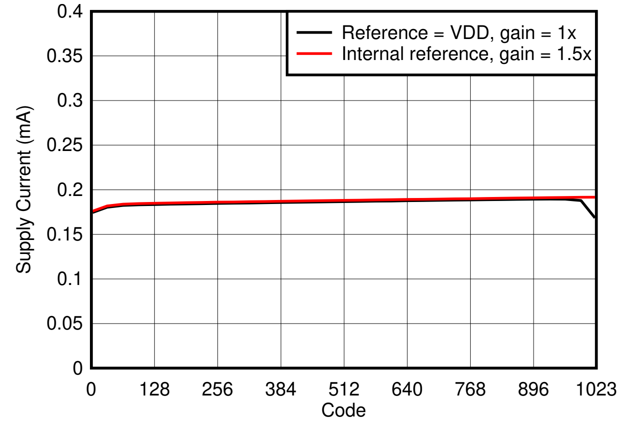
7.11 Typical Characteristics (continued)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)



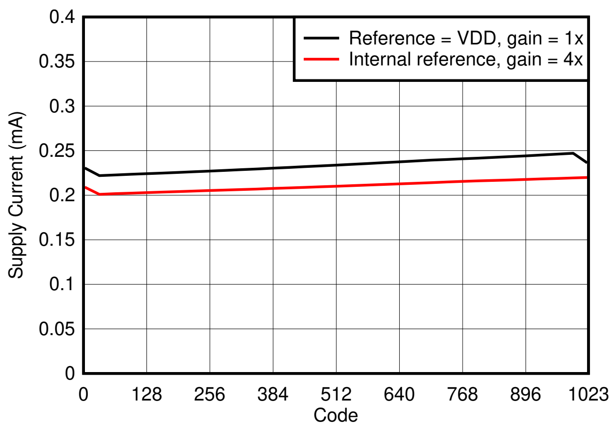
Reference = V_{DD}

Figure 7-27. Full-Scale Error vs Supply Voltage



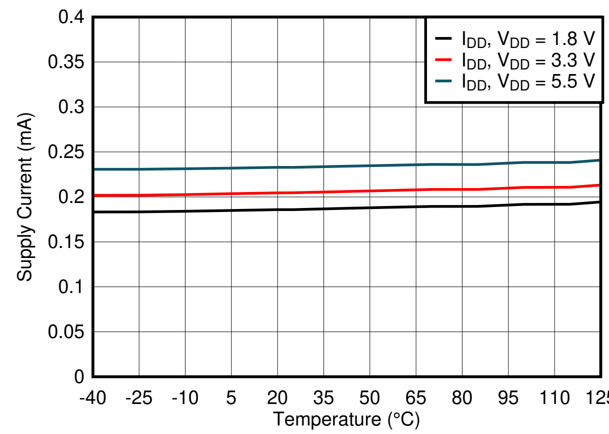
V_{DD} = 1.8 V

Figure 7-28. Supply Current vs Digital Input Code



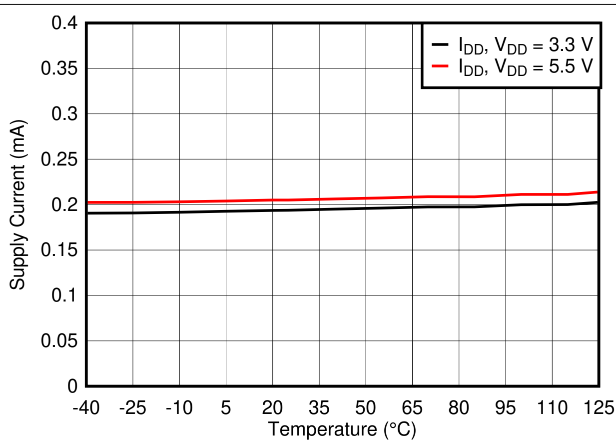
V_{DD} = 5.5 V

Figure 7-29. Supply Current vs Digital Input Code



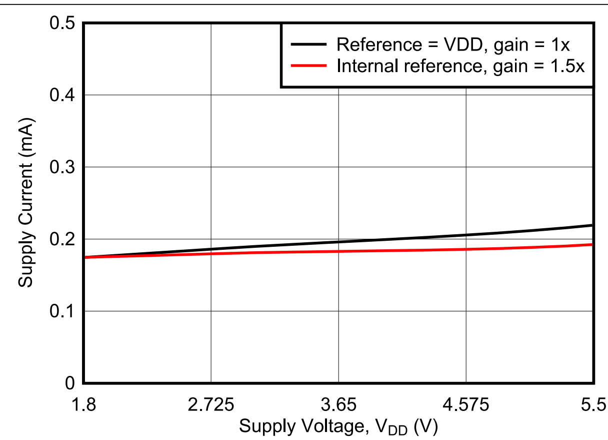
Reference = V_{DD}, DAC at midscale

Figure 7-30. Supply Current vs Temperature



Internal reference (gain = 4x), DAC at midscale

Figure 7-31. Supply Current vs Temperature

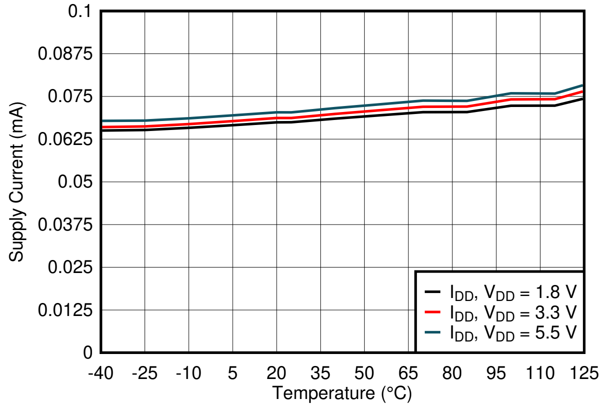


DAC at midscale

Figure 7-32. Supply Current vs Supply Voltage

7.11 Typical Characteristics (continued)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)



Reference = V_{DD}, DAC powered down

Figure 7-33. Power-Down Current vs Temperature

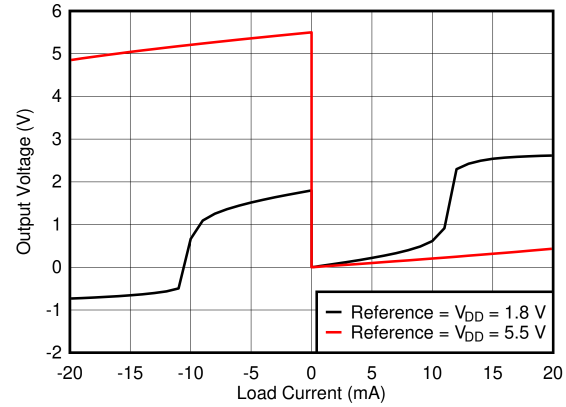
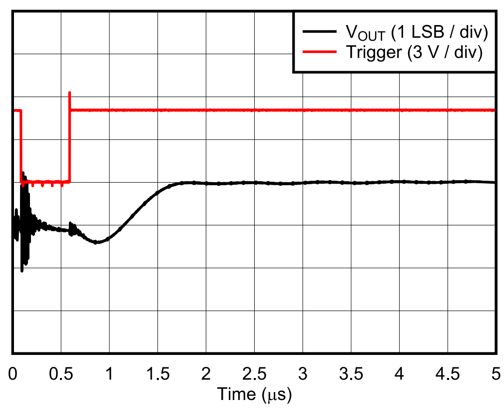
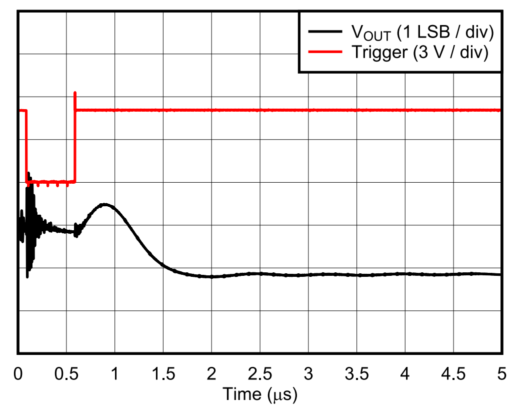


Figure 7-34. Source and Sink Capability



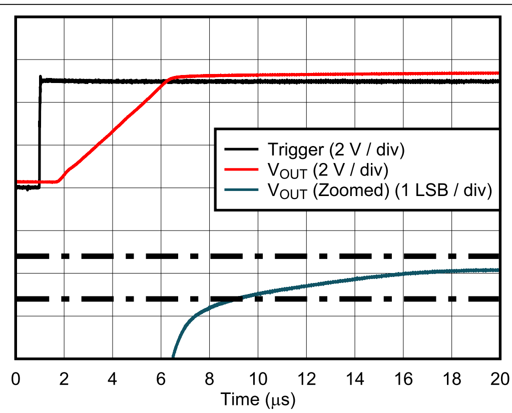
Reference = V_{DD} = 5.5 V, DAC code transition from midscale to midscale + 1 LSB, DAC load = 5kΩ || 200pF

Figure 7-35. Glitch Impulse, Rising Edge, 1-LSB Step



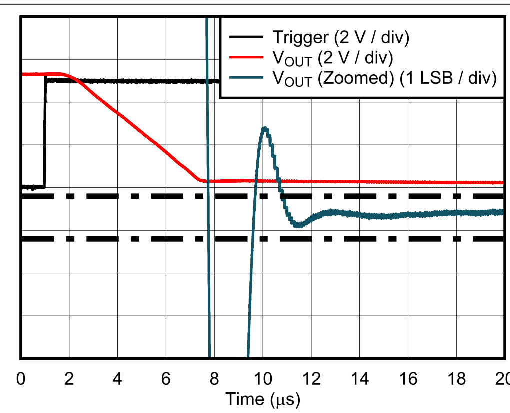
Reference = V_{DD} = 5.5 V, DAC code transition from midscale to midscale – 1 LSB, DAC load = 5kΩ || 200pF

Figure 7-36. Glitch Impulse, Falling Edge, 1-LSB Step



Reference = V_{DD} = 5.5 V, DAC load = 5kΩ || 200pF

Figure 7-37. Full-Scale Settling Time, Rising Edge

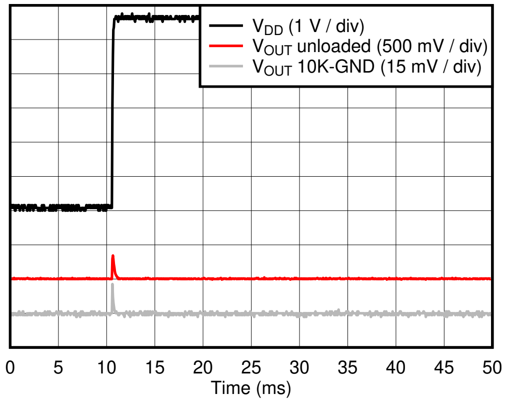


Reference = V_{DD} = 5.5 V, DAC load = 5kΩ || 200pF

Figure 7-38. Full-Scale Settling Time, Falling Edge

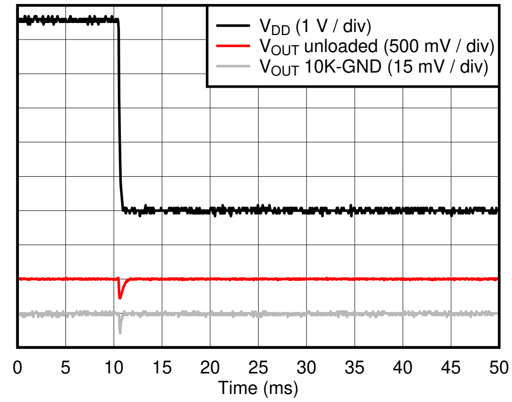
7.11 Typical Characteristics (continued)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)



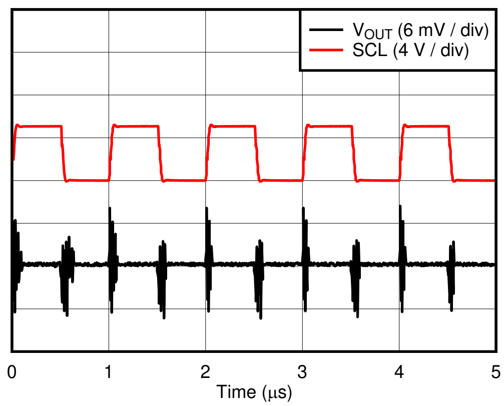
Reference = V_{DD} = 5.5 V

Figure 7-39. Power-on Glitch



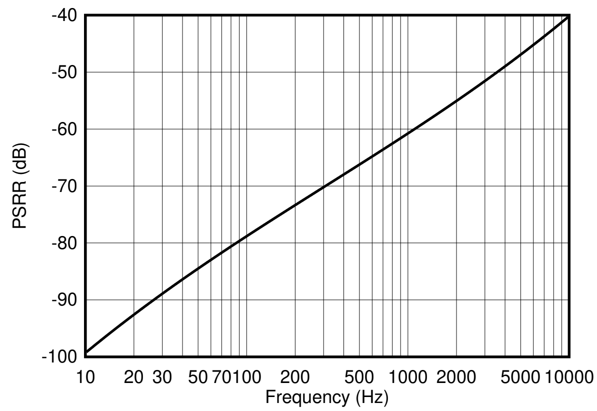
Reference = V_{DD} = 5.5 V

Figure 7-40. Power-off Glitch



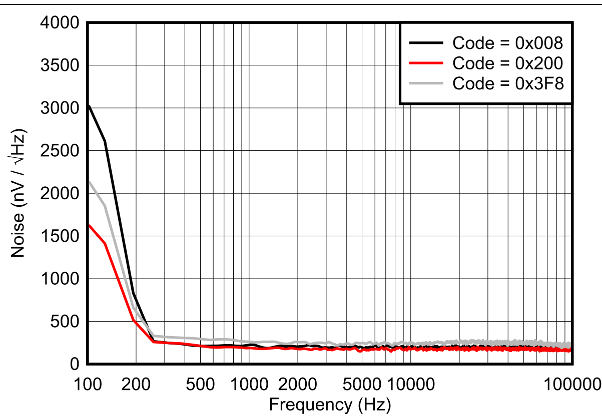
Reference = V_{DD} = 5.5 V, Fast+ mode, DAC at midscale, DAC load = 5kΩ || 200pF

Figure 7-41. Clock Feedthrough



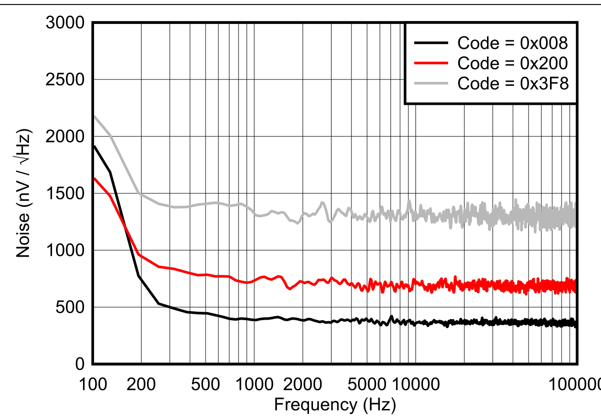
Internal reference (gain = 4x), V_{DD} = 5.25 V + 0.25 V_{PP}, DAC at midscale, DAC load = 5kΩ || 200pF

Figure 7-42. DAC Output AC PSRR vs Frequency



Reference = V_{DD} = 5.5 V

Figure 7-43. DAC Output Noise Spectral Density

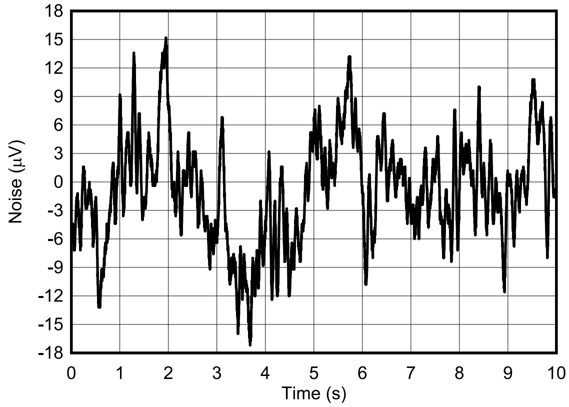


Internal reference (gain = 4x), V_{DD} = 5.5 V

Figure 7-44. DAC Output Noise Spectral Density

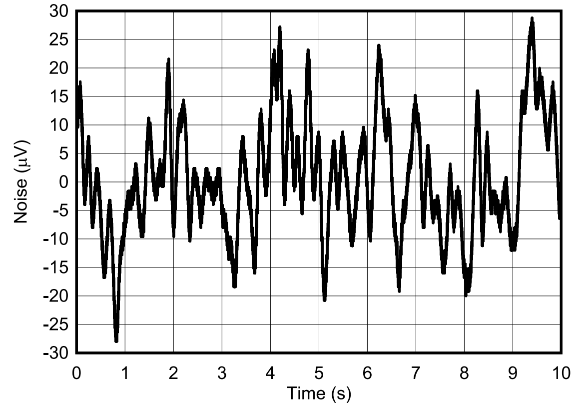
7.11 Typical Characteristics (continued)

at T_A = 25°C, 10-bit DAC, and DAC outputs unloaded (unless otherwise noted)



Reference = V_{DD} = 5.5 V, DAC at midscale

Figure 7-45. DAC Output Noise: 0.1 Hz to 10 Hz



Internal reference (gain = 4x), V_{DD} = 5.5 V, DAC at midscale

Figure 7-46. DAC Output Noise: 0.1 Hz to 10 Hz

8 Detailed Description

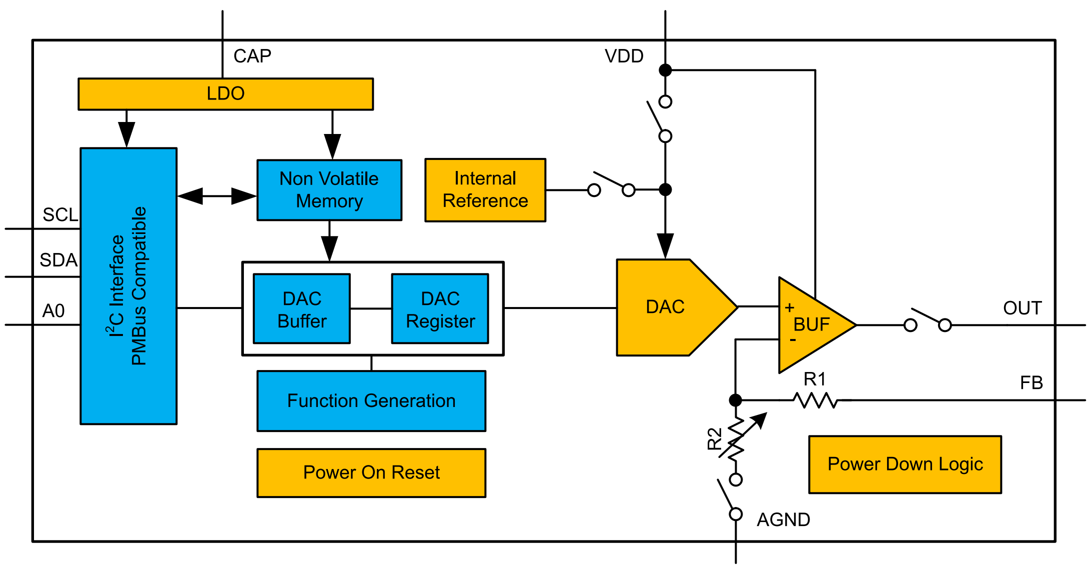
8.1 Overview

The 10-bit DAC53401-Q1 and 8-bit DAC43401-Q1 (DACx3401-Q1) are a pin-compatible family of automotive, buffered voltage-output, smart digital-to-analog converters (DACs). These smart DACs contain nonvolatile memory (NVM), an internal reference, a PMBus-compatible I^2C interface, and a force-sense output. The DACx3401-Q1 operate with either an internal reference or with a power supply as the reference, and provide a full-scale output of 1.8 V to 5.5 V.

The devices communicate through an I^2C interface and support I^2C standard mode (100 kbps), fast mode (400 kbps), and fast mode plus (1 Mbps). These devices also support specific PMBus commands such as *turn on/off*, *margin high or low*, and more. The DACx3401-Q1 also include digital slew rate control, and support basic signal generation such as *square*, *ramp*, and *sawtooth* waveforms. These devices can generate pulse-width modulation (PWM) output with the combination of the triangular or sawtooth waveform and the FB pin. These features enable DACx3401-Q1 to go beyond the limitations of a conventional DAC that depends on a processor to function. Because of processor-less operation and the smart feature set, the DACx3401-Q1 are called smart DACs.

The DACx3401-Q1 devices have a power-on-reset (POR) circuit that makes sure all the registers start with default or user-programmed settings using NVM. The DAC output powers on in high-impedance mode (default); this setting can be programmed to 10kΩ-GND using NVM.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Digital-to-Analog Converter (DAC) Architecture

The DACx3401-Q1 family of devices consists of string architecture with an output buffer amplifier. *Section 8.2* shows the DAC architecture within the block diagram. This DAC architecture operates from a 1.8-V to 5.5-V power supply. These devices consume only 0.2 mA of current when using a 1.8-V power supply. The DAC output pin starts up in high impedance mode making it an excellent choice for power-supply control applications. To change the power-up mode to 10kΩ-GND, program the DAC_PDN bit (address: D1h), and load these bits in the device NVM. The DACx3401-Q1 devices include a *smart* feature set to enable processor-less operation and high-integration. The NVM enables a predictable startup. The integrated functions and the FB pin enable PWM output for control applications. The FB pin enables this device to be used as a programmable comparator. The digital slew rate control and the Hi-Z power-down modes enable a hassle-free voltage margining and function.

8.3.1.1 Reference Selection and DAC Transfer Function

The device writes the input data to the DAC data registers in straight-binary format. After a power-on or a reset event, the device sets all DAC registers to the values set in the NVM.

8.3.1.1.1 Power Supply as Reference

By default, the DACx3401-Q1 operate with the power-supply pin (VDD) as a reference. Equation 1 shows DAC transfer function when the power-supply pin is used as reference.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{DD} \tag{1}$$

where

- N is the resolution in bits, either 8 (DAC43401-Q1) or 10 (DAC53401-Q1).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC register.
- DAC_DATA ranges from 0 to 2^N – 1.
- V_{DD} is used as the DAC reference voltage.

8.3.1.1.2 Internal Reference

The DACx3401-Q1 also contain an internal reference that is disabled by default. Enable the internal reference by writing 1 to REF_EN (address D1h). The internal reference generates a fixed 1.21-V voltage (typical). Using DAC_SPAN (address D1h) bits, gain of 1.5x, 2x, 3x, 4x can be achieved for the DAC output voltage (V_{OUT}) Equation 2 shows DAC transfer function when the internal reference is used.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \times GAIN \tag{2}$$

where

- N is the resolution in bits, either 8 (DAC43401-Q1) or 10 (DAC53401-Q1).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC register
- DAC_DATA ranges from 0 to 2^N – 1.
- V_{REF} is the internal reference voltage = 1.21 V.
- GAIN = 1.5x, 2x, 3x, 4x based on DAC_SPAN (address D1h) bits.

8.3.2 DAC Update

The DAC output pin (OUT) is updated at the end of I^2C DAC write frame.

8.3.2.1 DAC Update Busy

The DAC_UPDATE_BUSY bit (address D0h) is set to 1 by the device when certain DAC update operations, such as *function generation*, *transition to margin high or low*, or any of the medical alarms are in progress. When the DAC_UPDATE_BUSY bit is set to 1, do not write to any of the DAC registers. After the DAC update operation is completed (DAC_UPDATE_BUSY = 0), any of the DAC registers can be written.

8.3.3 Nonvolatile Memory (EEPROM or NVM)

The DACx3401-Q1 contain nonvolatile memory (NVM) bits. These memory bits are user programmable and erasable, and retain the set values in the absence of a power supply. All the register bits, as shown in Table 8-1, can be stored in the device NVM by setting NVM_PROG = 1 (address D3h). The NVM_BUSY bit (address D0h) is set to 1 by device when a NVM write or reload operation is ongoing. During this time, the device blocks all write operations to the device. The NVM_BUSY bit is set to 0 after the write or reload operation is complete; at this point, all write operations to the device are allowed. The default value for all the registers in the DACx3401-Q1 is loaded from NVM as soon as a POR event is issued. Do not perform a read operation from the DAC register while NVM_BUSY = 1.

Table 8-1. NVM Programmable Registers

REGISTER ADDRESS	REGISTER NAME	BIT ADDRESS	BIT NAME
D1h	GENERAL_CONFIG	15:14	FUNC_CONFIG
		13	DEVICE_LOCK
		11:9	CODE_STEP
		8:5	SLEW_RATE
		4:3	DAC_PDN
		2	REF_EN
		1:0	DAC_SPAN
D3h	TRIGGER	8	START_FUNC_GEN
10h	DAC_DATA	11:2	DAC_DATA
25h	DAC_MARGIN_HIGH	11:4	MARGIN_HIGH (8 most significant bits)
26h	DAC_MARGIN_LOW	11:4	MARGIN_LOW (8 most significant bits)

The DACx3401-Q1 also implement NVM_RELOAD bit (address D3h). Set this bit to 1 for the device to start an NVM reload operation. After the operation is complete, the device autoresets this bit to 0. During the NVM_RELOAD operation, the NVM_BUSY bit is set to 1.

8.3.3.1 NVM Cyclic Redundancy Check

The DACx3401-Q1 implement a cyclic redundancy check (CRC) feature for the device NVM to make sure that the data stored in the device NVM is uncorrupted. There are two types of CRC alarm bits implemented in DACx3401-Q1:

- NVM_CRC_ALARM_USER
- NVM_CRC_ALARM_INTERNAL

The NVM_CRC_ALARM_USER bit indicates the status of user-programmable NVM bits, and the NVM_CRC_ALARM_INTERNAL bit indicates the status of internal NVM bits The CRC feature is implemented by storing a 10-Bit CRC (CRC-10-ATM) along with the NVM data each time NVM program operation (write or reload) is performed and during the device start up. The device reads the NVM data and validates the data with the stored CRC. The CRC alarm bits (NVM_CRC_ALARM_USER and NVM_CRC_ALARM_INTERNAL address D0h) report any errors after the data are read from the device NVM.

8.3.3.2 NVM_CRC_ALARM_USER Bit

A logic 1 on NVM_CRC_ALARM_USER bit indicates that the user-programmable NVM data is corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and any DAC registers can be written to or read from. To reset the alarm bits to 0, issue a software reset (see *Section 8.3.6*) command, or cycle power to the DAC. Alternatively, cycle the power to reload the user-programmable NVM bits.

8.3.3.3 NVM_CRC_ALARM_INTERNAL Bit

A logic 1 on NVM_CRC_ALARM_INTERNAL bit indicates that the internal NVM data is corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and any DAC registers can be written to or read from. To reset the alarm bits to 0, issue a software reset (see *Section 8.3.6*) command or cycle power to the DAC.

8.3.4 Programmable Slew Rate

When the DAC data registers are written, the voltage on DAC output (V_{OUT}) immediately transitions to the new code following the slew rate and settling time specified in *Section 7.5*. The slew rate control feature allows the user to control the rate at which the output voltage (V_{OUT}) changes. When this feature is enabled (using SLEW_RATE[3:0] bits), the DAC output changes from the current code to the code in MARGIN_HIGH (address 25h) or MARGIN_LOW (address 26h) registers (when margin high or low commands are issued to the DAC) using the step and rate set in CODE_STEP and SLEW_RATE bits. With the default slew rate control setting (CODE_STEP and SLEW_RATE bits, address D1h), the output changes smoothly at a rate limited by the output drive circuitry and the attached load. Using this feature, the output steps digitally at a rate defined by bits CODE_STEP and SLEW_RATE on address D1h. SLEW_RATE defines the rate at which the digital slew updates; CODE_STEP defines the amount by which the output value changes at each update. Table 8-2 and Table 8-3 show different settings for CODE_STEP and SLEW_RATE.

When the slew rate control feature is used, the output changes happen at the programmed slew rate. This configuration results in a staircase formation at the output. Do not write to CODE_STEP, SLEW_RATE, or DAC_DATA during the output slew.

Table 8-2. Code Step

REGISTER ADDRESS AND NAME	CODE_STEP[2]	CODE_STEP[1]	CODE_STEP[0]	COMMENT
D1h, GENERAL_CONFIG	0	0	0	Code step size = 1 LSB (default)
	0	0	1	Code step size = 2 LSB
	0	1	0	Code step size = 3 LSB
	0	1	1	Code step size = 4 LSB
	1	0	0	Code step size = 6 LSB
	1	0	1	Code step size = 8 LSB
	1	1	0	Code step size = 16 LSB
	1	1	1	Code step size = 32 LSB

Table 8-3. Slew Rate

REGISTER ADDRESS AND NAME	SLEW_RATE[3]	SLEW_RATE[2]	SLEW_RATE[1]	SLEW_RATE[0]	COMMENT
D1h, GENERAL_CONFIG	0	0	0	0	25.6 µs (per step)
	0	0	0	1	25.6 µs × 1.25 (per step)
	0	0	1	0	25.6 µs × 1.50 (per step)
	0	0	1	1	25.6 µs × 1.75 (per step)
	0	1	0	0	204.8 µs (per step)
	0	1	0	1	204.8 µs × 1.25 (per step)
	0	1	1	0	204.8 µs × 1.50 (per step)
	0	1	1	1	204.8 µs × 1.75 (per step)
	1	0	0	0	1.6384 ms (per step)
	1	0	0	1	1.6384 ms × 1.25 (per step)
	1	0	1	0	1.6384 ms × 1.50 (per step)
	1	0	1	1	1.6384 ms × 1.75 (per step)
	1	1	0	0	12 µs (per step)
	1	1	0	1	8 µs (per step)
	1	1	1	0	4 µs (per step)
	1	1	1	1	No slew (default)

8.3.5 Power-on-Reset (POR)

The DACx3401-Q1 family of devices includes a power-on reset (POR) function that controls the output voltage at power up. After the V_{DD} supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a 30-ms, POR delay. The default value for all the registers in the DACx3401-Q1 is loaded from NVM as soon as the POR event is issued.

When the device powers up, a POR circuit sets the device to the default mode. The POR circuit requires specific V_{DD} levels, as indicated in Figure 8-1, in order to make sure that the internal capacitors discharge and reset the device on power up. To make sure that a POR occurs, V_{DD} must be less than 0.7 V for at least 1 ms. When V_{DD} drops to less than 1.65 V, but remains greater than 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, initiate a POR. When V_{DD} remains greater than 1.65 V, a POR does not occur.

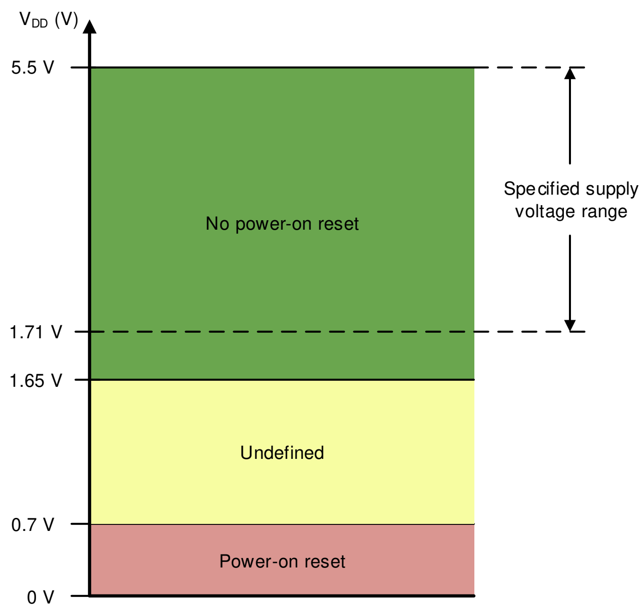


Figure 8-1. Threshold Levels for V_{DD} POR Circuit

8.3.6 Software Reset

To initiate a device software reset event, write the reserved code 1010 to the SW_RESET (address D3h). A software reset initiates a POR event.

8.3.7 Device Lock Feature

The DACx3401-Q1 implement a device lock feature that prevents an accidental or unintended write to the DAC registers. The device locks all the registers when the DEVICE_LOCK bit (address D1h) is set to 1. To bypass the DEVICE_LOCK setting, write 0101 to the DEVICE_UNLOCK_CODE bits (address D3h).

8.3.8 PMBus Compatibility

The PMBus protocol is an I^2C-based communication standard for power-supply management. PMBus contains standard command codes tailored to power supply applications. The DACx3401-Q1 implement some PMBus commands such as *Turn Off*, *Turn On*, *Margin Low*, *Margin High*, *Communication Failure Alert Bit (CML)*, as well as *PMBUS revision*. Figure 8-2 shows typical PMBus connections. The EN_PMBus bit (Bit 12, address D1h) must be set to 1 to enable the PMBus protocol.

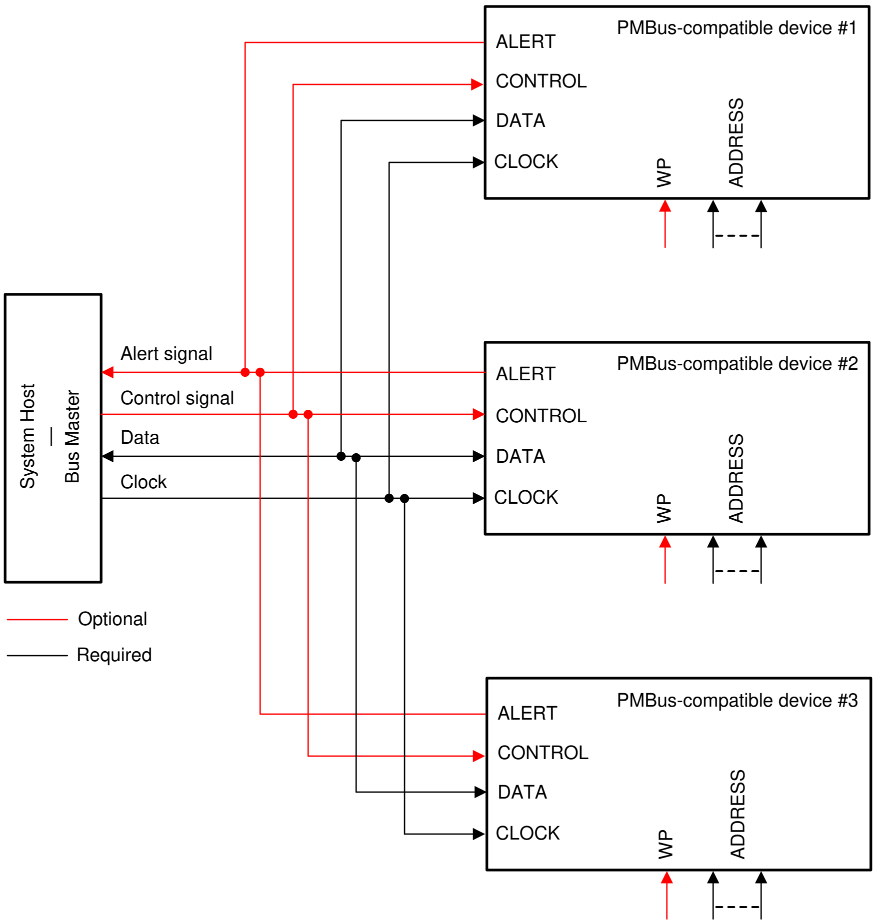


Figure 8-2. PMBus Connections

Similar to I^2C, PMBus is a variable length packet of 8-bit data bytes, each with a receiver acknowledge, wrapped between a start and stop bit. The first byte is always a 7-bit *slave address* followed by a *write* bit, sometimes called the *even address* that identifies the intended receiver of the packet. The second byte is an 8-bit *command* byte, identifying the PMBus command being transmitted using the respective command code. After the command byte, the transmitter either sends data associated with the command to write to the receiver command register (from most significant byte to least significant byte), or sends a new start bit indicating the desire to read the data associated with the command register from the receiver. After, the receiver transmits the data following the same most significant byte first format (see Table 8-7).

8.4 Device Functional Modes

8.4.1 Power Down Mode

The DACx3401-Q1 output amplifier and internal reference can be independently powered down through the DAC_PDN bits (address D1h). At power up, the DAC output and the internal reference are disabled by default. In power-down mode, the DAC output (OUT pin) is in a high-impedance state. To change this state to 10kΩ-A $_{GND}$ (at power up), use the DAC_PDN bits (address D1h).

The DAC power-up state can be programmed to any state (power-down or normal mode) using the NVM. Table 8-4 shows the DAC power-down bits.

Table 8-4. DAC Power-Down Bits

REGISTER ADDRESS AND NAME	DAC_PDN[1]	DAC_PDN[0]	DESCRIPTION
D1h, GENERAL_CONFIG	0	0	Power up
	0	1	Power down to 10 kΩ
	1	0	Power down to high impedance (Hi-Z) (default)
	1	1	Power down to 10 kΩ

8.4.2 Continuous Waveform Generation (CWG) Mode

The DACx3401-Q1 implement a continuous waveform generation feature. To set the device to this mode, set the START_FUNC_GEN (address D3h) to 1. In this mode, the DAC output pin (OUT) generates a continuous waveform based on the FUNC_CONFIG bits (address D1h). Table 8-5 shows the continuous waveforms that can be generated in this mode. The frequency of the waveform depends on the resistive and capacitive load on the OUT pin, high and low codes, and slew rate settings as shown in the following equations.

$$f_{SQUARE-WAVE} = \frac{1}{2 \times SLEW\_RATE} \tag{3}$$

$$f_{TRIANGLE-WAVE} = \frac{1}{2 \times SLEW\_RATE \times \left(\frac{MARGIN\_HIGH - MARGIN\_LOW + 1}{CODE\_STEP} \right)} \tag{4}$$

$$f_{SAWTOOTH-WAVE} = \frac{1}{SLEW\_RATE \times \left(\frac{MARGIN\_HIGH - MARGIN\_LOW + 1}{CODE\_STEP} \right)} \tag{5}$$

where:

- SLEW_RATE is the programmable DAC slew rate specified in Table 8-3.
- MARGIN_HIGH and MARGIN_LOW are the programmable DAC codes.
- CODE_STEP is the programmable DAC step code in Table 8-2.

Table 8-5. FUNC_CONFIG bits

REGISTER ADDRESS AND NAME	FUNC_CONFIG[1]	FUNC_CONFIG[0]	DESCRIPTION
D1h, GENERAL_CONFIG	0	0	Generates a triangle wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code with slope defined by SLEW_RATE (address D1h) bits
	0	1	Generates Saw-Tooth wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code, with rising slope defined by SLEW_RATE (address D1h) bits and immediate falling edge
	1	0	Generates Saw-Tooth wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code, with falling slope defined by SLEW_RATE (address D1h) bits and immediate rising edge
	1	1	Generates a square wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code with pulse high and low period defined by SLEW_RATE (address D1h) bits

8.4.3 PMBus Compatibility Mode

The DACx3401-Q1 I^2C interface implements some of the PMBus commands. Table 8-6 shows the supported PMBus commands that are implemented in DACx3401-Q1.The DAC uses MARGIN_LOW (address 26h), MARGIN_HIGH (address 25h) bits, SLEW_RATE, and CODE_STEP bits (address D1h) for PMBUS_OPERATION_CMD. The EN_PMBus bit (Bit 12, address D1h) must be set to 1 to enable the PMBus protocol.

Table 8-6. PMBus Operation Commands

REGISTER ADDRESS AND NAME	PMBUS_OPERATION_CMD[15:8]	DESCRIPTION
01h, PMBUS_OPERATION	00h	Turn off
	80h	Turn on
	94h	Margin low
	A4h	Margin high

The DACx3401-Q1 also implement PMBus features such as group command protocol and communication time-out failure. The CML bit (address 78h) indicates a communication fault in the PMBus. This bit is reset by writing 1. In case of timeout, if the SDA line is held low, the SDA line stays low during the time-out event until next SCL pulse is received.

To get the PMBus version, read the PMBUS_VERSION bits (address 98h).

8.5 Programming

The DACx3401-Q1 devices have a 2-wire serial interface (SCL and SDA), and one address pin (A0), as shown in the pin diagram of *Section 6*. The I^2C bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C-compatible devices connect to the I^2C bus through the open drain I/O pins, SDA and SCL.

The I^2C specification states that the device that controls communication is called a *master*, and the devices that are controlled by the master are called *slaves*. The master device generates the SCL signal. The master device also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the master. The master device on an I^2C bus is typically a microcontroller or digital signal processor (DSP). The DACx3401-Q1 family operates as a slave device on the I^2C bus. A slave device acknowledges master commands, and upon master control, receives or transmits data.

Typically, theDACx3401-Q1 family operates as a slave receiver. A master device writes to the DACx3401-Q1, a slave receiver. However, if a master device requires the DACx3401-Q1 internal register data, the DACx3401-Q1 operate as a slave transmitter. In this case, the master device reads from the DACx3401-Q1. According to I^2C terminology, read and write refer to the master device.

The DACx3401-Q1 family is a slave and supports the following data transfer modes:

- Standard mode (100 kbps)
- Fast mode (400 kbps)
- Fast mode plus (1.0 Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, both modes are referred to as *F/S-mode* in this document. The fast mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current would be 3 mA; similar to the case of standard and fast modes. The DACx3401-Q1 family supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device: start or repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the rising edge of the ACK bit, following the second byte.

Other than specific timing signals, the I^2C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. An acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. A not-acknowledge is when the SDA line is left high during the high period of the ninth clock cycle, as shown in Figure 8-3.

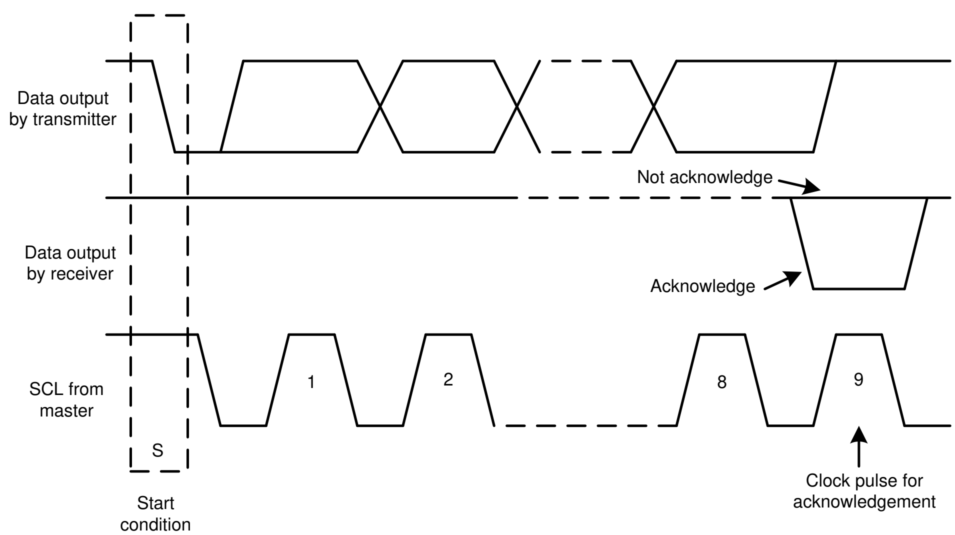


Figure 8-3. Acknowledge and Not Acknowledge on the I^2C Bus

8.5.1 F/S Mode Protocol

The following steps explain a complete transaction in F/S mode.

1. The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 8-4. All I^2C-compatible devices recognize a start condition.
2. The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/$\overline{W}$) on the SDA line. During all transmissions, the master makes sure that data are valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, as shown in Figure 8-5. All devices recognize the address sent by the master and compare the address to the respective internal fixed address. Only the slave device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the 9th SCL cycle, as shown in Figure 8-3. When the master detects this acknowledge, the communication link with a slave has been established.
3. The master generates further SCL cycles to transmit (R/$\overline{W}$ bit 0) or receive (R/$\overline{W}$ bit 1) data to the slave. In either case, the receiver must acknowledge the data sent by the transmitter. The acknowledge signal can be generated by the master or by the slave, depending on which is the receiver. The 9-bit valid data sequences consists of 8-data bits and 1 acknowledge-bit, and can continue as long as necessary.
4. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high, as shown in Figure 8-4. This action releases the bus and stops the communication link with the addressed slave. All I^2C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all slave devices then wait for a start condition followed by a matching address.

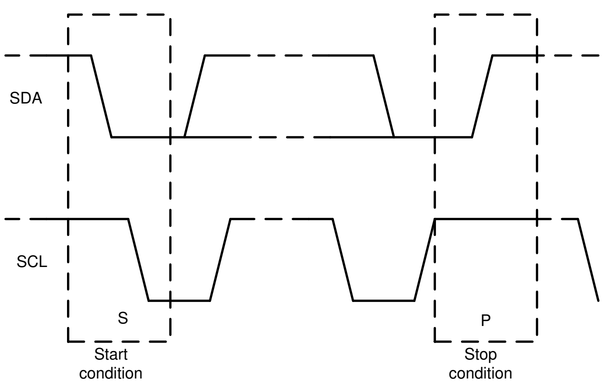


Figure 8-4. Start and Stop Conditions

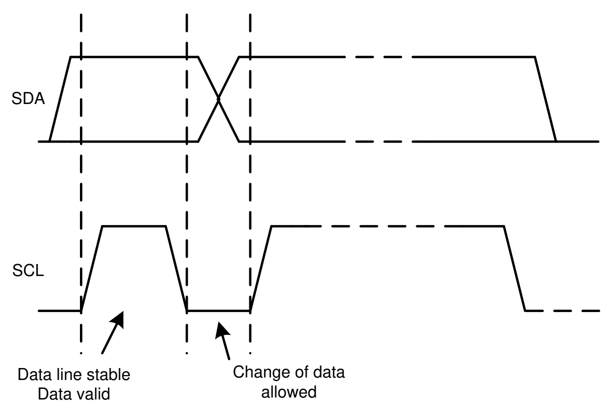


Figure 8-5. Bit Transfer on the I^2C Bus

8.5.2 I2C Update Sequence

For a single update, the DACx3401-Q1 require a start condition, a valid I2C address byte, a command byte, and two data bytes, as listed in Table 8-7.

Table 8-7. Update Sequence

MSB	....	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte Section 8.5.2.1				Command byte Section 8.5.2.2				Data byte - MSDB				Data byte - LSDB			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

After each byte is received, the DACx3401-Q1 family acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse, as shown in Figure 8-6. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I2C address byte selects the DACx3401-Q1 devices.

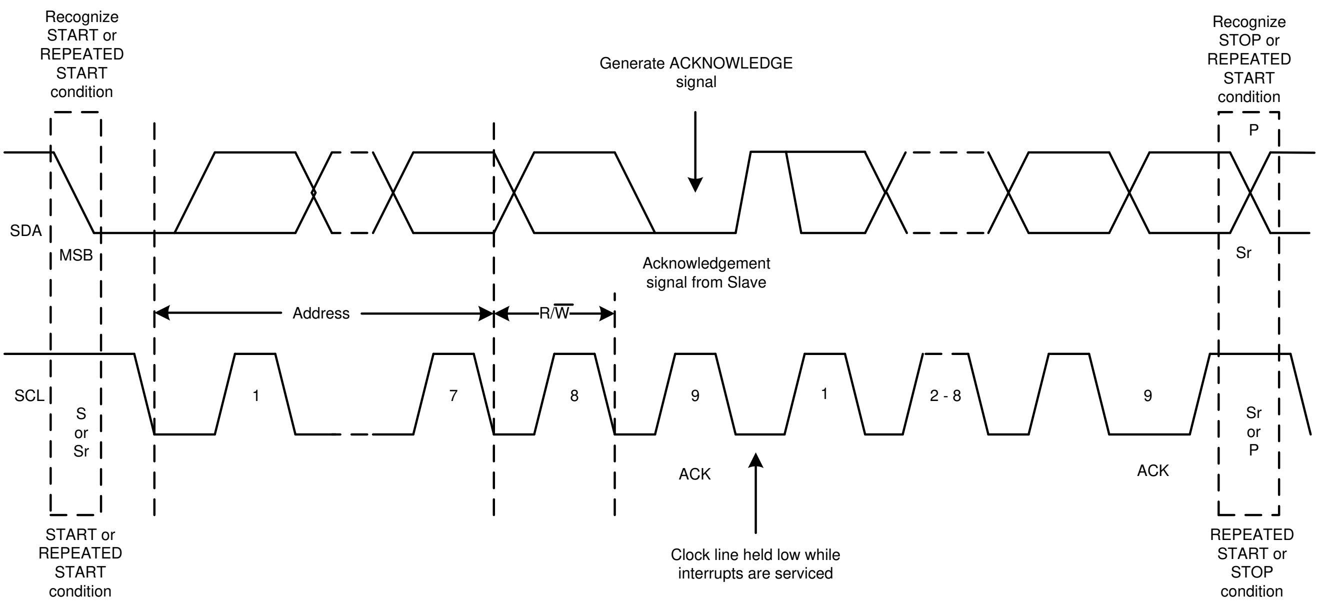


Figure 8-6. I2C Bus Protocol

The command byte sets the operating mode of the selected DACx3401-Q1 device. For a data update to occur when the operating mode is selected by this byte, the DACx3401-Q1 device must receive two data bytes: the most significant data byte (MSDB) and least significant data byte (LSDB). The DACx3401-Q1 device performs an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400 kHz), the maximum DAC update rate is limited to 10 kSPS. Using the fast mode plus (clock = 1 MHz), the maximum DAC update rate is limited to 25 kSPS. When a stop condition is received, the DACx3401-Q1 device releases the I2C bus and awaits a new start condition.

8.5.2.1 Address Byte

The address byte, as shown in Table 8-8, is the first byte received from the master device following the start condition. The first four bits (MSBs) of the address are factory preset to 1001. The next three bits of the address are controlled by the A0 pin. The A0 pin input can be connected to VDD, AGND, SCL, or SDA. The A0 pin is sampled during the first byte of each data frame to determine the address. The device latches the value of the address pin, and consequently responds to that particular address according to Table 8-9.

Table 8-8. Address Byte

COMMENT	MSB							LSB
—	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/ $\overline{W}$
General address	1	0	0	1	See Table 8-9 (slave address column)			0 or 1
Broadcast address	1	0	0	0	1	1	1	0

The DACx3401-Q1 supports broadcast addressing, which is used for synchronously updating or powering down multiple DACx3401-Q1 devices. When the broadcast address is used, the DACx3401-Q1 responds regardless of the address pin state. Broadcast is supported only in write mode.

Table 8-9. Address Format

SLAVE ADDRESS	A0 PIN
000	AGND
001	VDD
010	SDA
011	SCL

8.5.2.2 Command Byte

Table 8-10 lists the command byte.

Table 8-10. Command Byte (Register Names)

ADDRESS	REGISTER NAME
D0h	STATUS
D1h	GENERAL_CONFIG
D3h	TRIGGER
21h	DAC_DATA
25h	DAC_MARGIN_HIGH
26h	DAC_MARGIN_LOW
01h	PMBUS_OP
78h	PMBUS_STATUS_BYTE
98h	PMBUS_VERSION

8.5.3 I²C Read Sequence

To read any register the following command sequence must be used:

1. Send a start or repeated start command with a slave address and the $R/\overline{W}$ bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the slave address and the $R/\overline{W}$ bit set to 1 for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The master must acknowledge this byte.
5. Finally, the device writes out the LSDB of the register.

An alternative reading method allows for reading back the value of the last register written. The sequence is a start or repeated start with the slave address and the $R/\overline{W}$ bit set to 1, and the two bytes of the last register are read out.

The broadcast address cannot be used for reading.

Table 8-11. Read Sequence

S	MSB	…	$R/\overline{W}$ (0)	ACK	MSB	…	LSB	ACK	Sr	MSB	…	$R/\overline{W}$ (1)	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK
	ADDRESS BYTE Section 8.5.2.1				COMMAND BYTE Section 8.5.2.2				Sr	ADDRESS BYTE Section 8.5.2.1				MSDB				LSDB			
From Master				Slave	From Master			Slave	From Master				Slave	From Slave			Master	From Slave			Master

8.6 Register Map

Table 8-12. Register Map

<table>
<tr><th rowspan="2">ADDR</th><th colspan="8">MOST SIGNIFICANT DATA BYTE (MSDB)</th><th colspan="8">LEAST SIGNIFICANT DATA BYTE (LSDB)</th></tr>
<tr><th>BIT15</th><th>BIT14</th><th>BIT13</th><th>BIT12</th><th>BIT11</th><th>BIT10</th><th>BIT9</th><th>BIT8</th><th>BIT7</th><th>BIT6</th><th>BIT5</th><th>BIT4</th><th>BIT3</th><th>BIT2</th><th>BIT1</th><th>BIT0</th></tr>
<tr><td>D0h</td><td>NVM_ CRC_ ALARM_ USER</td><td>NVM_ CRC_ ALARM_ INTERNAL</td><td>NVM_ BUSY</td><td>DAC_ UPDATE_ BUSY</td><td colspan="6">X[(1)]</td><td colspan="4">DEVICE_ID</td><td colspan="2">VERSION_ID</td></tr>
<tr><td>D1h</td><td colspan="2">FUNC_CONFIG</td><td>DEVICE_ LOCK</td><td>EN_ PMBUS</td><td colspan="3">CODE_STEP</td><td colspan="4">SLEW_RATE</td><td colspan="2">DAC_PDN</td><td>REF_ EN</td><td colspan="2">DAC_SPAN</td></tr>
<tr><td>D3h</td><td colspan="4">DEVICE_UNLOCK_CODE</td><td colspan="2">X</td><td>DEVICE_ CONFIG_ RESET</td><td>START_ FUNC_ GEN</td><td>PMBUS_ MARGIN_ HIGH</td><td>PMBUS_ MARGIN_ LOW</td><td>NVM_ RELOAD</td><td>NVM_ PROG</td><td colspan="4">SW_RESET</td></tr>
<tr><td>21h</td><td colspan="4">X</td><td colspan="10">DAC_DATA[9:0] (10-Bit) or DAC_DATA[7:0] (8-Bit)</td><td colspan="2">X</td></tr>
<tr><td>25h</td><td colspan="4">X</td><td colspan="10">MARGIN_HIGH[9:0] (10-Bit) or MARGIN_HIGH[7:0] (8-Bit)</td><td colspan="2">X</td></tr>
<tr><td>26h</td><td colspan="4">X</td><td colspan="10">MARGIN_LOW[9:0] (10-Bit) or MARGIN_LOW[7:0] (8-Bit)</td><td colspan="2">X</td></tr>
<tr><td>01h</td><td colspan="8">PMBUS_OPERATION_CMD</td><td colspan="8">N/A</td></tr>
<tr><td>78h</td><td colspan="6">X</td><td>CML</td><td colspan="9">N/A</td></tr>
<tr><td>98h</td><td colspan="8">PMBUS_VERSION</td><td colspan="8">N/A</td></tr>
</table>

(1) X = Don't care.

Table 8-13. Register Names

ADDRESS	REGISTER NAME	SECTION
D0h	STATUS	Section 8.6.1
D1h	GENERAL_CONFIG	Section 8.6.2
D3h	TRIGGER	Section 8.6.3
21h	DAC_DATA	Section 8.6.4
25h	DAC_MARGIN_HIGH	Section 8.6.5
26h	DAC_MARGIN_LOW	Section 8.6.6
01h	PMBUS_OPERATION	Section 8.6.7
78h	PMBUS_STATUS_BYTE	Section 8.6.8
98h	PMBUS_VERSION	Section 8.6.9

Table 8-14. Access Type Codes

Access Type	Code	Description
X	X	Don't care
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1 STATUS Register (address = D0h) [reset = 000Ch or 0014h]

Figure 8-7. STATUS Register

15	14	13	12	11-6	5-2	1-0
NVM_CRC_ ALARM_ USER	NVM_CRC_ ALARM_ INTERNAL	NVM_ BUSY	DAC_ UPDATE_ BUSY	X	DEVICE_ID	VERSION_ID
R-0h	R-0h	R-0h	R-0h	X-00h	10-bit: R-0Ch 8-bit: R-14h	

Table 8-15. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NVM_CRC_ALARM_USER	R	0	0 : No CRC error in user NVM bits 1: CRC error in user NVM bits
14	NVM_CRC_ALARM_INTERNAL	R	0	0 : No CRC error in internal NVM 1: CRC error in internal NVM bits
13	NVM_BUSY	R	0	0 : NVM write or load completed,write to DAC registers allowed 1 : NVM write or load in progress, write to DAC registers not allowed
12	DAC_UPDATE_BUSY	R	0	0 : DAC outputs updated, write to DAC registers allowed 1 : DAC outputs update in progress, write to DAC registers not allowed
11 - 6	X	X	00h	Don't care
5 - 2	DEVICE_ID	R	DAC53401-Q1: 0Ch DAC43401-Q1: 14h	DAC53401-Q1: 0Ch DAC43401-Q1: 14h
1 - 0	VERSION_ID			

8.6.2 GENERAL_CONFIG Register (address = D1h) [reset = 01F0h]

Figure 8-8. GENERAL_CONFIG Register

15-14	13	12	11-9	8-5	4-3	2	1-0
FUNC_ CONFIG	DEVICE_ LOCK	EN_ PMBUS	CODE_STEP	SLEW_RATE	DAC_PDN	REF_EN	DAC_SPAN
R/ $\overline{W}$-0h	$\overline{W}$-0h	R/ $\overline{W}$-0h	R/ $\overline{W}$-0h	R/ $\overline{W}$-Fh	R/ $\overline{W}$-2h	R/ $\overline{W}$-0h	R/ $\overline{W}$-0h

Table 8-16. GENERAL_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	FUNC_CONFIG	R/ $\overline{W}$	00	00 : Generates a triangle wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code with slope defined by SLEW_RATE (address D1h) bits. 01: Generates Saw-Tooth wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code, with rising slope defined by SLEW_RATE (address D1h) bits and immediate falling edge. 10: Generates Saw-Tooth wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code, with falling slope defined by SLEW_RATE (address D1h) bits and immediate rising edge. 11: Generates a square wave between MARGIN_HIGH (address 25h) code to MARGIN_LOW (address 26h) code with pulse high and low period defined by SLEW_RATE (address D1h) bits.
13	DEVICE_LOCK	$\overline{W}$	0	0 : Device not locked 1: Device locked, the device locks all the registers. This bit can be reset (unlock device) by writing 0101 to the DEVICE_UNLOCK_CODE bits (address D3h)
12	EN_PMBUS	R/ $\overline{W}$	0	0: PMBus mode disabled 1: PMBus mode enabled

Table 8-16. GENERAL_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11 - 9	CODE_STEP	R/ $\overline{W}$	000	Code step for programmable slew rate control. 000: Code step size = 1 LSB (default) 001: Code step size = 2 LSB 010: Code step size = 3 LSB 011: Code step size = 4 LSB 100: Code step size = 6 LSB 101: Code step size = 8 LSB 110: Code step size = 16 LSB 111: Code step size = 32 LSB
8 - 5	SLEW_RATE	R/ $\overline{W}$	1111	Slew rate for programmable slew rate control. 0000: 25.6 µs (per step) 0001: 25.6 µs × 1.25 (per step) 0010: 25.6 µs × 1.50 (per step) 0011: 25.6 µs × 1.75 (per step) 0100: 204.8 µs (per step) 0101: 204.8 µs × 1.25 (per step) 0110: 204.8 µs × 1.50 (per step) 0111: 204.8 µs × 1.75 (per step) 1000: 1.6384 ms (per step) 1001: 1.6384 ms × 1.25 (per step) 1010: 1.6384 ms × 1.50 (per step) 1011: 1.6384 ms × 1.75 (per step) 1100: 12 µs (per step) 1101: 8 µs (per step) 1110: 4 µs (per step) 1111: No slew (default)
4 - 3	DAC_PDN	R/ $\overline{W}$	10	00: Power up 01: Power down to 10K 10: Power down to high impedance (default) 11: Power down to 10K
2	REF_EN	R/ $\overline{W}$	0	0: Internal reference disabled, V_{DD} is DAC reference voltage, DAC output range from 0 to V_{DD}. 1: Internal reference enabled, DAC reference = 1.21 V
1 - 0	DAC_SPAN	R/ $\overline{W}$	00	Only applicable when internal reference is enabled. 00: Reference to V_{OUT} gain 1.5X 01: Reference to V_{OUT} gain 2X 10: Reference to V_{OUT} gain 3X 11: Reference to V_{OUT} gain 4X

8.6.3 TRIGGER Register (address = D3h) [reset = 0008h]

Figure 8-9. TRIGGER Register

15 14 13 12	11 10	9	8	7	6	5	4	3 2 1 0
DEVICE_UNLOCK_CODE	X	DEVICE_ CONFIG_ RESET	START_ FUNC_ GEN	PMBUS_ MARGIN_ HIGH	PMBUS_ MARGIN_ LOW	NVM_ RELOAD	NVM_ PROG	SW_RESET
$\overline{W}$-0h	X	$\overline{W}$-0h	$\overline{W}$-0h	R/ $\overline{W}$-0h	R/ $\overline{W}$-0h	$\overline{W}$-0h	$\overline{W}$-0h	$\overline{W}$-8h

Table 8-17. TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	DEVICE_UNLOCK_CODE	$\overline{W}$	0000	Write 0101 to unlock the device to bypass DEVICE_LOCK bit.
11 - 10	X	X	0h	Don't care
9	DEVICE_CONFIG_RESET	$\overline{W}$	0	0: Device configuration reset not initiated 1: Device configuration reset initiated. All registers loaded with factory reset values.
8	START_FUNC_GEN	$\overline{W}$	0	0: Continuous waveform generation mode disabled 1: Continuous waveform generation mode enabled, device generates continuous waveform based on FUNC_CONFIG (D1h), MARGIN_LOW (address 18h), and SLEW_RATE (address D1h) bits.
7	PMBUS_MARGIN_HIGH	R/ $\overline{W}$	0	0: PMBus margin high command not initiated 1: PMBus margin high command initiated, DAC output margins high to MARGIN_HIGH code (address 25h). This bit automatically resets to 0 after the DAC code reaches MARGIN_HIGH value.
6	PMBUS_MARGIN_LOW	R/ $\overline{W}$	0	0: PMBus margin low command not initiated 1: PMBus margin low command initiated, DAC output margins low to MARGIN_LOW code (address 26h). This bit automatically resets to 0 after the DAC code reaches MARGIN_LOW value.
5	NVM_RELOAD	$\overline{W}$	0	0: NVM reload not initiated 1: NVM reload initiated, applicable DAC registers loaded with corresponding NVM. NVM_BUSY bit set to 1 while this operation is in progress. This bit is self-resetting.
4	NVM_PROG	$\overline{W}$	0	0: NVM write not initiated 1: NVM write initiated, NVM corresponding to applicable DAC registers loaded with existing register settings. NVM_BUSY bit set to 1 while this operation is in progress. This bit is self-resetting.
3 - 0	SW_RESET	$\overline{W}$	1000	1000: Software reset not initiated 1010: Software reset initiated, DAC registers loaded with corresponding NVMs, all other registers loaded with default settings.

8.6.4 DAC_DATA Register (address = 21h) [reset = 0000h]

Figure 8-10. DAC_DATA Register

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="4">X</td><td colspan="10">DAC_DATA[9:0] / DAC_DATA[7:0] – MSB Left aligned</td><td colspan="2">X</td></tr>
<tr><td colspan="4">X-0h</td><td colspan="10">$\overline{W}$-000h</td><td colspan="2">X-0h</td></tr>
</table>

Table 8-18. DAC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	X	X	0h	Don't care
11-2	DAC_DATA[9:0] / DAC_DATA[7:0]	$\overline{W}$	000h	Writing to the DAC_DATA register forces the respective DAC channel to update the active register data to the DAC_DATA. Data are in straight binary format and use the following format: DACx3401-Q1: { DATA[9:0] } DACx3401-Q1: { DATA[7:0], X, X } X = Don’t care bits
1-0	X	X	0h	Don't care

8.6.5 DAC_MARGIN_HIGH Register (address = 25h) [reset = 0000h]

Figure 8-11. DAC_MARGIN_HIGH Register

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="4">X</td><td colspan="10">MARGIN_HIGH[9:0] / MARGIN_HIGH[7:0] – MSB Left aligned</td><td colspan="2">X</td></tr>
<tr><td colspan="4">X-0h</td><td colspan="10">$\overline{W}$-000h</td><td colspan="2">X-0h</td></tr>
</table>

Table 8-19. DAC_MARGIN_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	X	X	0h	Don't care
11-2	MARGIN_HIGH[9:0] / MARGIN_HIGH[7:0] – MSB Left aligned	$\overline{W}$	000h	Margin high code for DAC output. Data are in straight binary format and use the following format: DACx3401-Q1: { MARGIN_HIGH[[9:0] } DACx3401-Q1: { MARGIN_HIGH[[7:0], X, X } X = Don’t care bits
1-0	X	X	0h	Don't care

8.6.6 DAC_MARGIN_LOW Register (address = 26h) [reset = 0000h]

Figure 8-12. DAC_MARGIN_LOW Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				MARGIN_LOW[9:0] / MARGIN_LOW[7:0] – MSB Left aligned										X	
X-0h				$\overline{W}$-000h										X-0h	

Table 8-20. DAC_MARGIN_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	X	X	0h	Don't care
11-2	MARGIN_LOW[9:0] / MARGIN_LOW[7:0] – MSB Left aligned	$\overline{W}$	000h	Margin low code for DAC output. Data are in straight binary format and follows the format below: DACx3401-Q1: { MARGIN_LOW[[9:0] } DACx3401-Q1: { MARGIN_LOW[[7:0], X, X } X = Don't care bits
1-0	X	X	0h	Don't care

8.6.7 PMBUS_OPERATION Register (address = 01h) [reset = 0000h]

Figure 8-13. PMBUS_OPERATION Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMBUS_OPERATION_CMD								X							
R/$\overline{W}$-00h								X-00h							

Table 8-21. PMBUS_OPERATION Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	PMBUS_OPERATION_CMD	R/$\overline{W}$	00h	PMBus operation commands 00h: Turn off 80h: Turn on A4h: Margin high, DAC output margins high to MARGIN_HIGH code (address 25h) 94h: Margin low, DAC output margins low to MARGIN_LOW code (address 26h)
7 - 0	X	X	00h	Not applicable

8.6.8 PMBUS_STATUS_BYTE Register (address = 78h) [reset = 0000h]

Figure 8-14. PMBUS_STATUS_BYTE Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X						CML	X								
X-00h						R/$\overline{W}$-0h	X-000h								

Table 8-22. PMBUS_STATUS_BYTE Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	X	X	00h	Don't care
9	CML	R/$\overline{W}$	0	0: No communication Fault 1: PMBus communication fault for timeout, write with incorrect number of clocks, read before write command, and so more; reset this bit by writing 1.
8 - 0	X	X	000h	Not applicable

8.6.9 PMBUS_VERSION Register (address = 98h) [reset = 2200h]

Figure 8-15. PMBUS_VERSION Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMBUS_VERSION								X							
R-22h								X-00h							

Table 8-23. PMBUS_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	PMBUS_VERSION	R	22h	PMBus version
7 - 0	X	X	00h	Not applicable

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DACx3401-Q1 are buffered, force-sense output, single-channel, DACs that include an NVM and internal reference and are available in a tiny 3 mm × 3 mm package. This device interfaces to a processor using I^2C. There are 4 I^2C addresses possible by configuring the A0 pin as shown in Table 7-5. The NVM allows processor-less operation of this device after programming at factory. The force-sense output can work with a transitor to create a programmable current sink that can bias LEDs. These digipots are designed for general-purpose applications in a wide range of end equipment. Some of the most common applications for these devices are power-supply margining and control, adaptive voltage scaling (AVS), *set-and-forget* LED biasing in automotive applications and mobile projectors, general-purpose function generation, and programmable comparator applications (such as standalone PWM control loops and offset and gain trimming in precision circuits).

9.2 Typical Applications

This section explains the design details of three primary applications of DACx3401-Q1: programmable LED biasing, and power-supply margining.

9.2.1 Programmable LED Biasing

LED and laser biasing or driving circuits often require accuracy and stability of the luminosity with respect to variation in temperature, electrical conditions, and physical characteristics. This accuracy and stability are most effectively achieved using a precision DAC, such as the DACx3401-Q1. The DACx3401-Q1 have additional features, such as the V_{FB} pin that compensates for the gate-to-source voltage of the transistor (V_{GS}) drop and the drift of the MOSFET. The NVM allows the microprocessor to *set-and-forget* the LED biasing value, even during a power cycle. Figure 9-1 shows the circuit diagram for LED biasing.

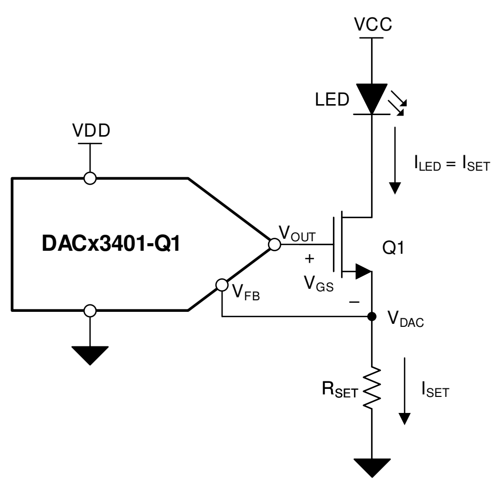


Figure 9-1. LED Biasing

9.2.1.1 Design Requirements

- DAC output range: 0 V to 2.4 V
- LED current range: 0 mA to 20 mA

9.2.1.2 Detailed Design Procedure

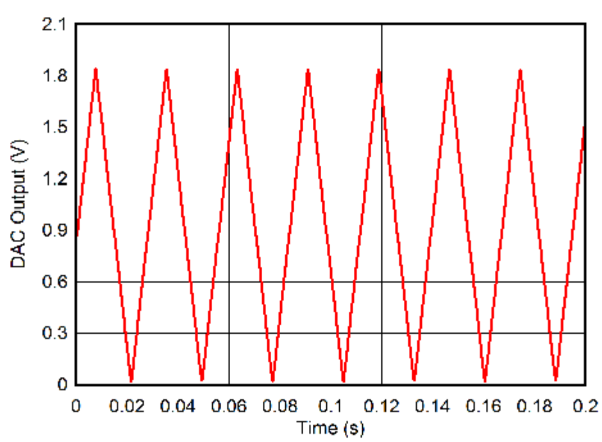
The DAC sets the source current of a MOSFET using the integrated buffer, as shown in Figure 9-1. Connect the LED between the power supply and the drain of the MOSFET. This configuration allows the DAC to control or set the amount of current through the LED. The integrated buffer controls the gate-source voltage of the MOSFET inside the feedback loop, thus compensating this drop and corresponding drift due to temperature, current, and ageing of the MOSFET. Calculate the value of the LED current set by the DAC using Equation 6. In order to generate 0 mA to 20 mA from a 0-V to 2.4-V DAC output range, the value of R_{SET} resistor is 120-Ω. Select the internal reference with a span of 2x. Given a V_{GS} of 1.2 V, the V_{DD} of the DAC must be at least 3.6 V. Select a V_{DD} of 5 V to allow variation of V_{GS} across temperature. When the V_{DD} headroom is a constraint, use a bipolar junction transistor (BJT) in place of the MOSFET. BJTs have much less V_{BE} drop as compared to a V_{GS} of a MOSFET. A MOSFET provides a much better match between the current through the set register and the LED current, as compared to a BJT.

$$I_{SET} = \frac{V_{DAC}}{R_{SET}} \tag{6}$$

The pseudocode for getting started with an LED biasing application is as follows:

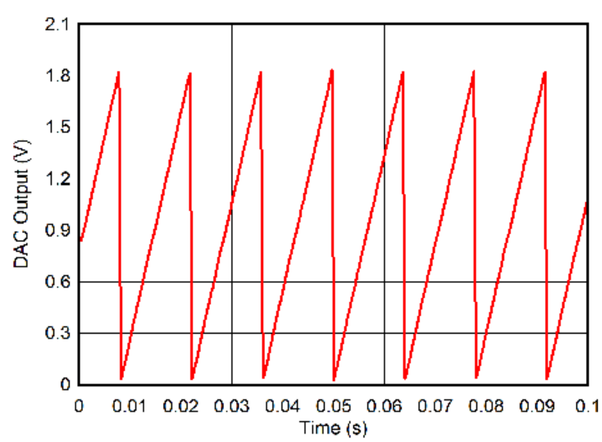
```
//SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
//Power-up the device, enable internal reference with 2x output span
WRITE GENERAL_CONFIG(0xD1), 0x11, 0xE5
//Write DAC code (12-bit aligned)
WRITE DAC_DATA(0x21), 0x07, 0xFC
//Write settings to the NVM
WRITE TRIGGER(0xD3), 0x00, 0x10
```

9.2.1.3 Application Curves



LED breathing effect in triangular pattern

Figure 9-2. Triangular Waveform



LED breathing effect in sawtooth pattern

Figure 9-3. Sawtooth Waveform

9.2.2 Power-Supply Margining

A power-supply margining circuit is used to test and trim the output of a power converter. This circuit is used to test a system by margining the power supplies, for adaptive voltage scaling, or to program a desired value at the output. Adjustable power supplies, such as LDOs and DC/DC converters, provide a feedback or adjust input that is used to set the desired output. A precision voltage-output DAC is an excellent choice to control the power-supply output linearly. Figure 9-4 shows a control circuit for a switch-mode power supply (SMPS) using the DACx3401-Q1. Typical applications include communications equipment, enterprise servers, test and measurement, automotive processor modules,and general-purpose power-supply modules.

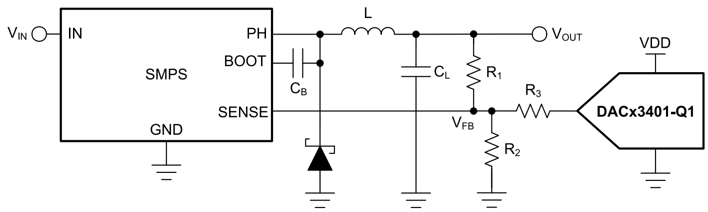


Figure 9-4. Power-Supply Margining

9.2.2.1 Design Requirements

- Power supply nominal output: 3.3 V
- Reference voltage of the converter (V_{FB}): 0.6 V
- Margin: ±10% (that is, 2.97 V to 3.63 V)
- DAC output range: 1.8 V
- Nominal current through R_1 and R_2: 100 μA

9.2.2.2 Detailed Design Procedure

The DACx3401-Q1 features a Hi-Z power-down mode that is set by default at power-up, unless the device is programmed otherwise using NVM. When the DAC output is at Hi-Z, the current through R_3 is zero and the SMPS is set at the nominal output voltage of 3.3 V. To have the same nominal condition when the DAC powers up, bring up the device at the same output as V_{FB} (that is, 0.6 V). This configuration makes sure there is no current through R_3 even at power-up. Calculate R_1 as (V_{OUT} – V_{FB}) / 100 μA = 27 kΩ.

To achieve ±10% margin-high and margin-low conditions, the DAC must sink or source additional current through R_1. Calculate the current from the DAC (I_{MARGIN}) using Equation 7 as 12 μA.

$$I_{MARGIN} = \left(\frac{V_{OUT} \times (1 + MARGIN) - V_{FB}}{R_1} \right) - I_{NOMINAL} \tag{7}$$

where:

- I_{MARGIN} is the margin current sourced or sinked from the DAC.
- MARGIN is the percentage margin value divided by 100.
- $I_{NOMINAL}$ is the nominal current through R_1 and R_2.

To calculate the value of R_3, first decide the DAC output range; for safe operation in the linear region, avoid the codes near zero-scale and full-scale. A DAC output of 20 mV is a safe consideration as the minimum output, and (1.8 V – 0.6 V – 20 mV = 1.18 V) as the maximum output. When the DAC output is at 20 mV, the power supply goes to margin high, and when the DAC output is at 1.18 V, the power supply goes to margin low. Calculate the value of R_3 using Equation 8 as 48.3 kΩ. Choose a standard resistor value and adjust the DAC outputs. Choosing R_3 = 47 kΩ gives the DAC margin high code as 1.164 V and the DAC margin low code as 36 mV.

$$R_3 = \frac{|V_{DAC} - V_{FB}|}{I_{MARGIN}} \tag{8}$$

The DACx3401-Q1 have a slew rate feature that is used to toggle between margin high, margin low, and nominal outputs with a defined slew rate. See Table 8-16 for the slew rate setting details.

Note

The MARGIN HIGH register value in DACx3401-Q1 results in the MARGIN LOW value at the power supply output. Similarly, the MARGIN LOW register value in DACx3401-Q1 results in the MARGIN HIGH value at the power-supply output.

The pseudocode for getting started with a power-supply control application is as follows:

```
//SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
//Write DAC code (12-bit aligned) for nominal output
//For a 1.8-V output range, the 10-bit hex code for 0.6 V is 0x0155. With 12-bit alignment, it
becomes 0x0554
WRITE DAC_DATA(0x21), 0x05, 0x54
//Write DAC code (12-bit aligned) for margin-low output at the power supply
//For a 1.8-V output range, the 10-bit hex code for 1.164 V is 0x0296. With 12-bit alignment, it
becomes 0x0A58
WRITE DAC_MARGIN_HIGH(0x25), 0x0A, 0x58
//Write DAC code (12-bit aligned) for margin-high output at the power supply
//For a 1.8-V output range, the 10-bit hex code for 36 mV is 0x14. With 12-bit alignment, it becomes
0x50
WRITE DAC_MARGIN_LOW(0x26), 0x00, 0x50
//Power-up the device with enable internal reference with 1.5x output span. This will output the
nominal voltage (0.6 V)
//CODE_STEP: 2 LSB, SLEW_RATE: 25.6 µs
WRITE GENERAL_CONFIG(0xD1), 0x12, 0x14
//Trigger margin-low output at the power supply
WRITE TRIGGER(0xD3), 0x00, 0x80
//Trigger margin-high output at the power supply
WRITE TRIGGER(0xD3), 0x00, 0x40
//Write back DAC code (12-bit aligned) for nominal output
WRITE DAC_DATA(0x21), 0x05, 0x54
```

9.2.2.3 Application Curves

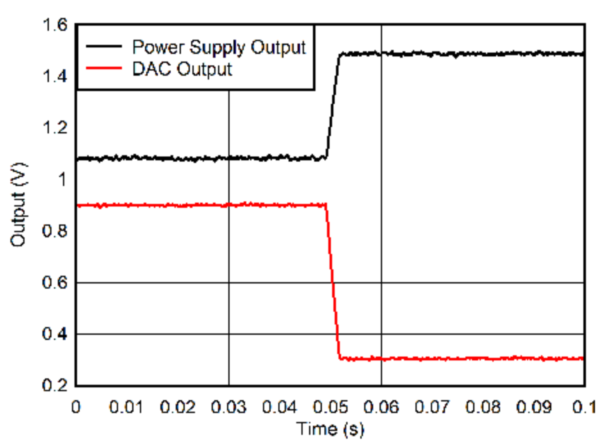


Figure 9-5. Power-Supply Margin High

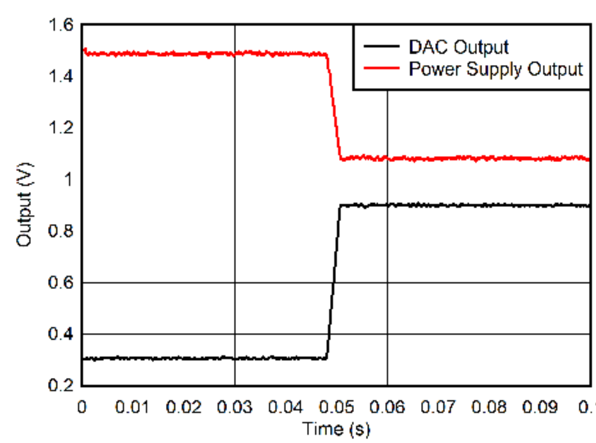


Figure 9-6. Power Supply Margin Low

10 Power Supply Recommendations

The DACx3401-Q1 family of devices does not require specific supply sequencing. These devices require a single power supply, V_{DD}. Use a 0.1-µF decoupling capacitor for the V_{DD} pin. Use a bypass capacitor with a value around 1.5-µF for the CAP pin.

11 Layout

11.1 Layout Guidelines

The DACx3401-Q1 pin configuration separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate the digital and analog traces, and place decoupling capacitors close to the device pins.

11.2 Layout Example

Figure 11-1 shows an example layout drawing with decoupling capacitors and pullup resistors.

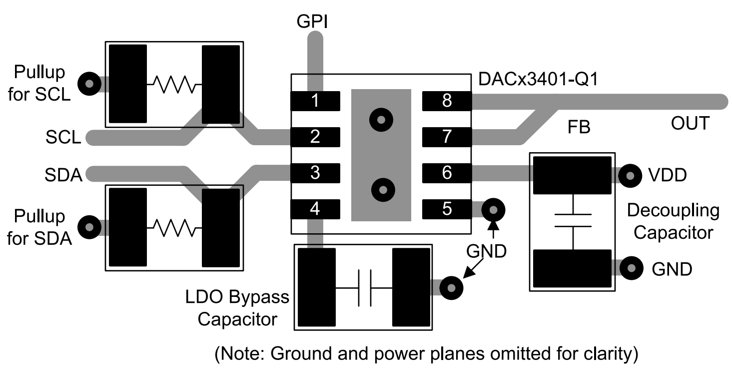


Figure 11-1. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Texas, Instruments *DAC53401EVM* user's guide

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

PMBus™ is a trademark of SMIF, Inc.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC43401DSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	44Q1
DAC43401DSGRQ1.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	44Q1
DAC43401DSGTQ1	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	44Q1
DAC43401DSGTQ1.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	44Q1
DAC53401DSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54Q1
DAC53401DSGRQ1.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54Q1
DAC53401DSGTQ1	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54Q1
DAC53401DSGTQ1.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DAC43401-Q1, DAC53401-Q1 :

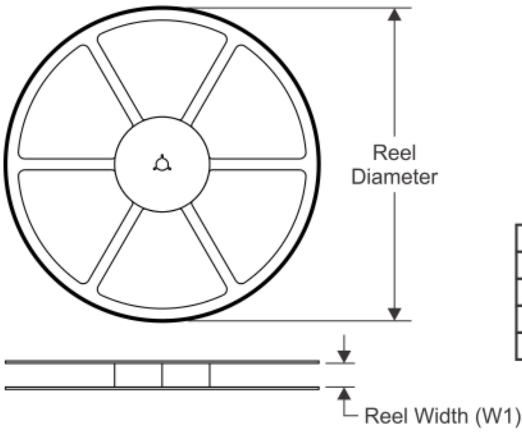
- Catalog : DAC43401, DAC53401

NOTE: Qualified Version Definitions:

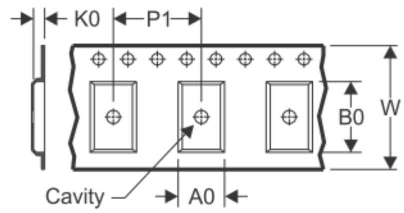
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

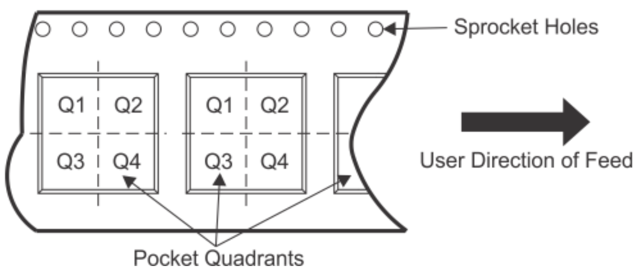


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

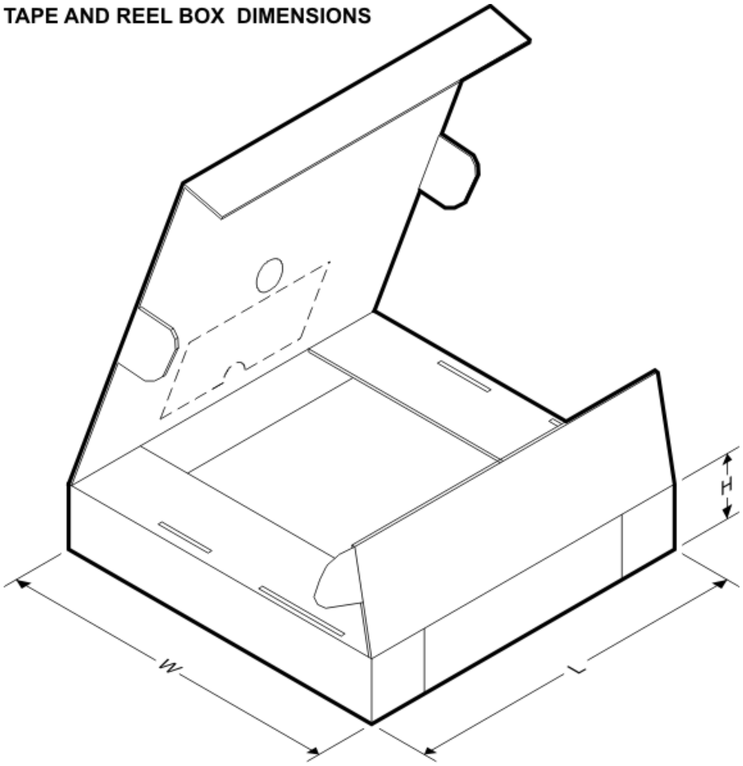
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC43401DSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DAC43401DSGTQ1	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DAC53401DSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DAC53401DSGTQ1	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

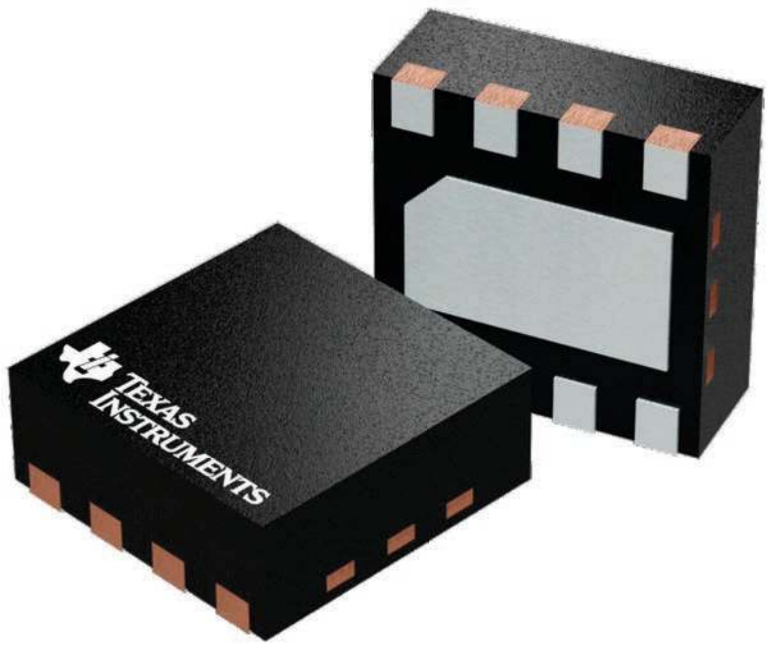
TAPE AND REEL BOX DIMENSIONS

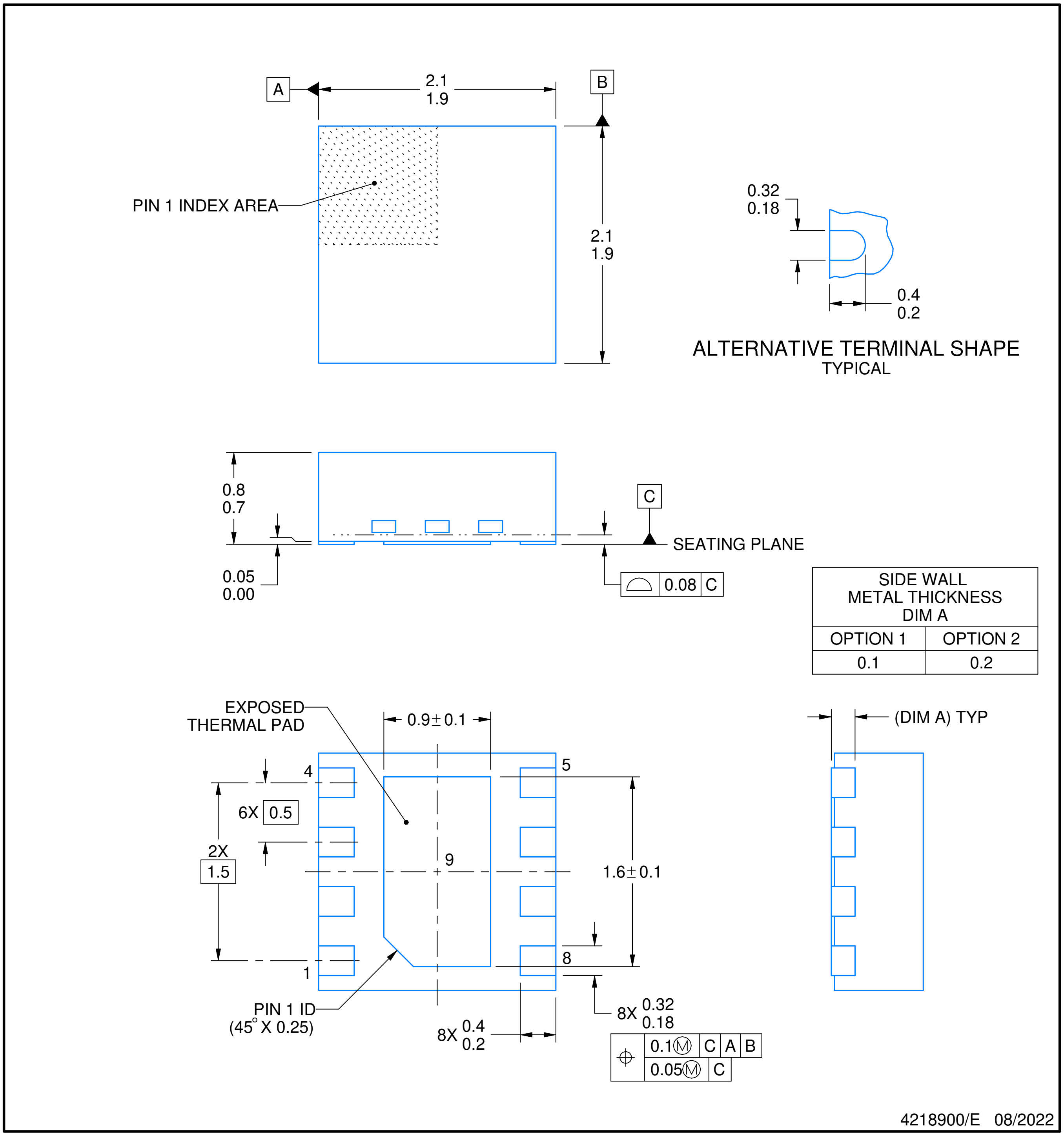


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC43401DSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
DAC43401DSGTQ1	WSON	DSG	8	250	210.0	185.0	35.0
DAC53401DSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
DAC53401DSGTQ1	WSON	DSG	8	250	210.0	185.0	35.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

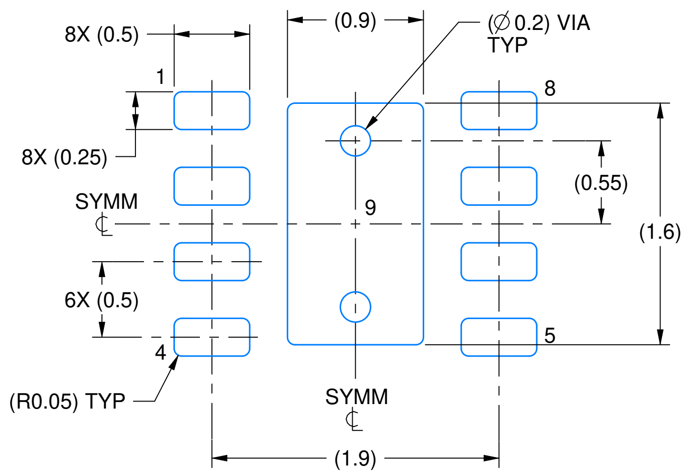




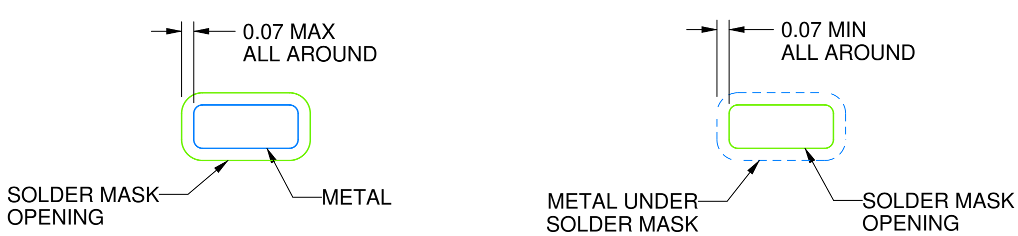
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

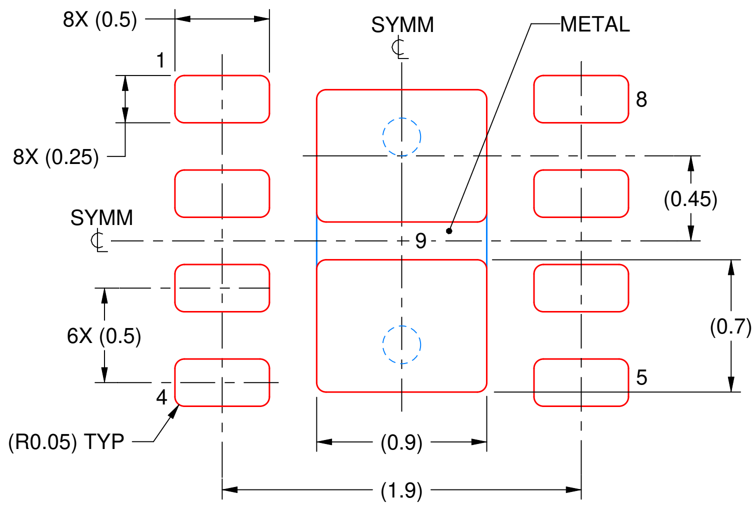
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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