

# ANTREX Electronics

Electronic Components Sourcing Information

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## Product Reference Information

**Part Number:** AM2632COKFHMZCZRQ1  
**Manufacturer:** Texas Instruments  
**Package:** 324-LFBGA  
**Availability:** Please confirm with sales

**Product Page:**

<https://antrexco.com/product/details/texas-instruments/am2632cokfhmzcqr1.html>

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**Note:**

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

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# AM263x Sitara™ Microcontrollers with Real-Time Control

## 1 Features

### Processor Cores:

- Single, dual, and quad-core Arm® Cortex®-R5F MCU with each core running up to 400MHz
  - 16KB I-cache with 64-bit ECC per CPU core
  - 16KB D-cache with 32-bit ECC per CPU core
  - 64KB Tightly-Coupled Memory (TCM) with 32-bit ECC per CPU core
  - Lockstep or Dual-core capable clusters

### Memory Subsystem:

- 2MB of On-Chip RAM (OCSRAM)
  - 4 Banks x 512KB
  - ECC error protection
  - Internal DMA engine support

### System on Chip (SoC) Services and Architecture:

- 1x EDMA to support data movement functions
- Device Boot supported from the following interfaces:
  - UART (Primary/Backup)
  - QSPI NOR Flash (4S/1S) (Primary)
- Interprocessor communication modules
  - SPINLOCK module for synchronizing processes running on multiple cores
  - MAILBOX functionality implemented through CTRLMMR registers
- Central Platform Time Sync (CPTS) support with time-sync and compare-event interrupt routers

### Media and Data Storage:

- 1x 4-bit Multi-Media Card/Secure Digital (MMC/SD) interface
- General-Purpose Memory Controller (GPMC)
  - 16-bit parallel data bus with 22-bit address bus
  - Up to 4MB addressable memory space
  - Integrated Error Location Module (ELM) support for error checking

### General Connectivity:

- 6x Universal Asynchronous RX-TX (UART)
- 5x Serial Peripheral Interface (SPI) controllers
- 5x Local Interconnect Network (LIN) ports
- 4x Inter-Integrated Circuit (I2C) ports
- 4x Modular Controller Area Network (MCAN) modules with CAN-FD support
- 1x Quad Serial Peripheral Interface (QSPI)
- 4x Fast Serial Interface Transmitters (FSITX)
- 4x Fast Serial Interface Receivers (FSIRX)
- Up to 139 General-Purpose I/O (GPIO) pins

### Sensing & Actuation:

- Real-time Control Subsystem (CONTROLSS)
- Flexible Input/Output Crossbars (XBAR)
- 5x 12-bit Analog-to-Digital Converters (ADC)
  - 6-input SAR ADC up to 4MSPS
    - 6x Single-ended channels **OR**
    - 3x Differential channels
  - Highly Configurable ADC Digital Logic
    - XBAR Start of Conversion Triggers (SOC)
    - User-defined Sample and Hold (S+H)
    - Flexible Post-Processing Blocks (PPB)
- 10x Analog Comparators with Type-A programmable DAC reference (CMPSSA)
- 10x Analog Comparators with Type-B programmable DAC reference (CMPSSB)
- 1x 12-bit Digital-to-Analog Converter (DAC)
- 32x Pulse Width Modulation (EPWM) modules
  - Single or Dual PWM channels
  - Advanced PWM Configurations
  - Extended HRPWM time resolution
- 10x Enhanced Capture (ECAP) modules
- 3x Enhanced Quadrature Encoder Pulse (EQEP) modules
- 2x 4-Ch Sigma-Delta Filter Modules (SDFM)
- Additional Signal-multiplex Crossbars (XBAR)

### Industrial Connectivity:

- Programmable Real-Time Unit (PRU-SS) and PRU-Industrial Communication Subsystem (PRU-ICSS)
  - Dual core Programmable Realtime Unit Subsystem (PRU0 / PRU1)
    - Deterministic Hardware
    - Dynamic Firmware
  - 20-channel enhanced input (eGPI) per PRU
  - 20-channel enhanced output (eGPO) per PRU
  - Embedded Peripherals and Memory
    - 1x UART, 1x ECAP
    - 1x MDIO, 1x IEP,
    - 1x 32KB Shared General Purpose RAM
    - 2x 8KB Shared Data RAM
    - 1x 16KB IRAM per PRU
    - ScratchPad (SPAD), MAC/CRC
  - Digital encoder and sigma-delta control loops
  - The PRU-ICSS enables advanced industrial protocols including:
    - EtherCAT®, Ethernet/IP™,
    - PROFINET®, IO-Link® for order
  - Dedicated Interrupt Controller (INTC)
  - Dynamic CONTROLSS XBAR Integration



## High-Speed Interfaces:

- Integrated Ethernet switch supporting two external ports
  - MII (10/100), RMII (10/100), or RGMII (10/100/1000)
  - IEEE 1588 (2008 Annex D, Annex E, Annex F) with 802.1AS PTP
  - Clause 45 MDIO PHY management
  - 512x ALE engine-based Packet Classifiers
  - Priority flow control with up to 2KB packet size
  - Four CPU hardware interrupt pacing
  - IP/UDP/TCP checksum offload in hardware

## Security:

- Hardware Security Module (HSM) with support for Auto SHE 1.1/EVITA
- Secure boot support
  - Device Take Over Protection
  - Hardware-enforced root-of-trust
  - Authenticated boot
  - SW Anti-rollback protection
- Debug security
  - Secure device debug only after proper authentication
  - Ability to disable device debug functionality
- Device ID and Key Management
  - Support for OTP Memory (FUSEROM)
    - Store root keys & other security fields
  - Separate EFUSE controllers and FUSE ROMs
  - Unique Public Device Identifiers (UIDs)
- Memory Protection Units (MPU)
  - Dedicated Arm® MPU per Cortex®-R5F core
  - System MPU - present at various interfaces in the SoC (MPU or Firewall)
  - 8-16 programmable regions
    - Enable/Privilege ID
    - Start/End Address
    - Read/Write/Cachable
    - Secure/Non-Secure
- Cryptographic Acceleration
  - Cryptographic cores with DMA Support
  - AES - 128/192/256-bit key sizes
  - SHA2 - 256/384/512-bit support
  - DRBG with pseudo and true random number generator
  - PKA (public key accelerator) to assist in RSA/ECC processing

## Functional Safety:

- Enables design of systems with functional safety requirements
  - Error Signaling Module (ESM) with designated SAFETY\_ERRORn pin
  - ECC or parity on calculation-critical memories
  - Built-In Self-Test (BIST) and fault-injection for CPU and on-chip RAM
  - Runtime internal diagnostic modules including voltage, temperature, and clock monitoring, windowed watchdog timers, CRC engines for memory integrity checks
- [Functional Safety-Compliant](#) [Industrial]
  - Developed for functional safety applications
  - Documentation to be made available to aid IEC 61508 functional safety system design
  - Systematic capability up to SIL-3
  - Hardware integrity up to SIL-3
  - Safety-related certification
    - [IEC 61508 certified up to SIL-3 by TUV SUD](#)
- [Functional Safety-Compliant](#) [Automotive]
  - Developed for functional safety applications
  - Documentation to be made available to aid ISO 26262 functional safety system design
  - Systematic capability up to ASIL-D
  - Hardware integrity up to ASIL-D
  - Safety-related certification
    - [ISO 26262 certified up to ASIL-D by TUV SUD](#)

## Technology / Package:

- AEC-Q100 qualified for automotive applications
- 45nm technology
- ZCZ Package
  - 324-pin NFBGA
  - 15.0mm x 15.0mm
  - 0.8mm pitch

## 2 Applications

- [Single & Multi Axis Servo Drives](#)
- [AC Inverter & VF Drives](#)
- [Solar Energy](#)
- [EV Charging](#)
- [Renewable Energy Storage](#)
- [Traction Inverters](#)
- [Onboard Chargers](#)
- [DC-DC Converters](#)
- [Battery Management Systems](#)
- [Combo Box Architectures](#)
- [IO Aggregators](#)
- [Domain Controllers](#)

### 3 Description

The AM263x Sitara™ Arm® Microcontrollers are built to meet the complex real-time processing needs of next generation industrial and automotive embedded products. The AM263x MCU family consists of multiple pin-to-pin compatible devices with up to four 400MHz Arm® Cortex®-R5F cores. As an option, the Arm® R5F subsystem can be programmed to run in lockstep or dual-core mode for a multiple functional safety configurations. The industrial communications subsystem (PRU-ICSS) enables integrated industrial Ethernet communication protocols such as PROFINET®, Ethernet/IP®, EtherCAT® (among many others), standard Ethernet connectivity, and even custom I/O interfaces. The family is designed for the future of motor control and digital power applications with advanced analog sensing and digital actuation modules.

The multiple R5F cores are arranged in cluster subsystems with 256KB of shared tightly coupled memory (TCM) along with 2MB of shared SRAM, greatly reducing the need for external memory. Extensive ECC is included for on-chip memories, peripherals, and interconnects for enhanced reliability. Granular firewalls managed by the Hardware Security Manager (HSM) enable developers to implement stringent security-minded system design requirements. Cryptographic acceleration and secure boot are also available on AM263x devices.

TI provides a complete set of microcontroller software and development tools for the AM263x family of microcontrollers.

#### Package Information

| PART NUMBER <sup>(1) (2)</sup> | PACKAGE            | PACKAGE SIZE <sup>(3)</sup> |
|--------------------------------|--------------------|-----------------------------|
| AM2634...ZCZ                   | ZCZ (nFBGA, 324)   | 15.0mm × 15.0mm             |
| AM2632...ZCZ                   | ZCZ (nFBGA, 324)   | 15.0mm × 15.0mm             |
| AM2631...ZCZ                   | ZCZ (nFBGA, 324)   | 15.0mm × 15.0mm             |
| AM2634...ZCZQ1                 | ZCZQ1 (nFBGA, 324) | 15.0mm × 15.0mm             |
| AM2632...ZCZQ1                 | ZCZQ1 (nFBGA, 324) | 15.0mm × 15.0mm             |
| AM2631...ZCZQ1                 | ZCZQ1 (nFBGA, 324) | 15.0mm × 15.0mm             |

(1) For more information, see [Section 11](#).

(2) All devices are available in both tray or tape and reel packaging.

(3) The Package size (length x width) is a nominal value and includes pins, where applicable.

### 3.1 Functional Block Diagram

Figure 3-1 is the functional block diagram for the device.

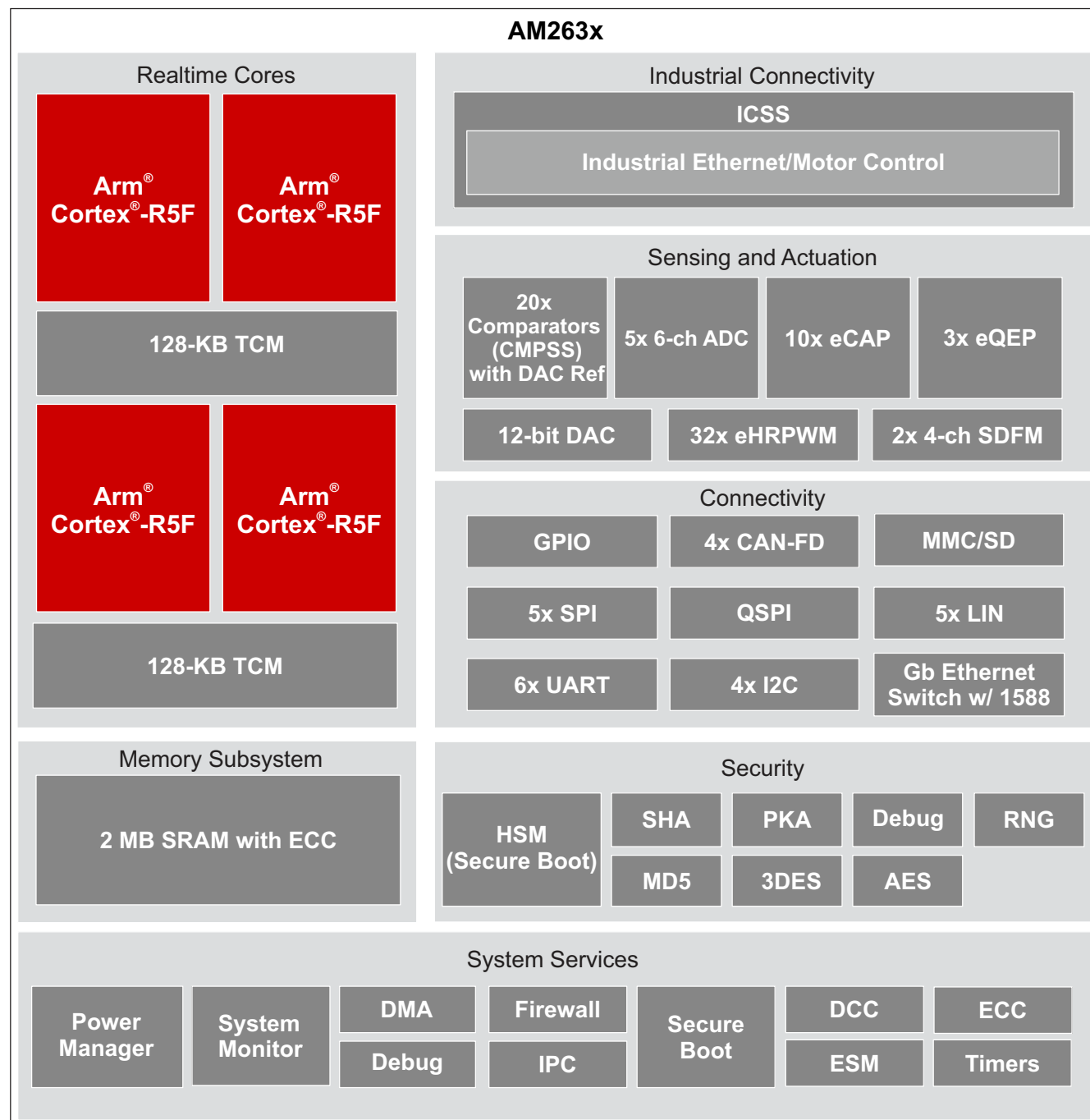


Figure 3-1. Functional Block Diagram

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## 4 Device Comparison

Table 4-1 shows a comparison between devices, highlighting the differences.

**Table 4-1. Device Comparison**

| FEATURES                                                  | REFERENCE NAME       | AM2634 <sup>(1)</sup>                                                             | AM2632 <sup>(1)</sup>                                                             | AM2631                         |
|-----------------------------------------------------------|----------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|--------------------------------|
| JTAG Device ID Comparison (Features)                      |                      |                                                                                   |                                                                                   |                                |
| JTAG Device ID <sup>(2)</sup>                             | Industrial:          | M: 0x4111BBE6<br>L: 0x41119BE6<br>K: 0x41117BE6<br>E: 0x4110BBE6<br>D: 0x41109BE6 | M: 0x4109BBE6<br>L: 0x41099BE6<br>K: 0x41097BE6<br>E: 0x4108BBA6<br>D: 0x41089BA6 | E: 0x4104B3A6<br>D: 0x410493A6 |
|                                                           | Extended Automotive: | K: 0x41117BFE<br>D: 0x41109BFE (Grade O)<br>D: 0x41109C3E (Grade P)               | K: 0x41097BFE<br>D: 0x41089BFE (Grade O)<br>D: 0x41089C3E (Grade P)               | D: 0x410493BE                  |
| Processors and Accelerators                               |                      |                                                                                   |                                                                                   |                                |
| Speed Grade                                               |                      | See <a href="#">Section 6.6, Operating Performance Points</a>                     |                                                                                   |                                |
| Arm® Cortex-R5F                                           | R5FSS                | 4                                                                                 | 2                                                                                 | 1                              |
| Hardware Security Module                                  | HSM                  | Yes                                                                               |                                                                                   |                                |
| Crypto Accelerators                                       | Security             | Yes                                                                               |                                                                                   |                                |
| Program and Data Storage                                  |                      |                                                                                   |                                                                                   |                                |
| On-Chip Shared Memory (RAM)                               | OCSRAM               | See <a href="#">Section 6.6, Operating Performance Points</a>                     |                                                                                   |                                |
| R5F Tightly Coupled Memory (TCM)                          | TCM                  | 256KB <sup>(9)</sup>                                                              |                                                                                   |                                |
| General-Purpose Memory Controller                         | GPMP                 | 4MB                                                                               |                                                                                   |                                |
| Peripherals                                               |                      |                                                                                   |                                                                                   |                                |
| Modular Controller Area Network Interface                 | MCAN                 | 4                                                                                 |                                                                                   |                                |
| Full CAN-FD Support                                       | MCAN                 | 4                                                                                 |                                                                                   |                                |
| General-Purpose I/O                                       | GPIO                 | Up to 139                                                                         |                                                                                   |                                |
| Serial Peripheral Interface                               | SPI                  | 5                                                                                 |                                                                                   |                                |
| Universal Asynchronous Receiver and Transmitter           | UART                 | 6                                                                                 |                                                                                   |                                |
| Local Interconnect Network                                | LIN                  | 5                                                                                 |                                                                                   |                                |
| Inter-Integrated Circuit Interface                        | I2C                  | 4                                                                                 |                                                                                   |                                |
| Analog-to-Digital Converter                               | ADC                  | 3 <sup>(4)</sup> or 5 <sup>(5)</sup>                                              | 3 <sup>(4)</sup> or 5 <sup>(5)</sup>                                              | 3                              |
| Comparator Modules                                        | CMPSS                | 12 <sup>(4)</sup> or 20 <sup>(5)</sup>                                            | 12 <sup>(4)</sup> or 20 <sup>(5)</sup>                                            | 12                             |
| Digital-to-Analog Converter                               | DAC                  | 1                                                                                 |                                                                                   |                                |
| Programmable Real-Time Unit Subsystem <sup>(6)</sup>      | PRU-ICSS             | 0 or 1                                                                            |                                                                                   |                                |
| Industrial Communication Subsystem Support <sup>(7)</sup> | PRU-ICSS             | Optional                                                                          |                                                                                   |                                |
| Gigabit Ethernet Interface                                | CPSW                 | Yes (2-port)                                                                      |                                                                                   |                                |
| Multi-Media Card/Secure Digital Interface                 | MMCSD                | 1                                                                                 |                                                                                   |                                |
| Enhanced High-Resolution Pulse-Width Modulator Module     | EHRPWM               | 16 <sup>(3)</sup> or 32 <sup>(5)</sup>                                            | 16 <sup>(4)</sup> or 32 <sup>(5)</sup>                                            | 16                             |
| Enhanced Capture Module                                   | ECAP                 | 5 <sup>(4)</sup> or 10 <sup>(5)</sup>                                             | 5 <sup>(4)</sup> or 10 <sup>(5)</sup>                                             | 5                              |
| Enhanced Quadrature Encoder Pulse Module                  | EQEP                 | 2 <sup>(4)</sup> or 3 <sup>(5)</sup>                                              | 2 <sup>(4)</sup> or 3 <sup>(5)</sup>                                              | 2                              |
| Sigma Delta Filter Module                                 | SDFM                 | 1 <sup>(4)</sup> or 2 <sup>(5)</sup>                                              | 1 <sup>(4)</sup> or 2 <sup>(5)</sup>                                              | 1                              |
| Fast Serial Interface                                     | FSI                  | 4x FSI_RX + 4x FSI_TX                                                             |                                                                                   |                                |
| Quad SPI Flash Interface                                  | QSPI                 | 1                                                                                 |                                                                                   |                                |
| Miscellaneous                                             |                      |                                                                                   |                                                                                   |                                |
| Junction Temperature                                      |                      | Industrial: –40°C to 105°C                                                        |                                                                                   |                                |
|                                                           |                      | Extended Automotive: –40°C to 150°C                                               |                                                                                   |                                |
|                                                           |                      | Automotive: –40°C to 125°C                                                        |                                                                                   |                                |
| Automotive Qualification                                  |                      | AEC-Q100 <sup>(8)</sup> Option                                                    |                                                                                   |                                |

- (1) Developed for Functional Safety applications, the device supports hardware integrity upto ASIL-D or SIL-3. Refer to the related documentation for more details.
- (2) "X:" letter refers to feature parameter and (Grade "X") refers to Grade in the [Section 6.6, Operating Performance Points](#) table.
- (3) For more details about the CTRLMMR\_WKUP\_JTAG\_DEVICE\_ID register and DEVICE\_ID bit field, see the device TRM.
- (4) Standard Analog configuration contains 3x ADC, 16x EHRPWM, 5x eCAP, 2x EQEP, 1x SDFM, 12x CMPSS
- (5) Enhanced Analog configuration contains 5x ADC, 32x EHRPWM, 10x eCAP, 3x EQEP, 2x SDFM, 20x CMPSS
- (6) Programmable Real-Time Unit Subsystem is available when selecting an orderable part number that includes a feature code of D, E, F, K, L, or M. Refer to the [Nomenclature Description](#) table for definition of feature codes.
- (7) Industrial Communication Subsystem Support is available when selecting an orderable part number that includes a feature code of D, E, F, K, L, or M. Refer to the [Nomenclature Description](#) table for definition of feature codes.

- (8) AEC-Q100 qualification is applicable to select part number variants as indicated by the Automotive Designator (Q1) identifier in the [Nomenclature Description](#) table.
- (9) Each R5FSS cluster supports 128KB of Tightly-Coupled Memory (TCM). When configured as Single-Core or Lockstep operating mode, individual cores can utilize the entire 128KB of TCM memory, while in Dual-Core mode, each core may only utilize its designated half (64KB TCM).

## 4.1 Related Products

**Sitara™ Microcontrollers** Family of Arm® Cortex®-R based high performance microcontrollers with advanced networking, real-time control, and signal processing accelerators to meet emerging MCU requirements for industrial and automotive applications.

**Sitara™ Processors** Family of broad, scalable processors based on Arm® Cortex®-A cores with flexible accelerators, peripherals, connectivity and unified software support – an excellent choice for sensors to servers. Sitara™ processors have the features and reliability necessary for the latest industrial and automotive application-level requirements.

**Sitara™ Microcontrollers - Evaluation Modules** TI provides device-specific Evaluation Module (EVM) designs to help kick-start product development. See the [AM263x ControlCard](#) and [AM263x LaunchPad](#) for more information.

**Products to complete your design** The following list of products are frequently purchased or used in conjunction with the AM263x device to meet your system design requirements.

- [TPS653850A-Q1](#) - Functional safety compliant multi-rail power supply for safety MCUs with 350mA I/O rail.
- [TPS3704-Q1](#) - Automotive multichannel window supervisor with very-high accuracy and compact form factor.
- [DP83TG720S-Q1](#) - 1000BASE-T1 automotive Ethernet PHY with RGMII.
- [DP83826E](#) - Low latency 10/100-Mbps Ethernet PHY with MII interface and enhanced mode.
- [TCAN1042H-Q1](#) - Automotive 70-V bus-fault-protected CAN transceiver with flexible data-rate.

## 5 Terminal Configuration and Functions

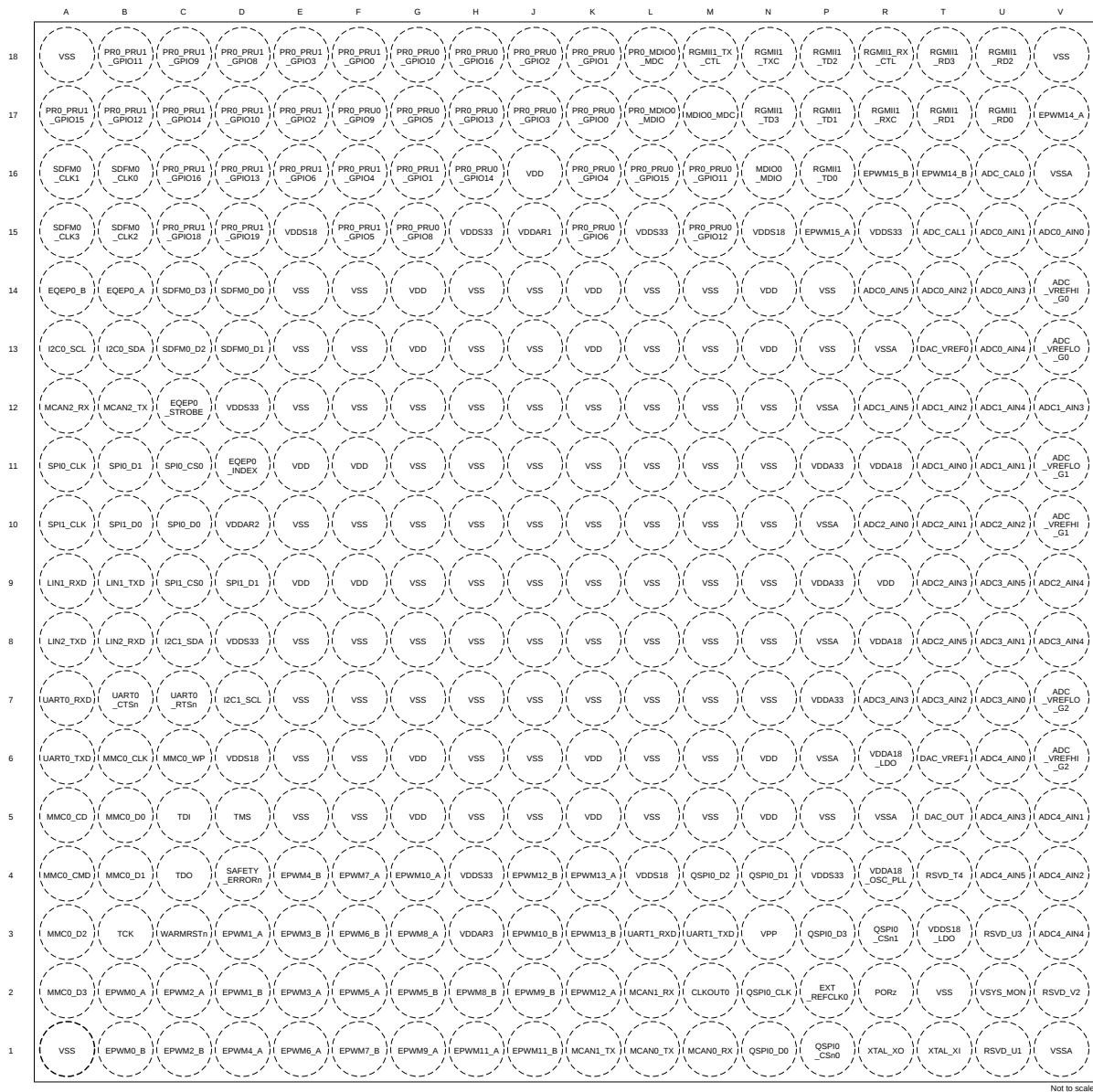
### 5.1 Pin Diagram

#### Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

The diagrams in this section are used in conjunction with the other Terminal Configuration and Functions tables to locate signal names and ball grid numbers.

#### 5.1.1 ZCZ Pin Diagram



## 5.2 Pin Attributes

The following list describes the contents of each column in the *Pin Attributes* table:

1. **Ball Number:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **Ball Name:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **Signal Name:** Signal name of all dedicated and pin multiplexed signal functions associated with a ball.

---

### Note

The *Pin Attributes* table, defines the SoC pin multiplexed signal function implemented at the pin and **does not** define secondary multiplexing of signal functions implemented in device subsystems. Secondary multiplexing of signal functions are not described in this table. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

---

4. **Mux Mode:** The MUXMODE value associated with each pin multiplexed signal function:
  - MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.
  - MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only defined valid values of MUXMODE can be used.
  - Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz. These input signal functions are fixed to their respective pins and are not programmable via MUXMODE.
  - An empty box or "-" means Not Applicable.

---

### Note

- The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when PORz is deasserted.
  - Configuring two pins to the same pin multiplexed signal function can yield unexpected results and is not supported. This can be prevented with proper software configuration.
  - Configuring a pad to an undefined multiplexing mode results in undefined behavior and must be avoided.
- 

5. **Type:** Signal type and direction:
  - I = Input
  - O = Output
  - ID = Input, with open-drain output function
  - OD = Output, with open-drain output function
  - IO = Input, Output, or simultaneously Input and Output
  - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
  - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
  - OZ = Output with three-state output function
  - A = Analog
  - CAP = LDO capacitor
  - PWR = Power
  - GND = Ground
6. **DSIS:** The deselected input state (DSIS) indicates the state driven to the subsystem input (logic "0", logic "1", or "pad" level) when the pin multiplexed signal function is not selected by MUXMODE.
  - 0: **Logic 0** driven to the subsystem input.
  - 1: **Logic 1** driven to the subsystem input.
  - pad: Logic state of the pad is driven to the subsystem input.

- An empty box, NA, or "-" means Not Applicable.
7. **Ball State During Reset (RX/TX/PULL):** State of the terminal while PORz is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
- RX (Input buffer)
    - Off: The input buffer is **disabled**.
    - On: The input buffer is **enabled**.
  - TX (Output buffer)
    - Off: The output buffer is **disabled**.
    - Low: The output buffer is **enabled** and drives  $V_{OL}$ .
  - PULL (Internal pull resistors)
    - Off: Internal pull resistors are turned **off**.
    - Up: Internal **pull-up** resistor is turned on.
    - Down: Internal **pull-down** resistor is turned on.
    - NA: No internal pull resistor.
  - An empty box, or "-" means Not Applicable.
8. **Ball State After Reset (RX/TX/PULL):** State of the terminal after PORz is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
- RX (Input buffer)
    - Off: The input buffer is **disabled**.
    - On: The input buffer is **enabled**.
  - TX (Output buffer)
    - Off: The output buffer is **disabled**.
    - SS: The subsystem selected with MUXMODE determines the output buffer state.
  - PULL (Internal pull resistors)
    - Off: Internal pull resistors are turned **off**.
    - Up: Internal **pull-up resistor** is turned on.
    - Down: Internal **pull-down resistor** is turned on.
    - NA: No internal pull resistor.
  - An empty box, NA, or "-" means Not Applicable.
9. **Mux Mode After Reset:** The value found in this column defines the **default** pin multiplexed signal function after PORz is deasserted.
- An empty box, NA, or "-" means Not Applicable.
10. **I/O Voltage:** This column describes I/O **operating voltage** options of the respective power supply, when applicable.
- An empty box, NA, or "-" means Not Applicable.
- For more information, see valid operating voltage range defined for each power supply in *Recommended Operating Conditions*.
11. **Power:** The power supply of the associated I/O, when applicable.
- An empty box, NA, or "-" means Not Applicable.
12. **Hys:** Indicates if the input buffer associated with this I/O has hysteresis:
- Yes: Hysteresis Support
  - No: **No** Hysteresis Support
  - An empty box, NA, or "-" means Not Applicable.
- For more information, see the hysteresis values in *Electrical Characteristics*.
13. **Pull Type:** Indicates the presence of an internal pull-up or pull-down resistor. Internal resistors can be enabled or disabled via software.
- PU: Internal pull-up Only

- PD: Internal pull-down Only
- PU/PD: Internal pull-up and pull-down
- An empty box, NA, or "-" means No internal pull.

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**Note**

Configuring two pins to the same pin multiplexed signal function is not supported as this yields unexpected results. Issues can be easily prevented with the proper software configuration.

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This must be avoided.

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14. **Buffer Type:** This column defines the buffer type associated with a terminal. This information can be used to determine the applicable Electrical Characteristics table.

- An empty box, NA, or "-" means Not Applicable.

For electrical characteristics, refer to the appropriate buffer type table in *Electrical Characteristics*.

15. **Pad Configuration Register Name:** This is the name of the device pad/pin configuration register.
16. **Pad Configuration Register Address:** This is the memory address of the device pad/pin configuration register.
17. **Pad Configuration Register Default Value:** This is the default value of the register device pad/pin configuration register after PORz is deasserted.

**Table 5-1. Pin Attributes (ZCZ Package)**

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET RX/TX/PULL [7] | BALL STATE AFTER RESET RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|----------|----------------------------------------|---------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| V15             | ADC0_AIN0                                                                     | ADC0_AIN0       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| U15             | ADC0_AIN1                                                                     | ADC0_AIN1       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| T14             | ADC0_AIN2                                                                     | ADC0_AIN2       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| U14             | ADC0_AIN3                                                                     | ADC0_AIN3       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| U13             | ADC0_AIN4                                                                     | ADC0_AIN4       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| R14             | ADC0_AIN5                                                                     | ADC0_AIN5       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| T11             | ADC1_AIN0                                                                     | ADC1_AIN0       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| U11             | ADC1_AIN1                                                                     | ADC1_AIN1       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| T12             | ADC1_AIN2                                                                     | ADC1_AIN2       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| V12             | ADC1_AIN3                                                                     | ADC1_AIN3       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| U12             | ADC1_AIN4                                                                     | ADC1_AIN4       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| R12             | ADC1_AIN5                                                                     | ADC1_AIN5       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| R10             | ADC2_AIN0                                                                     | ADC2_AIN0       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| T10             | ADC2_AIN1                                                                     | ADC2_AIN1       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| U10             | ADC2_AIN2                                                                     | ADC2_AIN2       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| T9              | ADC2_AIN3                                                                     | ADC2_AIN3       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| V9              | ADC2_AIN4                                                                     | ADC2_AIN4       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| T8              | ADC2_AIN5                                                                     | ADC2_AIN5       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| U7              | ADC3_AIN0                                                                     | ADC3_AIN0       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| U8              | ADC3_AIN1                                                                     | ADC3_AIN1       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| T7              | ADC3_AIN2                                                                     | ADC3_AIN2       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| R7              | ADC3_AIN3                                                                     | ADC3_AIN3       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| V8              | ADC3_AIN4                                                                     | ADC3_AIN4       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| U9              | ADC3_AIN5                                                                     | ADC3_AIN5       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| U6              | ADC4_AIN0                                                                     | ADC4_AIN0       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| V5              | ADC4_AIN1                                                                     | ADC4_AIN1       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| V4              | ADC4_AIN2                                                                     | ADC4_AIN2       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| U5              | ADC4_AIN3                                                                     | ADC4_AIN3       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| V3              | ADC4_AIN4                                                                     | ADC4_AIN4       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| U4              | ADC4_AIN5                                                                     | ADC4_AIN5       |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| U16             | ADC_CAL0                                                                      | ADC_CAL0        |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| T15             | ADC_CAL1                                                                      | ADC_CAL1        |              | I        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| V14             | ADC_VREFHI_G0                                                                 | ADC_VREFHI_G0   |              | A        |                                        |                                       |                          | 1.8V            | VDDA_CIO   |          | AnalogCIO        |                |
| V10             | ADC_VREFHI_G1                                                                 | ADC_VREFHI_G1   |              | A        |                                        |                                       |                          | 1.8V            | VDDA_CIO   |          | AnalogCIO        |                |
| V6              | ADC_VREFHI_G2                                                                 | ADC_VREFHI_G2   |              | A        |                                        |                                       |                          | 1.8V            | VDDA_CIO   |          | AnalogCIO        |                |
| V13             | ADC_VREFLO_G0                                                                 | ADC_VREFLO_G0   |              | A        |                                        |                                       |                          | 1.8V            | VDDA_CIO   |          | AnalogCIO        |                |
| V11             | ADC_VREFLO_G1                                                                 | ADC_VREFLO_G1   |              | A        |                                        |                                       |                          | 1.8V            | VDDA_CIO   |          | AnalogCIO        |                |

Table 5-1. Pin Attributes (ZCZ Package) (continued)

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET RX/TX/PULL [7] | BALL STATE AFTER RESET RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|----------|----------------------------------------|---------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| V7              | ADC_VREFLO_G2                                                                 | ADC_VREFLO_G2   |              | A        |                                        |                                       |                          | 1.8V            | VDDA_CIO   |          | AnalogCIO        |                |
| M2              | CLKOUT0                                                                       | CLKOUT0         | 0            | O        | Off / Off / Off                        | Off / SS / Off                        | 0                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 | CLKOUT0_CFG_REG<br>0x5310 0228<br>0x0000 0570                                 | GPIO138         | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| T5              | DAC_OUT                                                                       | DAC_OUT         |              | O        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| T13             | DAC_VREF0                                                                     | DAC_VREF0       |              | A        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| T6              | DAC_VREF1                                                                     | DAC_VREF1       |              | A        |                                        |                                       |                          | 3.3V            | VDDA_CIO   |          | AnalogCIO        |                |
| B2              | EPWM0_A                                                                       | EPWM0_A         | 0            | O        | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 | EPWM0_A_CFG_REG<br>0x5310 00AC<br>0x0000 05F7                                 | GPIO43          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| B1              | EPWM0_B                                                                       | EPWM0_B         | 0            | O        | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 | EPWM0_B_CFG_REG<br>0x5310 00B0<br>0x0000 05F7                                 | GPIO44          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| D3              | EPWM1_A                                                                       | EPWM1_A         | 0            | O        | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 | EPWM1_A_CFG_REG<br>0x5310 00B4<br>0x0000 05F7                                 | GPIO45          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| D2              | EPWM1_B                                                                       | EPWM1_B         | 0            | O        | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 | EPWM1_B_CFG_REG<br>0x5310 00B8<br>0x0000 05F7                                 | GPIO46          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| C2              | EPWM2_A                                                                       | EPWM2_A         | 0            | O        | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 | EPWM2_A_CFG_REG<br>0x5310 00BC<br>0x0000 05F7                                 | GPIO47          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| C1              | EPWM2_B                                                                       | EPWM2_B         | 0            | O        | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 | EPWM2_B_CFG_REG<br>0x5310 00C0<br>0x0000 05F7                                 | GPIO48          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| E2              | EPWM3_A                                                                       | EPWM3_A         | 0            | O        | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 | EPWM3_A_CFG_REG<br>0x5310 00C4<br>0x0000 05F7                                 | GPIO49          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| E3              | EPWM3_B                                                                       | EPWM3_B         | 0            | O        | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 | EPWM3_B_CFG_REG<br>0x5310 00C8<br>0x0000 05F7                                 | GPIO50          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| D1              | EPWM4_A                                                                       | EPWM4_A         | 0            | O        | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 | EPWM4_A_CFG_REG<br>0x5310 00CC<br>0x0000 05F7                                 | GPIO51          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |

**Table 5-1. Pin Attributes (ZCZ Package) (continued)**

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET<br>RX/TX/PULL [7] | BALL STATE AFTER RESET<br>RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|----------|-------------------------------------------|------------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| E4              | EPWM4_B<br>EPWM4_B_CFG_REG<br>0x5310 00D0<br>0x0000 05F7                      | EPWM4_B         | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSITX1_CLK      | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO52          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| F2              | EPWM5_A<br>EPWM5_A_CFG_REG<br>0x5310 00D4<br>0x0000 05F7                      | EPWM5_A         | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSITX1_DATA0    | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO53          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| G2              | EPWM5_B<br>EPWM5_B_CFG_REG<br>0x5310 00D8<br>0x0000 05F7                      | EPWM5_B         | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSITX1_DATA1    | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO54          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| E1              | EPWM6_A<br>EPWM6_A_CFG_REG<br>0x5310 00DC<br>0x0000 05F7                      | EPWM6_A         | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSIRX1_CLK      | 6            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO55          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| F3              | EPWM6_B<br>EPWM6_B_CFG_REG<br>0x5310 00E0<br>0x0000 05F7                      | EPWM6_B         | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSIRX1_DATA0    | 6            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO56          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| F4              | EPWM7_A<br>EPWM7_A_CFG_REG<br>0x5310 00E4<br>0x0000 05F7                      | EPWM7_A         | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSIRX1_DATA1    | 6            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO57          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| F1              | EPWM7_B<br>EPWM7_B_CFG_REG<br>0x5310 00E8<br>0x0000 05F7                      | EPWM7_B         | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | GPIO58          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| G3              | EPWM8_A<br>EPWM8_A_CFG_REG<br>0x5310 00EC<br>0x0000 05F7                      | EPWM8_A         | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART4_TXD       | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | I2C3_SDA        | 2            | IOD      |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | FSITX2_CLK      | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO59          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| H2              | EPWM8_B<br>EPWM8_B_CFG_REG<br>0x5310 00F0<br>0x0000 05F7                      | EPWM8_B         | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART4_RXD       | 1            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | I2C3_SCL        | 2            | IOD      |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | FSITX2_DATA0    | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO60          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| G1              | EPWM9_A<br>EPWM9_A_CFG_REG<br>0x5310 00F4<br>0x0000 05F7                      | EPWM9_A         | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSITX2_DATA1    | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO61          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |

Table 5-1. Pin Attributes (ZCZ Package) (continued)

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET<br>RX/TX/PULL [7] | BALL STATE AFTER RESET<br>RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|----------|-------------------------------------------|------------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| J2              | EPWM9_B<br>EPWM9_B_CFG_REG<br>0x5310 00F8<br>0x0000 05F7                      | EPWM9_B         | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART1_RTSn      | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | FSIRX2_CLK      | 6            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO62          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| G4              | EPWM10_A<br>EPWM10_A_CFG_REG<br>0x5310 00FC<br>0x0000 05F7                    | EPWM10_A        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART1_CTSn      | 1            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | FSIRX2_DATA0    | 6            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO63          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| J3              | EPWM10_B<br>EPWM10_B_CFG_REG<br>0x5310 0100<br>0x0000 05F7                    | EPWM10_B        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART2_RTSn      | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | FSIRX2_DATA1    | 6            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO64          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| H1              | EPWM11_A<br>EPWM11_A_CFG_REG<br>0x5310 0104<br>0x0000 05F7                    | EPWM11_A        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART2_CTSn      | 1            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_CLKLB     | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO65          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| J1              | EPWM11_B<br>EPWM11_B_CFG_REG<br>0x5310 0108<br>0x0000 05F7                    | EPWM11_B        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART3_RTSn      | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_OEn_REn   | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO66          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| K2              | EPWM12_A<br>EPWM12_A_CFG_REG<br>0x5310 010C<br>0x0000 05F7                    | EPWM12_A        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART3_CTSn      | 1            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SPI4_CS1        | 2            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_WEn       | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO67          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| J4              | EPWM12_B<br>EPWM12_B_CFG_REG<br>0x5310 0110<br>0x0000 05F7                    | EPWM12_B        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART1_DCDn      | 1            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_CSn0      | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO68          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| K4              | EPWM13_A<br>EPWM13_A_CFG_REG<br>0x5310 0114<br>0x0000 05F7                    | EPWM13_A        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART1_RIn       | 1            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD0       | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO69          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| K3              | EPWM13_B<br>EPWM13_B_CFG_REG<br>0x5310 0118<br>0x0000 05F7                    | EPWM13_B        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART1_DTRn      | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD1       | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO70          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |

**Table 5-1. Pin Attributes (ZCZ Package) (continued)**

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET<br>RX/TX/PULL [7] | BALL STATE AFTER RESET<br>RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|----------|-------------------------------------------|------------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| V17             | EPWM14_A<br>EPWM14_A_CFG_REG<br>0x5310 011C<br>0x0000 05F7                    | EPWM14_A        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART1_DSRn      | 1            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD2       | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO71          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| T16             | EPWM14_B<br>EPWM14_B_CFG_REG<br>0x5310 0120<br>0x0000 05F7                    | EPWM14_B        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | MII1_RX_ER      | 2            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD3       | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO72          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| P15             | EPWM15_A<br>EPWM15_A_CFG_REG<br>0x5310 0124<br>0x0000 05F7                    | EPWM15_A        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART5_TXD       | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII1_COL        | 2            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD4       | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO73          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| R16             | EPWM15_B<br>EPWM15_B_CFG_REG<br>0x5310 0128<br>0x0000 05F7                    | EPWM15_B        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART5_RXD       | 1            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII1_CRS        | 2            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD5       | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO74          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| B14             | EQEP0_A<br>EQEP0_A_CFG_REG<br>0x5310 0208<br>0x0000 05F7                      | UART4_RTSn      | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | SPI4_CLK        | 3            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO130         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP0_A         | 8            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_CLK0      | 9            | I        |                                           |                                          |                          |                 |            |          |                  |                |
| A14             | EQEP0_B<br>EQEP0_B_CFG_REG<br>0x5310 020C<br>0x0000 05F7                      | UART4_CTSn      | 0            | I        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | SPI4_CS0        | 3            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO131         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP0_B         | 8            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_D0        | 9            | I        |                                           |                                          |                          |                 |            |          |                  |                |
| D11             | EQEP0_INDEX<br>EQEP0_INDEX_CFG_REG<br>0x5310 0214<br>0x0000 05F7              | UART4_RXD       | 0            | I        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | LIN4_RXD        | 1            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SPI4_D1         | 3            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO133         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP0_INDEX     | 8            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_D1        | 9            | I        |                                           |                                          |                          |                 |            |          |                  |                |

Table 5-1. Pin Attributes (ZCZ Package) (continued)

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET RX/TX/PULL [7] | BALL STATE AFTER RESET RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|----------|----------------------------------------|---------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| C12             | EQEP0_STROBE<br>EQEP0_STROBE_CFG_REG<br>0x5310 0210<br>0x0000 05F7            | UART4_TXD       | 0            | O        | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | LIN4_TXD        | 1            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | SPI4_D0         | 3            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO132         | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP0_STROBE    | 8            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_CLK1      | 9            | I        |                                        |                                       |                          |                 |            |          |                  |                |
| P2              | EXT_REFCLK0<br>EXT_REFCLK0_CFG_REG<br>0x5310 01E4<br>0x0000 05F7              | EXT_REFCLK0     | 0            | I        | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | XBAROUT15       | 5            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO121         | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP1_INDEX     | 9            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| A13             | I2C0_SCL<br>I2C0_SCL_CFG_REG<br>0x5310 021C<br>0x0000 05F7                    | I2C0_SCL        | 0            | IOD      | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | I2C OD           |                |
|                 |                                                                               | GPIO135         | 7            | IOD      |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP2_B         | 8            | ID       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_CLK3      | 9            | ID       |                                        |                                       |                          |                 |            |          |                  |                |
| B13             | I2C0_SDA<br>I2C0_SDA_CFG_REG<br>0x5310 0218<br>0x0000 05F7                    | I2C0_SDA        | 0            | IOD      | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | I2C OD           |                |
|                 |                                                                               | GPIO134         | 7            | IOD      |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP2_A         | 8            | ID       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_CLK2      | 9            | ID       |                                        |                                       |                          |                 |            |          |                  |                |
| D7              | I2C1_SCL<br>I2C1_SCL_CFG_REG<br>0x5310 005C<br>0x0000 05F7                    | I2C1_SCL        | 0            | IOD      | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | SPI3_CS0        | 2            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | XBAROUT7        | 5            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO23          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| C8              | I2C1_SDA<br>I2C1_SDA_CFG_REG<br>0x5310 0060<br>0x0000 05F7                    | I2C1_SDA        | 0            | IOD      | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | SPI3_CLK        | 2            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | XBAROUT8        | 5            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO24          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| A9              | LIN1_RXD<br>LIN1_RXD_CFG_REG<br>0x5310 004C<br>0x0000 05F7                    | LIN1_RXD        | 0            | IO       | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART1_RXD       | 1            | I        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | SPI2_CS0        | 2            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | XBAROUT5        | 5            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO19          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| B9              | LIN1_TXD<br>LIN1_TXD_CFG_REG<br>0x5310 0050<br>0x0000 05F7                    | LIN1_TXD        | 0            | IO       | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART1_TXD       | 1            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | SPI2_CLK        | 2            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | XBAROUT6        | 5            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO20          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |

**Table 5-1. Pin Attributes (ZCZ Package) (continued)**

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET<br>RX/TX/PULL [7] | BALL STATE AFTER RESET<br>RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|----------|-------------------------------------------|------------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| B8              | LIN2_RXD<br>LIN2_RXD_CFG_REG<br>0x5310 0054<br>0x0000 05F7                    | LIN2_RXD        | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART2_RXD       | 1            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SPI2_D0         | 2            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO21          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| A8              | LIN2_TXD<br>LIN2_TXD_CFG_REG<br>0x5310 0058<br>0x0000 05F7                    | LIN2_TXD        | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART2_TXD       | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SPI2_D1         | 2            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO22          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| M1              | MCAN0_RX<br>MCAN0_RX_CFG_REG<br>0x5310 001C<br>0x0000 05F7                    | MCAN0_RX        | 0            | I        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | SPI4_CS0        | 1            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO7           | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| L1              | MCAN0_TX<br>MCAN0_TX_CFG_REG<br>0x5310 0020<br>0x0000 05F7                    | MCAN0_TX        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | SPI4_CLK        | 1            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO8           | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| L2              | MCAN1_RX<br>MCAN1_RX_CFG_REG<br>0x5310 0024<br>0x0000 05F7                    | MCAN1_RX        | 0            | I        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | SPI4_D0         | 1            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO9           | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| K1              | MCAN1_TX<br>MCAN1_TX_CFG_REG<br>0x5310 0028<br>0x0000 05F7                    | MCAN1_TX        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | SPI4_D1         | 1            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO10          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| A12             | MCAN2_RX<br>MCAN2_RX_CFG_REG<br>0x5310 0224<br>0x0000 05F7                    | MCAN2_RX        | 0            | I        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART2_RTSn      | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO137         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP2_INDEX     | 8            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_D3        | 9            | I        |                                           |                                          |                          |                 |            |          |                  |                |
| B12             | MCAN2_TX<br>MCAN2_TX_CFG_REG<br>0x5310 0220<br>0x0000 05F7                    | MCAN2_TX        | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART1_RTSn      | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO136         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP2_STROBE    | 8            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_D2        | 9            | I        |                                           |                                          |                          |                 |            |          |                  |                |
| M17             | MDIO0_MDC<br>MDIO0_MDC_CFG_REG<br>0x5310 00A8<br>0x0000 05F7                  | MDIO0_MDC       | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | GPIO42          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| N16             | MDIO0_MDIO<br>MDIO0_MDIO_CFG_REG<br>0x5310 00A4<br>0x0000 05F7                | MDIO0_MDIO      | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | GPIO41          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |

Table 5-1. Pin Attributes (ZCZ Package) (continued)

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET<br>RX/TX/PULL [7] | BALL STATE AFTER RESET<br>RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|----------|-------------------------------------------|------------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| A5              | MMC0_CD<br>MMC0_CD_CFG_REG<br>0x5310 0150<br>0x0000 05F7                      | MMC0_CD         | 0            | I        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART0_CTSn      | 1            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | I2C2_SDA        | 2            | IOD      |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM20_B        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD15      | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO84          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_D3        | 8            | I        |                                           |                                          |                          |                 |            |          |                  |                |
| B6              | MMC0_CLK<br>MMC0_CLK_CFG_REG<br>0x5310 0134<br>0x0000 05F7                    | MMC0_CLK        | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART0_RXD       | 1            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | LIN0_RXD        | 2            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM17_A        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD8       | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO77          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_CLK0      | 8            | I        |                                           |                                          |                          |                 |            |          |                  |                |
| A4              | MMC0_CMD<br>MMC0_CMD_CFG_REG<br>0x5310 0138<br>0x0000 05F7                    | MMC0_CMD        | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART0_TXD       | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | LIN0_TXD        | 2            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM17_B        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD9       | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO78          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_D0        | 8            | I        |                                           |                                          |                          |                 |            |          |                  |                |
| C6              | MMC0_WP<br>MMC0_WP_CFG_REG<br>0x5310 014C<br>0x0000 05F7                      | MMC0_WP         | 0            | I        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART0_RTSn      | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | I2C2_SCL        | 2            | IOD      |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM20_A        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD14      | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO83          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_CLK3      | 8            | I        |                                           |                                          |                          |                 |            |          |                  |                |
| B5              | MMC0_D0<br>MMC0_D0_CFG_REG<br>0x5310 013C<br>0x0000 05F7                      | MMC0_D0         | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART2_RXD       | 1            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | I2C1_SCL        | 2            | IOD      |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM18_A        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD10      | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO79          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_CLK1      | 8            | I        |                                           |                                          |                          |                 |            |          |                  |                |

**Table 5-1. Pin Attributes (ZCZ Package) (continued)**

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET<br>RX/TX/PULL [7] | BALL STATE AFTER RESET<br>RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|----------|-------------------------------------------|------------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| B4              | MMC0_D1<br>MMC0_D1_CFG_REG<br>0x5310 0140<br>0x0000 05F7                      | MMC0_D1         | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | EPWM18_B        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD11      | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO80          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_D1        | 8            | I        |                                           |                                          |                          |                 |            |          |                  |                |
| A3              | MMC0_D2<br>MMC0_D2_CFG_REG<br>0x5310 0144<br>0x0000 05F7                      | MMC0_D2         | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART2_TXD       | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | I2C1_SDA        | 2            | IOD      |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM19_A        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD12      | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO81          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_CLK2      | 8            | I        |                                           |                                          |                          |                 |            |          |                  |                |
| A2              | MMC0_D3<br>MMC0_D3_CFG_REG<br>0x5310 0148<br>0x0000 05F7                      | MMC0_D3         | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART3_RTSn      | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM19_B        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD13      | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO82          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM1_D2        | 8            | I        |                                           |                                          |                          |                 |            |          |                  |                |
| R2              | PORz                                                                          | PORz            |              | I        |                                           |                                          | 0                        | 3.3V            | VDDSHV0    | Yes      | RESET            |                |
| L18             | PR0_MDIO0_MDC<br>PR0_MDIO0_MDC_CFG_REG<br>0x5310 0158<br>0x0000 05F7          | PR0_MDIO0_MDC   | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | EPWM21_B        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_CSn3      | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO86          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| L17             | PR0_MDIO0_MDIO<br>PR0_MDIO0_MDIO_CFG_REG<br>0x5310 0154<br>0x0000 05F7        | PR0_MDIO0_MDIO  | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | EPWM21_A        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_CSn2      | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO85          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| K17             | PR0_PRU0_GPIO0<br>PR0_PRU0_GPIO0_CFG_REG<br>0x5310 0174<br>0x0000 05F7        | PR0_PRU0_GPIO0  | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RMII2_RXD0      | 2            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | RGMI2_RD0       | 3            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII2_RXD0       | 4            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM25_A        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A1        | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO93          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |

Table 5-1. Pin Attributes (ZCZ Package) (continued)

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET<br>RX/TX/PULL [7] | BALL STATE AFTER RESET<br>RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|----------|-------------------------------------------|------------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| K18             | PR0_PRU0_GPIO1<br>PR0_PRU0_GPIO1_CFG_REG<br>0x5310 0178<br>0x0000 05F7        | PR0_PRU0_GPIO1  | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RMII2_RXD1      | 2            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | RGMII2_RD1      | 3            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII2_RXD1       | 4            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM25_B        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A2        | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO94          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| J18             | PR0_PRU0_GPIO2<br>PR0_PRU0_GPIO2_CFG_REG<br>0x5310 017C<br>0x0000 05F7        | PR0_PRU0_GPIO2  | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RGMII2_RD2      | 3            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII2_RXD2       | 4            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM26_A        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A3        | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO95          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| J17             | PR0_PRU0_GPIO3<br>PR0_PRU0_GPIO3_CFG_REG<br>0x5310 0180<br>0x0000 05F7        | PR0_PRU0_GPIO3  | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RGMII2_RD3      | 3            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII2_RXD3       | 4            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM26_B        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A4        | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO96          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| K16             | PR0_PRU0_GPIO4<br>PR0_PRU0_GPIO4_CFG_REG<br>0x5310 0170<br>0x0000 05F7        | PR0_PRU0_GPIO4  | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RGMII2_RX_CTL   | 3            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII2_RXDV       | 4            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM24_B        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A0        | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO92          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| G17             | PR0_PRU0_GPIO5<br>PR0_PRU0_GPIO5_CFG_REG<br>0x5310 015C<br>0x0000 05F7        | PR0_PRU0_GPIO5  | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RMII2_RX_ER     | 2            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII2_RX_ER      | 4            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM22_A        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_DIR       | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO87          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |

**Table 5-1. Pin Attributes (ZCZ Package) (continued)**

| BALL<br>NUMBER<br>[1] | BALL NAME [2]/<br>IOMUX<br>REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET [9] | IO<br>VOLTAGE<br>[10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [14] | PULL<br>TYPE<br>[13] |
|-----------------------|----------------------------------------------------------------------------------|-----------------|-----------------|----------|----------------------------------------------------|---------------------------------------------------|-----------------------------------|-----------------------|------------|-------------|---------------------|----------------------|
| K15                   | PR0_PRU0_GPIO6<br>PR0_PRU0_GPIO6_CFG_REG<br>0x5310 016C<br>0x0000 05F7           | PR0_PRU0_GPIO6  | 0               | IO       | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | RMII2_REF_CLK   | 2               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | RGMII2_RXC      | 3               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | MII2_RXCLK      | 4               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | EPWM24_A        | 5               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPMC0_CSn1      | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO91          | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| G15                   | PR0_PRU0_GPIO8<br>PR0_PRU0_GPIO8_CFG_REG<br>0x5310 0168<br>0x0000 05F7           | PR0_PRU0_GPIO8  | 0               | IO       | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | EPWM23_B        | 5               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPMC0_WPn       | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO90          | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| F17                   | PR0_PRU0_GPIO9<br>PR0_PRU0_GPIO9_CFG_REG<br>0x5310 0160<br>0x0000 05F7           | PR0_PRU0_GPIO9  | 0               | IO       | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | PR0_UART0_CTSn  | 3               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | MII2_COL        | 4               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | EPWM22_B        | 5               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPMC0_CLK       | 6               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO88          | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| G18                   | PR0_PRU0_GPIO10<br>PR0_PRU0_GPIO10_CFG_REG<br>0x5310 0164<br>0x0000 05F7         | PR0_PRU0_GPIO10 | 0               | IO       | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | RMII2_CRS_DV    | 2               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | PR0_UART0_RTSn  | 3               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | MII2_CRS        | 4               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | EPWM23_A        | 5               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPMC0_WAIT0     | 6               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO89          | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| M16                   | PR0_PRU0_GPIO11<br>PR0_PRU0_GPIO11_CFG_REG<br>0x5310 018C<br>0x0000 05F7         | PR0_PRU0_GPIO11 | 0               | IO       | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | RMII2_TXD0      | 2               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | RGMII2_TD0      | 3               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | MII2_TXD0       | 4               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | EPWM28_A        | 5               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPMC0_A7        | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO99          | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |

Table 5-1. Pin Attributes (ZCZ Package) (continued)

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET<br>RX/TX/PULL [7] | BALL STATE AFTER RESET<br>RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|----------|-------------------------------------------|------------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| M15             | PR0_PRU0_GPIO12<br>PR0_PRU0_GPIO12_CFG_REG<br>0x5310 0190<br>0x0000 05F7      | PR0_PRU0_GPIO12 | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RMII2_TXD1      | 2            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | RGMII2_TD1      | 3            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII2_TXD1       | 4            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM28_B        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A8        | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO100         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| H17             | PR0_PRU0_GPIO13<br>PR0_PRU0_GPIO13_CFG_REG<br>0x5310 0194<br>0x0000 05F7      | PR0_PRU0_GPIO13 | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RGMII2_TD2      | 3            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII2_TXD2       | 4            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM29_A        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A9        | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO101         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| H16             | PR0_PRU0_GPIO14<br>PR0_PRU0_GPIO14_CFG_REG<br>0x5310 0198<br>0x0000 05F7      | PR0_PRU0_GPIO14 | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RGMII2_TD3      | 3            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII2_TXD3       | 4            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM29_B        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A10       | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO102         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| L16             | PR0_PRU0_GPIO15<br>PR0_PRU0_GPIO15_CFG_REG<br>0x5310 0188<br>0x0000 05F7      | PR0_PRU0_GPIO15 | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RMII2_TX_EN     | 2            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | RGMII2_TX_CTL   | 3            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII2_TX_EN      | 4            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM27_B        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A6        | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO98          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| H18             | PR0_PRU0_GPIO16<br>PR0_PRU0_GPIO16_CFG_REG<br>0x5310 0184<br>0x0000 05F7      | PR0_PRU0_GPIO16 | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RGMII2_TXC      | 3            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII2_TXCLK      | 4            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM27_A        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A5        | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO97          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| F18             | PR0_PRU1_GPIO0<br>PR0_PRU1_GPIO0_CFG_REG<br>0x5310 01B4<br>0x0000 05F7        | PR0_PRU1_GPIO0  | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSITX2_DATA1    | 3            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | TRC_DATA6       | 4            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A13       | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO109         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |

**Table 5-1. Pin Attributes (ZCZ Package) (continued)**

| BALL<br>NUMBER<br>[1] | BALL NAME [2]/<br>IOMUX<br>REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET [9] | IO<br>VOLTAGE<br>[10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [14] | PULL<br>TYPE<br>[13] |
|-----------------------|----------------------------------------------------------------------------------|-----------------|-----------------|----------|----------------------------------------------------|---------------------------------------------------|-----------------------------------|-----------------------|------------|-------------|---------------------|----------------------|
| G16                   | PR0_PRU1_GPIO1<br>PR0_PRU1_GPIO1_CFG_REG<br>0x5310 01B8<br>0x0000 05F7           | PR0_PRU1_GPIO1  | 0               | IO       | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | FSIRX2_CLK      | 3               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | TRC_DATA7       | 4               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPMC0_A14       | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO110         | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| E17                   | PR0_PRU1_GPIO2<br>PR0_PRU1_GPIO2_CFG_REG<br>0x5310 01BC<br>0x0000 05F7           | PR0_PRU1_GPIO2  | 0               | IO       | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | FSIRX2_DATA0    | 3               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | TRC_DATA8       | 4               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPMC0_A15       | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO111         | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| E18                   | PR0_PRU1_GPIO3<br>PR0_PRU1_GPIO3_CFG_REG<br>0x5310 01C0<br>0x0000 05F7           | PR0_PRU1_GPIO3  | 0               | IO       | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | FSIRX2_DATA1    | 3               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | TRC_DATA9       | 4               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPMC0_A16       | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO112         | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| F16                   | PR0_PRU1_GPIO4<br>PR0_PRU1_GPIO4_CFG_REG<br>0x5310 01B0<br>0x0000 05F7           | PR0_PRU1_GPIO4  | 0               | IO       | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | FSITX2_DATA0    | 3               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | TRC_DATA5       | 4               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPMC0_A12       | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO108         | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| F15                   | PR0_PRU1_GPIO5<br>PR0_PRU1_GPIO5_CFG_REG<br>0x5310 019C<br>0x0000 05F7           | PR0_PRU1_GPIO5  | 0               | IO       | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | TRC_DATA0       | 4               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | EPWM30_A        | 5               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPMC0_OEn_REn   | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO103         | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| E16                   | PR0_PRU1_GPIO6<br>PR0_PRU1_GPIO6_CFG_REG<br>0x5310 01AC<br>0x0000 05F7           | PR0_PRU1_GPIO6  | 0               | IO       | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | FSITX2_CLK      | 3               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | TRC_DATA4       | 4               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPMC0_A11       | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO107         | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| D18                   | PR0_PRU1_GPIO8<br>PR0_PRU1_GPIO8_CFG_REG<br>0x5310 01A8<br>0x0000 05F7           | PR0_PRU1_GPIO8  | 0               | IO       | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | TRC_DATA3       | 4               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | EPWM31_B        | 5               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPMC0_WEn       | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO106         | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |

Table 5-1. Pin Attributes (ZCZ Package) (continued)

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET<br>RX/TX/PULL [7] | BALL STATE AFTER RESET<br>RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|----------|-------------------------------------------|------------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| C18             | PR0_PRU1_GPIO9<br>PR0_PRU1_GPIO9_CFG_REG<br>0x5310 01A0<br>0x0000 05F7        | PR0_PRU1_GPIO9  | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | PR0_UART0_RXD   | 3            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | TRC_DATA1       | 4            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM30_B        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_BE0n_CLE  | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO104         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| D17             | PR0_PRU1_GPIO10<br>PR0_PRU1_GPIO10_CFG_REG<br>0x5310 01A4<br>0x0000 05F7      | PR0_PRU1_GPIO10 | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | PR0_UART0_TXD   | 3            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | TRC_DATA2       | 4            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM31_A        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_BE1n      | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO105         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| B18             | PR0_PRU1_GPIO11<br>PR0_PRU1_GPIO11_CFG_REG<br>0x5310 01CC<br>0x0000 05F7      | PR0_PRU1_GPIO11 | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSITX3_DATA1    | 3            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | TRC_DATA12      | 4            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A19       | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO115         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| B17             | PR0_PRU1_GPIO12<br>PR0_PRU1_GPIO12_CFG_REG<br>0x5310 01D0<br>0x0000 05F7      | PR0_PRU1_GPIO12 | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSIRX3_CLK      | 3            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | TRC_DATA13      | 4            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A20       | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO116         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| D16             | PR0_PRU1_GPIO13<br>PR0_PRU1_GPIO13_CFG_REG<br>0x5310 01D4<br>0x0000 05F7      | PR0_PRU1_GPIO13 | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSIRX3_DATA0    | 3            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | TRC_DATA14      | 4            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | XBAROUT11       | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A21       | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO117         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| C17             | PR0_PRU1_GPIO14<br>PR0_PRU1_GPIO14_CFG_REG<br>0x5310 01D8<br>0x0000 05F7      | PR0_PRU1_GPIO14 | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSIRX3_DATA1    | 3            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | TRC_DATA15      | 4            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | XBAROUT12       | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_CS0       | 6            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO118         | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |

**Table 5-1. Pin Attributes (ZCZ Package) (continued)**

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3]             | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET RX/TX/PULL [7] | BALL STATE AFTER RESET RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------------------|--------------|----------|----------------------------------------|---------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| A17             | PR0_PRU1_GPIO15<br>PR0_PRU1_GPIO15_CFG_REG<br>0x5310 01C8<br>0x0000 05F7      | PR0_PRU1_GPIO15             | 0            | IO       | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSITX3_DATA0                | 3            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | TRC_DATA11                  | 4            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A18                   | 6            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO114                     | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| C16             | PR0_PRU1_GPIO16<br>PR0_PRU1_GPIO16_CFG_REG<br>0x5310 01C4<br>0x0000 05F7      | PR0_PRU1_GPIO16             | 0            | IO       | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSITX3_CLK                  | 3            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | TRC_DATA10                  | 4            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_A17                   | 6            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO113                     | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| C15             | PR0_PRU1_GPIO18<br>PR0_PRU1_GPIO18_CFG_REG<br>0x5310 01E0<br>0x0000 05F7      | PR0_PRU1_GPIO18             | 0            | IO       | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART3_TXD                   | 2            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | PR0_IEP0_EDIO_DATA_IN_OUT31 | 3            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | TRC_CTL                     | 4            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | XBAROUT14                   | 5            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_WAIT1                 | 6            | I        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO120                     | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP1_B                     | 9            | I        |                                        |                                       |                          |                 |            |          |                  |                |
| D15             | PR0_PRU1_GPIO19<br>PR0_PRU1_GPIO19_CFG_REG<br>0x5310 01DC<br>0x0000 05F7      | PR0_PRU1_GPIO19             | 0            | IO       | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART3_RXD                   | 2            | I        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | PR0_IEP0_EDC_SYNC_OUT0      | 3            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | TRC_CLK                     | 4            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | XBAROUT13                   | 5            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO119                     | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP1_A                     | 9            | I        |                                        |                                       |                          |                 |            |          |                  |                |
| N2              | QSPI0_CLK<br>QSPI0_CLK_CFG_REG<br>0x5310 0008<br>0x0000 05F7                  | QSPI0_CLK                   | 0            | O        | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | GPIO2                       | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| LB              | QSPI0_CLKLB<br>QSPI0_CLKLB_CFG_REG<br>0x5310 0244<br>0x5F0                    | QSPI0_CLKLB                 | 0            | IO       | On / Off / Down                        | On / On / Down                        | 0                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
| P1              | QSPI0_CSn0<br>QSPI0_CSn0_CFG_REG<br>0x5310 0000<br>0x0000 05F7                | QSPI0_CSn0                  | 0            | O        | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | GPIO0                       | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |

Table 5-1. Pin Attributes (ZCZ Package) (continued)

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5]  | BALL STATE DURING RESET<br>RX/TX/PULL [7] | BALL STATE AFTER RESET<br>RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|-----------|-------------------------------------------|------------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| R3              | QSPI0_CSn1<br>QSPI0_CSn1_CFG_REG<br>0x5310 0004<br>0x0000 05F7                | QSPI0_CSn1      | 0            | O         | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | XBAROUT0        | 5            | O         |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO1           | 7            | IO        |                                           |                                          |                          |                 |            |          |                  |                |
| N1              | QSPI0_D0<br>QSPI0_D0_CFG_REG<br>0x5310 000C<br>0x0000 05D7                    | QSPI0_D0        | 0            | IO        | On / Off / Off                            | On / Off / Off                           | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | GPIO3           | 7            | IO        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SOP0            |              | Bootstrap |                                           |                                          |                          |                 |            |          |                  |                |
| N4              | QSPI0_D1<br>QSPI0_D1_CFG_REG<br>0x5310 0010<br>0x0000 05D7                    | QSPI0_D1        | 0            | I         | On / Off / Off                            | On / Off / Off                           | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | GPIO4           | 7            | IO        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SOP1            |              | Bootstrap |                                           |                                          |                          |                 |            |          |                  |                |
| M4              | QSPI0_D2<br>QSPI0_D2_CFG_REG<br>0x5310 0014<br>0x0000 05F7                    | QSPI0_D2        | 0            | I         | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | GPIO5           | 7            | IO        |                                           |                                          |                          |                 |            |          |                  |                |
| P3              | QSPI0_D3<br>QSPI0_D3_CFG_REG<br>0x5310 0018<br>0x0000 05F7                    | QSPI0_D3        | 0            | I         | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | GPIO6           | 7            | IO        |                                           |                                          |                          |                 |            |          |                  |                |
| R17             | RGMII1_RXC<br>RGMII1_RXC_CFG_REG<br>0x5310 0074<br>0x0000 05F7                | RGMII1_RXC      | 0            | I         | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RMII1_REF_CLK   | 1            | IO        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII1_RXCLK      | 2            | I         |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | FSITX0_CLK      | 6            | O         |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO29          | 7            | IO        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP2_A         | 8            | I         |                                           |                                          |                          |                 |            |          |                  |                |
| R18             | RGMII1_RX_CTL<br>RGMII1_RX_CTL_CFG_REG<br>0x5310 0078<br>0x0000 05F7          | RGMII1_RX_CTL   | 0            | I         | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RMII1_RX_ER     | 1            | I         |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII1_RXDV       | 2            | I         |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | FSITX0_DATA0    | 6            | O         |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO30          | 7            | IO        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP2_B         | 8            | I         |                                           |                                          |                          |                 |            |          |                  |                |
| N18             | RGMII1_TXC<br>RGMII1_TXC_CFG_REG<br>0x5310 008C<br>0x0000 05F7                | RGMII1_TXC      | 0            | O         | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | MII1_TXCLK      | 2            | I         |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | FSITX1_CLK      | 6            | O         |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO35          | 7            | IO        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP0_INDEX     | 8            | IO        |                                           |                                          |                          |                 |            |          |                  |                |

**Table 5-1. Pin Attributes (ZCZ Package) (continued)**

| BALL<br>NUMBER<br>[1] | BALL NAME [2]/<br>IOMUX<br>REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET [9] | IO<br>VOLTAGE<br>[10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [14] | PULL<br>TYPE<br>[13] |
|-----------------------|----------------------------------------------------------------------------------|-----------------|-----------------|----------|----------------------------------------------------|---------------------------------------------------|-----------------------------------|-----------------------|------------|-------------|---------------------|----------------------|
| M18                   | RGMII1_TX_CTL<br>RGMII1_TX_CTL_CFG_REG<br>0x5310 0090<br>0x0000 05F7             | RGMII1_TX_CTL   | 0               | O        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | RMII1_TX_EN     | 1               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | MII1_TX_EN      | 2               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | FSITX1_DATA0    | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO36          | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | EQEP0_STROBE    | 8               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| U17                   | RGMII1_RD0<br>RGMII1_RD0_CFG_REG<br>0x5310 007C<br>0x0000 05F7                   | RGMII1_RD0      | 0               | I        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | RMII1_RXD0      | 1               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | MII1_RXD0       | 2               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | FSITX0_DATA1    | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO31          | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | EQEP2_STROBE    | 8               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| T17                   | RGMII1_RD1<br>RGMII1_RD1_CFG_REG<br>0x5310 0080<br>0x0000 05F7                   | RGMII1_RD1      | 0               | I        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | RMII1_RXD1      | 1               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | MII1_RXD1       | 2               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | FSIRX0_CLK      | 6               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO32          | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | EQEP2_INDEX     | 8               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| U18                   | RGMII1_RD2<br>RGMII1_RD2_CFG_REG<br>0x5310 0084<br>0x0000 05F7                   | RGMII1_RD2      | 0               | I        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | MII1_RXD2       | 2               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | FSIRX0_DATA0    | 6               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO33          | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | EQEP0_A         | 8               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| T18                   | RGMII1_RD3<br>RGMII1_RD3_CFG_REG<br>0x5310 0088<br>0x0000 05F7                   | RGMII1_RD3      | 0               | I        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | MII1_RXD3       | 2               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | FSIRX0_DATA1    | 6               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO34          | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | EQEP0_B         | 8               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| P16                   | RGMII1_TD0<br>RGMII1_TD0_CFG_REG<br>0x5310 0094<br>0x0000 05F7                   | RGMII1_TD0      | 0               | O        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | RMII1_TXD0      | 1               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | MII1_TXD0       | 2               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | FSITX1_DATA1    | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO37          | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | EQEP1_A         | 8               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |

Table 5-1. Pin Attributes (ZCZ Package) (continued)

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3]        | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET<br>RX/TX/PULL [7] | BALL STATE AFTER RESET<br>RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|------------------------|--------------|----------|-------------------------------------------|------------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| P17             | RGMII1_TD1<br>RGMII1_TD1_CFG_REG<br>0x5310 0098<br>0x0000 05F7                | RGMII1_TD1             | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RMII1_TXD1             | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII1_TXD1              | 2            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | FSIRX1_CLK             | 6            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO38                 | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP1_B                | 8            | I        |                                           |                                          |                          |                 |            |          |                  |                |
| P18             | RGMII1_TD2<br>RGMII1_TD2_CFG_REG<br>0x5310 009C<br>0x0000 05F7                | RGMII1_TD2             | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | RMII1_CRS_DV           | 1            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MII1_TXD2              | 2            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | FSIRX1_DATA0           | 6            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO39                 | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP1_STROBE           | 8            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| N17             | RGMII1_TD3<br>RGMII1_TD3_CFG_REG<br>0x5310 00A0<br>0x0000 05F7                | RGMII1_TD3             | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | MII1_TXD3              | 2            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | FSIRX1_DATA1           | 6            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO40                 | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP1_INDEX            | 8            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| T4              | RSVD_T4                                                                       | RSVD_T4                |              | RSVD     |                                           |                                          |                          |                 | Reserved   |          | Reserved         |                |
| U1              | RSVD_U1                                                                       | RSVD_U1                |              | RSVD     |                                           |                                          |                          |                 | Reserved   |          | Reserved         |                |
| U3              | RSVD_U3                                                                       | RSVD_U3                |              | RSVD     |                                           |                                          |                          |                 | Reserved   |          | Reserved         |                |
| V2              | RSVD_V2                                                                       | RSVD_V2                |              | RSVD     |                                           |                                          |                          |                 | Reserved   |          | Reserved         |                |
| D4              | SAFETY_ERRORn<br>SAFETY_ERRORn_CFG_REG<br>0x5310 0230<br>0x410                | SAFETY_ERRORn          | 0            | OD       | On / Off / Down                           | On / NA / Down                           | 0                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
| B16             | SDFM0_CLK0<br>SDFM0_CLK0_CFG_REG<br>0x5310 01E8<br>0x0000 05F7                | CLKOUT1                | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | GPIO122                | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM0_CLK0             | 8            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EQEP1_STROBE           | 9            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| A16             | SDFM0_CLK1<br>SDFM0_CLK1_CFG_REG<br>0x5310 01F0<br>0x0000 05F7                | PR0_PRU1_GPIO7         | 0            | IO       | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | CPTS0_TS_SYNC          | 1            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | UART5_RTSn             | 2            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | PR0_IEP0_EDC_SYNC_OUT1 | 3            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | I2C3_SDA               | 5            | IOD      |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO124                | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SDFM0_CLK1             | 8            | I        |                                           |                                          |                          |                 |            |          |                  |                |

**Table 5-1. Pin Attributes (ZCZ Package) (continued)**

| BALL<br>NUMBER<br>[1] | BALL NAME [2]/<br>IOMUX<br>REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3]             | MUX<br>MODE [4] | TYPE [5] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET [9] | IO<br>VOLTAGE<br>[10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [14] | PULL<br>TYPE<br>[13] |
|-----------------------|----------------------------------------------------------------------------------|-----------------------------|-----------------|----------|----------------------------------------------------|---------------------------------------------------|-----------------------------------|-----------------------|------------|-------------|---------------------|----------------------|
| B15                   | SDFM0_CLK2<br>SDFM0_CLK2_CFG_REG<br>0x5310 01F8<br>0x0000 05F7                   | UART5_TXD                   | 0               | O        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | I2C3_SCL                    | 5               | IOD      |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPMC0_ADVn_ALE              | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO126                     | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | SDFM0_CLK2                  | 8               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| A15                   | SDFM0_CLK3<br>SDFM0_CLK3_CFG_REG<br>0x5310 0200<br>0x0000 05F7                   | MCAN3_TX                    | 0               | O        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | UART5_RXD                   | 1               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO128                     | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | SDFM0_CLK3                  | 8               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| D14                   | SDFM0_D0<br>SDFM0_D0_CFG_REG<br>0x5310 01EC<br>0x0000 05F7                       | PR0_ECAP0_APWM_OUT          | 0               | O        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | GPIO123                     | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | SDFM0_D0                    | 8               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| D13                   | SDFM0_D1<br>SDFM0_D1_CFG_REG<br>0x5310 01F4<br>0x0000 05F7                       | PR0_PRU1_GPIO17             | 0               | IO       | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | UART5_CTSn                  | 2               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | PR0_IEP0_EDIO_DATA_IN_OUT30 | 3               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO125                     | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | SDFM0_D1                    | 8               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| C13                   | SDFM0_D2<br>SDFM0_D2_CFG_REG<br>0x5310 01FC<br>0x0000 05F7                       | UART5_RXD                   | 0               | I        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | GPIO127                     | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | SDFM0_D2                    | 8               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| C14                   | SDFM0_D3<br>SDFM0_D3_CFG_REG<br>0x5310 0204<br>0x0000 05F7                       | MCAN3_RX                    | 0               | I        | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | GPIO129                     | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | SDFM0_D3                    | 8               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| A11                   | SPI0_CLK<br>SPI0_CLK_CFG_REG<br>0x5310 0030<br>0x0000 05D7                       | SPI0_CLK                    | 0               | IO       | On / Off / Off                                     | On / Off / Off                                    | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | UART3_TXD                   | 1               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | LIN3_TXD                    | 2               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | FSITX0_CLK                  | 6               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO12                      | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | SOP2                        | Bootstrap       | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
| A10                   | SPI1_CLK<br>SPI1_CLK_CFG_REG<br>0x5310 0040<br>0x0000 05F7                       | SPI1_CLK                    | 0               | IO       | Off / Off / Off                                    | Off / Off / Off                                   | 7                                 | 3.3V                  | VDDSHV0    | Yes         | LVCMOS              | PU/PD                |
|                       |                                                                                  | UART4_RXD                   | 1               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | LIN4_RXD                    | 2               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | XBAROUT2                    | 5               | O        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | FSIRX0_CLK                  | 6               | I        |                                                    |                                                   |                                   |                       |            |             |                     |                      |
|                       |                                                                                  | GPIO16                      | 7               | IO       |                                                    |                                                   |                                   |                       |            |             |                     |                      |

Table 5-1. Pin Attributes (ZCZ Package) (continued)

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET RX/TX/PULL [7] | BALL STATE AFTER RESET RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|----------|----------------------------------------|---------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| C11             | SPI0_CS0<br>SPI0_CS0_CFG_REG<br>0x5310 002C<br>0x0000 05F7                    | SPI0_CS0        | 0            | IO       | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART3_RXD       | 1            | I        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | LIN3_RXD        | 2            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO11          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| C10             | SPI0_D0<br>SPI0_D0_CFG_REG<br>0x5310 0034<br>0x0000 05D7                      | SPI0_D0         | 0            | IO       | On / Off / Off                         | On / Off / Off                        | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSITX0_DATA0    | 6            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO13          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | SOP3            | Bootstrap    | I        |                                        |                                       |                          |                 |            |          |                  |                |
| B11             | SPI0_D1<br>SPI0_D1_CFG_REG<br>0x5310 0038<br>0x0000 05F7                      | SPI0_D1         | 0            | IO       | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | FSITX0_DATA1    | 6            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO14          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| C9              | SPI1_CS0<br>SPI1_CS0_CFG_REG<br>0x5310 003C<br>0x0000 05F7                    | SPH_CS0         | 0            | IO       | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART4_TXD       | 1            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | LIN4_TXD        | 2            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | XBAROUT1        | 5            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO15          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| B10             | SPI1_D0<br>SPI1_D0_CFG_REG<br>0x5310 0044<br>0x0000 05F7                      | SPI1_D0         | 0            | IO       | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART5_TXD       | 1            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | XBAROUT3        | 5            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | FSIRX0_DATA0    | 6            | I        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO17          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| D9              | SPI1_D1<br>SPI1_D1_CFG_REG<br>0x5310 0048<br>0x0000 05F7                      | SPH_D1          | 0            | IO       | Off / Off / Off                        | Off / Off / Off                       | 7                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
|                 |                                                                               | UART5_RXD       | 1            | I        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | XBAROUT4        | 5            | O        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | FSIRX0_DATA1    | 6            | I        |                                        |                                       |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO18          | 7            | IO       |                                        |                                       |                          |                 |            |          |                  |                |
| B3              | TCK<br>TCK_CFG_REG<br>0x5310 0240<br>0x210                                    | TCK             | 0            | I        | On / NA / Up                           | On / NA / Up                          | 0                        | 3.3V            | VDDSHV0    | Yes      | HIGH HYST        |                |
| C5              | TDI<br>TDI_CFG_REG<br>0x5310 0234<br>0x6D0                                    | TDI             | 0            | I        | On / Off / Up                          | On / Off / Up                         | 0                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |
| C4              | TDO<br>TDO_CFG_REG<br>0x5310 0238<br>0x630                                    | TDO             | 0            | O        | Off / Off / Up                         | Off / NA / Up                         | 0                        | 3.3V            | VDDSHV0    | Yes      | LVCMOS           | PU/PD          |

**Table 5-1. Pin Attributes (ZCZ Package) (continued)**

| BALL NUMBER [1] | BALL NAME [2]/<br>IOMUX REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL STATE DURING RESET<br>RX/TX/PULL [7] | BALL STATE AFTER RESET<br>RX/TX/PULL [8] | MUX MODE AFTER RESET [9] | IO VOLTAGE [10] | POWER [11] | HYS [12] | BUFFER TYPE [14] | PULL TYPE [13] |
|-----------------|-------------------------------------------------------------------------------|-----------------|--------------|----------|-------------------------------------------|------------------------------------------|--------------------------|-----------------|------------|----------|------------------|----------------|
| D5              | TMS<br>TMS_CFG_REG<br>0x5310 023C<br>0x610                                    | TMS             | 0            | IO       | On / Off / Up                             | On / NA / Up                             | 0                        | 3.3V            | VDDSHV0    | Yes      | LVC MOS          | PU/PD          |
| B7              | UART0_CTSn<br>UART0_CTSn_CFG_REG<br>0x5310 0068<br>0x0000 05F7                | UART0_CTSn      | 0            | I        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVC MOS          | PU/PD          |
|                 |                                                                               | I2C2_SDA        | 1            | IOD      |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SPI3_D1         | 2            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MCAN3_RX        | 3            | I        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SPI0_CS1        | 4            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | XBAROUT10       | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO26          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| C7              | UART0_RTSn<br>UART0_RTSn_CFG_REG<br>0x5310 0064<br>0x0000 05F7                | UART0_RTSn      | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVC MOS          | PU/PD          |
|                 |                                                                               | I2C2_SCL        | 1            | IOD      |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | SPI3_D0         | 2            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | MCAN3_TX        | 3            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | XBAROUT9        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO25          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               |                 |              |          |                                           |                                          |                          |                 |            |          |                  |                |
| A7              | UART0_RXD<br>UART0_RXD_CFG_REG<br>0x5310 006C<br>0x0000 05F7                  | UART0_RXD       | 0            | I        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVC MOS          | PU/PD          |
|                 |                                                                               | LIN0_RXD        | 1            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO27          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| A6              | UART0_TXD<br>UART0_TXD_CFG_REG<br>0x5310 0070<br>0x0000 05F7                  | UART0_TXD       | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVC MOS          | PU/PD          |
|                 |                                                                               | LIN0_TXD        | 1            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO28          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| L3              | UART1_RXD<br>UART1_RXD_CFG_REG<br>0x5310 012C<br>0x0000 05F7                  | UART1_RXD       | 0            | I        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVC MOS          | PU/PD          |
|                 |                                                                               | LIN1_RXD        | 1            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM16_A        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD6       | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO75          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
| M3              | UART1_TXD<br>UART1_TXD_CFG_REG<br>0x5310 0130<br>0x0000 05F7                  | UART1_TXD       | 0            | O        | Off / Off / Off                           | Off / Off / Off                          | 7                        | 3.3V            | VDDSHV0    | Yes      | LVC MOS          | PU/PD          |
|                 |                                                                               | LIN1_TXD        | 1            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | EPWM16_B        | 5            | O        |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPMC0_AD7       | 6            | IO       |                                           |                                          |                          |                 |            |          |                  |                |
|                 |                                                                               | GPIO76          | 7            | IO       |                                           |                                          |                          |                 |            |          |                  |                |

**Table 5-1. Pin Attributes (ZCZ Package) (continued)**

| BALL<br>NUMBER<br>[1]                                                                                   | BALL NAME [2]/<br>IOMUX<br>REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET [9] | IO<br>VOLTAGE<br>[10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [14] | PULL<br>TYPE<br>[13] |
|---------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|-----------------|-----------------|----------|----------------------------------------------------|---------------------------------------------------|-----------------------------------|-----------------------|------------|-------------|---------------------|----------------------|
| E11, E9,<br>F11, F9,<br>G13, G14,<br>G5, G6,<br>J16, K13,<br>K14, K5,<br>K6, N13,<br>N14, N5,<br>N6, R9 | VDD                                                                              | VDD             |                 | PWR      |                                                    |                                                   |                                   | 1.2V                  |            |             |                     |                      |
| R11, R8                                                                                                 | VDDA18                                                                           | VDDA18          |                 | PWR      |                                                    |                                                   |                                   | 1.8V                  |            |             |                     |                      |
| R6                                                                                                      | VDDA18_LDO                                                                       | VDDA18_LDO      |                 | PWR      |                                                    |                                                   |                                   | 1.8V                  |            |             |                     |                      |
| R4                                                                                                      | VDDA18_OSC_PLL                                                                   | VDDA18_OSC_PLL  |                 | PWR      |                                                    |                                                   |                                   | 1.8V                  |            |             |                     |                      |
| P11, P7,<br>P9                                                                                          | VDDA33                                                                           | VDDA33          |                 | PWR      |                                                    |                                                   |                                   | 3.3V                  |            |             |                     |                      |
| J15                                                                                                     | VDDAR1                                                                           | VDDAR1          |                 | PWR      |                                                    |                                                   |                                   | 1.2V                  |            |             |                     |                      |
| D10                                                                                                     | VDDAR2                                                                           | VDDAR2          |                 | PWR      |                                                    |                                                   |                                   | 1.2V                  |            |             |                     |                      |
| H3                                                                                                      | VDDAR3                                                                           | VDDAR3          |                 | PWR      |                                                    |                                                   |                                   | 1.2V                  |            |             |                     |                      |
| D6, E15,<br>L4, N15                                                                                     | VDDS18                                                                           | VDDS18          |                 | PWR      |                                                    |                                                   |                                   | 1.8V                  |            |             |                     |                      |
| T3                                                                                                      | VDDS18_LDO                                                                       | VDDS18_LDO      |                 | PWR      |                                                    |                                                   |                                   | 1.8V                  |            |             |                     |                      |
| D12, D8,<br>H15, H4,<br>L15, P4,<br>R15                                                                 | VDDS33                                                                           | VDDS33          |                 | PWR      |                                                    |                                                   |                                   | 3.3V                  |            |             |                     |                      |
| N3                                                                                                      | VPP                                                                              | VPP             |                 | PWR      |                                                    |                                                   |                                   | VPP                   |            |             |                     |                      |

**Table 5-1. Pin Attributes (ZCZ Package) (continued)**

| BALL<br>NUMBER<br>[1]                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | BALL NAME [2]/<br>IOMUX<br>REGISTER [15]/<br>ADDRESS [16]/<br>DEFAULT VALUE [17] | SIGNAL NAME [3] | MUX<br>MODE [4] | TYPE [5] | BALL<br>STATE<br>DURING<br>RESET<br>RX/TX/PULL [7] | BALL<br>STATE<br>AFTER<br>RESET<br>RX/TX/PULL [8] | MUX<br>MODE<br>AFTER<br>RESET [9] | IO<br>VOLTAGE<br>[10] | POWER [11] | HYS<br>[12] | BUFFER<br>TYPE [14] | PULL<br>TYPE<br>[13] |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|-----------------|-----------------|----------|----------------------------------------------------|---------------------------------------------------|-----------------------------------|-----------------------|------------|-------------|---------------------|----------------------|
| A1, A18,<br>E10, E12,<br>E13, E14,<br>E5, E6,<br>E7, E8,<br>F10, F12,<br>F13, F14,<br>F5, F6, F7,<br>F8, G10,<br>G11, G12,<br>G7, G8,<br>G9, H10,<br>H11, H12,<br>H13, H14,<br>H5, H6,<br>H7, H8,<br>H9, J10,<br>J11, J12,<br>J13, J14,<br>J5, J6, J7,<br>J8, J9,<br>K10, K11,<br>K12, K7,<br>K8, K9,<br>L10, L11,<br>L12, L13,<br>L14, L5,<br>L6, L7, L8,<br>L9, M10,<br>M11, M12,<br>M13, M14,<br>M5, M6,<br>M7, M8,<br>M9, N10,<br>N11, N12,<br>N7, N8,<br>N9, P13,<br>P14, P5,<br>T2, V18 | VSS                                                                              | VSS             |                 | GND      |                                                    |                                                   |                                   | VSS                   |            |             |                     |                      |
| P10, P12,<br>P6, P8,<br>R13, R5,<br>V1, V16                                                                                                                                                                                                                                                                                                                                                                                                                                                   | VSSA                                                                             | VSSA            |                 | AGND     |                                                    |                                                   |                                   | VSSA                  |            |             |                     |                      |
| U2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | VSYS_MON                                                                         | VSYS_MON        |                 | PWR      |                                                    |                                                   |                                   | 0.9V                  | VDDA_CIO   |             | AnalogCIO           |                      |
| C3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | WARMRSTn<br>WARMRSTn_CFG_REG<br>0x5310 022C<br>0x510                             | WARMRSTn        | 0               | IO       | On / Off / Off                                     | On / NA / Off                                     | 0                                 | 3.3V                  | VDDSHV0    |             | FS OD               |                      |
| T1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | XTAL_XI                                                                          | XTAL_XI         |                 | I        |                                                    |                                                   | 0                                 | 1.8V                  | VDDS_OSC   | Yes         | HFOSC               |                      |
| R1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | XTAL_XO                                                                          | XTAL_XO         |                 | O        |                                                    |                                                   | 0                                 | 1.8V                  | VDDS_OSC   |             | HFOSC               |                      |

## 5.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

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### Note

Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via IOMUX pad configuration registers. Some device subsystems provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

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2. **PIN TYPE:** Signal direction and type:

- I = Input
- O = Output
- IO = Input, Output, or simultaneously Input and Output
- ID = Input with open-drain output function
- OD = Output, with open-drain output function
- IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
- IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
- OZ = Output with three-state output function
- A = Analog
- CAP = LDO capacitor
- PWR = Power
- GND = Ground

3. **DESCRIPTION:** Description of the signal

4. **BALL:** Associated ball number

For more information on the I/O cell configurations, see the *Pad Configuration Registers* section within the *Device Configuration* chapter of the device TRM.

### 5.3.1 ADC

**Table 5-2. ADC0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                         | ZCZ PIN [4] |
|-----------------|--------------|---------------------------------------------------------|-------------|
| ADC0_AIN0       | I            | ADC Analog Input 0 (+IN0)<br>CMPSSA0: inH (+IN)         | V15         |
| ADC0_AIN1       | I            | ADC Analog Input 1 (-IN0)<br>CMPSSA0: inL (-IN)         | U15         |
| ADC0_AIN2       | I            | ADC Analog Input 2 (+IN1)<br>CMPSSA1: inH (+IN)         | T14         |
| ADC0_AIN3       | I            | ADC Analog Input 3 (-IN1)<br>CMPSSA1: inL (-IN)         | U14         |
| ADC0_AIN4       | I            | ADC Analog Input 4 (+IN2)<br>CMPSSB0: inH/inL (+IN/-IN) | U13         |
| ADC0_AIN5       | I            | ADC Analog Input 5 (-IN2)<br>CMPSSB1: inH/inL (+IN/-IN) | R14         |

**Table 5-3. ADC1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                         | ZCZ PIN [4] |
|-----------------|--------------|---------------------------------------------------------|-------------|
| ADC1_AIN0       | I            | ADC Analog Input 0 (+IN0)<br>CMPSSA2: inH (+IN)         | T11         |
| ADC1_AIN1       | I            | ADC Analog Input 1 (-IN0)<br>CMPSSA2: inL (-IN)         | U11         |
| ADC1_AIN2       | I            | ADC Analog Input 2 (+IN1)<br>CMPSSA3: inH (+IN)         | T12         |
| ADC1_AIN3       | I            | ADC Analog Input 3 (-IN1)<br>CMPSSA3: inL (-IN)         | V12         |
| ADC1_AIN4       | I            | ADC Analog Input 4 (+IN2)<br>CMPSSB2: inH/inL (+IN/-IN) | U12         |
| ADC1_AIN5       | I            | ADC Analog Input 5 (-IN2)<br>CMPSSB3: inH/inL (+IN/-IN) | R12         |

**Table 5-4. ADC2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                         | ZCZ PIN [4] |
|-----------------|--------------|---------------------------------------------------------|-------------|
| ADC2_AIN0       | I            | ADC Analog Input 0 (+IN0)<br>CMPSSA4: inH (+IN)         | R10         |
| ADC2_AIN1       | I            | ADC Analog Input 1 (-IN0)<br>CMPSSA4: inL (-IN)         | T10         |
| ADC2_AIN2       | I            | ADC Analog Input 2 (+IN1)<br>CMPSSA5: inH (+IN)         | U10         |
| ADC2_AIN3       | I            | ADC Analog Input 3 (-IN1)<br>CMPSSA5: inL (-IN)         | T9          |
| ADC2_AIN4       | I            | ADC Analog Input 4 (+IN2)<br>CMPSSB4: inH/inL (+IN/-IN) | V9          |
| ADC2_AIN5       | I            | ADC Analog Input 5 (-IN2)<br>CMPSSB5: inH/inL (+IN/-IN) | T8          |

**Table 5-5. ADC3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                 | ZCZ PIN [4] |
|-----------------|--------------|-------------------------------------------------|-------------|
| ADC3_AIN0       | I            | ADC Analog Input 0 (+IN0)<br>CMPSSA6: inH (+IN) | U7          |
| ADC3_AIN1       | I            | ADC Analog Input 1 (-IN0)<br>CMPSSA6: inL (-IN) | U8          |

**Table 5-5. ADC3 Signal Descriptions (continued)**

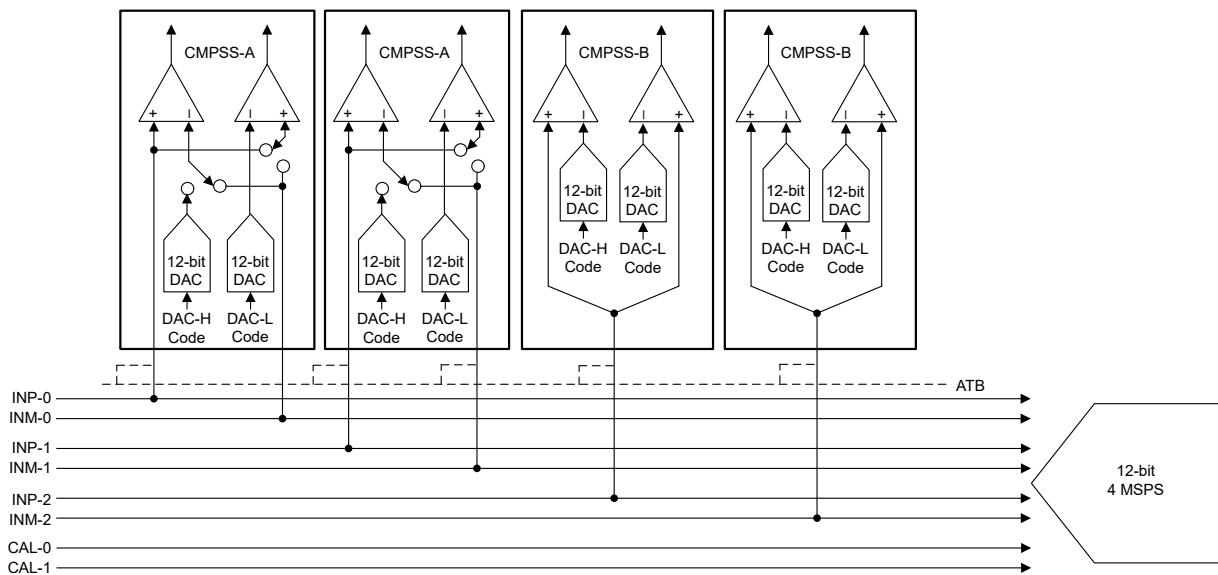
| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                         | ZCZ PIN [4] |
|-----------------|--------------|---------------------------------------------------------|-------------|
| ADC3_AIN2       | I            | ADC Analog Input 2 (+IN1)<br>CMPSSA7: inH (+IN)         | T7          |
| ADC3_AIN3       | I            | ADC Analog Input 3 (-IN1)<br>CMPSSA7: inL (-IN)         | R7          |
| ADC3_AIN4       | I            | ADC Analog Input 4 (+IN2)<br>CMPSSB6: inH/inL (+IN/-IN) | V8          |
| ADC3_AIN5       | I            | ADC Analog Input 5 (-IN2)<br>CMPSSB7: inH/inL (+IN/-IN) | U9          |

**Table 5-6. ADC4 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                         | ZCZ PIN [4] |
|-----------------|--------------|---------------------------------------------------------|-------------|
| ADC4_AIN0       | I            | ADC Analog Input 0 (+IN0)<br>CMPSSA8: inH (+IN)         | U6          |
| ADC4_AIN1       | I            | ADC Analog Input 1 (-IN0)<br>CMPSSA8: inL (-IN)         | V5          |
| ADC4_AIN2       | I            | ADC Analog Input 2 (+IN1)<br>CMPSSA9: inH (+IN)         | V4          |
| ADC4_AIN3       | I            | ADC Analog Input 3 (-IN1)<br>CMPSSA9: inL (-IN)         | U5          |
| ADC4_AIN4       | I            | ADC Analog Input 4 (+IN2)<br>CMPSSB8: inH/inL (+IN/-IN) | V3          |
| ADC4_AIN5       | I            | ADC Analog Input 5 (-IN2)<br>CMPSSB9: inH/inL (+IN/-IN) | U4          |

### 5.3.1.1 ADC-CMPSS Signal Connections

In each ADC, two sets of differential pins shall be shared with pins of two CMPSSA and remaining one pair of differential pins shall be connected to two independent pins of CMPSSB. These pins are demonstrated in [Figure 5-1](#) and [Table 5-7](#) where the CHSEL values determine how the inputs are fed into ADC.



**Figure 5-1. CMPSS and ADC Connections**

**Table 5-7. Connectivity between ADC Inputs to CMPSS Signals**

| Signal/Pin Name | ADC Input        | CMPSS Input               |
|-----------------|------------------|---------------------------|
| ADC0 Channels   |                  |                           |
| ADC0_AIN0       | ADC0:inp0 (+IN0) | CMPSSA0:inH (+IN)         |
| ADC0_AIN1       | ADC0:inm0 (-IN0) | CMPSSA0:inL (-IN)         |
| ADC0_AIN2       | ADC0:inp1 (+IN1) | CMPSSA1:inH (+IN)         |
| ADC0_AIN3       | ADC0:inm1 (-IN1) | CMPSSA1:inL (-IN)         |
| ADC0_AIN4       | ADC0:inp2 (+IN2) | CMPSSB0:inH/inL (+IN/-IN) |
| ADC0_AIN5       | ADC0:inm2 (-IN2) | CMPSSB1:inH/inL (+IN/-IN) |
| ADC_CAL1        | ADC0:inm3 (-IN3) | X                         |
| ADC_CAL0        | ADC0:inp3 (+IN3) | X                         |
| ADC1 Channels   |                  |                           |
| ADC1_AIN0       | ADC1:inp0 (+IN0) | CMPSSA2:inH (+IN)         |
| ADC1_AIN1       | ADC1:inm0 (-IN0) | CMPSSA2:inL (-IN)         |
| ADC1_AIN2       | ADC1:inp1 (+IN1) | CMPSSA3:inH (+IN)         |
| ADC1_AIN3       | ADC1:inm1 (-IN1) | CMPSSA3:inL (-IN)         |
| ADC1_AIN4       | ADC1:inp2 (+IN2) | CMPSSB2:inH/inL (+IN/-IN) |
| ADC1_AIN5       | ADC1:inm2 (-IN2) | CMPSSB3:inH/inL (+IN/-IN) |
| ADC_CAL1        | ADC1:inm3 (-IN3) | X                         |
| ADC_CAL0        | ADC1:inp3 (+IN3) | X                         |
| ADC2 Channels   |                  |                           |
| ADC2_AIN0       | ADC2:inp0 (+IN0) | CMPSSA4:inH (+IN)         |
| ADC2_AIN1       | ADC2:inm0 (-IN0) | CMPSSA4:inL (-IN)         |
| ADC2_AIN2       | ADC2:inp1 (+IN1) | CMPSSA5:inH (+IN)         |
| ADC2_AIN3       | ADC2:inm1 (-IN1) | CMPSSA5:inL (-IN)         |
| ADC2_AIN4       | ADC2:inp2 (+IN2) | CMPSSB4:inH/inL (+IN/-IN) |
| ADC2_AIN5       | ADC2:inm2 (-IN2) | CMPSSB5:inH/inL (+IN/-IN) |
| ADC_CAL1        | ADC2:inm3 (-IN3) | X                         |
| ADC_CAL0        | ADC2:inp3 (+IN3) | X                         |
| ADC3 Channels   |                  |                           |
| ADC3_AIN0       | ADC3:inp0 (+IN0) | CMPSSA6:inH (+IN)         |
| ADC3_AIN1       | ADC3:inm0 (-IN0) | CMPSSA6:inL (-IN)         |
| ADC3_AIN2       | ADC3:inp1 (+IN1) | CMPSSA7:inH (+IN)         |
| ADC3_AIN3       | ADC3:inm1 (-IN1) | CMPSSA7:inL (-IN)         |
| ADC3_AIN4       | ADC3:inp2 (+IN2) | CMPSSB6:inH/inL (+IN/-IN) |
| ADC3_AIN5       | ADC3:inm2 (-IN2) | CMPSSB7:inH/inL (+IN/-IN) |
| ADC_CAL1        | ADC3:inm3 (-IN3) | X                         |
| ADC_CAL0        | ADC3:inp3 (+IN3) | X                         |
| ADC4 Channels   |                  |                           |
| ADC4_AIN0       | ADC4:inp0 (+IN0) | CMPSSA8:inH (+IN)         |
| ADC4_AIN1       | ADC4:inm0 (-IN0) | CMPSSA8:inL (-IN)         |
| ADC4_AIN2       | ADC4:inp1 (+IN1) | CMPSSA9:inH (+IN)         |
| ADC4_AIN3       | ADC4:inm1 (-IN1) | CMPSSA9:inL (-IN)         |
| ADC4_AIN4       | ADC4:inp2 (+IN2) | CMPSSB8:inH/inL (+IN/-IN) |
| ADC4_AIN5       | ADC4:inm2 (-IN2) | CMPSSB9:inH/inL (+IN/-IN) |
| ADC_CAL0        | ADC4:inp3 (+IN3) | X                         |
| ADC_CAL1        | ADC4:inm3 (-IN3) | X                         |

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**Note**

In the **ADC Input** column in [ADC-CMPSS Signal Connectivity Table](#) above, "inp" stands for positive inputs and "inm" stands for negative inputs.

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### 5.3.2 ADC\_CAL

**Table 5-8. ADC\_CAL Signal Descriptions**

| SIGNAL NAME [1]         | PIN TYPE [2] | DESCRIPTION [3]       | ZCZ PIN [4] |
|-------------------------|--------------|-----------------------|-------------|
| ADC_CAL0 <sup>(1)</sup> | I            | ADC Calibration Pin 0 | U16         |
| ADC_CAL1 <sup>(1)</sup> | I            | ADC Calibration Pin 1 | T15         |

(1) This pin is shared between ADC[0:4].

### 5.3.3 ADC\_VREF

**Table 5-9. ADC\_VREF Signal Descriptions**

| SIGNAL NAME [1] <sup>(5)</sup> | PIN TYPE [2] | DESCRIPTION [3]          | ZCZ PIN [4] |
|--------------------------------|--------------|--------------------------|-------------|
| ADC_VREFHI_G0                  | A            | ADC Reference (Positive) | V14         |
| ADC_VREFHI_G1 <sup>(2)</sup>   | A            | ADC Reference (Positive) | V10         |
| ADC_VREFHI_G2                  | A            | ADC Reference (Positive) | V6          |
| ADC_VREFLO_G0 <sup>(1)</sup>   | A            | ADC Reference (Negative) | V13         |
| ADC_VREFLO_G1 <sup>(3)</sup>   | A            | ADC Reference (Negative) | V11         |
| ADC_VREFLO_G2 <sup>(4)</sup>   | A            | ADC Reference (Negative) | V7          |

(1) This pin should be connected (shorted) to analog ground (VSSA).

(2) This pin can be connected (shorted) to ADC\_VREFHI\_G0.

(3) This pin can be connected (shorted) to ADC\_VREFLO\_G0.

(4) This pin can be connected (shorted) to analog ground (VSSA).

(5) See the *Layout Guidelines* section and Hardware Design Guideline ([SPRABJ8](#)) for additional details on connecting these pins.

### 5.3.4 CPSW

**Table 5-10. CPSW0 RGMII1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]        | ZCZ PIN [4] |
|-----------------|--------------|------------------------|-------------|
| RGMII1_RXC      | I            | RGMII Receive Clock    | R17         |
| RGMII1_RX_CTL   | I            | RGMII Receive Control  | R18         |
| RGMII1_TXC      | O            | RGMII Transmit Clock   | N18         |
| RGMII1_TX_CTL   | O            | RGMII Transmit Control | M18         |
| RGMII1_RD0      | I            | RGMII Receive Data 0   | U17         |
| RGMII1_RD1      | I            | RGMII Receive Data 1   | T17         |
| RGMII1_RD2      | I            | RGMII Receive Data 2   | U18         |
| RGMII1_RD3      | I            | RGMII Receive Data 3   | T18         |
| RGMII1_TD0      | O            | RGMII Transmit Data 0  | P16         |
| RGMII1_TD1      | O            | RGMII Transmit Data 1  | P17         |
| RGMII1_TD2      | O            | RGMII Transmit Data 2  | P18         |
| RGMII1_TD3      | O            | RGMII Transmit Data 3  | N17         |

**Table 5-11. CPSW0 RGMII2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]        | ZCZ PIN [4] |
|-----------------|--------------|------------------------|-------------|
| RGMII2_RXC      | I            | RGMII Receive Clock    | K15         |
| RGMII2_RX_CTL   | I            | RGMII Receive Control  | K16         |
| RGMII2_TXC      | O            | RGMII Transmit Clock   | H18         |
| RGMII2_TX_CTL   | O            | RGMII Transmit Control | L16         |
| RGMII2_RD0      | I            | RGMII Receive Data 0   | K17         |
| RGMII2_RD1      | I            | RGMII Receive Data 1   | K18         |
| RGMII2_RD2      | I            | RGMII Receive Data 2   | J18         |
| RGMII2_RD3      | I            | RGMII Receive Data 3   | J17         |

**Table 5-11. CPSW0 RGMII2 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]       | ZCZ PIN [4] |
|-----------------|--------------|-----------------------|-------------|
| RGMII2_TD0      | O            | RGMII Transmit Data 0 | M16         |
| RGMII2_TD1      | O            | RGMII Transmit Data 1 | M15         |
| RGMII2_TD2      | O            | RGMII Transmit Data 2 | H17         |
| RGMII2_TD3      | O            | RGMII Transmit Data 3 | H16         |

**Table 5-12. CPSW0 RMII1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                 | ZCZ PIN [4] |
|-----------------|--------------|---------------------------------|-------------|
| RMII1_CRS_DV    | I            | RMII Carrier Sense / Data Valid | P18         |
| RMII1_REF_CLK   | IO           | RMII Reference Clock            | R17         |
| RMII1_RX_ER     | I            | RMII Receive Data Error         | R18         |
| RMII1_TX_EN     | O            | RMII Transmit Enable            | M18         |
| RMII1_RXD0      | I            | RMII Receive Data 0             | U17         |
| RMII1_RXD1      | I            | RMII Receive Data 1             | T17         |
| RMII1_TXD0      | O            | RMII Transmit Data 0            | P16         |
| RMII1_TXD1      | O            | RMII Transmit Data 1            | P17         |

**Table 5-13. CPSW0 RMII2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                 | ZCZ PIN [4] |
|-----------------|--------------|---------------------------------|-------------|
| RMII2_CRS_DV    | I            | RMII Carrier Sense / Data Valid | G18         |
| RMII2_REF_CLK   | IO           | RMII Reference Clock            | K15         |
| RMII2_RX_ER     | I            | RMII Receive Data Error         | G17         |
| RMII2_TX_EN     | O            | RMII Transmit Enable            | L16         |
| RMII2_RXD0      | I            | RMII Receive Data 0             | K17         |
| RMII2_RXD1      | I            | RMII Receive Data 1             | K18         |
| RMII2_TXD0      | O            | RMII Transmit Data 0            | M16         |
| RMII2_TXD1      | O            | RMII Transmit Data 1            | M15         |

**Table 5-14. CPSW0 MII1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]        | ZCZ PIN [4] |
|-----------------|--------------|------------------------|-------------|
| MII1_COL        | I            | MII Collision Detected | P15         |
| MII1_CRS        | I            | MII Carrier Sense      | R16         |
| MII1_RXCLK      | I            | MII Receive Clock      | R17         |
| MII1_RXDV       | I            | MII Receive Data Valid | R18         |
| MII1_RX_ER      | I            | MII Receive Data Error | T16         |
| MII1_TXCLK      | I            | MII Transmit Clock     | N18         |
| MII1_TX_EN      | O            | MII Transmit Enable    | M18         |
| MII1_RXD0       | I            | MII Receive Data 0     | U17         |
| MII1_RXD1       | I            | MII Receive Data 1     | T17         |
| MII1_RXD2       | I            | MII Receive Data 2     | U18         |
| MII1_RXD3       | I            | MII Receive Data 3     | T18         |
| MII1_TXD0       | O            | MII Transmit Data 0    | P16         |
| MII1_TXD1       | O            | MII Transmit Data 1    | P17         |
| MII1_TXD2       | O            | MII Transmit Data 2    | P18         |
| MII1_TXD3       | O            | MII Transmit Data 3    | N17         |

**Table 5-15. CPSW0 MII2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]        | ZCZ PIN [4] |
|-----------------|--------------|------------------------|-------------|
| MII2_COL        | I            | MII Collision Detected | F17         |
| MII2_CRS        | I            | MII Carrier Sense      | G18         |
| MII2_RXCLK      | I            | MII Receive Clock      | K15         |
| MII2_RXDV       | I            | MII Receive Data Valid | K16         |
| MII2_RX_ER      | I            | MII Receive Error      | G17         |
| MII2_TXCLK      | I            | MII Transmit Clock     | H18         |
| MII2_TX_EN      | O            | MII Transmit Enable    | L16         |
| MII2_RXD0       | I            | MII Receive Data 0     | K17         |
| MII2_RXD1       | I            | MII Receive Data 1     | K18         |
| MII2_RXD2       | I            | MII Receive Data 2     | J18         |
| MII2_RXD3       | I            | MII Receive Data 3     | J17         |
| MII2_TXD0       | O            | MII Transmit Data 0    | M16         |
| MII2_TXD1       | O            | MII Transmit Data 1    | M15         |
| MII2_TXD2       | O            | MII Transmit Data 2    | H17         |
| MII2_TXD3       | O            | MII Transmit Data 3    | H16         |

**Table 5-16. MDIO0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MDIO0_MDC       | O            | MDIO Clock      | M17         |
| MDIO0_MDIO      | IO           | MDIO Data       | N16         |

### 5.3.5 CPTS

**Table 5-17. CPTS0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                    | ZCZ PIN [4] |
|-----------------|--------------|------------------------------------|-------------|
| CPTS0_TS_SYNC   | O            | CPTS Time Stamp Counter Bit Output | A16         |

### 5.3.6 DAC

**Table 5-18. DAC Signal Descriptions**

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]         | ZCZ PIN [4] |
|-------------------|--------------|-------------------------|-------------|
| DAC_OUT           | O            | DAC Output              | T5          |
| DAC_VREF0 (1) (2) | A            | DAC Voltage Reference 0 | T13         |
| DAC_VREF1 (1) (2) | A            | DAC Voltage Reference 1 | T6          |

(1) See the *Layout Guidelines* sections for details on connecting these pins.

(2) This pin can be connected (shorted) to VDDA18\_LDO.

### 5.3.7 Emulation and Debug

**Table 5-19. Trace Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| TRC_CLK         | O            | Trace Clock     | D15         |
| TRC_CTL         | O            | Trace Control   | C15         |
| TRC_DATA0       | O            | Trace Data 0    | F15         |
| TRC_DATA1       | O            | Trace Data 1    | C18         |
| TRC_DATA2       | O            | Trace Data 2    | D17         |
| TRC_DATA3       | O            | Trace Data 3    | D18         |
| TRC_DATA4       | O            | Trace Data 4    | E16         |

**Table 5-19. Trace Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| TRC_DATA5       | O            | Trace Data 5    | F16         |
| TRC_DATA6       | O            | Trace Data 6    | F18         |
| TRC_DATA7       | O            | Trace Data 7    | G16         |
| TRC_DATA8       | O            | Trace Data 8    | E17         |
| TRC_DATA9       | O            | Trace Data 9    | E18         |
| TRC_DATA10      | O            | Trace Data 10   | C16         |
| TRC_DATA11      | O            | Trace Data 11   | A17         |
| TRC_DATA12      | O            | Trace Data 12   | B18         |
| TRC_DATA13      | O            | Trace Data 13   | B17         |
| TRC_DATA14      | O            | Trace Data 14   | D16         |
| TRC_DATA15      | O            | Trace Data 15   | C17         |

**Table 5-20. JTAG Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]             | ZCZ PIN [4] |
|-----------------|--------------|-----------------------------|-------------|
| TCK             | I            | JTAG Test Clock Input       | B3          |
| TDI             | I            | JTAG Test Data Input        | C5          |
| TDO             | O            | JTAG Test Data Output       | C4          |
| TMS             | IO           | JTAG Test Mode Select Input | D5          |

### 5.3.8 EPWM

**Table 5-21. EPWM0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM0_A         | O            | EPWM Output A   | B2          |
| EPWM0_B         | O            | EPWM Output B   | B1          |

**Table 5-22. EPWM1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM1_A         | O            | EPWM Output A   | D3          |
| EPWM1_B         | O            | EPWM Output B   | D2          |

**Table 5-23. EPWM2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM2_A         | O            | EPWM Output A   | C2          |
| EPWM2_B         | O            | EPWM Output B   | C1          |

**Table 5-24. EPWM3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM3_A         | O            | EPWM Output A   | E2          |
| EPWM3_B         | O            | EPWM Output B   | E3          |

**Table 5-25. EPWM4 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM4_A         | O            | EPWM Output A   | D1          |
| EPWM4_B         | O            | EPWM Output B   | E4          |

**Table 5-26. EPWM5 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM5_A         | O            | EPWM Output A   | F2          |
| EPWM5_B         | O            | EPWM Output B   | G2          |

**Table 5-27. EPWM6 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM6_A         | O            | EPWM Output A   | E1          |
| EPWM6_B         | O            | EPWM Output B   | F3          |

**Table 5-28. EPWM7 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM7_A         | O            | EPWM Output A   | F4          |
| EPWM7_B         | O            | EPWM Output B   | F1          |

**Table 5-29. EPWM8 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM8_A         | O            | EPWM Output A   | G3          |
| EPWM8_B         | O            | EPWM Output B   | H2          |

**Table 5-30. EPWM9 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM9_A         | O            | EPWM Output A   | G1          |
| EPWM9_B         | O            | EPWM Output B   | J2          |

**Table 5-31. EPWM10 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM10_A        | O            | EPWM Output A   | G4          |
| EPWM10_B        | O            | EPWM Output B   | J3          |

**Table 5-32. EPWM11 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM11_A        | O            | EPWM Output A   | H1          |
| EPWM11_B        | O            | EPWM Output B   | J1          |

**Table 5-33. EPWM12 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM12_A        | O            | EPWM Output A   | K2          |
| EPWM12_B        | O            | EPWM Output B   | J4          |

**Table 5-34. EPWM13 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM13_A        | O            | EPWM Output A   | K4          |
| EPWM13_B        | O            | EPWM Output B   | K3          |

**Table 5-35. EPWM14 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM14_A        | O            | EPWM Output A   | V17         |

**Table 5-35. EPWM14 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM14_B        | O            | EPWM Output B   | T16         |

**Table 5-36. EPWM15 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM15_A        | O            | EPWM Output A   | P15         |
| EPWM15_B        | O            | EPWM Output B   | R16         |

**Table 5-37. EPWM16 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM16_A        | O            | EPWM Output A   | L3          |
| EPWM16_B        | O            | EPWM Output B   | M3          |

**Table 5-38. EPWM17 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM17_A        | O            | EPWM Output A   | B6          |
| EPWM17_B        | O            | EPWM Output B   | A4          |

**Table 5-39. EPWM18 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM18_A        | O            | EPWM Output A   | B5          |
| EPWM18_B        | O            | EPWM Output B   | B4          |

**Table 5-40. EPWM19 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM19_A        | O            | EPWM Output A   | A3          |
| EPWM19_B        | O            | EPWM Output B   | A2          |

**Table 5-41. EPWM20 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM20_A        | O            | EPWM Output A   | C6          |
| EPWM20_B        | O            | EPWM Output B   | A5          |

**Table 5-42. EPWM21 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM21_A        | O            | EPWM Output A   | L17         |
| EPWM21_B        | O            | EPWM Output B   | L18         |

**Table 5-43. EPWM22 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM22_A        | O            | EPWM Output A   | G17         |
| EPWM22_B        | O            | EPWM Output B   | F17         |

**Table 5-44. EPWM23 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM23_A        | O            | EPWM Output A   | G18         |

**Table 5-44. EPWM23 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM23_B        | O            | EPWM Output B   | G15         |

**Table 5-45. EPWM24 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM24_A        | O            | EPWM Output A   | K15         |
| EPWM24_B        | O            | EPWM Output B   | K16         |

**Table 5-46. EPWM25 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM25_A        | O            | EPWM Output A   | K17         |
| EPWM25_B        | O            | EPWM Output B   | K18         |

**Table 5-47. EPWM26 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM26_A        | O            | EPWM Output A   | J18         |
| EPWM26_B        | O            | EPWM Output B   | J17         |

**Table 5-48. EPWM27 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM27_A        | O            | EPWM Output A   | H18         |
| EPWM27_B        | O            | EPWM Output B   | L16         |

**Table 5-49. EPWM28 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM28_A        | O            | EPWM Output A   | M16         |
| EPWM28_B        | O            | EPWM Output B   | M15         |

**Table 5-50. EPWM29 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM29_A        | O            | EPWM Output A   | H17         |
| EPWM29_B        | O            | EPWM Output B   | H16         |

**Table 5-51. EPWM30 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM30_A        | O            | EPWM Output A   | F15         |
| EPWM30_B        | O            | EPWM Output B   | C18         |

**Table 5-52. EPWM31 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EPWM31_A        | O            | EPWM Output A   | D17         |
| EPWM31_B        | O            | EPWM Output B   | D18         |

**5.3.9 EQEP****Table 5-53. EQEP0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]         | ZCZ PIN [4] |
|-----------------|--------------|-------------------------|-------------|
| EQEP0_A         | I            | EQEP Quadrature Input A | B14, U18    |

**Table 5-53. EQEP0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]         | ZCZ PIN [4] |
|-----------------|--------------|-------------------------|-------------|
| EQEP0_B         | I            | EQEP Quadrature Input B | A14, T18    |
| EQEP0_INDEX     | IO           | EQEP Index              | D11, N18    |
| EQEP0_STROBE    | IO           | EQEP Strobe             | C12, M18    |

**Table 5-54. EQEP1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]         | ZCZ PIN [4] |
|-----------------|--------------|-------------------------|-------------|
| EQEP1_A         | I            | EQEP Quadrature Input A | D15, P16    |
| EQEP1_B         | I            | EQEP Quadrature Input B | C15, P17    |
| EQEP1_INDEX     | IO           | EQEP Index              | N17, P2     |
| EQEP1_STROBE    | IO           | EQEP Strobe             | B16, P18    |

**Table 5-55. EQEP2 Signal Descriptions**

| SIGNAL NAME [1]        | PIN TYPE [2] | DESCRIPTION [3]         | ZCZ PIN [4] |
|------------------------|--------------|-------------------------|-------------|
| EQEP2_A <sup>(1)</sup> | I            | EQEP Quadrature Input A | B13, R17    |
| EQEP2_B <sup>(2)</sup> | I            | EQEP Quadrature Input B | A13, R18    |
| EQEP2_INDEX            | IO           | EQEP Index              | A12, T17    |
| EQEP2_STROBE           | IO           | EQEP Strobe             | B12, U17    |

(1) EQEP2\_A is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer when using ball B13.

(2) EQEP2\_B is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer when using ball A13.

### 5.3.10 FSI

**Table 5-56. FSIRX0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSIRX0_CLK      | I            | FSI Clock       | A10, T17    |
| FSIRX0_DATA0    | I            | FSI Data 0      | B10, U18    |
| FSIRX0_DATA1    | I            | FSI Data 1      | D9, T18     |

**Table 5-57. FSIRX1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSIRX1_CLK      | I            | FSI Clock       | E1, P17     |
| FSIRX1_DATA0    | I            | FSI Data 0      | F3, P18     |
| FSIRX1_DATA1    | I            | FSI Data 1      | F4, N17     |

**Table 5-58. FSIRX2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSIRX2_CLK      | I            | FSI Clock       | G16, J2     |
| FSIRX2_DATA0    | I            | FSI Data 0      | E17, G4     |
| FSIRX2_DATA1    | I            | FSI Data 1      | E18, J3     |

**Table 5-59. FSIRX3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSIRX3_CLK      | I            | FSI Clock       | B17         |
| FSIRX3_DATA0    | I            | FSI Data 0      | D16         |
| FSIRX3_DATA1    | I            | FSI Data 1      | C17         |

**Table 5-60. FSITX0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSITX0_CLK      | O            | FSI Clock       | A11, R17    |
| FSITX0_DATA0    | O            | FSI Data 0      | C10, R18    |
| FSITX0_DATA1    | O            | FSI Data 1      | B11, U17    |

**Table 5-61. FSITX1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSITX1_CLK      | O            | FSI Clock       | E4, N18     |
| FSITX1_DATA0    | O            | FSI Data 0      | F2, M18     |
| FSITX1_DATA1    | O            | FSI Data 1      | G2, P16     |

**Table 5-62. FSITX2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSITX2_CLK      | O            | FSI Clock       | E16, G3     |
| FSITX2_DATA0    | O            | FSI Data 0      | F16, H2     |
| FSITX2_DATA1    | O            | FSI Data 1      | F18, G1     |

**Table 5-63. FSITX3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| FSITX3_CLK      | O            | FSI Clock       | C16         |
| FSITX3_DATA0    | O            | FSI Data 0      | A17         |
| FSITX3_DATA1    | O            | FSI Data 1      | B18         |

### 5.3.11 GPIO

**Table 5-64. GPIO Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ZCZ PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| GPIO0           | IO           | General Purpose Input/Output | P1          |
| GPIO1           | IO           | General Purpose Input/Output | R3          |
| GPIO2           | IO           | General Purpose Input/Output | N2          |
| GPIO3           | IO           | General Purpose Input/Output | N1          |
| GPIO4           | IO           | General Purpose Input/Output | N4          |
| GPIO5           | IO           | General Purpose Input/Output | M4          |
| GPIO6           | IO           | General Purpose Input/Output | P3          |
| GPIO7           | IO           | General Purpose Input/Output | M1          |
| GPIO8           | IO           | General Purpose Input/Output | L1          |
| GPIO9           | IO           | General Purpose Input/Output | L2          |
| GPIO10          | IO           | General Purpose Input/Output | K1          |
| GPIO11          | IO           | General Purpose Input/Output | C11         |
| GPIO12          | IO           | General Purpose Input/Output | A11         |
| GPIO13          | IO           | General Purpose Input/Output | C10         |
| GPIO14          | IO           | General Purpose Input/Output | B11         |
| GPIO15          | IO           | General Purpose Input/Output | C9          |
| GPIO16          | IO           | General Purpose Input/Output | A10         |
| GPIO17          | IO           | General Purpose Input/Output | B10         |
| GPIO18          | IO           | General Purpose Input/Output | D9          |
| GPIO19          | IO           | General Purpose Input/Output | A9          |

**Table 5-64. GPIO Signal Descriptions (continued)**

| SIGNAL NAME [1]        | PIN TYPE [2] | DESCRIPTION [3]              | ZCZ PIN [4] |
|------------------------|--------------|------------------------------|-------------|
| GPIO100                | IO           | General Purpose Input/Output | M15         |
| GPIO101                | IO           | General Purpose Input/Output | H17         |
| GPIO102                | IO           | General Purpose Input/Output | H16         |
| GPIO103                | IO           | General Purpose Input/Output | F15         |
| GPIO104                | IO           | General Purpose Input/Output | C18         |
| GPIO105                | IO           | General Purpose Input/Output | D17         |
| GPIO106                | IO           | General Purpose Input/Output | D18         |
| GPIO107                | IO           | General Purpose Input/Output | E16         |
| GPIO108                | IO           | General Purpose Input/Output | F16         |
| GPIO109                | IO           | General Purpose Input/Output | F18         |
| GPIO110                | IO           | General Purpose Input/Output | G16         |
| GPIO111                | IO           | General Purpose Input/Output | E17         |
| GPIO112                | IO           | General Purpose Input/Output | E18         |
| GPIO113                | IO           | General Purpose Input/Output | C16         |
| GPIO114                | IO           | General Purpose Input/Output | A17         |
| GPIO115                | IO           | General Purpose Input/Output | B18         |
| GPIO116                | IO           | General Purpose Input/Output | B17         |
| GPIO117                | IO           | General Purpose Input/Output | D16         |
| GPIO118                | IO           | General Purpose Input/Output | C17         |
| GPIO119                | IO           | General Purpose Input/Output | D15         |
| GPIO120                | IO           | General Purpose Input/Output | C15         |
| GPIO121                | IO           | General Purpose Input/Output | P2          |
| GPIO122                | IO           | General Purpose Input/Output | B16         |
| GPIO123                | IO           | General Purpose Input/Output | D14         |
| GPIO124                | IO           | General Purpose Input/Output | A16         |
| GPIO125                | IO           | General Purpose Input/Output | D13         |
| GPIO126                | IO           | General Purpose Input/Output | B15         |
| GPIO127                | IO           | General Purpose Input/Output | C13         |
| GPIO128                | IO           | General Purpose Input/Output | A15         |
| GPIO129                | IO           | General Purpose Input/Output | C14         |
| GPIO130                | IO           | General Purpose Input/Output | B14         |
| GPIO131                | IO           | General Purpose Input/Output | A14         |
| GPIO132                | IO           | General Purpose Input/Output | C12         |
| GPIO133                | IO           | General Purpose Input/Output | D11         |
| GPIO134 <sup>(1)</sup> | IOD          | General Purpose Input/Output | B13         |
| GPIO135 <sup>(2)</sup> | IOD          | General Purpose Input/Output | A13         |
| GPIO136                | IO           | General Purpose Input/Output | B12         |
| GPIO137                | IO           | General Purpose Input/Output | A12         |
| GPIO138                | IO           | General Purpose Input/Output | M2          |
| GPIO20                 | IO           | General Purpose Input/Output | B9          |
| GPIO21                 | IO           | General Purpose Input/Output | B8          |
| GPIO22                 | IO           | General Purpose Input/Output | A8          |
| GPIO23                 | IO           | General Purpose Input/Output | D7          |
| GPIO24                 | IO           | General Purpose Input/Output | C8          |
| GPIO25                 | IO           | General Purpose Input/Output | C7          |

**Table 5-64. GPIO Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ZCZ PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| GPIO26          | IO           | General Purpose Input/Output | B7          |
| GPIO27          | IO           | General Purpose Input/Output | A7          |
| GPIO28          | IO           | General Purpose Input/Output | A6          |
| GPIO29          | IO           | General Purpose Input/Output | R17         |
| GPIO30          | IO           | General Purpose Input/Output | R18         |
| GPIO31          | IO           | General Purpose Input/Output | U17         |
| GPIO32          | IO           | General Purpose Input/Output | T17         |
| GPIO33          | IO           | General Purpose Input/Output | U18         |
| GPIO34          | IO           | General Purpose Input/Output | T18         |
| GPIO35          | IO           | General Purpose Input/Output | N18         |
| GPIO36          | IO           | General Purpose Input/Output | M18         |
| GPIO37          | IO           | General Purpose Input/Output | P16         |
| GPIO38          | IO           | General Purpose Input/Output | P17         |
| GPIO39          | IO           | General Purpose Input/Output | P18         |
| GPIO40          | IO           | General Purpose Input/Output | N17         |
| GPIO41          | IO           | General Purpose Input/Output | N16         |
| GPIO42          | IO           | General Purpose Input/Output | M17         |
| GPIO43          | IO           | General Purpose Input/Output | B2          |
| GPIO44          | IO           | General Purpose Input/Output | B1          |
| GPIO45          | IO           | General Purpose Input/Output | D3          |
| GPIO46          | IO           | General Purpose Input/Output | D2          |
| GPIO47          | IO           | General Purpose Input/Output | C2          |
| GPIO48          | IO           | General Purpose Input/Output | C1          |
| GPIO49          | IO           | General Purpose Input/Output | E2          |
| GPIO50          | IO           | General Purpose Input/Output | E3          |
| GPIO51          | IO           | General Purpose Input/Output | D1          |
| GPIO52          | IO           | General Purpose Input/Output | E4          |
| GPIO53          | IO           | General Purpose Input/Output | F2          |
| GPIO54          | IO           | General Purpose Input/Output | G2          |
| GPIO55          | IO           | General Purpose Input/Output | E1          |
| GPIO56          | IO           | General Purpose Input/Output | F3          |
| GPIO57          | IO           | General Purpose Input/Output | F4          |
| GPIO58          | IO           | General Purpose Input/Output | F1          |
| GPIO59          | IO           | General Purpose Input/Output | G3          |
| GPIO60          | IO           | General Purpose Input/Output | H2          |
| GPIO61          | IO           | General Purpose Input/Output | G1          |
| GPIO62          | IO           | General Purpose Input/Output | J2          |
| GPIO63          | IO           | General Purpose Input/Output | G4          |
| GPIO64          | IO           | General Purpose Input/Output | J3          |
| GPIO65          | IO           | General Purpose Input/Output | H1          |
| GPIO66          | IO           | General Purpose Input/Output | J1          |
| GPIO67          | IO           | General Purpose Input/Output | K2          |
| GPIO68          | IO           | General Purpose Input/Output | J4          |
| GPIO69          | IO           | General Purpose Input/Output | K4          |
| GPIO70          | IO           | General Purpose Input/Output | K3          |

**Table 5-64. GPIO Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ZCZ PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| GPIO71          | IO           | General Purpose Input/Output | V17         |
| GPIO72          | IO           | General Purpose Input/Output | T16         |
| GPIO73          | IO           | General Purpose Input/Output | P15         |
| GPIO74          | IO           | General Purpose Input/Output | R16         |
| GPIO75          | IO           | General Purpose Input/Output | L3          |
| GPIO76          | IO           | General Purpose Input/Output | M3          |
| GPIO77          | IO           | General Purpose Input/Output | B6          |
| GPIO78          | IO           | General Purpose Input/Output | A4          |
| GPIO79          | IO           | General Purpose Input/Output | B5          |
| GPIO80          | IO           | General Purpose Input/Output | B4          |
| GPIO81          | IO           | General Purpose Input/Output | A3          |
| GPIO82          | IO           | General Purpose Input/Output | A2          |
| GPIO83          | IO           | General Purpose Input/Output | C6          |
| GPIO84          | IO           | General Purpose Input/Output | A5          |
| GPIO85          | IO           | General Purpose Input/Output | L17         |
| GPIO86          | IO           | General Purpose Input/Output | L18         |
| GPIO87          | IO           | General Purpose Input/Output | G17         |
| GPIO88          | IO           | General Purpose Input/Output | F17         |
| GPIO89          | IO           | General Purpose Input/Output | G18         |
| GPIO90          | IO           | General Purpose Input/Output | G15         |
| GPIO91          | IO           | General Purpose Input/Output | K15         |
| GPIO92          | IO           | General Purpose Input/Output | K16         |
| GPIO93          | IO           | General Purpose Input/Output | K17         |
| GPIO94          | IO           | General Purpose Input/Output | K18         |
| GPIO95          | IO           | General Purpose Input/Output | J18         |
| GPIO96          | IO           | General Purpose Input/Output | J17         |
| GPIO97          | IO           | General Purpose Input/Output | H18         |
| GPIO98          | IO           | General Purpose Input/Output | L16         |
| GPIO99          | IO           | General Purpose Input/Output | M16         |

(1) GPIO134 is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.

(2) GPIO135 is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.

### 5.3.12 GPMC

**Table 5-65. GPMC0 Signal Descriptions**

| SIGNAL NAME [1]            | PIN TYPE [2] | DESCRIPTION [3]                                                                             | ZCZ PIN [4] |
|----------------------------|--------------|---------------------------------------------------------------------------------------------|-------------|
| GPMC0_ADVn_ALE             | O            | GPMC Address Valid (active low) or Address Latch Enable                                     | B15         |
| GPMC0_CLK <sup>(2)</sup>   | IO           | GPMC Clock                                                                                  | F17         |
| GPMC0_CLKLB <sup>(1)</sup> | IO           | GPMC Clock Loopback                                                                         | H1          |
| GPMC0_DIR                  | O            | GPMC Data Bus Signal Direction Control                                                      | G17         |
| GPMC0_OEn_REn              | O            | GPMC Output Enable (active low) or Read Enable (active low)                                 | F15, J1     |
| GPMC0_WEn                  | O            | GPMC Write Enable (active low)                                                              | D18, K2     |
| GPMC0_WPn                  | O            | GPMC Flash Write Protect (active low)                                                       | G15         |
| GPMC0_A0                   | O            | GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories | K16         |

**Table 5-65. GPMC0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                                                                | ZCZ PIN [4] |
|-----------------|--------------|----------------------------------------------------------------------------------------------------------------|-------------|
| GPMC0_A1        | O            | GPMC Address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode                       | K17         |
| GPMC0_A2        | O            | GPMC Address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode                       | K18         |
| GPMC0_A3        | O            | GPMC Address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode                       | J18         |
| GPMC0_A4        | O            | GPMC Address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode                       | J17         |
| GPMC0_A5        | O            | GPMC Address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode                       | H18         |
| GPMC0_A6        | O            | GPMC Address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode                       | L16         |
| GPMC0_A7        | O            | GPMC Address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode                       | M16         |
| GPMC0_A8        | O            | GPMC Address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode                       | M15         |
| GPMC0_A9        | O            | GPMC Address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode                       | H17         |
| GPMC0_A10       | O            | GPMC Address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode                      | H16         |
| GPMC0_A11       | O            | GPMC Address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | E16         |
| GPMC0_A12       | O            | GPMC Address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | F16         |
| GPMC0_A13       | O            | GPMC Address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | F18         |
| GPMC0_A14       | O            | GPMC Address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | G16         |
| GPMC0_A15       | O            | GPMC Address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | E17         |
| GPMC0_A16       | O            | GPMC Address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | E18         |
| GPMC0_A17       | O            | GPMC Address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | C16         |
| GPMC0_A18       | O            | GPMC Address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | A17         |
| GPMC0_A19       | O            | GPMC Address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | B18         |
| GPMC0_A20       | O            | GPMC Address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | B17         |
| GPMC0_A21       | O            | GPMC Address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | D16         |
| GPMC0_AD0       | IO           | GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode | K4          |
| GPMC0_AD1       | IO           | GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode | K3          |
| GPMC0_AD2       | IO           | GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode | V17         |
| GPMC0_AD3       | IO           | GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 4 Output in A/D multiplexed mode | T16         |
| GPMC0_AD4       | IO           | GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 5 Output in A/D multiplexed mode | P15         |
| GPMC0_AD5       | IO           | GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 6 Output in A/D multiplexed mode | R16         |

**Table 5-65. GPMC0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                                                                  | ZCZ PIN [4] |
|-----------------|--------------|------------------------------------------------------------------------------------------------------------------|-------------|
| GPMC0_AD6       | IO           | GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 7 Output in A/D multiplexed mode   | L3          |
| GPMC0_AD7       | IO           | GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 8 Output in A/D multiplexed mode   | M3          |
| GPMC0_AD8       | IO           | GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 9 Output in A/D multiplexed mode   | B6          |
| GPMC0_AD9       | IO           | GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 10 Output in A/D multiplexed mode  | A4          |
| GPMC0_AD10      | IO           | GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode | B5          |
| GPMC0_AD11      | IO           | GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode | B4          |
| GPMC0_AD12      | IO           | GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode | A3          |
| GPMC0_AD13      | IO           | GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode | A2          |
| GPMC0_AD14      | IO           | GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode | C6          |
| GPMC0_AD15      | IO           | GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode | A5          |
| GPMC0_BE0n_CLE  | O            | GPMC Lower-Byte Enable (active low) or Command Latch Enable                                                      | C18         |
| GPMC0_BE1n      | O            | GPMC Upper-Byte Enable (active low)                                                                              | D17         |
| GPMC0_CSn0      | O            | GPMC Chip Select 0 (active low)                                                                                  | C17, J4     |
| GPMC0_CSn1      | O            | GPMC Chip Select 1 (active low)                                                                                  | K15         |
| GPMC0_CSn2      | O            | GPMC Chip Select 2 (active low)                                                                                  | L17         |
| GPMC0_CSn3      | O            | GPMC Chip Select 3 (active low)                                                                                  | L18         |
| GPMC0_WAIT0     | I            | GPMC External Indication of Wait                                                                                 | G18         |
| GPMC0_WAIT1     | I            | GPMC External Indication of Wait                                                                                 | C15         |

- (1) GPMC0\_CLKLB is a clock loopback signal used internally for retiming purposes.  
(2) The RXACTIVE bit of the MSS\_IOMUX:PR0\_PRU0\_GPO9\_CFG\_REG register must be set to 0x1 and the TX\_DIS bit of the MSS\_IOMUX:PR0\_PRU0\_GPO9\_CFG\_REG register must be reset to 0x0 when GPMC0 is operating in synchronous mode.

### 5.3.13 I2C

**Table 5-66. I2C0 Signal Descriptions**

| SIGNAL NAME [1]         | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-------------------------|--------------|-----------------|-------------|
| I2C0_SCL <sup>(2)</sup> | IOD          | I2C Clock       | A13         |
| I2C0_SDA <sup>(1)</sup> | IOD          | I2C Data        | B13         |

- (1) I2C0\_SDA is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.  
(2) I2C0\_SCL is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.

**Table 5-67. I2C1 Signal Descriptions**

| SIGNAL NAME [1]         | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-------------------------|--------------|-----------------|-------------|
| I2C1_SCL <sup>(1)</sup> | IOD          | I2C Clock       | B5, D7      |
| I2C1_SDA <sup>(2)</sup> | IOD          | I2C Data        | A3, C8      |

- (1) I2C1\_SCL is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.  
(2) I2C1\_SDA is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.

**Table 5-68. I2C2 Signal Descriptions**

| SIGNAL NAME [1]         | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-------------------------|--------------|-----------------|-------------|
| I2C2_SCL <sup>(1)</sup> | IOD          | I2C Clock       | C6, C7      |
| I2C2_SDA <sup>(2)</sup> | IOD          | I2C Data        | A5, B7      |

- (1) I2C2\_SCL is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.
- (2) I2C2\_SDA is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.

**Table 5-69. I2C3 Signal Descriptions**

| SIGNAL NAME [1]         | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-------------------------|--------------|-----------------|-------------|
| I2C3_SCL <sup>(2)</sup> | IOD          | I2C Clock       | B15, H2     |
| I2C3_SDA <sup>(1)</sup> | IOD          | I2C Data        | A16, G3     |

- (1) I2C3\_SDA is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.
- (2) I2C3\_SCL is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.

**Note**

I2C signals that are implemented on an LVCMOS voltage buffer pin can be configured to operate as open-drain outputs by configuring the I2C module to source a constant low output and toggle the output enable. The output buffer drives low when enabled and is high impedance when disabled.

The (I2C OD FS) are the only IO voltage buffers which are fail-safe. These are implemented for I2C0 pins only. Other IOs do not allow any potential greater than (VDD + 0.3V) to be applied. This means you can not source any potential to these pins when power is off. All attached devices that can source a potential to these IOs must be powered from the same power supply that is sourcing the respective IO power rail.

**5.3.14 LIN****Table 5-70. LIN0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ZCZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| LIN0_RXD        | IO           | LIN Receive Data  | A7, B6      |
| LIN0_TXD        | IO           | LIN Transmit Data | A4, A6      |

**Table 5-71. LIN1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ZCZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| LIN1_RXD        | IO           | LIN Receive Data  | A9, L3      |
| LIN1_TXD        | IO           | LIN Transmit Data | B9, M3      |

**Table 5-72. LIN2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ZCZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| LIN2_RXD        | IO           | LIN Receive Data  | B8          |
| LIN2_TXD        | IO           | LIN Transmit Data | A8          |

**Table 5-73. LIN3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ZCZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| LIN3_RXD        | IO           | LIN Receive Data  | C11         |
| LIN3_TXD        | IO           | LIN Transmit Data | A11         |

**Table 5-74. LIN4 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ZCZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| LIN4_RXD        | IO           | LIN Receive Data  | A10, D11    |
| LIN4_TXD        | IO           | LIN Transmit Data | C12, C9     |

### 5.3.15 MCAN

**Table 5-75. MCAN0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ZCZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN0_RX        | I            | MCAN Receive Data  | M1          |
| MCAN0_TX        | O            | MCAN Transmit Data | L1          |

**Table 5-76. MCAN1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ZCZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN1_RX        | I            | MCAN Receive Data  | L2          |
| MCAN1_TX        | O            | MCAN Transmit Data | K1          |

**Table 5-77. MCAN2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ZCZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN2_RX        | I            | MCAN Receive Data  | A12         |
| MCAN2_TX        | O            | MCAN Transmit Data | B12         |

**Table 5-78. MCAN3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ZCZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN3_RX        | I            | MCAN Receive Data  | B7, C14     |
| MCAN3_TX        | O            | MCAN Transmit Data | A15, C7     |

### 5.3.16 SPI (MCSPi)

**Table 5-79. SPI0 Signal Descriptions**

| SIGNAL NAME [1]         | PIN TYPE [2] | DESCRIPTION [3]   | ZCZ PIN [4] |
|-------------------------|--------------|-------------------|-------------|
| SPI0_CLK <sup>(1)</sup> | IO           | SPI Clock (SOP2)  | A11         |
| SPI0_CS0                | IO           | SPI Chip Select 0 | C11         |
| SPI0_CS1                | IO           | SPI Chip Select 1 | B7          |
| SPI0_D0 <sup>(2)</sup>  | IO           | SPI Data 0 (SOP3) | C10         |
| SPI0_D1                 | IO           | SPI Data 1        | B11         |

(1) The SPI0\_CLK pin is also used as SOP2 bootmode configuration pin.

(2) The SPI0\_D0 pin is also used as SOP3 bootmode configuration pin.

**Table 5-80. SPI1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ZCZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI1_CLK        | IO           | SPI Clock         | A10         |
| SPI1_CS0        | IO           | SPI Chip Select 0 | C9          |
| SPI1_D0         | IO           | SPI Data 0        | B10         |
| SPI1_D1         | IO           | SPI Data 1        | D9          |

**Table 5-81. SPI2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ZCZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI2_CLK        | IO           | SPI Clock         | B9          |
| SPI2_CS0        | IO           | SPI Chip Select 0 | A9          |

**Table 5-81. SPI2 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| SPI2_D0         | IO           | SPI Data 0      | B8          |
| SPI2_D1         | IO           | SPI Data 1      | A8          |

**Table 5-82. SPI3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ZCZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI3_CLK        | IO           | SPI Clock         | C8          |
| SPI3_CS0        | IO           | SPI Chip Select 0 | D7          |
| SPI3_D0         | IO           | SPI Data 0        | C7          |
| SPI3_D1         | IO           | SPI Data 1        | B7          |

**Table 5-83. SPI4 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ZCZ PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI4_CLK        | IO           | SPI Clock         | B14, L1     |
| SPI4_CS0        | IO           | SPI Chip Select 0 | A14, M1     |
| SPI4_CS1        | IO           | SPI Chip Select 1 | K2          |
| SPI4_D0         | IO           | SPI Data 0        | C12, L2     |
| SPI4_D1         | IO           | SPI Data 1        | D11, K1     |

**5.3.17 MMC****Table 5-84. MMC0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]      | ZCZ PIN [4] |
|-----------------|--------------|----------------------|-------------|
| MMC0_CD         | I            | MMC/SD Card Detect   | A5          |
| MMC0_CLK        | IO           | MMC/SD Clock         | B6          |
| MMC0_CMD        | IO           | MMC/SD Command       | A4          |
| MMC0_WP         | I            | MMC/SD Write Protect | C6          |
| MMC0_D0         | IO           | MMC/SD Data          | B5          |
| MMC0_D1         | IO           | MMC/SD Data          | B4          |
| MMC0_D2         | IO           | MMC/SD Data          | A3          |
| MMC0_D3         | IO           | MMC/SD Data          | A2          |

**5.3.18 Power Supply****Table 5-85. Power Supply Signal Descriptions**

| SIGNAL NAME [1]    | PIN TYPE [2] | DESCRIPTION [3]        | ZCZ PIN [4]                                                                     |
|--------------------|--------------|------------------------|---------------------------------------------------------------------------------|
| VDD                | PWR          | 1.2V Core supply       | E11, E9, F11, F9, G13, G14, G5, G6, J16, K13, K14, K5, K6, N13, N14, N5, N6, R9 |
| VDDA18             | PWR          | 1.8V Analog supply     | R11, R8                                                                         |
| VDDA18_LDO (1) (2) | PWR          | 1.8V Analog LDO Output | R6                                                                              |
| VDDA18_OSC_PLL     | PWR          | 1.8V OSC PLL supply    | R4                                                                              |
| VDDA33             | PWR          | 3.3V Analog supply     | P11, P7, P9                                                                     |
| VDDAR1             | PWR          | 1.2V SRAM Array supply | J15                                                                             |
| VDDAR2             | PWR          | 1.2V SRAM Array supply | D10                                                                             |
| VDDAR3             | PWR          | 1.2V SRAM Array supply | H3                                                                              |
| VDDS18             | PWR          | 1.8V IO supply         | D6, E15, L4, N15                                                                |

**Table 5-85. Power Supply Signal Descriptions (continued)**

| SIGNAL NAME [1]    | PIN TYPE [2] | DESCRIPTION [3]              | ZCZ PIN [4]                                                                                                                                                                                                                                                                                                                                                                                                                                |
|--------------------|--------------|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDDS18_LDO (1) (3) | PWR          | 1.8V Digital LDO Output      | T3                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| VDDS33             | PWR          | 3.3V IO supply               | D12, D8, H15, H4,<br>L15, P4, R15                                                                                                                                                                                                                                                                                                                                                                                                          |
| VPP                | PWR          | eFuse ROM programming supply | N3                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| VSS                | GND          | Ground                       | A1, A18, E10,<br>E12, E13, E14,<br>E5, E6, E7, E8,<br>F10, F12, F13,<br>F14, F5, F6, F7,<br>F8, G10, G11,<br>G12, G7, G8, G9,<br>H10, H11, H12,<br>H13, H14, H5, H6,<br>H7, H8, H9, J10,<br>J11, J12, J13, J14,<br>J5, J6, J7, J8, J9,<br>K10, K11, K12, K7,<br>K8, K9, L10, L11,<br>L12, L13, L14, L5,<br>L6, L7, L8, L9,<br>M10, M11, M12,<br>M13, M14, M5,<br>M6, M7, M8, M9,<br>N10, N11, N12,<br>N7, N8, N9, P13,<br>P14, P5, T2, V18 |
| VSSA               | AGND         | Analog Ground                | P10, P12, P6, P8,<br>R13, R5, V1, V16                                                                                                                                                                                                                                                                                                                                                                                                      |

(1) See the *Layout Guidelines* sections for details on connecting this pin.

(2) PCB should directly route VDDA18\_LDO to all of the VDDA18 pins and the VDDA\_OSC\_PLL pin.

(3) PCB should directly route VDDS18\_LDO to all of the VDDS18 pins.

### 5.3.19 PRU-ICSS

**Table 5-86. PRU-ICSS ECAP Signal Descriptions**

| SIGNAL NAME [1]    | PIN TYPE [2] | DESCRIPTION [3]                                                            | ZCZ PIN [4] |
|--------------------|--------------|----------------------------------------------------------------------------|-------------|
| PR0_ECAP0_APWM_OUT | O            | PRU-ICSS Enhanced Capture (ECAP) Input or ECAP Auxiliary PWM (APWM) Output | D14         |

**Table 5-87. PRU-ICSS GPIO Signal Descriptions**

| SIGNAL NAME [1] (1) | PIN TYPE [2] | DESCRIPTION [3]                   | ZCZ PIN [4] |
|---------------------|--------------|-----------------------------------|-------------|
| PR0_PRU0_GPIO0      | IO           | PRU0 General Purpose Input/Output | K17         |
| PR0_PRU0_GPIO1      | IO           | PRU0 General Purpose Input/Output | K18         |
| PR0_PRU0_GPIO2      | IO           | PRU0 General Purpose Input/Output | J18         |
| PR0_PRU0_GPIO3      | IO           | PRU0 General Purpose Input/Output | J17         |
| PR0_PRU0_GPIO4      | IO           | PRU0 General Purpose Input/Output | K16         |
| PR0_PRU0_GPIO5      | IO           | PRU0 General Purpose Input/Output | G17         |
| PR0_PRU0_GPIO6      | IO           | PRU0 General Purpose Input/Output | K15         |
| PR0_PRU0_GPIO8      | IO           | PRU0 General Purpose Input/Output | G15         |
| PR0_PRU0_GPIO9      | IO           | PRU0 General Purpose Input/Output | F17         |
| PR0_PRU0_GPIO10     | IO           | PRU0 General Purpose Input/Output | G18         |
| PR0_PRU0_GPIO11     | IO           | PRU0 General Purpose Input/Output | M16         |
| PR0_PRU0_GPIO12     | IO           | PRU0 General Purpose Input/Output | M15         |
| PR0_PRU0_GPIO13     | IO           | PRU0 General Purpose Input/Output | H17         |

**Table 5-87. PRU-ICSS GPIO Signal Descriptions (continued)**

| SIGNAL NAME [1] <sup>(1)</sup> | PIN TYPE [2] | DESCRIPTION [3]                   | ZCZ PIN [4] |
|--------------------------------|--------------|-----------------------------------|-------------|
| PR0_PRU0_GPIO14                | IO           | PRU0 General Purpose Input/Output | H16         |
| PR0_PRU0_GPIO15                | IO           | PRU0 General Purpose Input/Output | L16         |
| PR0_PRU0_GPIO16                | IO           | PRU0 General Purpose Input/Output | H18         |
| PR0_PRU1_GPIO0                 | IO           | PRU1 General Purpose Input/Output | F18         |
| PR0_PRU1_GPIO1                 | IO           | PRU1 General Purpose Input/Output | G16         |
| PR0_PRU1_GPIO2                 | IO           | PRU1 General Purpose Input/Output | E17         |
| PR0_PRU1_GPIO3                 | IO           | PRU1 General Purpose Input/Output | E18         |
| PR0_PRU1_GPIO4                 | IO           | PRU1 General Purpose Input/Output | F16         |
| PR0_PRU1_GPIO5                 | IO           | PRU1 General Purpose Input/Output | F15         |
| PR0_PRU1_GPIO6                 | IO           | PRU1 General Purpose Input/Output | E16         |
| PR0_PRU1_GPIO7                 | IO           | PRU1 General Purpose Input/Output | A16         |
| PR0_PRU1_GPIO8                 | IO           | PRU1 General Purpose Input/Output | D18         |
| PR0_PRU1_GPIO9                 | IO           | PRU1 General Purpose Input/Output | C18         |
| PR0_PRU1_GPIO10                | IO           | PRU1 General Purpose Input/Output | D17         |
| PR0_PRU1_GPIO11                | IO           | PRU1 General Purpose Input/Output | B18         |
| PR0_PRU1_GPIO12                | IO           | PRU1 General Purpose Input/Output | B17         |
| PR0_PRU1_GPIO13                | IO           | PRU1 General Purpose Input/Output | D16         |
| PR0_PRU1_GPIO14                | IO           | PRU1 General Purpose Input/Output | C17         |
| PR0_PRU1_GPIO15                | IO           | PRU1 General Purpose Input/Output | A17         |
| PR0_PRU1_GPIO16                | IO           | PRU1 General Purpose Input/Output | C16         |
| PR0_PRU1_GPIO17                | IO           | PRU1 General Purpose Input/Output | D13         |
| PR0_PRU1_GPIO18                | IO           | PRU1 General Purpose Input/Output | C15         |
| PR0_PRU1_GPIO19                | IO           | PRU1 General Purpose Input/Output | D15         |

(1) PR0\_PRU0\_GPIO7, PR0\_PRU0\_GPIO17, PR0\_PRU0\_GPIO18, and PR0\_PRU0\_GPIO19, signals are not pinned out. The equivalent PR0\_PRU1\_GPIO signals are pinned out and available.

**Table 5-88. PRU-ICSS IEP Signal Descriptions**

| SIGNAL NAME [1]             | PIN TYPE [2] | DESCRIPTION [3]                                            | ZCZ PIN [4] |
|-----------------------------|--------------|------------------------------------------------------------|-------------|
| PR0_IEP0_EDC_SYNC_OUT0      | O            | PRU-ICSS Industrial Ethernet Distributed Clock Sync Output | D15         |
| PR0_IEP0_EDC_SYNC_OUT1      | O            | PRU-ICSS Industrial Ethernet Distributed Clock Sync Output | A16         |
| PR0_IEP0_EDIO_DATA_IN_OUT30 | IO           | PRU-ICSS Industrial Ethernet Digital I/O Data Input/Output | D13         |
| PR0_IEP0_EDIO_DATA_IN_OUT31 | IO           | PRU-ICSS Industrial Ethernet Digital I/O Data Input/Output | C15         |

**Table 5-89. PRU-ICSS MDIO Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]     | ZCZ PIN [4] |
|-----------------|--------------|---------------------|-------------|
| PR0_MDIO0_MDC   | O            | PRU-ICSS MDIO Clock | L18         |
| PR0_MDIO0_MDIO  | IO           | PRU-ICSS MDIO Data  | L17         |

**Table 5-90. PRU-ICSS UART Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                            | ZCZ PIN [4] |
|-----------------|--------------|--------------------------------------------|-------------|
| PR0_UART0_CTSn  | I            | PRU-ICSS UART Clear to Send (Active Low)   | F17         |
| PR0_UART0_RTSn  | O            | PRU-ICSS UART Request to Send (Active Low) | G18         |
| PR0_UART0_RXD   | I            | PRU-ICSS UART Receive Data                 | C18         |
| PR0_UART0_TXD   | O            | PRU-ICSS UART Transmit Data                | D17         |

### 5.3.20 QSPI

**Table 5-91. QSPI0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]        | ZCZ PIN [4] |
|-----------------|--------------|------------------------|-------------|
| QSPI0_CLK       | O            | QSPI Clock             | N2          |
| QSPI0_CLKLB (3) | IO           | QSPI Clock Loopback    | LB          |
| QSPI0_CSn0      | O            | QSPI Chip Select 0     | P1          |
| QSPI0_CSn1      | O            | QSPI Chip Select 1     | R3          |
| QSPI0_D0 (1)    | IO           | QSPI Data bit 0 (SOP0) | N1          |
| QSPI0_D1 (2)    | I            | QSPI Data bit 1 (SOP1) | N4          |
| QSPI0_D2        | I            | QSPI Data bit 2        | M4          |
| QSPI0_D3        | I            | QSPI Data bit 3        | P3          |

- (1) The QSPI0\_D0 pin is also used as SOP0 boot mode configuration pin.  
(2) The QSPI0\_D1 pin is also used as SOP1 boot mode configuration pin.  
(3) QSPI0\_CLKLB is a clock loopback signal used internally for retiming purposes.

### 5.3.21 Reserved and No Connect

**Table 5-92. Reserved Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                 | ZCZ PIN [4] |
|-----------------|--------------|-----------------------------------------------------------------|-------------|
| RSVD_T4         | RSVD         | Reserved (RSVD_T4). This pin must be connected to ground (VSS). | T4          |
| RSVD_U1         | RSVD         | Reserved (RSVD_U1). This pin must be connected to ground (VSS). | U1          |
| RSVD_U3         | RSVD         | Reserved (RSVD_U3). This pin must be left unconnected.          | U3          |
| RSVD_V2         | RSVD         | Reserved (RSVD_V2). This pin must be left unconnected.          | V2          |

### 5.3.22 SDFM

**Table 5-93. SDFM0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ZCZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| SDFM0_CLK0      | I            | SDFM Clock 0 Input | B16         |
| SDFM0_CLK1      | I            | SDFM Clock 1 Input | A16         |
| SDFM0_CLK2      | I            | SDFM Clock 2 Input | B15         |
| SDFM0_CLK3      | I            | SDFM Clock 3 Input | A15         |
| SDFM0_D0        | I            | SDFM Data 0 Input  | D14         |
| SDFM0_D1        | I            | SDFM Data 1 Input  | D13         |
| SDFM0_D2        | I            | SDFM Data 2 Input  | C13         |
| SDFM0_D3        | I            | SDFM Data 3 Input  | C14         |

**Table 5-94. SDFM1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ZCZ PIN [4] |
|-----------------|--------------|--------------------|-------------|
| SDFM1_CLK0      | I            | SDFM Clock 0 Input | B14, B6     |
| SDFM1_CLK1      | I            | SDFM Clock 1 Input | B5, C12     |
| SDFM1_CLK2 (1)  | I            | SDFM Clock 2 Input | A3, B13     |
| SDFM1_CLK3 (2)  | I            | SDFM Clock 3 Input | A13, C6     |
| SDFM1_D0        | I            | SDFM Data 0 Input  | A14, A4     |
| SDFM1_D1        | I            | SDFM Data 1 Input  | B4, D11     |
| SDFM1_D2        | I            | SDFM Data 2 Input  | A2, B12     |
| SDFM1_D3        | I            | SDFM Data 3 Input  | A12, A5     |

- (1) SDFM1\_CLK2 is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer when using ball B13.

(2) SDFM1\_CLK3 is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer when using ball A13.

### 5.3.23 System and Miscellaneous

#### 5.3.23.1 Boot Mode Configuration

**Table 5-95. Boot Mode Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                          | ZCZ PIN [4] |
|-----------------|--------------|------------------------------------------|-------------|
| SOP0            | I            | Boot Mode configuration bit 0 (QSPI0_D0) | N1          |
| SOP1            | I            | Boot Mode configuration bit 1 (QSPI0_D1) | N4          |
| SOP2            | I            | Boot Mode configuration bit 2 (SPI0_CLK) | A11         |
| SOP3            | I            | Boot Mode configuration bit 3 (SPI0_D0)  | C10         |

#### 5.3.23.2 Clocking

**Table 5-96. XTAL Signal Descriptions**

| SIGNAL NAME [1]        | PIN TYPE [2] | DESCRIPTION [3]                | ZCZ PIN [4] |
|------------------------|--------------|--------------------------------|-------------|
| XTAL_XI <sup>(1)</sup> | I            | External Crystal (XTAL) Input  | T1          |
| XTAL_XO <sup>(1)</sup> | O            | External Crystal (XTAL) Output | R1          |

(1) The XTAL interface requires a 25 MHz clock source.

**Table 5-97. Output Clock Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ZCZ PIN [4] |
|-----------------|--------------|-----------------|-------------|
| CLKOUT0         | O            | Output Clock 0  | M2          |
| CLKOUT1         | O            | Output Clock 1  | B16         |

**Table 5-98. External Reference Clock Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                | ZCZ PIN [4] |
|-----------------|--------------|--------------------------------|-------------|
| EXT_REFCLK0     | I            | External Reference Clock Input | P2          |

#### 5.3.23.3 SYSTEM

**Table 5-99. System Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                         | ZCZ PIN [4] |
|-----------------|--------------|---------------------------------------------------------|-------------|
| PORz            | I            | Device Power-On (PORz) cold reset                       | R2          |
| SAFETY_ERRORn   | OD           | ESM Safety Error Signal                                 | D4          |
| WARMRSTn        | IO           | Warm Reset Request (Input) / Warm Reset Status (Output) | C3          |

#### Note

The SAFETY\_ERRORn signal is implemented on an LVCMOS voltage buffer pin can be configured to operate as open-drain outputs by configuring the ESM module to source a constant low output and toggle the output enable. The output buffer drives low when enabled and is high impedance when disabled.

The (I2C OD FS) are the only IO voltage buffers which are fail-safe. These are implemented for I2C0 pins only. Other IOs do not allow any potential greater than (VDD + 0.3V) to be applied. This means you cannot source any potential to these pins when power is off. All attached devices that can source a potential to these IOs must be powered from the same power supply that is sourcing the respective IO power rail.

### 5.3.23.4 VMON

**Table 5-100. VMON Signal Descriptions**

| SIGNAL NAME [1]         | PIN TYPE [2] | DESCRIPTION [3]                                       | ZCZ PIN [4] |
|-------------------------|--------------|-------------------------------------------------------|-------------|
| VSYS_MON <sup>(1)</sup> | PWR          | External Voltage Monitor with 0.9 V (+/-3%) setpoint. | U2          |

(1) See the *Electrical Specifications - Safety Comparators* section for additional details on this pin.

### 5.3.24 UART

**Table 5-101. UART0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ZCZ PIN [4] |
|-----------------|--------------|-----------------------------------|-------------|
| UART0_CTSn      | I            | UART Clear to Send (active low)   | A5, B7      |
| UART0_RTSn      | O            | UART Request to Send (active low) | C6, C7      |
| UART0_RXD       | I            | UART Receive Data                 | A7, B6      |
| UART0_TXD       | O            | UART Transmit Data                | A4, A6      |

**Table 5-102. UART1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                       | ZCZ PIN [4] |
|-----------------|--------------|---------------------------------------|-------------|
| UART1_CTSn      | I            | UART Clear to Send (active low)       | G4          |
| UART1_DCDn      | I            | UART Data Carrier Detect (Active Low) | J4          |
| UART1_DSRn      | I            | UART Data Set Ready (Active Low)      | V17         |
| UART1_DTRn      | O            | UART Data Terminal Ready (Active Low) | K3          |
| UART1_RIn       | I            | UART Ring Indicator                   | K4          |
| UART1_RTSn      | O            | UART Request to Send (active low)     | B12, J2     |
| UART1_RXD       | I            | UART Receive Data                     | A9, L3      |
| UART1_TXD       | O            | UART Transmit Data                    | B9, M3      |

**Table 5-103. UART2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ZCZ PIN [4] |
|-----------------|--------------|-----------------------------------|-------------|
| UART2_CTSn      | I            | UART Clear to Send (active low)   | H1          |
| UART2_RTSn      | O            | UART Request to Send (active low) | A12, J3     |
| UART2_RXD       | I            | UART Receive Data                 | B5, B8      |
| UART2_TXD       | O            | UART Transmit Data                | A3, A8      |

**Table 5-104. UART3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ZCZ PIN [4] |
|-----------------|--------------|-----------------------------------|-------------|
| UART3_CTSn      | I            | UART Clear to Send (active low)   | K2          |
| UART3_RTSn      | O            | UART Request to Send (active low) | A2, J1      |
| UART3_RXD       | I            | UART Receive Data                 | C11, D15    |
| UART3_TXD       | O            | UART Transmit Data                | A11, C15    |

**Table 5-105. UART4 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ZCZ PIN [4]  |
|-----------------|--------------|-----------------------------------|--------------|
| UART4_CTSn      | I            | UART Clear to Send (active low)   | A14          |
| UART4_RTSn      | O            | UART Request to Send (active low) | B14          |
| UART4_RXD       | I            | UART Receive Data                 | A10, D11, H2 |
| UART4_TXD       | O            | UART Transmit Data                | C12, C9, G3  |

**Table 5-106. UART5 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ZCZ PIN [4]       |
|-----------------|--------------|-----------------------------------|-------------------|
| UART5_CTSn      | I            | UART Clear to Send (active low)   | D13               |
| UART5_RTSn      | O            | UART Request to Send (active low) | A16               |
| UART5_RXD       | I            | UART Receive Data                 | A15, C13, D9, R16 |
| UART5_TXD       | O            | UART Transmit Data                | B10, B15, P15     |

**5.3.25 XBAR****Table 5-107. Output XBAR Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]      | ZCZ PIN [4] |
|-----------------|--------------|----------------------|-------------|
| XBAROUT0        | O            | OUTPUTXBAR Signal 0  | R3          |
| XBAROUT1        | O            | OUTPUTXBAR Signal 1  | C9          |
| XBAROUT2        | O            | OUTPUTXBAR Signal 2  | A10         |
| XBAROUT3        | O            | OUTPUTXBAR Signal 3  | B10         |
| XBAROUT4        | O            | OUTPUTXBAR Signal 4  | D9          |
| XBAROUT5        | O            | OUTPUTXBAR Signal 5  | A9          |
| XBAROUT6        | O            | OUTPUTXBAR Signal 6  | B9          |
| XBAROUT7        | O            | OUTPUTXBAR Signal 7  | D7          |
| XBAROUT8        | O            | OUTPUTXBAR Signal 8  | C8          |
| XBAROUT9        | O            | OUTPUTXBAR Signal 9  | C7          |
| XBAROUT10       | O            | OUTPUTXBAR Signal 10 | B7          |
| XBAROUT11       | O            | OUTPUTXBAR Signal 11 | D16         |
| XBAROUT12       | O            | OUTPUTXBAR Signal 12 | C17         |
| XBAROUT13       | O            | OUTPUTXBAR Signal 13 | D15         |
| XBAROUT14       | O            | OUTPUTXBAR Signal 14 | C15         |
| XBAROUT15       | O            | OUTPUTXBAR Signal 15 | P2          |

## 5.4 Pin Connectivity Requirements

This section describes connectivity requirements for package balls that have specific connectivity requirements and package balls that can be unused.

### Note

All power balls must be supplied with the voltages specified in the *Recommended Operating Conditions* section, unless otherwise specified in *Signal Descriptions*.

For additional clarification, "leave unconnected" or "no connect" (NC) mean **no** signal traces are recommended to be connected to these device ball numbers.

**Table 5-108. Pin Connectivity Requirements**

| BALL NUMBER            | BALL NAME                                                               | PIN CONNECTIVITY REQUIREMENTS                                                                                                                                                                                                                                                                                                                                                                   |
|------------------------|-------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D4                     | SAFETY_ERRORn                                                           | Each of these balls must be connected to ground (VSS) through separate external pull resistors to ensure they are held to a valid logic low level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull-down may be used to hold a valid logic low level if no PCB signal trace is connected to the ball.                                         |
| B3<br>C5<br>D5         | TCK<br>TDI<br>TMS                                                       | Each of these balls must be connected to the corresponding power supply <sup>(1)</sup> through separate external pull resistors to ensure these balls are held to a valid logic high level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull-up may be used to hold a valid logic high level if no PCB signal trace is connected to the ball. |
| A13<br>B13             | I2C0_SCL<br>I2C0_SDA                                                    | Each of these balls must be connected to the corresponding power supply <sup>(1)</sup> through separate external pull resistors to ensure these balls are held to a valid logic high level.                                                                                                                                                                                                     |
| N1<br>N4<br>A11<br>C10 | QSPI0_D0 (SOP0)<br>QSPI0_D1 (SOP1)<br>SPI0_CLK (SOP2)<br>SPI0_D0 (SOP3) | Each of these balls must be connected to the corresponding power supply <sup>(1)</sup> or ground (VSS) through separate external pull resistors to ensure these balls are held to a valid logic high or low level as appropriate to select the desired device boot mode.                                                                                                                        |
| ADC ZCZ PIN            | ADC[0:4]_AIN[0:5]                                                       | Any unused ADCx_AINy input ball for any ADC instance (ADC[0:4]_AIN[0:5]) must be connected (shorted) directly to ground (VSS).                                                                                                                                                                                                                                                                  |
| U16<br>T15             | ADC_CAL0<br>ADC_CAL1                                                    | If all ADCx_AINy inputs for all ADC instances (ADC[0:4]_AIN[0:5]) are not used, the ADC_CAL[0:1] analog ball must be connected (shorted) directly to ground (VSS).                                                                                                                                                                                                                              |
| U2                     | VSYS_MON                                                                | If VSYS_MON is not used, this ball may be connected (shorted) directly to ground (VSS).                                                                                                                                                                                                                                                                                                         |
| LVC MOS ZCZ PIN        | Any LVC MOS Voltage Buffer Pin                                          | If a pin has an associated IOMUX Pad Configuration Registration then the ball may remain unconnected. After PORz, the LVC MOS voltage buffer is configured to a default state compatible with an unconnected ball.                                                                                                                                                                              |

(1) To determine which power supply is associated with any IO, see POWER column of the *Pin Attributes* table.

### Note

Internal pull resistors are weak and can possibly not source enough current to maintain a valid logic level for some operating conditions. This can be the case when connected to components with leakage to the opposite logic level, or when external noise sources couple to signal traces attached to balls which are only pulled to a valid logic level by the internal resistor. Therefore, external pull resistors can be required to hold a valid logic level on balls with external connections.

If balls are allowed to float between valid logic levels, the input buffer can enter a high-current state which can damage the IO cell.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETER                             |                                                                               | MIN  | MAX                                                                           | UNIT |
|---------------------------------------|-------------------------------------------------------------------------------|------|-------------------------------------------------------------------------------|------|
| VDD                                   | 1.2V SOC core supply                                                          | −0.5 | 1.5                                                                           | V    |
| VDDAR1                                | 1.2V SRAM Array Supply 1                                                      | −0.5 | 1.5                                                                           | V    |
| VDDAR2                                | 1.2V SRAM Array Supply 2                                                      | −0.5 | 1.5                                                                           | V    |
| VDDAR3                                | 1.2V SRAM Array Supply 3                                                      | −0.5 | 1.5                                                                           | V    |
| VDDS18                                | 1.8V IO Bias Supply from Bias LDO routed through Board                        | −0.5 | 2.1                                                                           | V    |
| VDDS33                                | 3.3V IO Supply                                                                | −0.5 | 4.0                                                                           | V    |
| VDDA18_OSC_PLL                        | 1.8V Analog Supply for PLL. Routed from the 1.8V Analog LDO out through Board | −0.5 | 2.1                                                                           | V    |
| VDDA33                                | Analog 3.3V Supply                                                            | −0.5 | 4.0                                                                           | V    |
| VDDA18                                | 1.8V Analog Supply. Routed from the 1.8V Analog LDO out through Board         | −0.5 | 2.1                                                                           | V    |
| IO Pin Steady State Voltage           | 3.3V LVCMOS IO Buffer                                                         | −0.3 | $V_{DDS33}^{(3)} + 0.3$                                                       | V    |
|                                       | 3.3V I2C Open-Drain IO Buffers                                                | −0.3 | $V_{DDS33}^{(3)} + 0.3$                                                       | V    |
|                                       | XTAL Pad                                                                      | −0.5 | 2.1                                                                           | V    |
| Transient Overshoot and Undershoot    | All Other IO Terminals                                                        | −0.3 | $V_{DDS33}^{(3)} + 0.2 \times V_{DDS33}^{(3)}$ for up to 20% of signal period | V    |
|                                       | XTAL Pad<br>20% of VDDA18_OSC_PLL for up to 20% of signal period              |      | $0.2 \times V_{DDA18\_OSC\_PLL}$                                              | V    |
| Latch Up Performance Class II (150°C) | Latch-up I-test Performance (Current-Pulse Injection on each IO pin)          |      | ±100                                                                          | mA   |
|                                       | Latch-up Overvoltage Performance (Voltage Injection on each IO pin)           |      | ±100                                                                          | mA   |
| Output current                        | Digital output (per pin), $I_{OUT}$                                           | −20  | 20                                                                            | mA   |
| Storage temperature <sup>(4)</sup>    | $T_{stg}$                                                                     | −55  | 155                                                                           | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to VSS, unless otherwise noted.
- (3) VDDS33 is the voltage on the corresponding power-supply pin(s) for the IC.
- (4) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the [Semiconductor and IC Package Thermal Metrics Application Report](#).

## 6.2 Electrostatic Discharge (ESD) Extended Automotive Ratings

over recommended operating conditions (unless otherwise noted)

|             |                               |                                                         |                                 | VALUE | UNIT |
|-------------|-------------------------------|---------------------------------------------------------|---------------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic Discharge (ESD) | Human body model (HBM), per AEC-Q100-002 <sup>(1)</sup> |                                 | ±2000 | V    |
|             |                               | Charged device model (CDM), per AEC-Q100-011            | All pins                        | ±500  |      |
|             |                               |                                                         | Corner balls (A1, A18, V1, V18) | ±750  |      |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

## 6.3 Electrostatic Discharge (ESD) Industrial Ratings

over recommended operating conditions (unless otherwise noted)

|             |                               |                                                                       |  | VALUE | UNIT |
|-------------|-------------------------------|-----------------------------------------------------------------------|--|-------|------|
| $V_{(ESD)}$ | Electrostatic Discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>     |  | ±2000 | V    |
|             |                               | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> |  | ±500  |      |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.4 Power-On Hours (POH) Summary

over recommended operating conditions (unless otherwise noted)<sup>(1) (2) (3)</sup>

| PARAMETER          | INDUSTRIAL                                              | EXTENDED AUTOMOTIVE                          |
|--------------------|---------------------------------------------------------|----------------------------------------------|
| POH @ Temp Profile | 100K @ 97°C (100% @ 97°C)<br>70K @ 105°C (100% @ 105°C) | 20K @ Automotive Temp Profile <sup>(4)</sup> |

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

(2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.

(3) POH is a function of voltage, temperature, and time. Usage at higher voltages and temperatures will result in a reduction in POH.

(4) See *Automotive Temperature Profile* section

### 6.4.1 Automotive Temperature Profile

| $T_J$ (°C) | HOURS | DAYS | YEARS  | PERCENT OF TIME |
|------------|-------|------|--------|-----------------|
| –40        | 1200  | ≈50  | ≈0.14  | 6%              |
| 75         | 4000  | ≈167 | ≈0.46  | 20%             |
| 95         | 13000 | ≈541 | ≈1.48  | 65%             |
| 130        | 1600  | ≈67  | ≈0.18  | 8%              |
| 150        | 200   | ≈8.5 | ≈0.023 | 1%              |
| Total      | 20000 | ≈833 | ≈2.28  | 100%            |

## 6.5 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

| PARAMETER              | DESCRIPTION                                                              | MIN                   | NOM   | MAX   | UNIT |
|------------------------|--------------------------------------------------------------------------|-----------------------|-------|-------|------|
| VDD                    | 1.2V SOC Core Supply                                                     | 1.140                 | 1.200 | 1.260 | V    |
| VDDAR1, VDDAR2, VDDAR3 | SRAM Array Supplies                                                      | 1.140                 | 1.200 | 1.260 | V    |
| VDDS18                 | 1.8V IO Bias Supply from Bias LDO routed through board                   | 1.710                 | 1.800 | 1.890 | V    |
| VDDS33                 | 3.3V IO Supply                                                           | 3.135                 | 3.300 | 3.465 | V    |
| VDDA18_OSC_PLL         | 1.8V Analog supply for PLL. Routed from the Analog LDO out through board | 1.710                 | 1.800 | 1.890 | V    |
| VDDA33                 | Analog 3.3V Supply                                                       | 3.135                 | 3.300 | 3.465 | V    |
| VDDA18                 | 1.8V Analog supply. Routed from 1.8V Analog LDO out through Board        | 1.710                 | 1.800 | 1.890 | V    |
| T <sub>J</sub>         | Operating junction temperature range                                     | Industrial A          |       | 105   | °C   |
|                        |                                                                          | Automotive I          |       | 125   |      |
|                        |                                                                          | Extended Automotive M |       | 150   |      |

## 6.6 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each Operating Performance Point (OPP) for processor clocks, device core clocks, and available memory.

| DEVICE | GRADE | RAM (MB) | R5FSS (MHz) | HSM (MHz) | ICSS (MHz) | INFRA <sup>(1)</sup> (MHz) |
|--------|-------|----------|-------------|-----------|------------|----------------------------|
| AM263x | N     | 1        | 400         | 200       | 200        | 200                        |
| AM263x | O     | 2        | 400         | 200       | 200        | 200                        |
| AM263x | P     | 2        | 200         | 200       | 200        | 200                        |

- (1) Infrastructure includes all other modules and IP integrated in the device (such as CBASS/Interconnect and other SoC level peripherals) unless otherwise noted in the table.

## 6.7 Power Consumption Summary

[Section 6.7.1, Power Consumption - Maximum](#) shows the maximum current consumed by each rail and should be used for power supply selection. [Section 6.7.2, Power Consumption - Typical](#) shows the typical power consumption by Module. [Section 6.7.3, Power Consumption - Traction Inverter](#) shows the nominal power consumption of the SoC at different Junction Temperatures for a Traction Inverter application.

For application specific power usage estimates, reference the [AM263x Power Estimation Tool Application Note](#).

### 6.7.1 Power Consumption - Maximum

over recommended operating conditions (unless otherwise noted)

| SUPPLY NAME  | PARAMETER                                      | MIN | MAX <sup>(1)</sup> | UNIT |
|--------------|------------------------------------------------|-----|--------------------|------|
| VDD + VDDARn | Maximum Current Rating for Core Domain         |     | 2.5                | A    |
| VDDS33       | Maximum Current Rating for IO supply           |     | 200                | mA   |
| VDDA33       | Maximum Current Rating for 3.3-V Analog supply |     | 100                | mA   |

(1) The maximum values show the maximum possible current needed for each power rail, and are only intended for power supply selection. For power consumption in typical applications, see *Power Consumption - Typical*.

### 6.7.2 Power Consumption - Typical

Typical usecase power consumption summary,  $T_J = 85^\circ\text{C}$

|                   | PARAMETER        | TYP  | MAX | UNIT |
|-------------------|------------------|------|-----|------|
| Power Consumption | Cores and Memory | 360  |     | mW   |
|                   | Infrastructure   | 424  |     | mW   |
|                   | Peripherals      | 258  |     | mW   |
|                   | Total            | 1042 |     | mW   |

### 6.7.3 Power Consumption - Traction Inverter

Traction Inverter Application Power Consumption Across Temperature

|                   | PARAMETER                 | TYP  | MAX | UNIT |
|-------------------|---------------------------|------|-----|------|
| Power Consumption | $T_J = 85^\circ\text{C}$  | 1042 |     | mW   |
|                   | $T_J = 105^\circ\text{C}$ | 1120 |     | mW   |
|                   | $T_J = 125^\circ\text{C}$ | 1232 |     | mW   |
|                   | $T_J = 150^\circ\text{C}$ | 1460 |     | mW   |

## 6.8 Electrical Characteristics

### Note

The interfaces or signals described in [Section 6.8.1 Digital and Analog IO Electrical Characteristics](#) through [Section 6.8.6 Power Management Unit \(PMU\)](#) correspond to the interfaces or signals available in multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

### 6.8.1 Digital and Analog IO Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER               |                                                                    | MIN                                      | TYP   | MAX   | UNIT |
|-------------------------|--------------------------------------------------------------------|------------------------------------------|-------|-------|------|
| <b>PORz IO</b>          |                                                                    |                                          |       |       |      |
| V <sub>IH</sub>         | High-Level Input Voltage                                           | 1.35                                     |       |       | V    |
| V <sub>IL</sub>         | Low-Level Input Voltage                                            |                                          |       | 0.5   | V    |
| V <sub>HYS</sub>        | Hysteresis Voltage at an Input                                     | 0.070                                    |       |       | V    |
| I <sub>L</sub>          | Input Leakage Current                                              | –2                                       |       | 2     | μA   |
| <b>Warm Reset IO</b>    |                                                                    |                                          |       |       |      |
| V <sub>IH</sub>         | High-Level Input Voltage                                           | 2                                        |       |       | V    |
| V <sub>IL</sub>         | Low-Level Input Voltage                                            |                                          |       | 0.8   | V    |
| V <sub>HYS</sub>        | Hysteresis Voltage at an Input                                     | 0.347                                    |       |       | V    |
| V <sub>OL</sub>         | Low Level Output Voltage, Driver Enabled : I <sub>OL</sub> = 6 mA  |                                          |       | 0.45  | V    |
| I <sub>L</sub>          | Input Leakage Current, Receiver Disabled, Pull Disabled            | –57                                      |       |       | μA   |
| <b>TCK IO</b>           |                                                                    |                                          |       |       |      |
| V <sub>IH</sub>         | High-Level Input Voltage                                           | 2.15                                     |       |       | V    |
| V <sub>IL</sub>         | Low-Level Input Voltage                                            |                                          |       | 0.55  | V    |
| V <sub>HYS</sub>        | Hysteresis Voltage at an Input                                     | 0.4                                      |       |       | V    |
| I <sub>L</sub>          | Input Leakage Current, Receiver Disabled, Pull Disabled            | –3.9                                     | 8.9   | 17.2  | μA   |
|                         | Input Leakage Current, Receiver Disabled, Pullup Enabled           |                                          | 106.9 | 128.2 | μA   |
|                         | Input Leakage Current, Receiver Disabled, Pulldown Enabled         |                                          | 100.3 | 130.3 | μA   |
| <b>I2C OD IOs</b>       |                                                                    |                                          |       |       |      |
| V <sub>IH</sub>         | High-Level Input Voltage                                           | 2                                        |       |       | V    |
| V <sub>IL</sub>         | Low-Level Input Voltage                                            |                                          |       | 0.8   | V    |
| V <sub>HYS</sub>        | Hysteresis Voltage at an Input                                     | 0.165                                    |       |       | V    |
| I <sub>L</sub>          | Input Leakage Current, Receiver Disabled, Pull Disabled            | –18                                      |       | 18    | μA   |
| V <sub>OL</sub>         | Low Level Output Voltage, Driver Enabled : I <sub>OL</sub> = 3 mA  |                                          |       | 0.45  | V    |
| <b>All Other LVCMOS</b> |                                                                    |                                          |       |       |      |
| V <sub>IH</sub>         | High- Level Input Voltage                                          | 2                                        |       |       | V    |
| V <sub>IL</sub>         | Low-Level Input Voltage                                            |                                          |       | 0.8   | V    |
| V <sub>HYS</sub>        | Hysteresis Voltage at an Input                                     | 0.265                                    |       |       | V    |
| V <sub>OL</sub>         | Low Level Output Voltage, Driver Enabled : I <sub>OL</sub> = 6 mA  |                                          |       | 0.45  | V    |
| V <sub>OH</sub>         | High Level Output Voltage, Driver Enabled : I <sub>OH</sub> = 6 mA | VDD <sub>S33</sub> <sup>(1)</sup> – 0.45 |       |       | V    |

over recommended operating conditions (unless otherwise noted)

| PARAMETER      |                                                            | MIN  | TYP  | MAX | UNIT |
|----------------|------------------------------------------------------------|------|------|-----|------|
| I <sub>L</sub> | Input Leakage Current, Receiver Disabled, Pull Disabled    | –18  |      | 18  | μA   |
|                | Input Leakage Current, Receiver Disabled, Pullup Enabled   | –243 | –100 | –19 | μA   |
|                | Input Leakage Current, Receiver Disabled, Pulldown Enabled | 51   | 100  | 210 | μA   |

(1) V<sub>DDS33</sub> is the voltage on the corresponding power-supply pin on the IC.

### 6.8.2 Analog-to-Digital Converter (ADC)

over operating junction temperature range (unless otherwise noted)

| PARAMETER                               | TEST CONDITIONS                                                      | MIN  | TYP  | MAX                        | UNIT |
|-----------------------------------------|----------------------------------------------------------------------|------|------|----------------------------|------|
| V <sub>REFHI</sub>                      |                                                                      | 1.71 | 1.8  | 1.89                       | V    |
| Input Conversion Range (Vin+, Vin-)     | Must be < V <sub>DDA33</sub>                                         | 0    |      | 32/18 × V <sub>REFHI</sub> | V    |
| Power-up time                           |                                                                      |      |      | 500                        | μs   |
| Gain error                              |                                                                      | –5   | ±3   | 5                          | LSBs |
| Offset error                            |                                                                      | –4   | ±2   | 4                          | LSBs |
| Channel-to-channel gain error           |                                                                      |      | ±4   |                            | LSBs |
| Channel-to-channel offset error         |                                                                      |      | ±2   |                            | LSBs |
| ADC-to-ADC gain error                   | Same reference group                                                 |      | ±4   |                            | LSBs |
| ADC-to-ADC offset error                 | Same reference group                                                 |      | ±2   |                            | LSBs |
| DNL                                     | Controlled environment to minimize input noise                       | –1   | ±0.5 | 1                          | LSBs |
| INL                                     | Controlled environment to minimize input noise                       | –2   | ±1.0 | 2                          | LSBs |
| SNR                                     | Controlled environment to minimize input noise                       |      | 68   |                            | dB   |
| ENOB (Synchronous Operation)            |                                                                      |      | 11   |                            | bits |
| ENOB (Asynchronous Operation)           |                                                                      |      | 9.7  |                            | bits |
| ADC-to-ADC isolation                    | Synchronous operation                                                | –10  |      | 10                         | LSBs |
| V <sub>REFHI</sub> input current        |                                                                      |      | 400  |                            | μA   |
| Conversion time                         |                                                                      |      |      | 250                        | ns   |
| Input Leakage                           |                                                                      |      | 0.1  | 5                          | μA   |
| Power supply (V <sub>DDA33</sub> )      |                                                                      | 3.13 | 3.3  | 3.46                       | V    |
| Power supply (V <sub>DDA18</sub> )      |                                                                      | 1.71 | 1.8  | 1.89                       | V    |
| Power Consumption (V <sub>DDA33</sub> ) |                                                                      |      | 200  |                            | μA   |
| Power Consumption (V <sub>DDA18</sub> ) |                                                                      |      | 700  |                            | μA   |
| Maximum ADCCLK frequency                | With 50% duty cycle. Minimum pulse width must be maintained at 7.5ns |      | 50   | 66.667                     | MHz  |
| Sample time                             |                                                                      | 75   |      |                            | ns   |

### 6.8.3 Comparator Subsystem A (CMPSSA)

| SUBGROUP   | PARAMETER                                         | MIN  | TYP                                                               | MAX  | UNIT     |
|------------|---------------------------------------------------|------|-------------------------------------------------------------------|------|----------|
| Comparator | Power-up time                                     |      |                                                                   | 10   | μs       |
|            | Comparator input range                            | 0.1  | VDDA33 <sup>(1)</sup> – 50mV                                      |      | V        |
|            | Input referred offset error                       | –20  |                                                                   | 20   | mV       |
|            | Hysteresis (H1)                                   |      | NA                                                                |      | LSB      |
|            | Hysteresis (H2)                                   |      | 15                                                                |      | LSB      |
|            | Hysteresis (H3)                                   |      | 35                                                                |      | LSB      |
|            | Hysteresis (H4)                                   |      | 55                                                                |      | LSB      |
|            | Propagation delay                                 |      | 21                                                                | 50   | ns       |
| DAC        | DAC_VREF reference voltage                        | 1.71 | 1.8                                                               | 1.89 | V        |
|            | DAC output range                                  | 0.1  | Minimum of<br>33/18 × DAC_VREF or<br>VDDA33 <sup>(1)</sup> – 50mV |      | V        |
|            | Static offset error                               | –45  |                                                                   | 45   | mV       |
|            | Static gain error                                 | –2   |                                                                   | 2    | % of FSR |
|            | Static DNL                                        | >–1  |                                                                   | 4    | LSB      |
|            | Static INL                                        | –16  |                                                                   | 16   | LSB      |
|            | Settling time                                     |      |                                                                   | 1    | μs       |
|            | Resolution                                        |      | 12                                                                |      | bits     |
|            | DAC output disturbance (comparator trip kickback) | –100 |                                                                   | 100  | LSB      |
|            | DAC output disturbance (comparator trip kickback) |      | 200                                                               |      | ns       |
|            | DAC_VREF loading                                  |      | 37                                                                |      | kΩ       |
| Common     | Input Leakage                                     |      | 0.1                                                               | 5    | μA       |
|            | Power supply (VDDA33)                             | 3.13 | 3.3                                                               | 3.46 | V        |
|            | Power supply (VDDA18)                             | 1.71 | 1.8                                                               | 1.89 | V        |
|            | Power consumption (VDDA33)                        |      | 900                                                               |      | μA       |
|            | Power consumption (VDDA18)                        |      | 120                                                               |      | μA       |
|            | Failsafe Input current injection                  |      |                                                                   | 10   | mA       |

(1) VDDA33 is the voltage on the corresponding power-supply pin(s) on the IC.

#### 6.8.4 Comparator Subsystem B (CMPSSB)

| SUBGROUP   | PARAMETER                                         | MIN  | TYP                                                               | MAX  | UNIT     |
|------------|---------------------------------------------------|------|-------------------------------------------------------------------|------|----------|
| Comparator | Power-up time                                     |      |                                                                   | 10   | μs       |
|            | Comparator input range                            | 0.1  | VDDA33 <sup>(1)</sup> – 50mV                                      |      | V        |
|            | Input referred offset error                       | –20  |                                                                   | 20   | mV       |
|            | Hysteresis (H1)                                   |      | NA                                                                |      | LSB      |
|            | Hysteresis (H2)                                   |      | 15                                                                |      | LSB      |
|            | Hysteresis (H3)                                   |      | 35                                                                |      | LSB      |
|            | Hysteresis (H4)                                   |      | 55                                                                |      | LSB      |
|            | Propagation delay                                 |      | 21                                                                | 50   | ns       |
| DAC        | DAC_VREF reference voltage                        | 1.71 | 1.8                                                               | 1.89 | V        |
|            | DAC output range                                  | 0.1  | Minimum of<br>33/18 × DAC_VREF or<br>VDDA33 <sup>(1)</sup> – 50mV |      | V        |
|            | Static offset error                               | –45  |                                                                   | 45   | mV       |
|            | Static gain error                                 | –2   |                                                                   | 2    | % of FSR |
|            | Static DNL                                        | >–1  |                                                                   | 4    | LSB      |
|            | Static INL                                        | –16  |                                                                   | 16   | LSB      |
|            | Settling time                                     |      |                                                                   | 1    | μs       |
|            | Resolution                                        |      | 12                                                                |      | bits     |
|            | DAC output disturbance (comparator trip kickback) | –100 |                                                                   | 100  | LSB      |
|            | DAC output disturbance (comparator trip kickback) |      | 200                                                               |      | ns       |
|            | DAC_VREF loading                                  |      | 37                                                                |      | kΩ       |
|            |                                                   |      |                                                                   |      |          |
| Common     | Input Leakage                                     |      | 0.1                                                               | 5    | μA       |
|            | Power supply (VDDA33)                             | 3.13 | 3.3                                                               | 3.46 | V        |
|            | Power supply (VDDA18)                             | 1.71 | 1.8                                                               | 1.89 | V        |
|            | Power consumption (VDDA33)                        |      | 900                                                               |      | μA       |
|            | Power consumption (VDDA18)                        |      | 120                                                               |      | μA       |
|            | Failsafe input current injection                  |      |                                                                   | 10   | mA       |

(1) VDDA33 is the voltage on the corresponding power-supply pin(s) on the IC.

### 6.8.5 Digital-to-Analog Converter (DAC)

over operating junction temperature range (unless otherwise noted)

| PARAMETER                      | TEST CONDITIONS                                         | MIN  | TYP                         | MAX  | UNIT     |
|--------------------------------|---------------------------------------------------------|------|-----------------------------|------|----------|
| Power-up time                  |                                                         |      |                             | 1    | μs       |
| DAC_VREF                       |                                                         | 1.71 | 1.8                         | 1.89 | V        |
| Voltage output range           |                                                         | 0.3  | VDDA33 <sup>(1)</sup> – 0.3 |      | V        |
| Trimmed offset error           | Offset is checked at Midpoint (code 2048)               | –10  |                             | 10   | mV       |
| Gain error                     | DAC_VREF = 1.8V                                         | –2.5 |                             | 2.5  | % of FSR |
| DNL                            | Endpoint corrected                                      | –1   |                             | 1    | LSB      |
| INL                            | Endpoint corrected                                      | –20  |                             | 20   | LSB      |
| Settling time                  | Settling to 2 LSBs (~1.6mV) after 0.3V-to-3V transition |      | 2                           |      | μs       |
| Resolution                     |                                                         |      | 12                          |      | bits     |
| Capacitive load                | Output drive capability                                 |      |                             | 100  | pF       |
| Resistive load                 | Output drive capability                                 | 5    |                             |      | kΩ       |
| DAC_VREF loading               | DAC_VREF                                                |      | 64                          |      | kΩ       |
| Output noise (100 Hz- 100 KHz) | Integrated noise from 100 Hz to 100 kHz                 |      | 1                           |      | mVrms    |
| SNR @ 1KHz                     | 2MHz DACVALA update rate, 200kHz output filter          |      | 60                          |      | dB       |
| Power supply (VDDA33)          |                                                         | 3.13 | 3.3                         | 3.46 | V        |
| Power supply (VDDA18)          |                                                         | 1.71 | 1.8                         | 1.89 | V        |
| Power Consumption (VDDA33)     |                                                         |      | 850                         |      | μA       |
| Power Consumption (VDDA18)     |                                                         |      | 35                          |      | μA       |

(1) VDDA33 is the voltage on the corresponding power-supply pin(s) on the IC.

### 6.8.6 Power Management Unit (PMU)

over operating junction temperature range (unless otherwise noted)

| GROUP         | PARAMETER                       | MIN   | TYP | MAX   | UNIT |
|---------------|---------------------------------|-------|-----|-------|------|
| PMU           | Power supply (VDDA33)           | 3.1   | 3.3 | 3.46  | V    |
| Bandgap       | V <sub>REF</sub> trimmed        | 0.886 | 0.9 | 0.914 | V    |
| 1.8V LDO      | DC accuracy                     | 1.764 | 1.8 | 1.836 | V    |
|               | Transient load regulation       | 1.71  | 1.8 | 1.89  | V    |
|               | DC Load regulation              |       |     | 5     | mV   |
|               | Load current                    | 0     |     | 60    | mA   |
|               | Power up time                   |       |     | 800   | μs   |
|               | Inrush current                  |       |     | 150   | mA   |
|               | External decoupling capacitance | –20%  | 4.7 | 20%   | μF   |
| ADC Reference | Load Regulation                 |       | ±1  |       | mV   |
| ADC Reference | DC accuracy                     | 1.764 | 1.8 | 1.836 | V    |
|               | Power up time                   |       |     | 800   | μs   |
|               | Inrush current                  |       |     | 80    | mA   |
|               | External decoupling capacitance | –20%  | 4.7 | 20%   | μF   |

### 6.8.7 Safety Comparators

| PARAMETER |                                  |                 | MIN   | TYP   | MAX   | UNIT |
|-----------|----------------------------------|-----------------|-------|-------|-------|------|
| C0        | C0: 1.8-V Monitor Threshold      |                 | 1.40  | 1.5   | 1.6   | V    |
| C1        | BGAP Monitor                     | Lower Threshold | 0.75  | 0.8   | 0.85  | V    |
|           |                                  | Upper Threshold | 0.935 | 1     | 1.065 | V    |
| C2        | Monitors 1.8-V Supply vs BGAP    | Lower Threshold | 1.47  | 1.52  | 1.57  | V    |
|           |                                  | Upper Threshold | 2.13  | 2.195 | 2.26  | V    |
| C3        | Monitors 1.2-V vs BGAP           | Lower Threshold | 0.98  | 1.011 | 1.041 | V    |
|           |                                  | Upper Threshold | 1.407 | 1.451 | 1.494 | V    |
| C4        | Vref Monitor (ROK0)              | Lower Threshold | 1.56  | 1.61  | 1.66  | V    |
|           |                                  | Upper Threshold | 2.09  | 2.16  | 2.22  | V    |
| C5        | Monitors IO Bias Supply vs BGAP  | Lower Threshold | 1.47  | 1.52  | 1.57  | V    |
|           |                                  | Upper Threshold | 2.13  | 2.195 | 2.26  | V    |
| C6        | Vref Monitor (ROK0B)             | Lower Threshold | 1.56  | 1.61  | 1.66  | V    |
|           |                                  | Upper Threshold | 2.09  | 2.16  | 2.22  | V    |
| C7        | System Supply Monitor (VSYS_MON) | Lower Threshold | 0.873 | 0.9   | 0.927 | V    |
| C8        | UnderVoltage Threshold           |                 | 2.59  | 2.77  | 2.95  | V    |
| C9        | Vref Monitor (ROK1)              | Lower Threshold | 1.56  | 1.61  | 1.66  | V    |
|           |                                  | Upper Threshold | 2.09  | 2.16  | 2.22  | V    |

## 6.9 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses.

### 6.9.1 VPP Specifications

over recommended operating conditions (unless otherwise noted)

| PARAMETER   | DESCRIPTION                                                          | TEST CONDITIONS     | MIN           | NOM   | MAX   | UNIT |
|-------------|----------------------------------------------------------------------|---------------------|---------------|-------|-------|------|
| VDD         | Supply voltage range for the core domain during OTP operation        | Normal Operation    | 1.140         | 1.200 | 1.260 | V    |
| VPP         | Supply voltage range for the eFuse ROM domain                        | Normal Operation    | No Connection |       |       | V    |
|             | Supply voltage range for the eFuse ROM domain during OTP programming | OTP Programming     | 1.65          | 1.7   | 1.75  | V    |
| $I_{(VPP)}$ | VPP Current                                                          | $I_{(VPP)}$         |               |       | 100   | mA   |
| $T_A$       | Ambient Temperature                                                  | Ambient Temperature | 0             | 30    | 50    | °C   |

### 6.9.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.
- The VPP power supply must be ramped up after the proper device power-on sequence (for more details, see [Section 6.11.2.1, Power-On and Reset Sequencing](#)).

### 6.9.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-on sequencing. No voltage should be applied on the VPP terminal during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP terminal according to the specification in [Section 6.9.1, VPP Specifications](#).
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP terminal.

### 6.9.4 Impact to Your Hardware Warranty

You accept that e-Fusing the TI Devices with security keys permanently alters them. You acknowledge that the e-Fuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI Device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI Device inoperable and TI will be unable to confirm whether the TI Devices conformed to their specifications prior to the attempted e-Fuse.

CONSEQUENTLY, TI WILL HAVE NO LIABILITY (WARRANTY OR OTHERWISE) FOR ANY TI DEVICES THAT HAVE BEEN e-FUSED WITH SECURITY KEYS.

## 6.10 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the  $T_J$  value identified in [Section 6.5, Recommended Operating Conditions](#).

### 6.10.1 Package Thermal Characteristics

It is recommended to perform thermal simulations at the system level with the worst-case device power consumption.

| PARAMETER   | DESCRIPTION             | °C/W <sup>(1) (2)</sup> | AIR FLOW (m/s) <sup>(3)</sup> |
|-------------|-------------------------|-------------------------|-------------------------------|
| $RO_{JC}$   | Junction-to-case        | 5.6                     | N/A                           |
| $RO_{JB}$   | Junction-to-board       | 5.7                     | N/A                           |
| $RO_{JA}$   | Junction-to-free air    | 18.6                    | 0                             |
| $RO_{JA}$   | Junction-to-moving air  | 12.9                    | 1                             |
|             |                         | 11.8                    | 2                             |
|             |                         | 11.1                    | 3                             |
| $\Psi_{JT}$ | Junction-to-package top | 0.1                     | 0                             |
|             |                         | 0.4                     | 1                             |
|             |                         | 0.5                     | 2                             |
|             |                         | 0.6                     | 3                             |
| $\Psi_{JB}$ | Junction-to-board       | 5.6                     | 0                             |
|             |                         | 5.7                     | 1                             |
|             |                         | 5.7                     | 2                             |
|             |                         | 5.6                     | 3                             |

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [ $RO_{JC}$ ] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Packages

(2) °C/W = degrees Celsius per watt

(3) m/s = meters per second

## 6.11 Timing and Switching Characteristics

### Note

The default SLEWRATE settings in each pad configuration register must be used to provide timings, unless specific instructions are given otherwise.

### 6.11.1 Timing Parameters and Information

The timing parameter symbols used in *Timing and Switching Characteristics* sections are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in [Table 6-1](#):

**Table 6-1. Timing Parameters Subscripts**

| SYMBOL | PARAMETER                              |
|--------|----------------------------------------|
| c      | Cycle time (period)                    |
| d      | Delay time                             |
| dis    | Disable time                           |
| en     | Enable time                            |
| h      | Hold time                              |
| su     | Setup time                             |
| START  | Start bit                              |
| t      | Transition time                        |
| v      | Valid time                             |
| w      | Pulse duration (width)                 |
| X      | Unknown, changing, or don't care level |
| F      | Fall time                              |
| H      | High                                   |
| L      | Low                                    |
| R      | Rise time                              |
| V      | Valid                                  |
| IV     | Invalid                                |
| AE     | Active Edge                            |
| FE     | First Edge                             |
| LE     | Last Edge                              |
| Z      | High impedance                         |

## 6.11.2 Power Supply Sequencing

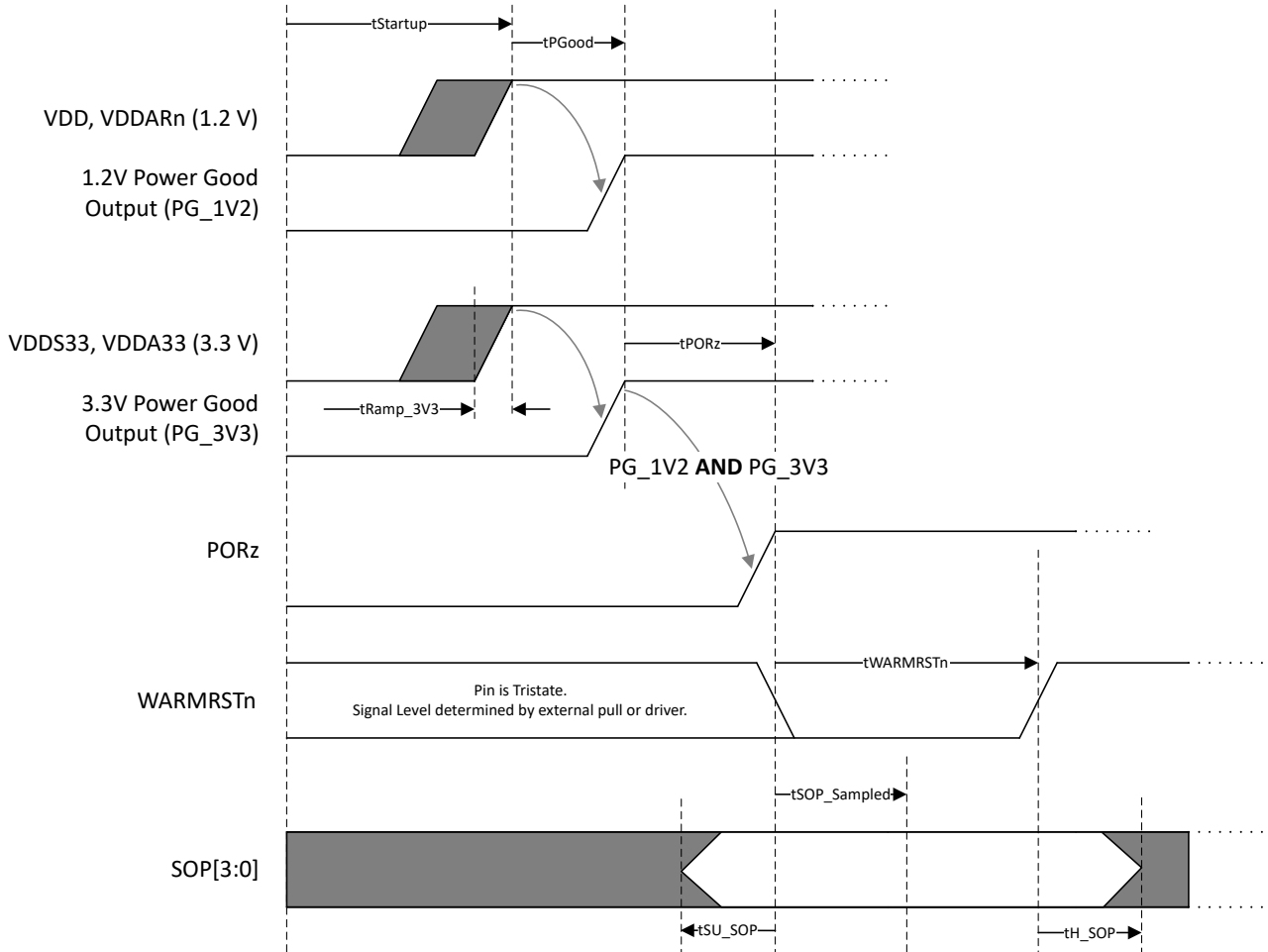
This section describes power supply sequencing required to provide proper device operation.

### 6.11.2.1 Power-On and Reset Sequencing

AM263x attempts to simplify the power reset requirements from previous Sitara MCU devices. There is no sequencing requirement with respect to the primary core digital VDD 1.2-V and I/O power 3.3-V rails. A pair of on-die LDO are supplied through the VDDS33 power net. These on-die LDO generate the required VDDS1V8 and VDDA1V8 1.8-V digital and analog power. The AM263x does require the minimum ramp time be respected for 3.3-V power-on. Additional PORz and SOP boot mode latch timing must be respected by the EVM design as well. [Figure 6-1](#) describes the device power-on sequencing.

**Table 6-2. AM263x Power-On Sequencing**

| PARAMETER                |                                                                                                                                                                                                                                                                | MIN | MAX | UNIT |
|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|
| t <sub>Startup</sub>     | Time for 1.2-V and 3.3-V DC-DC converters to startup after being enabled. This is an arbitrary amount of time - no constraint imposed by the device.                                                                                                           | –   | –   | ms   |
| t <sub>PGood</sub>       | Time for Power Good signals to be generated from DC-DC converters after rails are stable. This is an arbitrary amount of time - no constraint imposed by the device.                                                                                           | –   | –   | ms   |
| t <sub>Ramp_3V3</sub>    | Ramp time of the VDDS3V3 and VDDA3V3 supplies. This is a requirement imposed by the device.                                                                                                                                                                    | 0.1 | –   | ms   |
| t <sub>SOP_Sampled</sub> | Time from PORz de-assertion until the SOP[3:0] pins are sampled. This is a device internal pentameter. Sampling happens when the internally generated supplies are stable. For information only. Refer to TSU_SOP and TH_SOP parameters for application usage. | 0   | –   | ms   |
| t <sub>SU_SOP</sub>      | Setup time for SOP relative to PORz assertion.                                                                                                                                                                                                                 | 10  | –   | μs   |
| t <sub>H_SOP</sub>       | Hold time for SOP relative to WARMRSTn deassertion.                                                                                                                                                                                                            | 0   | –   | μs   |
| t <sub>WARMRSTn</sub>    | Time from PORz de-assertion until the device de-asserts the WARMRESETn signal.                                                                                                                                                                                 | 2.0 | –   | ms   |



**Figure 6-1. Power-On Sequencing**

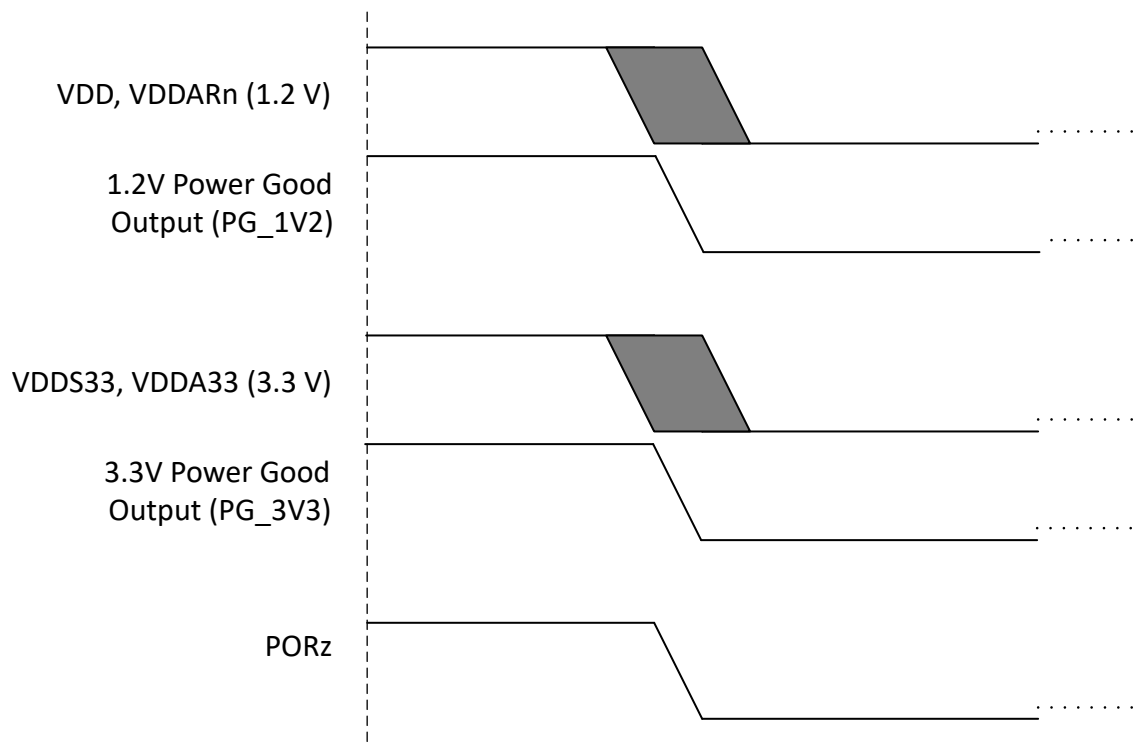
#### 6.11.2.1.1 Power Reset Sequence Description

The following set of steps shall occur on the EVM and AM263x to boot the device from power-on reset.

1. PORz is held low by the external power supply monitor
2. VDD core digital 1.2V and VDDS3V3/VDDA3V3 3.3V supplies ramp to their nominal voltages
  - a. This requires a logical AND be applied to the power good signal generated from each supply
3. SOP[3:0] pins held in their boot latch state
4. After PCB supplied power nets are stable, the external supply monitor will de-assert PORz
5. Device will startup 1.8V on-die LDO
6. After internal supply monitors show externally and internally generated supplies are stable, the SOP[3:0] pin states are latched
7. R5F cores are unhalted and SOP selected boot ROM execution begins

### 6.11.2.2 Power-Down Sequencing

Figure 6-2 describes the device power-down sequencing. The order of AM263x 1.2V and 3.3V does not matter.



**Figure 6-2. Power-Down Sequencing**

### 6.11.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

#### 6.11.3.1 System Timing Conditions

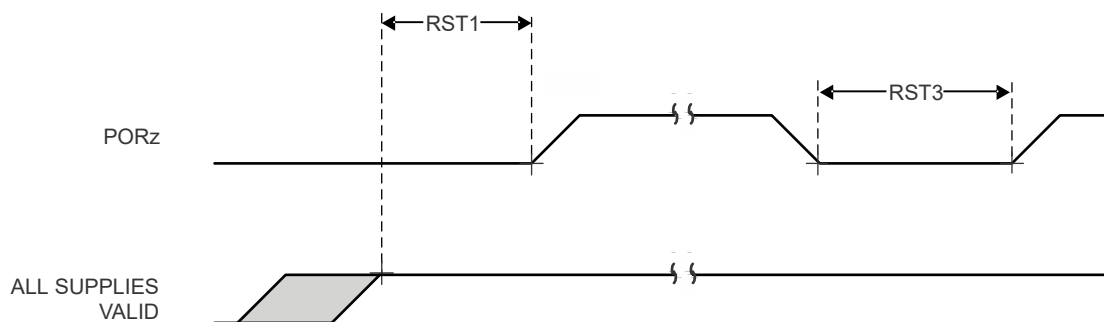
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 0.5 | 2   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 3   | 30  | pF   |

#### 6.11.3.2 Reset Timing

Tables and figures provided in this section define timing requirements and switching characteristics for reset related signals.

##### 6.11.3.2.1 PORz Timing Requirements

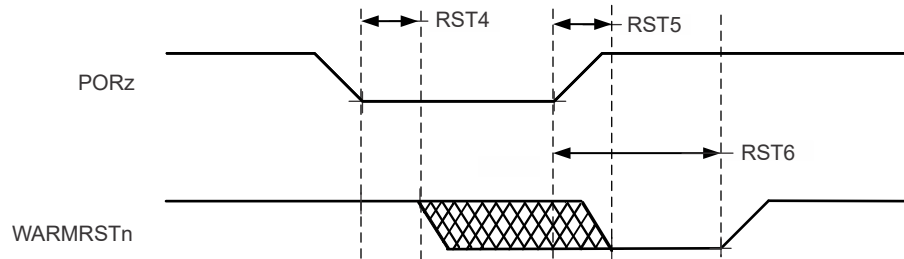
| NO.  | PARAMETER                     | DESCRIPTION                                                                                                  | MIN  | MAX | UNIT |
|------|-------------------------------|--------------------------------------------------------------------------------------------------------------|------|-----|------|
| RST1 | $t_{h(SUPPLIES\_VALID-PORz)}$ | Hold time, PORz active (low) at Power-up after supplies valid (using external crystal)                       | 0    |     | ns   |
| RST3 | $t_{w(PORzL)}$                | Pulse Width minimum, PORz low after Power-up (without removal of Power or system reference clock XTAL_XI/XO) | 1000 |     | ns   |



**Figure 6-3. PORz Timing Requirements**

##### 6.11.3.2.2 WARMRSTn Switching Characteristics

| NO.  | PARAMETER                | DESCRIPTION                                                  | MIN     | MAX     | UNIT |
|------|--------------------------|--------------------------------------------------------------|---------|---------|------|
| RST4 | $t_{d(PORzL-WARMRSTnZ)}$ | Delay time, PORz active (low) to WARMRSTn high impedance     | 0       | 0       | ns   |
| RST5 | $t_{d(PORzH-WARMRSTnL)}$ | Delay time, PORz inactive (high) to WARMRSTn active (low)    | 0       | 0       | ns   |
| RST6 | $t_{d(PORzH-WARMRSTnH)}$ | Delay time, PORz inactive (high) to WARMRSTn inactive (high) | 2000000 | 6000000 | ns   |

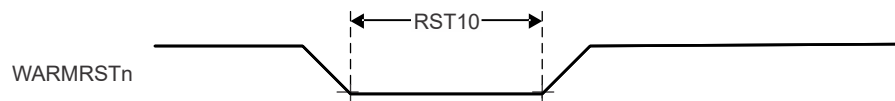


**Figure 6-4. WARMRSTn Switching Characteristics**

#### 6.11.3.2.3 WARMRSTn Timing Requirements

| NO.   | PARAMETER                         | DESCRIPTION                                | MIN | MAX      | UNIT |
|-------|-----------------------------------|--------------------------------------------|-----|----------|------|
| RST10 | $t_{w(WARMRSTnL)}$ <sup>(1)</sup> | Pulse Width minimum, WARMRSTn active (low) | 500 | 16384000 | ns   |

- (1) This timing parameter is controlled by the TOP\_RCM.WARM\_RSTTIME1/2/3 registers. See the Reset section of the Technical Reference Manual for more details.



**Figure 6-5. WARMRSTn Timing Requirements and Switching Characteristics**

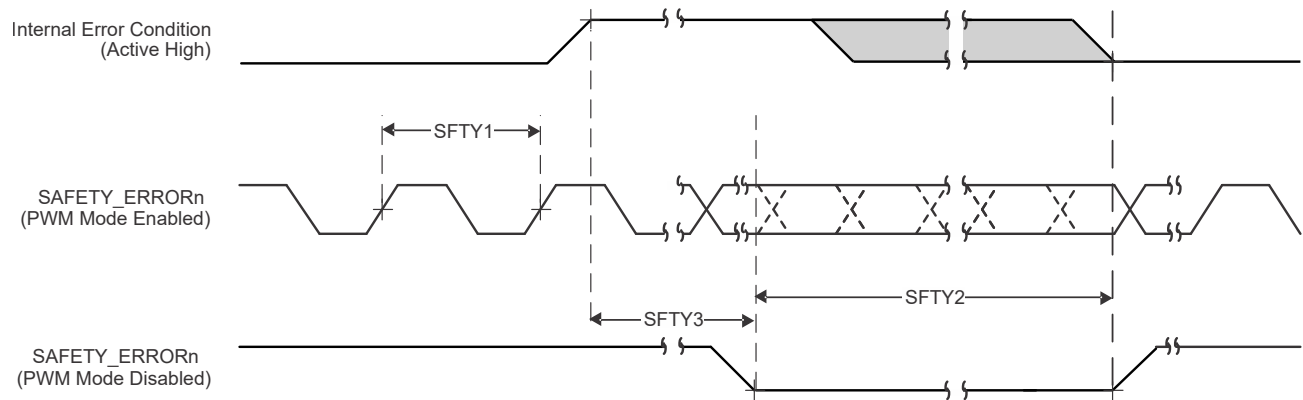
#### 6.11.3.3 Safety Signal Timing

Tables and figures provided in this section define switching characteristics for SAFETY\_ERRORn.

##### 6.11.3.3.1 SAFETY\_ERRORn Switching Characteristics

| NO.   | PARAMETER                                  | DESCRIPTION                                                                  | MIN                                                   | MAX | UNIT |
|-------|--------------------------------------------|------------------------------------------------------------------------------|-------------------------------------------------------|-----|------|
| SFTY1 | $t_{c(SAFETY\_ERRORn)}$                    | Cycle time minimum, SAFETY_ERRORn (PWM mode enabled)                         | $(P^{(1)} \times H^{(3)}) + (P^{(1)} \times L^{(4)})$ |     | ns   |
| SFTY2 | $t_{w(SAFETY\_ERRORn)}$                    | Pulse width minimum, SAFETY_ERRORn active (PWM mode disabled) <sup>(5)</sup> | $P^{(1)} \times R^{(2)}$                              |     | ns   |
| SFTY3 | $t_{d(ERROR\_CONDITION\_SAFETY\_ERRORnL)}$ | Delay time, ERROR_CONDITION to SAFETY_ERRORn active <sup>(5)</sup>           | $50 \times P^{(1)}$                                   |     | ns   |

- (1) P = ESM functional clock  
(2) R = Error Pin Counter Pre-Load Register count value  
(3) H = Error Pin PWM High Pre-Load Register count value  
(4) L = Error Pin PWM Low Pre-Load Register count value  
(5) When PWM mode is enabled, SAFETY\_ERRORn stops toggling after SFTY3 and will maintain its value (either high or low) until the error is cleared. When PWM mode is disabled, SAFETY\_ERRORn is active low



**Figure 6-6. MCU\_SAFETY\_ERRORn Timing Requirements and Switching Characteristics**

## 6.11.4 Clock Specifications

### 6.11.4.1 Input Clocks / Oscillators

#### 6.11.4.1.1 Crystal Oscillator (XTAL) Parameters

| PARAMETER           |                                                                          | MIN    | TYP | MAX   | UNIT |
|---------------------|--------------------------------------------------------------------------|--------|-----|-------|------|
| F <sub>xtal</sub>   | Crystal Parallel Resonance Frequency (Fundamental mode oscillation only) | -50ppm | 25  | 50ppm | MHz  |
| Duty Cycle          | Duty cycle output of XTAL                                                | 45     | 50  | 55    | %    |
| CC1                 | Capacitance of C <sub>L1</sub> + C <sub>PCBXI</sub>                      | 12     |     | 24    | pF   |
| CC2                 | Capacitance of C <sub>L2</sub> + C <sub>PCBXO</sub>                      | 12     |     | 24    | pF   |
| C <sub>shunt</sub>  | Crystal Circuit Shunt Capacitance                                        |        |     | 5     | pF   |
| ESR <sub>xtal</sub> | Crystal Effective Series Resistance                                      |        |     | 46    | Ω    |

#### 6.11.4.1.2 External Clock Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER         |                              | MIN                                                                                          | TYP  | MAX | UNIT |
|-------------------|------------------------------|----------------------------------------------------------------------------------------------|------|-----|------|
| C <sub>Pkg</sub>  | Shunt Capacitance of package |                                                                                              | 0.01 |     | pF   |
| P <sub>xtal</sub> | Power dissipation            | $0.5 \times \text{ESR} \times (2 \times \pi \times F_{\text{xtal}} \times C_L \times 1.8)^2$ |      |     | W    |
| t <sub>s</sub>    | Startup time                 |                                                                                              | 1.5  |     | ms   |

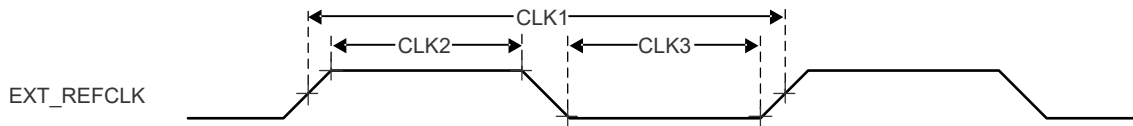
### 6.11.4.2 Clock Timing

Tables and figures provided in this section define timing requirements and switching characteristics for clock signals.

#### 6.11.4.2.1 Clock Timing Requirements

| NO.  | PARAMETER        | DESCRIPTION                             | MIN                     | MAX                     | UNIT |
|------|------------------|-----------------------------------------|-------------------------|-------------------------|------|
| CLK1 | tc(EXT_REFCLK)   | Cycle time minimum, EXT_REFCLK          | 10                      |                         | ns   |
| CLK2 | tw(EXT_REFCLK H) | Pulse Duration minimum, EXT_REFCLK high | E <sup>(1)</sup> × 0.45 | E <sup>(1)</sup> × 0.55 | ns   |
| CLK3 | tw(EXT_REFCLK L) | Pulse Duration minimum, EXT_REFCLK low  | E <sup>(1)</sup> × 0.45 | E <sup>(1)</sup> × 0.55 | ns   |

(1) E = EXT\_REFCLK cycle time



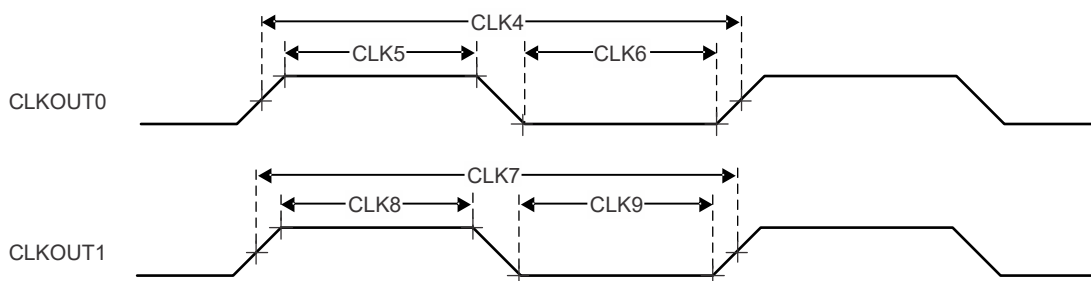
**Figure 6-7. Clock Timing Requirements**

#### 6.11.4.2.2 Clock Switching Characteristics

| NO.  | PARAMETER                | DESCRIPTION                          | MIN                  | MAX                  | UNIT |
|------|--------------------------|--------------------------------------|----------------------|----------------------|------|
| CLK4 | $t_{c}(\text{CLKOUT0})$  | Cycle time minimum, CLKOUT0          | 10                   |                      | ns   |
| CLK5 | $t_{w}(\text{CLKOUT0H})$ | Pulse Duration minimum, CLKOUT0 high | $A^{(1)} \times 0.4$ | $A^{(1)} \times 0.6$ | ns   |
| CLK6 | $t_{w}(\text{CLKOUT0L})$ | Pulse Duration minimum, CLKOUT0 low  | $A^{(1)} \times 0.4$ | $A^{(1)} \times 0.6$ | ns   |
| CLK7 | $t_{c}(\text{CLKOUT1})$  | Cycle time minimum, CLKOUT1          | 10                   |                      | ns   |
| CLK8 | $t_{w}(\text{CLKOUT1H})$ | Pulse Duration minimum, CLKOUT1 high | $B^{(2)} \times 0.4$ | $B^{(2)} \times 0.6$ | ns   |
| CLK9 | $t_{w}(\text{CLKOUT1L})$ | Pulse Duration minimum, CLKOUT1 low  | $B^{(2)} \times 0.4$ | $B^{(2)} \times 0.6$ | ns   |

(1) A = CLKOUT0 cycle time

(2) B = CLKOUT1 cycle time



**Figure 6-8. Clock Switching Characteristics**

## 6.11.5 Peripherals

### 6.11.5.1 2-port Gigabit Ethernet MAC (CPSW)

#### Note

The CPSW supports two external Ethernet ports and one internal port.

For more details about features and additional description information on the device CPSW (2-port Gigabit Ethernet MAC), see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

#### 6.11.5.1.1 CPSW MDIO Timing

##### 6.11.5.1.1.1 CPSW MDIO Timing Conditions

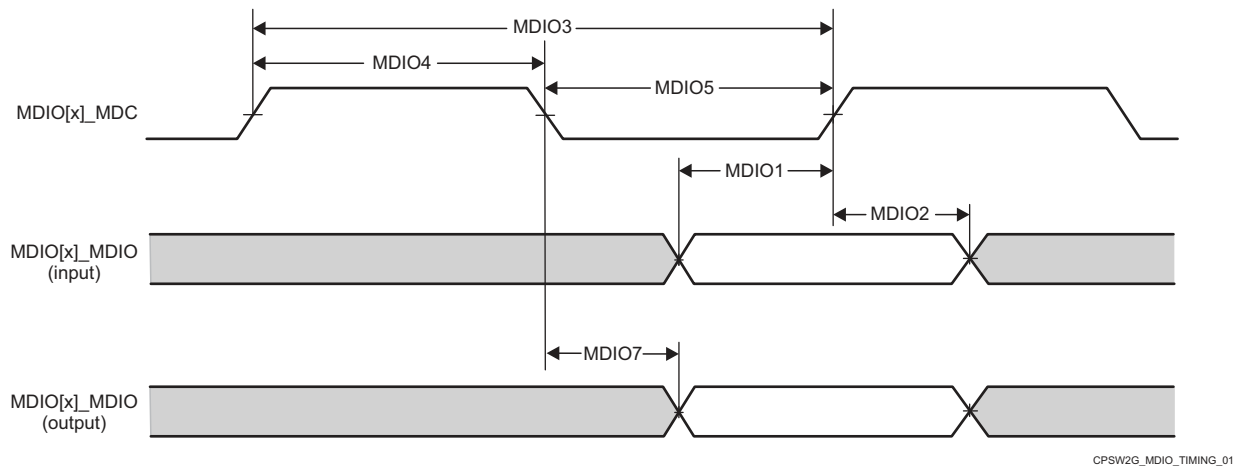
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 0.9 | 3.6 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 10  | 470 | pF   |

##### 6.11.5.1.1.2 CPSW MDIO Timing Requirements

| NO.   | PARAMETER                  | DESCRIPTION                                      | MIN | MAX | UNIT |
|-------|----------------------------|--------------------------------------------------|-----|-----|------|
| MDIO1 | t <sub>su</sub> (MDIO-MDC) | Setup time, MDIO_DATA valid before MDIO_CLK high | 45  |     | ns   |
| MDIO2 | t <sub>h</sub> (MDC-MDIO)  | Hold time, MDIO_DATA valid after MDIO_CLK high   | 0   |     | ns   |

##### 6.11.5.1.1.3 CPSW MDIO Switching Characteristics

| NO.   | PARAMETER                 | DESCRIPTION                                 | MIN | MAX | UNIT |
|-------|---------------------------|---------------------------------------------|-----|-----|------|
| MDIO3 | t <sub>c</sub> (MDC)      | Cycle time, MDIO_CLK                        | 400 |     | ns   |
| MDIO4 | t <sub>w</sub> (MDCH)     | Pulse duration, MDIO_CLK high               | 160 |     | ns   |
| MDIO5 | t <sub>w</sub> (MDCL)     | Pulse duration, MDIO_CLK low                | 160 |     | ns   |
| MDIO7 | t <sub>d</sub> (MDC_MDIO) | Delay time, MDIO_CLK low to MDIO_DATA valid | -10 | 10  | ns   |



CPSW2G\_MDIO\_TIMING\_01

**Figure 6-9. CPSW MDIO Timing Requirements and Switching Characteristics**

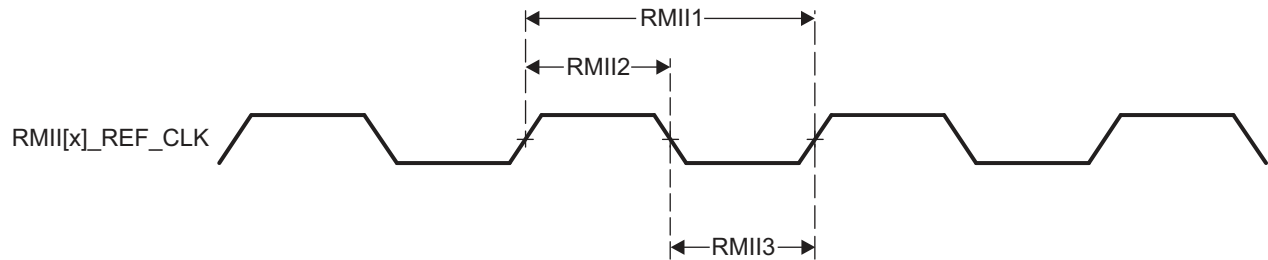
### 6.11.5.1.2 CPSW RMII Timing

#### 6.11.5.1.2.1 CPSW RMII Timing Conditions

| PARAMETER                |                         |            |  | MIN | MAX | UNIT |
|--------------------------|-------------------------|------------|--|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |            |  |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | VDD = 3.3V |  | 0.4 | 1.2 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |            |  |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance |            |  | 3   | 25  | pF   |

#### 6.11.5.1.2.2 CPSW RMII[x]\_REFCLK Timing Requirements - RMII Mode

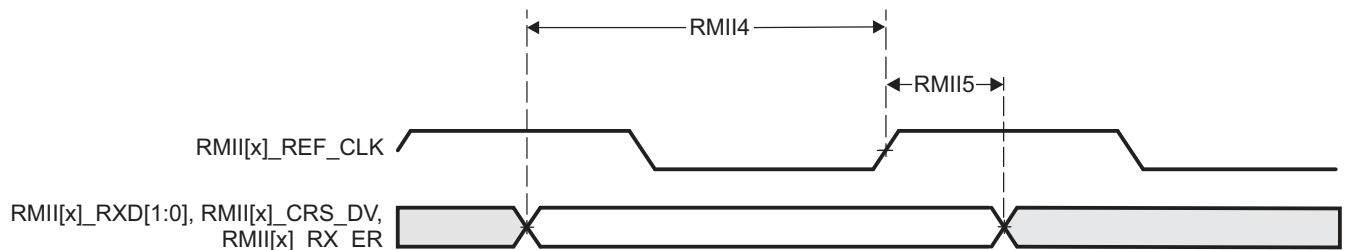
| NO.   | PARAMETER                 | DESCRIPTION                  | MIN    | MAX | UNIT |
|-------|---------------------------|------------------------------|--------|-----|------|
| RMII1 | t <sub>G</sub> (REF_CLK)  | Cycle time, REF_CLK          | 19.999 | 20  | ns   |
| RMII2 | t <sub>W</sub> (REF_CLKH) | Pulse duration, REF_CLK High | 7      | 13  | ns   |
| RMII3 | t <sub>W</sub> (REF_CLKL) | Pulse duration, REF_CLK Low  | 7      | 13  | ns   |



**Figure 6-10. CPSW RMII[x]\_REF\_CLK Timing Requirements – RMII Mode**

#### 6.11.5.1.2.3 CPSW RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, and RMII[x]\_RXER Timing Requirements - RMII Mode

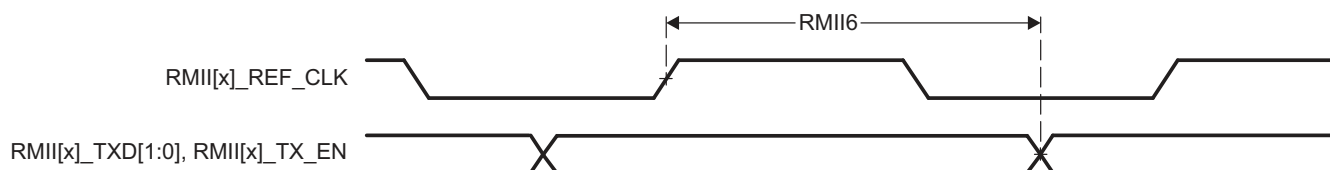
| NO.   | PARAMETER                        | DESCRIPTION                               | MIN | MAX | UNIT |
|-------|----------------------------------|-------------------------------------------|-----|-----|------|
| RMII4 | t <sub>SU</sub> (RXD-REF_CLK)    | Setup time, RXD[1:0] valid before REF_CLK | 4   |     | ns   |
|       | t <sub>SU</sub> (CRS_DV-REF_CLK) | Setup time, CRS_DV valid before REF_CLK   | 4   |     | ns   |
|       | t <sub>SU</sub> (RX_ER-REF_CLK)  | Setup time, RX_ER valid before REF_CLK    | 4   |     | ns   |
| RMII5 | t <sub>H</sub> (REF_CLK-RXD)     | Hold time, RXD[1:0] valid after REF_CLK   | 2   |     | ns   |
|       | t <sub>H</sub> (REF_CLK-CRS_DV)  | Hold time, CRS_DV valid after REF_CLK     | 2   |     | ns   |
|       | t <sub>H</sub> (REF_CLK-RX_ER)   | Hold time, RX_ER valid after REF_CLK      | 2   |     | ns   |



**Figure 6-11. CPSW RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, RMII[x]\_RX\_ER Timing Requirements – RMII Mode**

#### 6.11.5.1.2.4 CPSW RMII[x]\_TXD[1:0], and RMII[x]\_TXEN Switching Characteristics - RMII Mode

| NO.   | PARAMETER              | DESCRIPTION                                | MIN | MAX | UNIT |
|-------|------------------------|--------------------------------------------|-----|-----|------|
| RMII6 | $t_{d(REF\_CLK-TXD)}$  | Delay time, REF_CLK High to TXD[1:0] valid | 2   | 10  | ns   |
|       | $t_{d(REF\_CLK-TXEN)}$ | Delay time, REF_CLK to TXEN valid          | 2   | 10  | ns   |



**Figure 6-12. CPSW RMII[x]\_TXD[1:0], and RMII[x]\_TX\_EN Switching Characteristics – RMII Mode**

### 6.11.5.1.3 CPSW RGMII Timing

#### 6.11.5.1.3.1 CPSW RGMII Timing Conditions

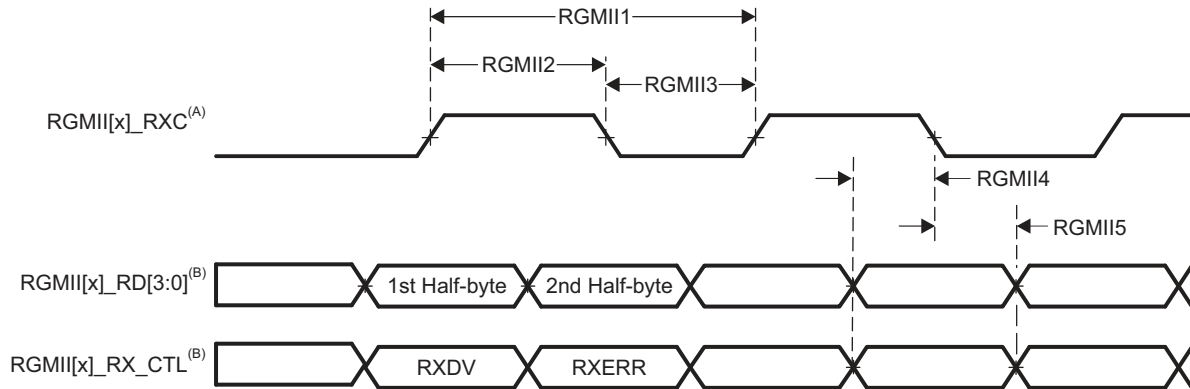
| PARAMETER                             |                                              |                                                     | MIN  | MAX | UNIT |
|---------------------------------------|----------------------------------------------|-----------------------------------------------------|------|-----|------|
| <b>INPUT CONDITIONS</b>               |                                              |                                                     |      |     |      |
| SR <sub>I</sub>                       | Input Slew Rate                              |                                                     | 2.64 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b>              |                                              |                                                     |      |     |      |
| C <sub>L</sub>                        | Output Load Capacitance                      |                                                     | 2    | 20  | pF   |
| <b>PCB Connectivity Requirements</b>  |                                              |                                                     |      |     |      |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation Delay mismatch across all traces | RGMII[x]_RXC<br>RGMII[x]_RD[3:0]<br>RGMII[x]_RX_CTL |      | 50  | ps   |
|                                       |                                              | RGMII[x]_TXC<br>RGMII[x]_TD[3:0]<br>RGMII[x]_TX_CTL |      | 50  | ps   |

#### 6.11.5.1.3.2 CPSW RGMII[x]\_RCLK Timing Requirements - RGMII Mode

| NO.    | PARAMETER            | DESCRIPTION              | MODE     | MIN | MAX | UNIT |
|--------|----------------------|--------------------------|----------|-----|-----|------|
| RGMII1 | t <sub>c</sub> (RXC) | Cycle time, RXC          | 10Mbps   | 360 | 440 | ns   |
|        |                      |                          | 100Mbps  | 36  | 44  | ns   |
|        |                      |                          | 1000Mbps | 7.2 | 8.8 | ns   |
| RGMII2 | tw(RXCH)             | Pulse duration, RXC high | 10Mbps   | 160 | 240 | ns   |
|        |                      |                          | 100Mbps  | 16  | 24  | ns   |
|        |                      |                          | 1000Mbps | 3.6 | 4.4 | ns   |
| RGMII3 | tw(RXCL)             | Pulse duration, RXC low  | 10Mbps   | 160 | 240 | ns   |
|        |                      |                          | 100Mbps  | 16  | 24  | ns   |
|        |                      |                          | 1000Mbps | 3.6 | 4.4 | ns   |

#### 6.11.5.1.3.3 CPSW RGMII[x]\_RD[3:0], and RGMII[x]\_RCTL Timing Requirements

| NO.    | PARAMETER                    | DESCRIPTION                                   | MODE     | MIN | MAX | UNIT |
|--------|------------------------------|-----------------------------------------------|----------|-----|-----|------|
| RGMII4 | t <sub>su</sub> (RD-RXC)     | Setup time, RD[3:0] valid before RXC high/low | 10Mbps   | 1   |     | ns   |
|        |                              |                                               | 100Mbps  | 1   |     | ns   |
|        |                              |                                               | 1000Mbps | 1   |     | ns   |
|        | t <sub>su</sub> (RX_CTL-RXC) | Setup time, RX_CTL valid before RXC high/low  | 10Mbps   | 1   |     | ns   |
|        |                              |                                               | 100Mbps  | 1   |     | ns   |
|        |                              |                                               | 1000Mbps | 1   |     | ns   |
| RGMII5 | t <sub>h</sub> (RXC-RD)      | Hold time, RD[3:0] valid after RXC high/low   | 10Mbps   | 1   |     | ns   |
|        |                              |                                               | 100Mbps  | 1   |     | ns   |
|        |                              |                                               | 1000Mbps | 1   |     | ns   |
|        | t <sub>h</sub> (RXC-RX_CTL)  | Hold time, RX_CTL valid after RXC high/low    | 10Mbps   | 1   |     | ns   |
|        |                              |                                               | 100Mbps  | 1   |     | ns   |
|        |                              |                                               | 1000Mbps | 1   |     | ns   |



- A. RGMII[x]\_RXC must be externally delayed relative to the data and control pins.  
B. Data and control information is received using both edges of the clocks. RGMII[x]\_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]\_RXC and data bits 7-4 on the falling edge of RGMII[x]\_RXC. Similarly, RGMII[x]\_RX\_CTL carries RXDV on rising edge of RGMII[x]\_RXC and RXERR on falling edge of RGMII[x]\_RXC.

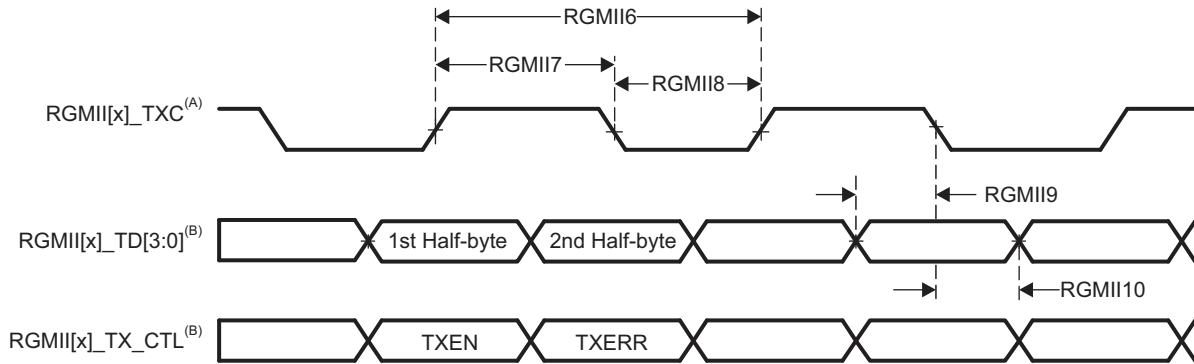
**Figure 6-13. CPSW RGMII[x]\_RXC, RGMII[x]\_RD[3:0], RGMII[x]\_RX\_CTL Timing Requirements - RGMII Mode**

#### 6.11.5.1.3.4 CPSW RGMII[x]\_TCLK Switching Characteristics - RGMII Mode

| NO.    | PARAMETER     | DESCRIPTION              | MODE     | MIN | MAX | UNIT |
|--------|---------------|--------------------------|----------|-----|-----|------|
| RGMII6 | $t_{c(TXC)}$  | Cycle time, TXC          | 10Mbps   | 360 | 440 | ns   |
|        |               |                          | 100Mbps  | 36  | 44  | ns   |
|        |               |                          | 1000Mbps | 7.2 | 8.8 | ns   |
| RGMII7 | $t_{w(TXCH)}$ | Pulse duration, TXC high | 10Mbps   | 160 | 240 | ns   |
|        |               |                          | 100Mbps  | 16  | 24  | ns   |
|        |               |                          | 1000Mbps | 3.6 | 4.4 | ns   |
| RGMII8 | $t_{w(TXCL)}$ | Pulse duration, TXC low  | 10Mbps   | 160 | 240 | ns   |
|        |               |                          | 100Mbps  | 16  | 24  | ns   |
|        |               |                          | 1000Mbps | 3.6 | 4.4 | ns   |

#### 6.11.5.1.3.5 CPSW RGMII[x]\_TD[3:0], and RGMII[x]\_TCTL Switching Characteristics - RGMII Mode

| NO.     | PARAMETER              | DESCRIPTION                                                          | MODE     | MIN | MAX | UNIT |
|---------|------------------------|----------------------------------------------------------------------|----------|-----|-----|------|
| RGMII9  | $t_{osu(TD-TXC)}$      | Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low   | 10Mbps   | 1.2 |     | ns   |
|         |                        |                                                                      | 100Mbps  | 1.2 |     | ns   |
|         |                        |                                                                      | 1000Mbps | 1.2 |     | ns   |
|         | $t_{osu(TX\_CTL-TXC)}$ | Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low    | 10Mbps   | 1.2 |     | ns   |
|         |                        |                                                                      | 100Mbps  | 1.2 |     | ns   |
|         |                        |                                                                      | 1000Mbps | 1.2 |     | ns   |
| RGMII10 | $t_{oh(TXC-TD)}$       | Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low | 10Mbps   | 1.2 |     | ns   |
|         |                        |                                                                      | 100Mbps  | 1.2 |     | ns   |
|         |                        |                                                                      | 1000Mbps | 1.2 |     | ns   |
|         | $t_{oh(TXC-TX\_CTL)}$  | Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low  | 10Mbps   | 1.2 |     | ns   |
|         |                        |                                                                      | 100Mbps  | 1.2 |     | ns   |
|         |                        |                                                                      | 1000Mbps | 1.2 |     | ns   |



- A. TxC is delayed internally before being driven to the  $\text{RGMII}[x]_{\text{TxC}}$  pin. This internal delay is by default enabled after POR.
- B. Data and control information is received using both edges of the clocks.  $\text{RGMII}[x]_{\text{TD}[3:0]}$  carries data bits 3-0 on the rising edge of  $\text{RGMII}[x]_{\text{TxC}}$  and data bits 7-4 on the falling edge of  $\text{RGMII}[x]_{\text{TxC}}$ . Similarly,  $\text{RGMII}[x]_{\text{TX\_CTL}}$  carries TXEN on rising edge of  $\text{RGMII}[x]_{\text{TxC}}$  and TXERR on falling edge of  $\text{RGMII}[x]_{\text{TxC}}$ .

**Figure 6-14. CPSW  $\text{RGMII}[x]_{\text{TxC}}$ ,  $\text{RGMII}[x]_{\text{TD}[3:0]}$ , and  $\text{RGMII}[x]_{\text{TX\_CTL}}$  Switching Characteristics - RGMII Mode**

### 6.11.5.2 Enhanced Capture (eCAP)

#### Note

The device has multiple eCAP modules. The generic CAP\_ prefix is used to represent the signal names for all eCAP instances.

For more information, see *Enhanced Capture (eCAP) Module* section in the device TRM.

#### 6.11.5.2.1 ECAP Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 2   | 7   | pF   |

#### 6.11.5.2.2 ECAP Timing Requirements

| NO.  | PARAMETER           | DESCRIPTION               |                      | MIN                                                           | MAX | UNIT |
|------|---------------------|---------------------------|----------------------|---------------------------------------------------------------|-----|------|
| CAP1 | t <sub>w(CAP)</sub> | Capture input pulse width | Asynchronous         | (2 + X <sup>(2)</sup> ) × P <sup>(1)</sup>                    |     | ns   |
|      |                     |                           | Synchronous          | (3 + X <sup>(2)</sup> ) × P <sup>(1)</sup>                    |     |      |
|      |                     |                           | With input qualifier | (2 + X <sup>(2)</sup> ) × P <sup>(1)</sup> + U <sup>(3)</sup> |     |      |

(1) P = sysclk period in ns.

(2) X = value of ECCTL0\_TYPE3[QUALPRD] setting.

(3) U = the input qualifier sampling window. See GPIO Electrical Data and Timing section for details on Input Qualifier Mode

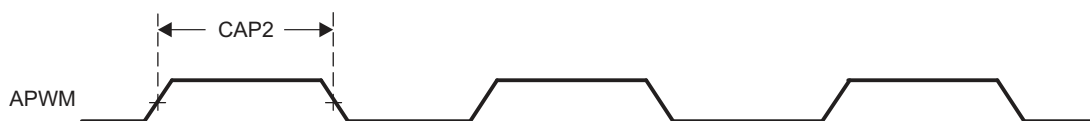


EPERIPHERALS\_TIMING\_01

Figure 6-15. ECAP Timings Requirements

#### 6.11.5.2.3 ECAP Switching Characteristics

| NO.  | PARAMETER            | DESCRIPTION                           | MIN | MAX | UNIT |
|------|----------------------|---------------------------------------|-----|-----|------|
| CAP2 | t <sub>w(APWM)</sub> | Pulse duration, APWMx output high/low | 10  |     | ns   |



EPERIPHERALS\_TIMING\_02

Figure 6-16. ECAP Switching Characteristics

### 6.11.5.3 Enhanced Pulse Width Modulation (ePWM)

#### Note

The device has multiple ePWM modules. The generic EHRPWM\_ prefix is used to represent the signal names for all ePWM instances.

For more information, see *Enhanced Pulse Width Modulation (ePWM) Module* section in the device TRM.

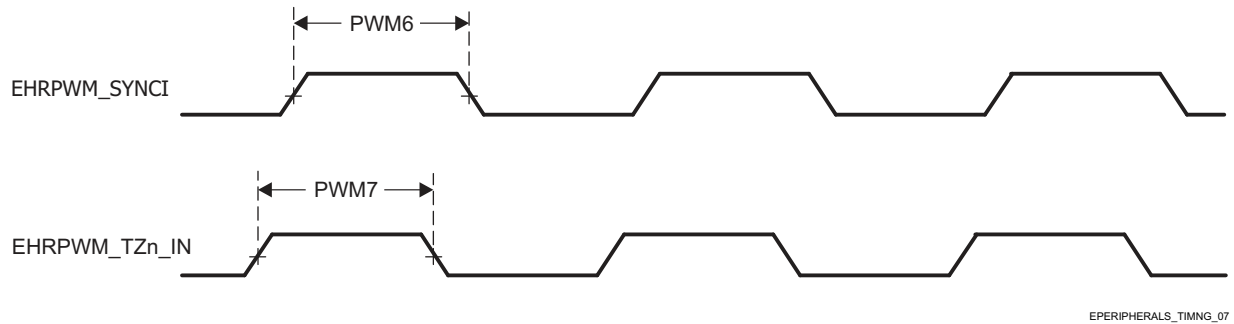
#### 6.11.5.3.1 EPWM Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 2   | 7   | pF   |

#### 6.11.5.3.2 EPWM Timing Requirements

| NO.  | PARAMETER               | DESCRIPTION                       | MIN               | MAX | UNIT |
|------|-------------------------|-----------------------------------|-------------------|-----|------|
| PWM6 | t <sub>w</sub> (SYNClN) | Pulse duration, EHRPWM_SYNCl      | 2P <sup>(1)</sup> |     | ns   |
| PWM7 | t <sub>w</sub> (TZ)     | Pulse duration, EHRPWM_TZn_IN low | 1P <sup>(1)</sup> |     | ns   |

(1) P = sysclk period in ns.

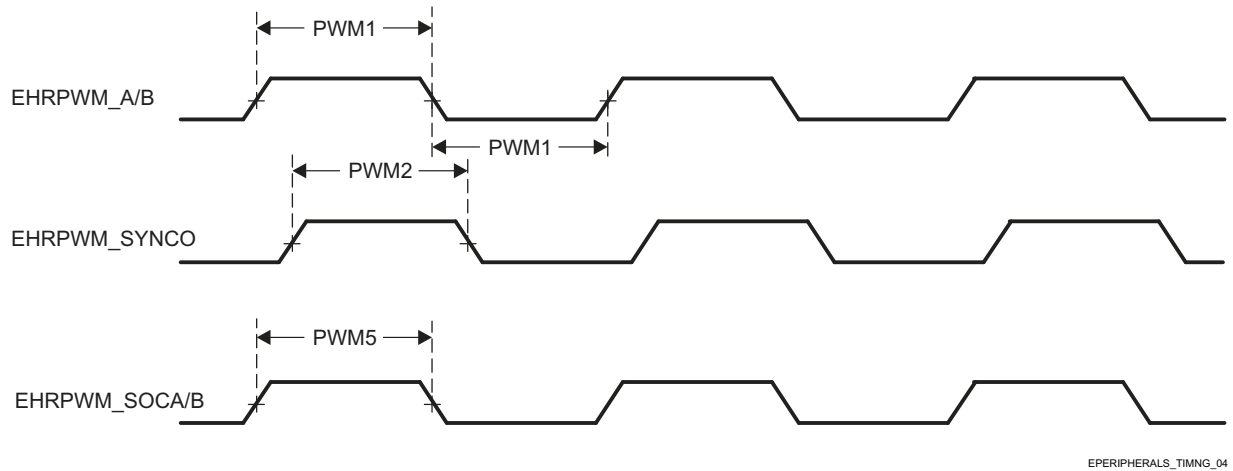


**Figure 6-17. EPWM Timing Requirements**

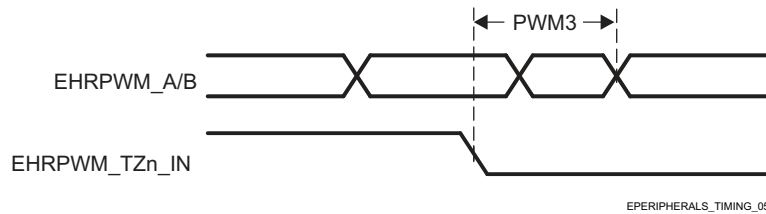
#### 6.11.5.3.3 EPWM Switching Characteristics

| NO.  | PARAMETER                | DESCRIPTION                                                    | MIN                | MAX | UNIT |
|------|--------------------------|----------------------------------------------------------------|--------------------|-----|------|
| PWM1 | t <sub>w</sub> (PWM)     | Pulse duration, EHRPWM_A/B high/low                            | 20                 |     | ns   |
| PWM2 | t <sub>w</sub> (SYNCOU)  | Pulse duration, EHRPWM_SYNCO                                   | 8P <sup>(1)</sup>  |     | ns   |
| PWM3 | t <sub>d</sub> (TZ-PWM)  | Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B forced high/low |                    | 30  | ns   |
| PWM4 | t <sub>d</sub> (TZ-PWMZ) | Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B Hi-Z            |                    | 30  | ns   |
| PWM5 | t <sub>w</sub> (SOC)     | Pulse duration, EHRPWM_SOC A/B output                          | 32P <sup>(1)</sup> |     | ns   |

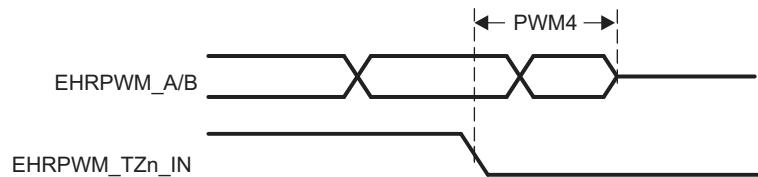
(1) P = sysclk period in ns.



**Figure 6-18. EHRPWM Switching Characteristics**



**Figure 6-19. EHRPWM\_TZn\_IN to EHRPWM\_A/B Forced Switching Characteristics**



**Figure 6-20. EHRPWM\_TZn\_IN to EHRPWM\_A/B Hi-Z Switching Characteristics**

#### EPWM Characteristics

| PARAMETER                                             | MIN | TYP | MAX | UNIT |
|-------------------------------------------------------|-----|-----|-----|------|
| Micro Edge Positioning (MEP) step size <sup>(1)</sup> |     | 115 | 310 | ps   |

- (1) The MEP step size will be largest at high temperature and minimum voltage on VDD. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage. Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

#### 6.11.5.4 Enhanced Quadrature Encoder Pulse (eQEP)

##### Note

The device has multiple eQEP modules. The generic QEP\_ prefix is used to represent the signal names for all eQEP instances.

For more information, see *Enhanced Quadrature Encoder Pulse (eQEP) Module* section in the device TRM.

##### 6.11.5.4.1 EQEP Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 2   | 7   | pF   |

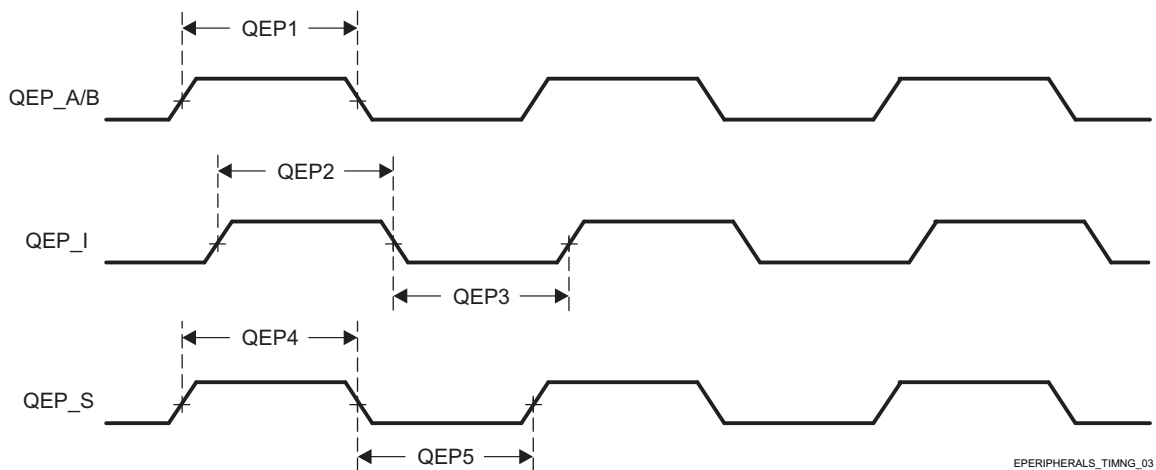
##### 6.11.5.4.2 EQEP Timing Requirements

| NO.  | PARAMETER              | DESCRIPTION               |                            | MIN                                        | MAX | UNIT |
|------|------------------------|---------------------------|----------------------------|--------------------------------------------|-----|------|
| QEP1 | t <sub>w(QEPP)</sub>   | QEP input period          | Synchronous <sup>(3)</sup> | 3P <sup>(1)</sup>                          |     | ns   |
|      |                        |                           | With input qualifier       | 2 × (P <sup>(1)</sup> + U <sup>(2)</sup> ) |     |      |
| QEP2 | t <sub>w(INDEXH)</sub> | QEP Index Input High time | Synchronous <sup>(3)</sup> | 2 + 3P <sup>(1)</sup>                      |     | ns   |
|      |                        |                           | With input qualifier       | 2P <sup>(1)</sup> + U <sup>(2)</sup>       |     |      |
| QEP3 | t <sub>w(INDEXL)</sub> | QEP Index Input Low time  | Synchronous <sup>(3)</sup> | 3P <sup>(1)</sup>                          |     | ns   |
|      |                        |                           | With input qualifier       | 2P <sup>(1)</sup> + U <sup>(2)</sup>       |     |      |
| QEP4 | t <sub>w(STROBH)</sub> | QEP Strobe High time      | Synchronous <sup>(3)</sup> | 3P <sup>(1)</sup>                          |     | ns   |
|      |                        |                           | With input qualifier       | 2P <sup>(1)</sup> + U <sup>(2)</sup>       |     |      |
| QEP5 | t <sub>w(STROBL)</sub> | QEP Strobe Input Low time | Synchronous <sup>(3)</sup> | 3P <sup>(1)</sup>                          |     | ns   |
|      |                        |                           | With input qualifier       | 2P <sup>(1)</sup> + U <sup>(2)</sup>       |     |      |

(1) P = sysclk period in ns.

(2) U = the input qualifier sampling window. See GPIO Electrical Data and Timing section for details on Input Qualifier Mode.

(3) The GPIO GPxQSELn Asynchronous mode should not be used for eQEP module input pins.



**Figure 6-21. EQEP Timing Requirements**

**6.11.5.4.3 EQEP Switching Characteristics**

| NO.  | PARAMETER              | DESCRIPTION                                                | MIN | MAX                          | UNIT |
|------|------------------------|------------------------------------------------------------|-----|------------------------------|------|
| QEP6 | $t_{d(CNTR)_{xin}}$    | Delay time, external clock to counter increment            |     | $4 + U^{(2)} + 6P^{(1)}$     | ns   |
| QEP7 | $t_{d(PCS-OUT)_{QEP}}$ | Delay time, QEP input edge to position compare sync output |     | $4 + U^{(2)} + 7P^{(1)} + 4$ | ns   |

(1) P = sysclk period in ns.

(2) U = the input qualifier sampling window. See GPIO Electrical Data and Timing section for details on Input Qualifier Mode.

### 6.11.5.5 Fast Serial Interface (FSI)

#### Note

The device has multiple FSI modules. FSI<sub>n</sub> is a generic prefix applied to FSI signal names, where n represents the specific FSI module.

For more information, see *Fast Serial Interface* section in the device TRM.

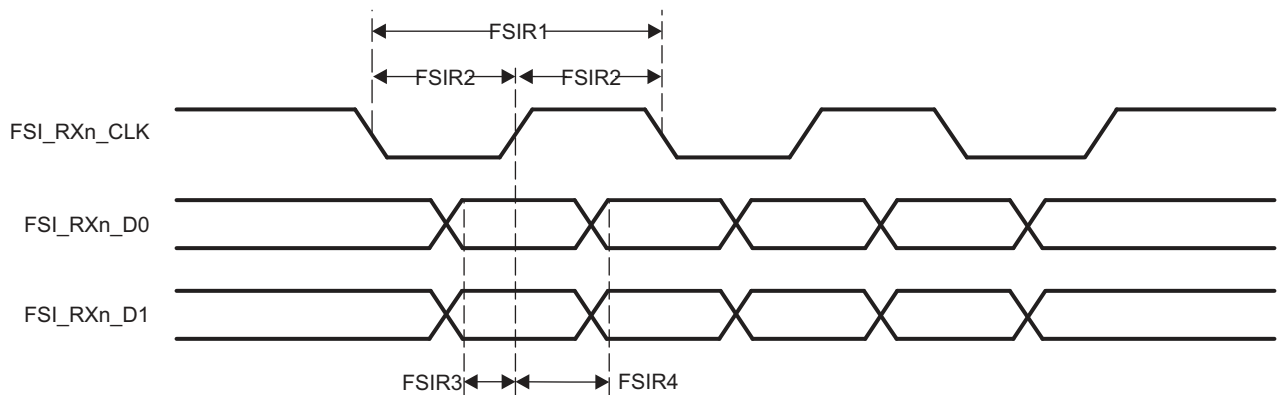
#### 6.11.5.5.1 FSI Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 0.8 | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 1   | 7   | pF   |

#### 6.11.5.5.2 FSIRX Timing Requirements

| NO.   | PARAMETER                    | DESCRIPTION                                        | MIN                      | MAX                      | UNIT |
|-------|------------------------------|----------------------------------------------------|--------------------------|--------------------------|------|
| FSIR1 | t <sub>c</sub> (RX_CLK)      | Cycle time, FSIRXn_CLK                             | 16.67                    |                          | ns   |
| FSIR2 | t <sub>w</sub> (RX_CLK)      | Pulse width, FSIRXn_CLK low or FSIRXn_CLK high     | 0.35P <sup>(1)</sup> – 1 | 0.65P <sup>(1)</sup> + 1 | ns   |
| FSIR3 | t <sub>d</sub> (RX_D–RX_CLK) | Delay time, FSIRXn_D[0:1] valid before FSIRXn_CLK  | 1.7                      |                          | ns   |
| FSIR4 | t <sub>h</sub> (RX_CLK–RX_D) | Hold time with respect to both edges of FSIRXn_CLK | 2                        |                          | ns   |

(1) P = T<sub>c</sub>(RXCLK) = RX Interface clock period in ns.



**Figure 6-22. FSI Timing Requirements**

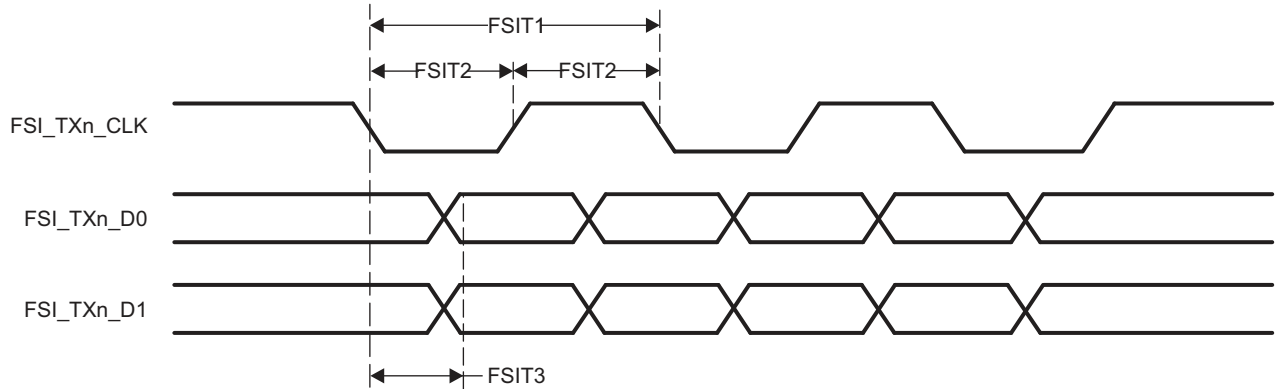
#### 6.11.5.5.3 FSIRX Switching Characteristics

| NO.        | PARAMETER                        | DESCRIPTION                                                                           | MIN | MAX | UNIT |
|------------|----------------------------------|---------------------------------------------------------------------------------------|-----|-----|------|
| FSIR5      | $t_{d(RX\_CLK)}$                 | FSIRXn_CLK delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31                        | 10  | 30  | ns   |
| FSIR6      | $t_{d(RX\_D0)}$                  | FSIRXn_D0 delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31                         | 10  | 30  | ns   |
| FSIR7      | $t_{d(RX\_D1)}$                  | FSIRXn_D1 delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31                         | 10  | 30  | ns   |
| FSIR8      | $t_{d(DELAY\_ELEMENT)}$          | Incremental delay of each delay line element for FSIRXn_CLK, FSIRXn_D0, and FSIRXn_D1 | 0.3 | 1   | ns   |
| FSIR_TD M1 | $t_{skew(RX\_CLK-TX\_TDM\_D)}$   | Delay skew between FSIRXn_TDM_CLK delay and FSIRXn_TDM_D[0:1]                         | -3  | 3   | ns   |
| FSIR_TD M2 | $t_{skew(RX\_CLK-TX\_TDM\_CLK)}$ | Delay time, FSIRXn_CLK input to FSITXn_TDM_CLK output                                 | 2   | 12  | ns   |
| FSIR_TD M3 | $t_{skew(RX\_D0-TX\_TDM\_D0)}$   | Delay time, FSIRXn_D0 input to FSITXn_TDM_D0 output                                   | 2   | 12  | ns   |
| FSIR_TD M4 | $t_{skew(RX\_D1-TX\_TDM\_D1)}$   | Delay time, FSIRXn_D1 input to FSITXn_TDM_D1 output                                   | 2   | 12  | ns   |

#### 6.11.5.5.4 FSITX Switching Characteristics

| NO.        | PARAMETER                           | DESCRIPTION                                                                           | MIN               | MAX               | UNIT |
|------------|-------------------------------------|---------------------------------------------------------------------------------------|-------------------|-------------------|------|
| FSIT1      | $t_c(TX\_CLK)$                      | Cycle time, FSITXn_CLK                                                                | 16.67             |                   | ns   |
| FSIT2      | $t_w(TX\_CLK)$                      | Pulse width, FSITXn_CLK low or FSITXn_CLK high                                        | $0.5P^{(1)} - 1$  | $0.5P^{(1)} + 1$  | ns   |
| FSIT3      | $t_d(TX\_CLK-TX\_D)$                | Delay time, FSITXn_Dx valid after FSITXn_CLK high or FSITXn_CLK low                   | $0.25P^{(1)} - 2$ | $0.25P^{(1)} + 2$ | ns   |
| FSIT4      | $t_d(TXCLKL)$                       | FSITXn_CLK delay compensation at TX_DLYLINE_CTRL[TXCLK_DLY]=31                        | 9.95              | 30                | ns   |
| FSIT5      | $t_d(TX\_D0)$                       | FSITXn_D0 delay compensation at TX_DLYLINE_CTRL[TXCLK_DLY]=31                         | 9.95              | 30                | ns   |
| FSIT6      | $t_d(TX\_D1)$                       | FSITXn_D1 delay compensation at TX_DLYLINE_CTRL[TXCLK_DLY]=31                         | 9.95              | 30                | ns   |
| FSIT7      | $t_d(TX\_DELAY\_ELEMENT)$           | Incremental delay of each delay line element for FSITXn_CLK, FSITXn_D0, and FSITXn_D1 | 0.3               | 1                 | ns   |
| FSIT_TD M1 | $t_{skew(TX\_TDM\_CLK-TX\_TDM\_D)}$ | Delay skew introduced between FSITXn_TDM_CLK delay and FSITXn_TDM_D[0:1] delays       | -2.5              | 2.5               | ns   |
| FSIT_TD M2 | $t_{skew(TX\_TDM\_CLK-TX\_CLK)}$    | Delay time, FSITXn_TDM_CLK input to FSITXn_CLK output                                 | 2                 | 12                | ns   |
| FSIT_TD M3 | $t_{skew(TX\_TDM\_D0-TX\_D0)}$      | Delay time, FSITXn_TDM_D0 input to FSITXn_D0 output                                   | 2                 | 12                | ns   |
| FSIT_TD M4 | $t_{skew(TX\_TDM\_D1-TX\_D1)}$      | Delay time, FSITXn_TDM_D1 input to FSITXn_D1 output                                   | 2                 | 12                | ns   |

(1)  $P = t_c(TX\_CLK)$  = FSITX Interface clock period in ns.

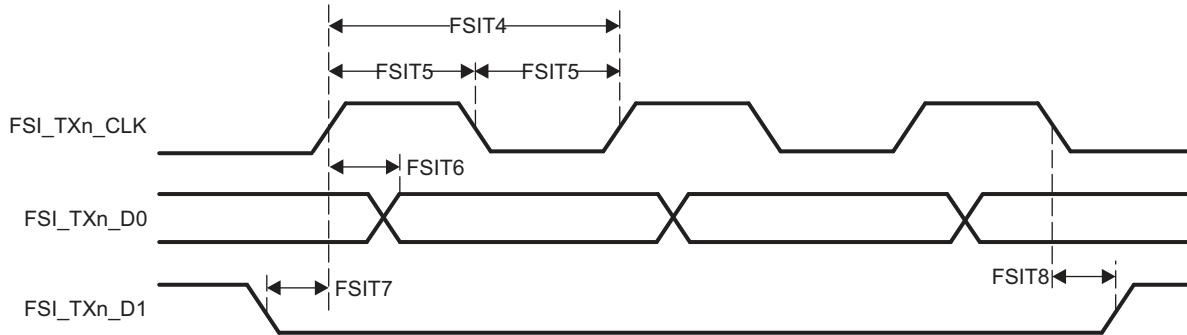


**Figure 6-23. FSI Switching Characteristics - FSI Mode**

#### 6.11.5.5 FSITX SPI Signaling Mode Switching Characteristics

| NO.   | PARAMETER                | DESCRIPTION                                    | MIN              | MAX              | UNIT |
|-------|--------------------------|------------------------------------------------|------------------|------------------|------|
| FSIT4 | $t_{c(TX\_CLK)}$         | Cycle time, FSITXn_CLK                         | 16.67            |                  | ns   |
| FSIT5 | $t_{w(TX\_CLK)}$         | Pulse width, FSITXn_CLK low or FSITXn_CLK high | $0.5P^{(1)} - 1$ | $0.5P^{(1)} + 1$ | ns   |
| FSIT6 | $t_{d(TX\_CLKH-TX\_D0)}$ | Delay time, FSITXn_CLK high to FSITXn_D0 valid |                  | 3                | ns   |
| FSIT7 | $t_{d(TX\_D1-TX\_CLK)}$  | Delay time, FSITXn_D1 low to FSITXn_CLK high   | $P^{(1)} - 3$    |                  | ns   |
| FSIT8 | $t_{d(TX\_CLK-TX\_D1)}$  | Delay time, FSITXn_CLK low to FSITXn_D1 high   | $P^{(1)}$        |                  | ns   |

(1)  $P = t_{c(TX\_CLK)}$  = FSITX Interface clock period in ns.



**Figure 6-24. FSI Switching Characteristics - SPI Mode**

### 6.11.5.6 General Purpose Input/Output (GPIO)

For more details about features and additional description information on the device GPIO, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see *General-Purpose Interface (GPIO)* section in the device TRM.

#### 6.11.5.6.1 GPIO Timing Conditions

| PARAMETER                |                         | BUFFER TYPE              | MIN  | MAX | UNIT |
|--------------------------|-------------------------|--------------------------|------|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |                          |      |     |      |
| SR <sub>I</sub>          | Input Slew Rate         |                          | 0.75 | 6.6 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |                          |      |     |      |
| C <sub>L</sub>           | Output Load Capacitance | LVC MOS                  | 3    | 10  | pF   |
|                          |                         | I2C OD FS <sup>(1)</sup> | 3    | 10  | pF   |

(1) A pull-up resistor is required for buffer type I2C OD FS.

#### 6.11.5.6.2 GPIO Timing Requirements

| NO. | PARAMETER                | DESCRIPTION               | BUFFER TYPE              | MIN                   | MAX | UNIT |
|-----|--------------------------|---------------------------|--------------------------|-----------------------|-----|------|
| D3  | t <sub>w</sub> (GPIO_IN) | Minimum Input Pulse Width | LVC MOS                  | 2P <sup>(1)</sup> + 2 |     | ns   |
| D4  |                          |                           | I2C OD FS <sup>(2)</sup> | 2P <sup>(1)</sup> + 2 |     | ns   |

(1) P = functional clock period in ns.

(2) A pull-up resistor is required for buffer type I2C OD FS.

#### 6.11.5.6.3 GPIO Switching Characteristics

| NO. | PARAMETER                 | DESCRIPTION                     | BUFFER TYPE              | MIN                       | MAX | UNIT |
|-----|---------------------------|---------------------------------|--------------------------|---------------------------|-----|------|
| D1  | t <sub>w</sub> (GPIO_OUT) | Minimum Output Pulse Width      | LVC MOS                  | 0.975P <sup>(1)</sup> – 2 |     | ns   |
| D2  | t <sub>w</sub> (GPIO_OUT) | Minimum Output Pulse Width Low  | I2C OD FS <sup>(2)</sup> | 2P <sup>(1)</sup> + 160   |     | ns   |
| D3  | t <sub>w</sub> (GPIO_OUT) | Minimum Output Pulse Width High | I2C OD FS <sup>(2)</sup> | 2P <sup>(1)</sup> + 160   |     | ns   |

(1) P = functional clock period in ns.

(2) A pull-up resistor is required for buffer type I2C OD FS.

### 6.11.5.7 General Purpose Memory Controller (GPMC)

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see the *General-Purpose Memory Controller (GPMC)* section in the device TRM.

#### 6.11.5.7.1 GPMC Timing Conditions

| PARAMETER                             |                                              |        | MIN  | MAX | UNIT |
|---------------------------------------|----------------------------------------------|--------|------|-----|------|
| <b>INPUT CONDITIONS</b>               |                                              |        |      |     |      |
| SR <sub>I</sub>                       | Input Slew Rate                              |        | 1.65 | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b>              |                                              |        |      |     |      |
| C <sub>L</sub>                        | Output Load Capacitance                      |        | 3    | 20  | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                              |        |      |     |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace              | 100MHz | 140  | 720 | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces |        |      | 200 | ps   |

#### 6.11.5.7.2 GPMC/NOR Flash Timing Requirements - Synchronous Mode 100MHz

(1) (2)

| NO. | PARAMETER                    | DESCRIPTION                                                          | MODE                             | MIN  | MAX | UNIT |
|-----|------------------------------|----------------------------------------------------------------------|----------------------------------|------|-----|------|
| F12 | t <sub>su</sub> (dV-clkH)    | Setup time, GPMC0_AD[31:0] valid before GPMC0_CLK high               | div_by_1_mode <sup>(4)</sup>     | 1.81 |     | ns   |
|     |                              |                                                                      | not_div_by_1_mode <sup>(5)</sup> | 1.06 |     | ns   |
| F13 | t <sub>h</sub> (clkH-dV)     | Hold time, GPMC0_AD[31:0] valid after GPMC0_CLK high                 | div_by_1_mode <sup>(4)</sup>     | 2.29 |     | ns   |
|     |                              |                                                                      | not_div_by_1_mode <sup>(5)</sup> | 2.29 |     | ns   |
| F21 | t <sub>su</sub> (waitV-clkH) | Setup time, GPMC0_WAIT[x] <sup>(3)</sup> valid before GPMC0_CLK high | div_by_1_mode <sup>(4)</sup>     | 1.81 |     | ns   |
|     |                              |                                                                      | not_div_by_1_mode <sup>(5)</sup> | 1.06 |     | ns   |
| F22 | t <sub>h</sub> (clkH-waitV)  | Hold time, GPMC0_WAIT[x] <sup>(3)</sup> valid after GPMC0_CLK high   | div_by_1_mode <sup>(4)</sup>     | 2.29 |     | ns   |
|     |                              |                                                                      | not_div_by_1_mode <sup>(5)</sup> | 2.29 |     | ns   |

- (1) 100MHz GPMC\_FCLK selected - CTRLMMR\_GPMC\_CLKSEL[0] CLK\_SEL = 1 = MAIN\_PLL2\_HSDIV7\_CLKOUT (100/60 MHz).
- (2) Trace length from GPMC pins to device assumed to be less than 4" and length matched to within 200ps for 100MHz Synchronous Mode.
- (3) In GPMC\_WAIT[x], x is equal to 0 or 1.
- (4) In div\_by\_1\_mode, GPMC0\_CLK refers to either GPMC0\_CLKOUT or GPMC0\_FCLK\_MUX (free-running). Both signals are pin-muxed to the same pin.  
GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:  
– GPMC0\_CLK frequency = GPMC\_FCLK frequency
- (5) In not\_div\_by\_1\_mode, GPMC0\_CLK only refers to GPMC0\_CLKOUT. GPMC0\_FCLK\_MUX cannot be clock divided to match the GPMC0\_CLKOUT frequency if GPMCFCLKDIVIDER > 0.  
GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 1h to 3h:  
– GPMC0\_CLK frequency = GPMC\_FCLK frequency / (2 to 4)

**6.11.5.7.3 GPMC/NOR Flash Switching Characteristics - Synchronous Mode 100MHz**

(18) (19) (20)

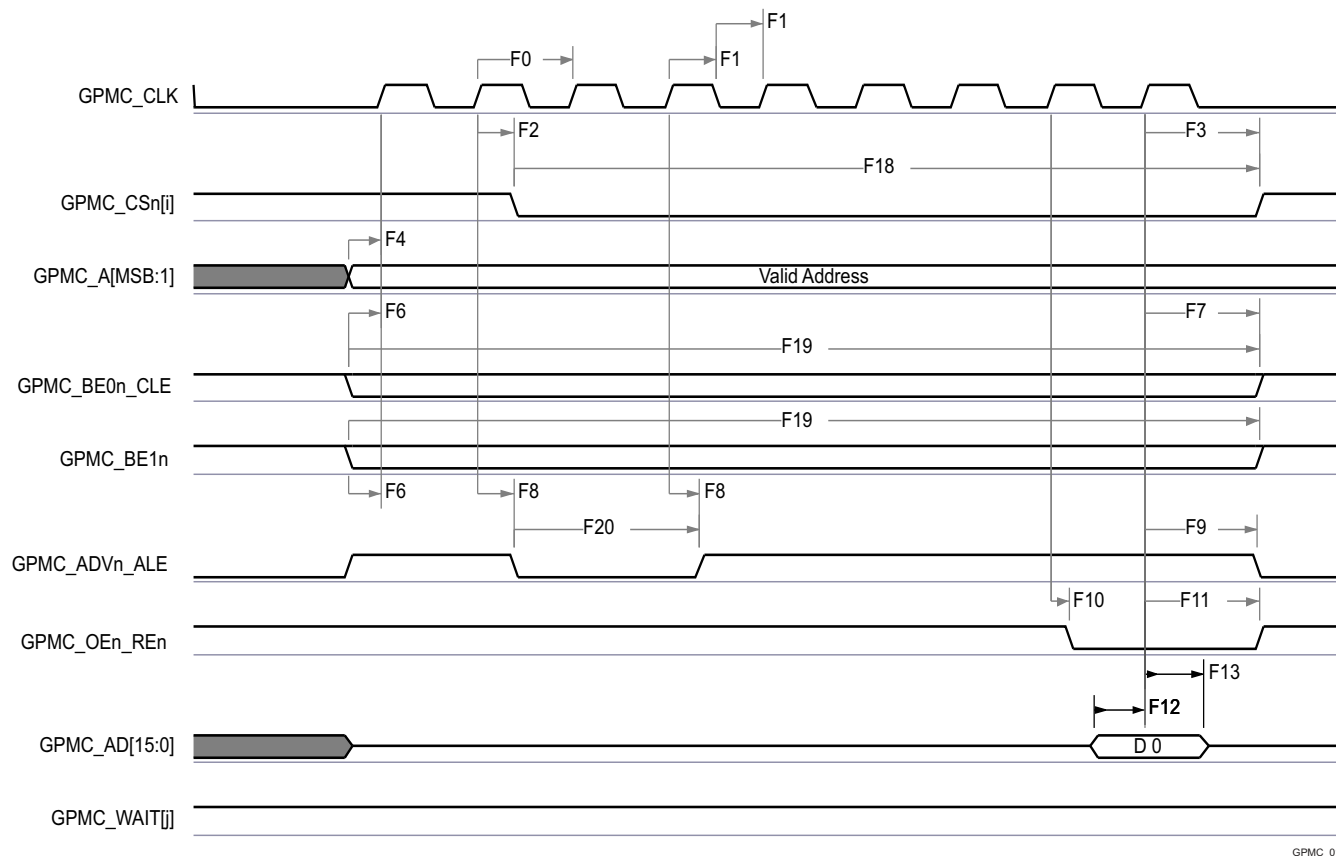
| NO. | PARAMETER                     | DESCRIPTION                                                                                                          | MODE  | MIN                                          | MAX                        | UNIT |
|-----|-------------------------------|----------------------------------------------------------------------------------------------------------------------|-------|----------------------------------------------|----------------------------|------|
| F0  | $t_{c(\text{clk})}$           | Clock period, GPMC0_CLK, GPMC0_FCLK_MUX                                                                              |       | 10 <sup>(21)</sup>                           |                            | ns   |
| F1  | $t_{w(\text{clk})}$           | Typical pulse duration, GPMC0_CLK high or low                                                                        |       | 0.475P <sup>(16)</sup> – 0.3 <sup>(21)</sup> |                            | ns   |
| F2  | $t_{d(\text{clkH-csnV})}$     | Delay time, GPMC0_CLK rising edge to GPMC0_CS <sub>n</sub> [x] <sup>(15)</sup> transition                            |       | F <sup>(6)</sup> – 2.2 <sup>(21)</sup>       | F <sup>(6)</sup> +3.75     | ns   |
| F3  | $t_{d(\text{clkH-csnIV})}$    | Delay time, GPMC0_CLK rising edge to GPMC0_CS <sub>n</sub> [x] <sup>(15)</sup> invalid                               |       | E <sup>(5)</sup> – 2.2                       | E <sup>(5)</sup> +3.18     | ns   |
| F4  | $t_{d(\text{aV-clk})}$        | Delay time, GPMC0_A[27:1] valid to GPMC0_CLK first edge                                                              |       | B <sup>(2)</sup> – 2.3 <sup>(21)</sup>       | B <sup>(2)</sup> + 4.5     | ns   |
| F5  | $t_{d(\text{clkH-aIV})}$      | Delay time, GPMC0_CLK rising edge to GPMC0_A[27:1] invalid                                                           |       | –2.3 <sup>(21)</sup>                         | 4.5                        | ns   |
| F6  | $t_{d(\text{be}[x]nV-clk)}$   | Delay time, GPMC0_BE0 <sub>n</sub> _CLE, GPMC0_BE1 <sub>n</sub> valid to GPMC0_CLK first edge                        |       | B <sup>(2)</sup> – 2.3 <sup>(21)</sup>       | B <sup>(2)</sup> + 1.9     | ns   |
| F7  | $t_{d(\text{clkH-be}[x]nIV)}$ | Delay time, GPMC0_CLK rising edge to GPMC0_BE0 <sub>n</sub> _CLE, GPMC0_BE1 <sub>n</sub> invalid <sup>(12)</sup>     |       | D <sup>(4)</sup> – 2.3 <sup>(21)</sup>       | D <sup>(4)</sup> + 1.9     | ns   |
| F7  | $t_{d(\text{clkL-be}[x]nIV)}$ | Delay time, GPMC0_CLK falling edge to GPMC0_BE0 <sub>n</sub> _CLE, GPMC0_BE1 <sub>n</sub> invalid <sup>(13)</sup>    |       | D <sup>(4)</sup> – 2.3 <sup>(21)</sup>       | D <sup>(4)</sup> + 1.9     | ns   |
| F7  | $t_{d(\text{clkL-be}[x]nIV)}$ | Delay time, GPMC0_CLK falling edge to GPMC0_BE0 <sub>n</sub> _CLE, GPMC0_BE1 <sub>n</sub> invalid <sup>(14)</sup>    |       | D <sup>(4)</sup> – 2.3 <sup>(21)</sup>       | D <sup>(4)</sup> + 1.9     | ns   |
| F8  | $t_{d(\text{clkH-advn})}$     | Delay time, GPMC0_CLK rising edge to GPMC0_ADV <sub>n</sub> _ALE transition                                          |       | G <sup>(7) (8)</sup> – 2.3 <sup>(21)</sup>   | G <sup>(7) (8)</sup> + 4.5 | ns   |
| F9  | $t_{d(\text{clkH-advnIV})}$   | Delay time, GPMC0_CLK rising edge to GPMC0_ADV <sub>n</sub> _ALE invalid                                             |       | D <sup>(4)</sup> – 2.3 <sup>(21)</sup>       | D <sup>(4)</sup> + 4.5     | ns   |
| F10 | $t_{d(\text{clkH-oen})}$      | Delay time, GPMC0_CLK rising edge to GPMC0_OE <sub>n</sub> _RE <sub>n</sub> transition                               |       | H <sup>(9)</sup> – 2.3 <sup>(21)</sup>       | H <sup>(9)</sup> + 3.5     | ns   |
| F11 | $t_{d(\text{clkH-oenIV})}$    | Delay time, GPMC0_CLK rising edge to GPMC0_OE <sub>n</sub> _RE <sub>n</sub> invalid                                  |       | H <sup>(9)</sup> – 2.3 <sup>(21)</sup>       | H <sup>(9)</sup> + 3.5     | ns   |
| F14 | $t_{d(\text{clkH-wen})}$      | Delay time, GPMC0_CLK rising edge to GPMC0_WE <sub>n</sub> transition                                                |       | I <sup>(10)</sup> – 2.3 <sup>(21)</sup>      | I <sup>(10)</sup> + 4.5    | ns   |
| F15 | $t_{d(\text{clkH-do})}$       | Delay time, GPMC0_CLK rising edge to GPMC0_AD[31:0] transition <sup>(12)</sup>                                       |       | J <sup>(11)</sup> – 2.3 <sup>(21)</sup>      | J <sup>(11)</sup> + 2.7    | ns   |
| F15 | $t_{d(\text{clkL-do})}$       | Delay time, GPMC0_CLK falling edge to GPMC0_AD[31:0] data bus transition <sup>(13)</sup>                             |       | J <sup>(11)</sup> – 2.3 <sup>(21)</sup>      | J <sup>(11)</sup> + 2.7    | ns   |
| F15 | $t_{d(\text{clkL-do})}$       | Delay time, GPMC0_CLK falling edge to GPMC0_AD[31:0] data bus transition <sup>(14)</sup>                             |       | J <sup>(11)</sup> – 2.3 <sup>(21)</sup>      | J <sup>(11)</sup> + 2.7    | ns   |
| F17 | $t_{d(\text{clkH-be}[x]n)}$   | Delay time, GPMC0_CLK rising edge to GPMC0_BE0 <sub>n</sub> _CLE transition <sup>(12)</sup>                          |       | J <sup>(11)</sup> – 2.3 <sup>(21)</sup>      | J <sup>(11)</sup> + 1.9    | ns   |
| F17 | $t_{d(\text{clkL-be}[x]n)}$   | Delay time, GPMC0_CLK falling edge to GPMC0_BE0 <sub>n</sub> _CLE, GPMC0_BE1 <sub>n</sub> transition <sup>(13)</sup> |       | J <sup>(11)</sup> – 2.3 <sup>(21)</sup>      | J <sup>(11)</sup> + 1.9    | ns   |
| F17 | $t_{d(\text{clkL-be}[x]n)}$   | Delay time, GPMC0_CLK falling edge to GPMC0_BE0 <sub>n</sub> _CLE, GPMC0_BE1 <sub>n</sub> transition <sup>(14)</sup> |       | J <sup>(11)</sup> – 2.3 <sup>(21)</sup>      | J <sup>(11)</sup> + 1.9    | ns   |
| F18 | $t_{w(\text{csnV})}$          | Pulse duration, GPMC0_CS <sub>n</sub> [x] <sup>(15)</sup> low                                                        | Read  | A <sup>(1)</sup>                             |                            | ns   |
|     |                               |                                                                                                                      | Write | A <sup>(1)</sup>                             |                            | ns   |
| F19 | $t_{w(\text{be}[x]nV)}$       | Pulse duration, GPMC0_BE0 <sub>n</sub> _CLE, GPMC0_BE1 <sub>n</sub> low                                              | Read  | C <sup>(3)</sup>                             |                            | ns   |
|     |                               |                                                                                                                      | Write | C <sup>(3)</sup>                             |                            | ns   |

(18) (19) (20)

| NO. | PARAMETER      | DESCRIPTION                        | MODE  | MIN               | MAX | UNIT |
|-----|----------------|------------------------------------|-------|-------------------|-----|------|
| F20 | $t_{w(advnV)}$ | Pulse duration, GPMC0_ADVn_ALE low | Read  | K <sup>(17)</sup> |     | ns   |
|     |                |                                    | Write | K <sup>(17)</sup> |     | ns   |

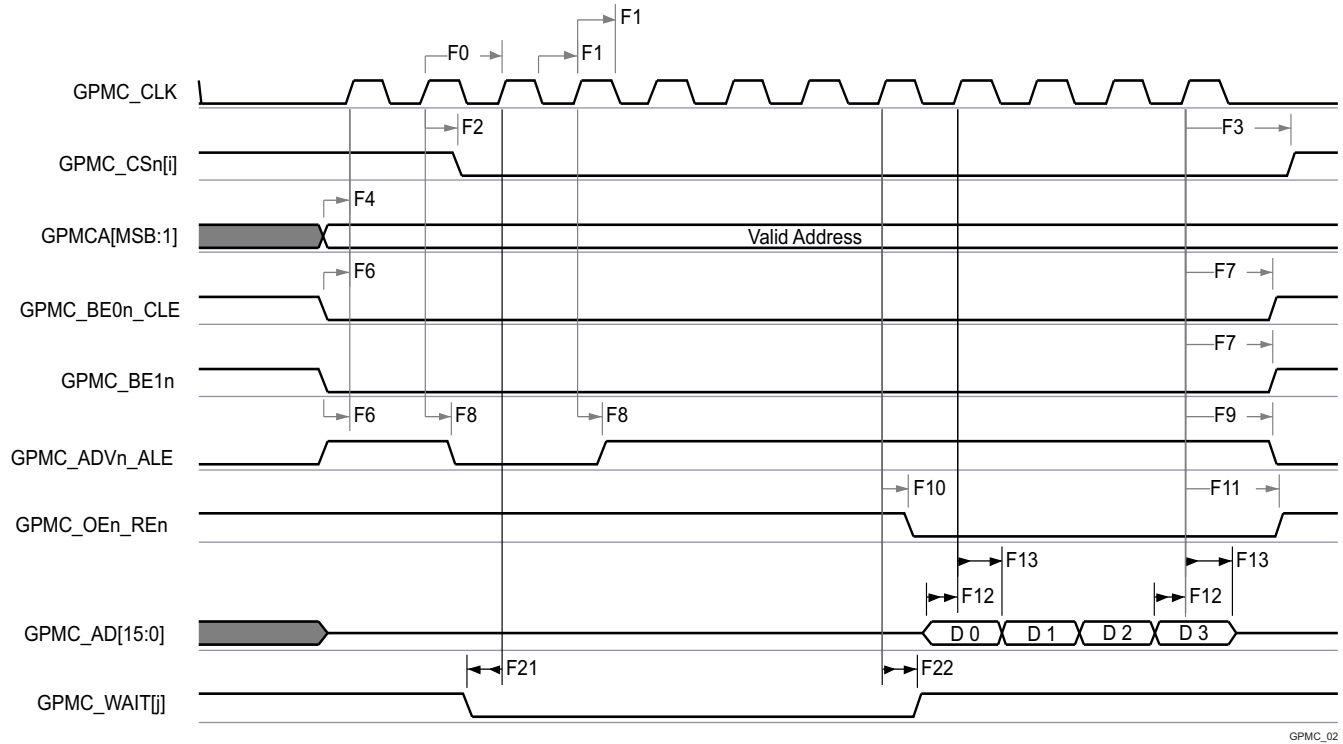
- (1) For single read:  $A = (CSRdOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(17)$   
For burst read:  $A = (CSRdOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(17)$   
For burst write:  $A = (CSWrOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(17)$   
With n being the page burst access number.
- (2)  $B = ClkActivationTime \times GPMC\_FCLK(17)$
- (3) For single read:  $C = RdCycleTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK(17)$   
For burst read:  $C = (RdCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(17)$   
For burst write:  $C = (WrCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(17)$   
With n being the page burst access number.
- (4) For single read:  $D = (RdCycleTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(17)$   
For burst read:  $D = (RdCycleTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(17)$   
For burst write:  $D = (WrCycleTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(17)$
- (5) For single read:  $E = (CSRdOffTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(17)$   
For burst read:  $E = (CSRdOffTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(17)$   
For burst write:  $E = (CSWrOffTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(17)$
- (6) For csn falling edge (CS activated):
  - Case GpmcFCLKDivider = 0:  
–  $F = 0.5 \times CSEExtraDelay \times GPMC\_FCLK(17)$
  - Case GpmcFCLKDivider = 1:  
–  $F = 0.5 \times CSEExtraDelay \times GPMC\_FCLK(17)$  if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
  - $F = (1 + 0.5 \times CSEExtraDelay) \times GPMC\_FCLK(17)$  otherwise
  - Case GpmcFCLKDivider = 2:  
–  $F = 0.5 \times CSEExtraDelay \times GPMC\_FCLK(17)$  if ((CSOnTime - ClkActivationTime) is a multiple of 3)
  - $F = (1 + 0.5 \times CSEExtraDelay) \times GPMC\_FCLK(17)$  if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
  - $F = (2 + 0.5 \times CSEExtraDelay) \times GPMC\_FCLK(17)$  if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)
- (7) For ADV falling edge (ADV activated):
  - Case GpmcFCLKDivider = 0:  
–  $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK(17)$
  - Case GpmcFCLKDivider = 1:  
–  $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK(17)$  if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  - $G = (1 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK(17)$  otherwise
  - Case GpmcFCLKDivider = 2:  
–  $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK(17)$  if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK(17)$  if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK(17)$  if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)
 For ADV rising edge (ADV deactivated) in Reading mode:
  - Case GpmcFCLKDivider = 0:  
–  $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK(17)$
  - Case GpmcFCLKDivider = 1:  
–  $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK(17)$  if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  - $G = (1 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK(17)$  otherwise
  - Case GpmcFCLKDivider = 2:  
–  $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK(17)$  if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK(17)$  if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK(17)$  if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)
- (8) For ADV rising edge (ADV deactivated) in Writing mode:
  - Case GpmcFCLKDivider = 0:  
–  $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK(17)$
  - Case GpmcFCLKDivider = 1:  
–  $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK(17)$  if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - $G = (1 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK(17)$  otherwise
  - Case GpmcFCLKDivider = 2:  
–  $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK(17)$  if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK(17)$  if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK(17)$  if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)
- (9) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):
  - Case GpmcFCLKDivider = 0:  
–  $H = 0.5 \times OEExtraDelay \times GPMC\_FCLK(17)$

- Case GpmcFCLKDivider = 1:  
–  $H = 0.5 \times OEEExtraDelay \times GPMC\_FCLK(17)$  if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)  
–  $H = (1 + 0.5 \times OEEExtraDelay) \times GPMC\_FCLK(17)$  otherwise
- Case GpmcFCLKDivider = 2:  
–  $H = 0.5 \times OEEExtraDelay \times GPMC\_FCLK(17)$  if ((OEOnTime - ClkActivationTime) is a multiple of 3)  
–  $H = (1 + 0.5 \times OEEExtraDelay) \times GPMC\_FCLK(17)$  if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)  
–  $H = (2 + 0.5 \times OEEExtraDelay) \times GPMC\_FCLK(17)$  if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)
- For OE rising edge (OE deactivated):
- Case GpmcFCLKDivider = 0:  
–  $H = 0.5 \times OEEExtraDelay \times GPMC\_FCLK(17)$
- Case GpmcFCLKDivider = 1:  
–  $H = 0.5 \times OEEExtraDelay \times GPMC\_FCLK(17)$  if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)  
–  $H = (1 + 0.5 \times OEEExtraDelay) \times GPMC\_FCLK(17)$  otherwise
- Case GpmcFCLKDivider = 2:  
–  $H = 0.5 \times OEEExtraDelay \times GPMC\_FCLK(17)$  if ((OEOffTime - ClkActivationTime) is a multiple of 3)  
–  $H = (1 + 0.5 \times OEEExtraDelay) \times GPMC\_FCLK(17)$  if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)  
–  $H = (2 + 0.5 \times OEEExtraDelay) \times GPMC\_FCLK(17)$  if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)
- (10) For WE falling edge (WE activated):
- Case GpmcFCLKDivider = 0:  
–  $I = 0.5 \times WEEExtraDelay \times GPMC\_FCLK(17)$
- Case GpmcFCLKDivider = 1:  
–  $I = 0.5 \times WEEExtraDelay \times GPMC\_FCLK(17)$  if (ClkActivationTime and WEOOnTime are odd) or (ClkActivationTime and WEOOnTime are even)  
–  $I = (1 + 0.5 \times WEEExtraDelay) \times GPMC\_FCLK(17)$  otherwise
- Case GpmcFCLKDivider = 2:  
–  $I = 0.5 \times WEEExtraDelay \times GPMC\_FCLK(17)$  if ((WEOOnTime - ClkActivationTime) is a multiple of 3)  
–  $I = (1 + 0.5 \times WEEExtraDelay) \times GPMC\_FCLK(17)$  if ((WEOOnTime - ClkActivationTime - 1) is a multiple of 3)  
–  $I = (2 + 0.5 \times WEEExtraDelay) \times GPMC\_FCLK(17)$  if ((WEOOnTime - ClkActivationTime - 2) is a multiple of 3)
- For WE rising edge (WE deactivated):
- Case GpmcFCLKDivider = 0:  
–  $I = 0.5 \times WEEExtraDelay \times GPMC\_FCLK(17)$
- Case GpmcFCLKDivider = 1:  
–  $I = 0.5 \times WEEExtraDelay \times GPMC\_FCLK(17)$  if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)  
–  $I = (1 + 0.5 \times WEEExtraDelay) \times GPMC\_FCLK(17)$  otherwise
- Case GpmcFCLKDivider = 2:  
–  $I = 0.5 \times WEEExtraDelay \times GPMC\_FCLK(17)$  if ((WEOffTime - ClkActivationTime) is a multiple of 3)  
–  $I = (1 + 0.5 \times WEEExtraDelay) \times GPMC\_FCLK(17)$  if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)  
–  $I = (2 + 0.5 \times WEEExtraDelay) \times GPMC\_FCLK(17)$  if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)
- (11)  $J = GPMC\_FCLK(17)$
- (12) First transfer only for CLK DIV 1 mode.
- (13) Half cycle; for all data after initial transfer for CLK DIV 1 mode.
- (14) Half cycle of GPMC\_CLK\_OUT; for all data for modes other than CLK DIV 1 mode. GPMC\_CLK\_OUT divide down from GPMC\_FCLK.
- (15) In GPMC\_CS[n], x is equal to 0, 1, 2 or 3. In GPMC\_WAIT[x], x is equal to 0 or 1.
- (16)  $P = GPMC\_CLK$  period in ns
- (17) For read:  $K = (ADVrdOffTime - ADVOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(17)$   
For write:  $K = (ADVWrOffTime - ADVOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(17)$
- (18) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.
- (19) 100MHz GPMC\_FCLK selected - CTRLMMR\_GPMC\_CLKSEL[0] CLK\_SEL = 1 = MAIN\_PLL2\_HSDIV7\_CLKOUT (100/60 MHz)
- (20) Trace length from GPMC pins to device assumed to be less than 4" and length matched to within 200ps for 100MHz Synchronous Mode.
- (21) In div\_by\_1\_mode, GPMC0\_CLK refers to either GPMC0\_CLKOUT or GPMC0\_FCLK\_MUX (free-running). Both signals are pin-muxed to the same pin
- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:  
– GPMC0\_CLK frequency = GPMC\_FCLK frequency
- In not\_div\_by\_1\_mode, GPMC0\_CLK only refers to GPMC0\_CLKOUT. GPMC0\_FCLK\_MUX cannot be clock divided to match the GPMC0\_CLKOUT frequency if GPMCFCLKDIVIDER > 0
- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 1h to 3h:  
– GPMC0\_CLK frequency = GPMC\_FCLK frequency / (2 to 4)



- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.  
B. In GPMC\_WAIT[j], j is equal to 0 or 1.

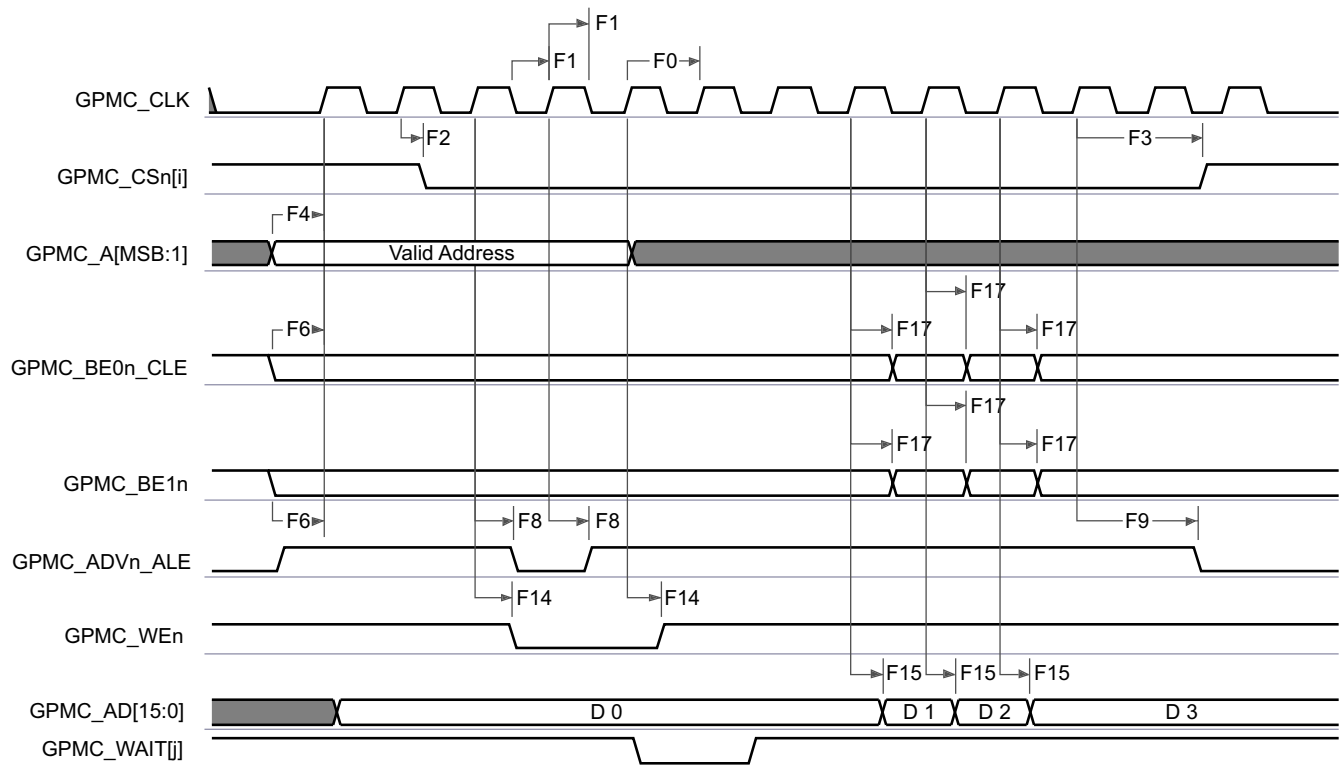
**Figure 6-25. GPMC and NOR Flash — Synchronous Single Read (GPMCFCLKDIVIDER = 0)**



GPMC\_02

- A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3.  
 B. In GPMC\_WAIT[j], j is equal to 0 or 1.

**Figure 6-26. GPMC and NOR Flash — Synchronous Burst Read — 4x16-bit (GPMCFCLKDIVIDER = 0)**

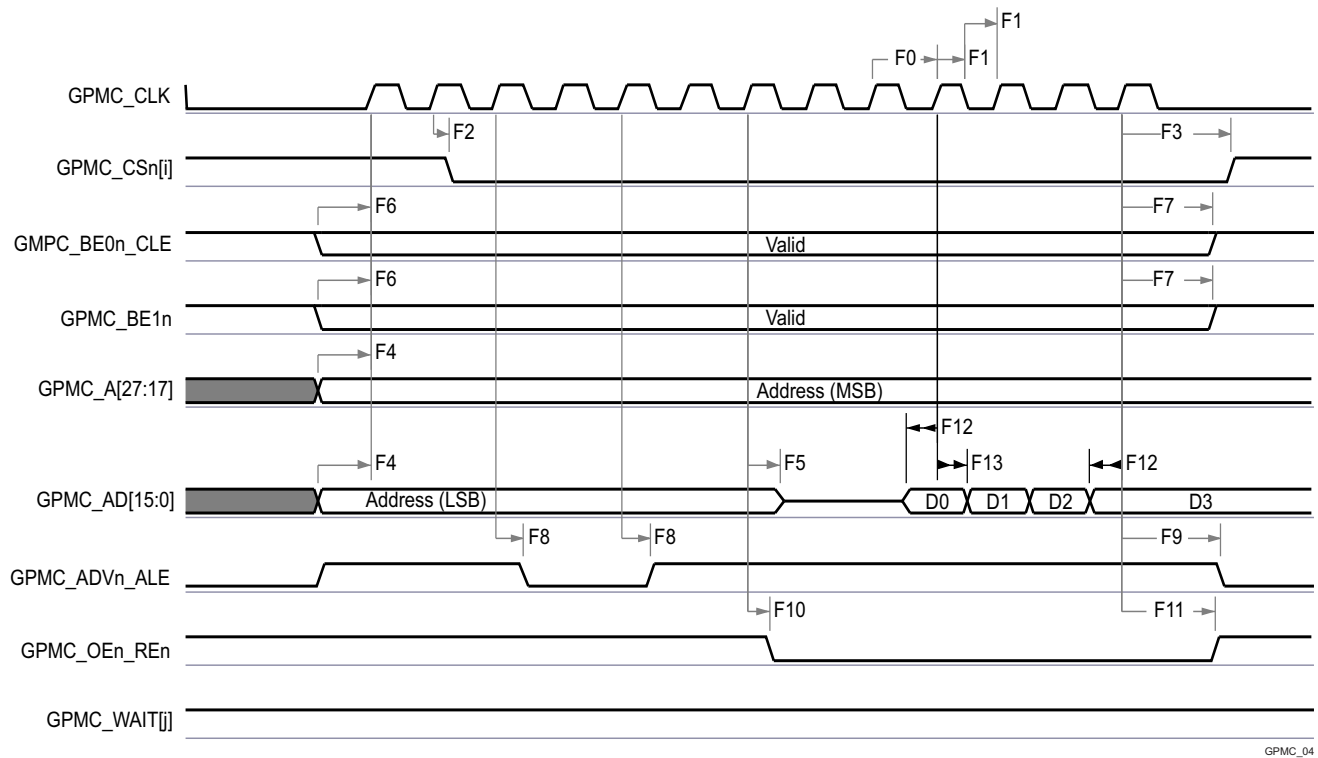


GPMC\_03

- A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3.

B. In GPMC\_WAIT[j], j is equal to 0 or 1.

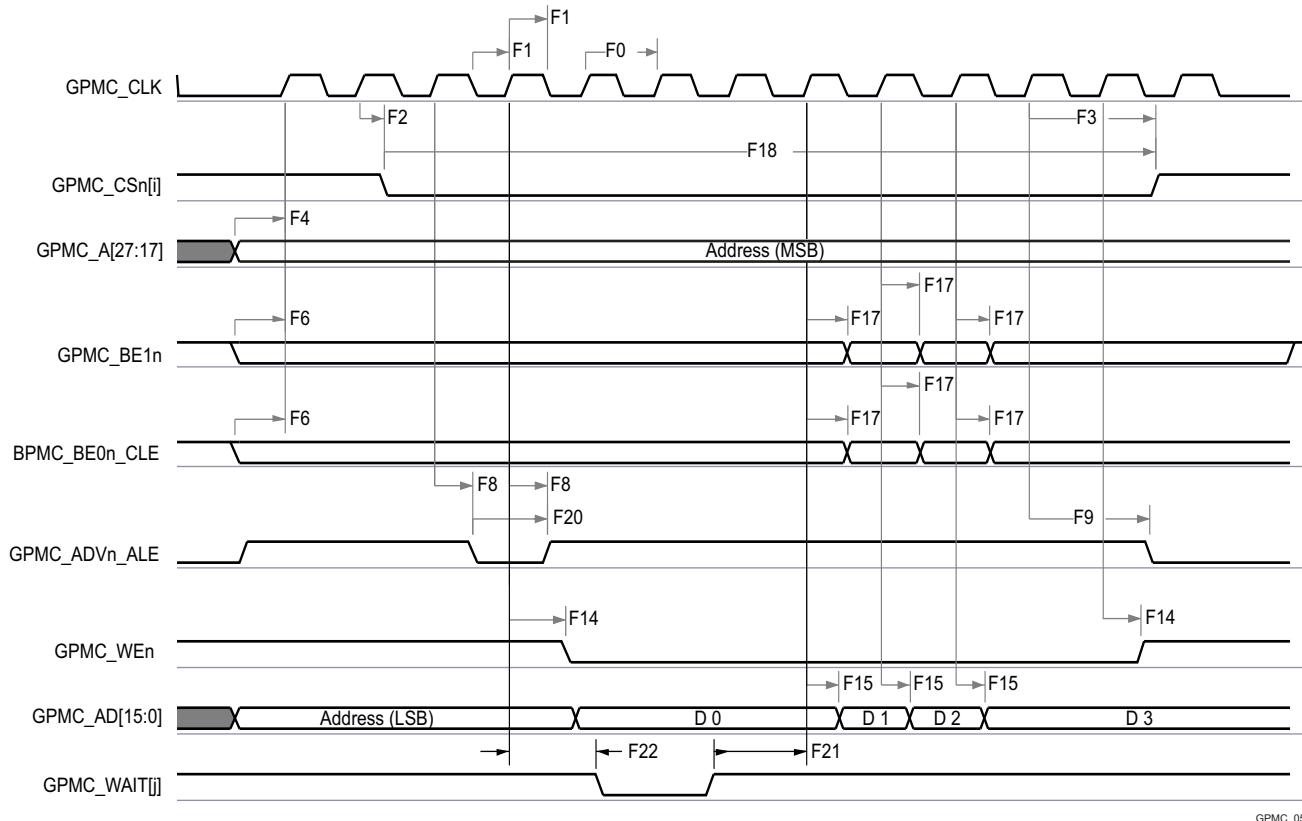
**Figure 6-27. GPMC and NOR Flash—Synchronous Burst Write (GPMCFCLKDIVIDER = 0)**



A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3.

B. In GPMC\_WAIT[j], j is equal to 0 or 1.

**Figure 6-28. GPMC and Multiplexed NOR Flash — Synchronous Burst Read**



- A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3.  
 B. In GPMC\_WAIT[j], j is equal to 0 or 1.

**Figure 6-29. GPMC and Multiplexed NOR Flash — Synchronous Burst Write**

#### 6.11.5.7.4 GPMC/NOR Flash Timing Requirements - Asynchronous Mode 100MHz

(6) (7)

| NO.                 | PARAMETER            | DESCRIPTION                           | MIN | MAX              | UNIT |
|---------------------|----------------------|---------------------------------------|-----|------------------|------|
| FA5 <sup>(1)</sup>  | $t_{acc(d)}$         | Data access time                      |     | H <sup>(5)</sup> | ns   |
| FA20 <sup>(2)</sup> | $t_{acc1-pgmode(d)}$ | Page mode successive data access time |     | P <sup>(4)</sup> | ns   |
| FA21 <sup>(3)</sup> | $t_{acc2-pgmode(d)}$ | Page mode first data access time      |     | H <sup>(5)</sup> | ns   |

- (1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
- (2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
- (3) The FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.
- (4)  $P = \text{PageBurstAccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}(6)$
- (5)  $H = \text{AccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}(6)$
- (6) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.
- (7) 133MHz GPMC\_FCLK selected - CTRLMMR\_GPMC\_CLKSEL[0] CLK\_SEL = 0 = MAIN\_PLL0\_HSDIV3\_CLKOUT (133/100/80 MHz)

**6.11.5.7.5 GPMC/NOR Flash Switching Characteristics - Asynchronous Mode 100MHz**

(14) (15)

| NO.  | PARAMETER             | DESCRIPTION                                                                           | MODE  | MIN                   | MAX                   | UNIT |
|------|-----------------------|---------------------------------------------------------------------------------------|-------|-----------------------|-----------------------|------|
| FA0  | $t_{w(be[x]nV)}$      | Pulse duration, GPMC0_BE0n_CLE, GPMC0_BE1n valid time                                 | Read  |                       | N <sup>(12)</sup>     | ns   |
|      |                       |                                                                                       | Write |                       | N <sup>(12)</sup>     | ns   |
| FA1  | $t_{w(csnV)}$         | Pulse duration, GPMC0_CSn[x] <sup>(13)</sup> low                                      | Read  |                       | A <sup>(1)</sup>      | ns   |
|      |                       |                                                                                       | Write |                       | A <sup>(1)</sup>      | ns   |
| FA3  | $t_{d(csnV-advnV)}$   | Delay time, GPMC0_CSn[x] <sup>(13)</sup> valid to GPMC0_ADVn_ALE invalid              | Read  | B <sup>(2)</sup> – 2  | B <sup>(2)</sup> + 2  | ns   |
|      |                       |                                                                                       | Write | B <sup>(2)</sup> – 2  | B <sup>(2)</sup> + 2  | ns   |
| FA4  | $t_{d(csnV-oenV)}$    | Delay time, GPMC0_CSn[x] <sup>(13)</sup> valid to GPMC0_OEn_REn invalid (Single read) |       | C <sup>(3)</sup> – 2  | C <sup>(3)</sup> + 2  | ns   |
| FA9  | $t_{d(aV-csnV)}$      | Delay time, GPMC0_A[27:1] valid to GPMC0_CSn[x] <sup>(13)</sup> valid                 |       | J <sup>(9)</sup> – 2  | J <sup>(9)</sup> + 2  | ns   |
| FA10 | $t_{d(be[x]nV-csnV)}$ | Delay time, GPMC0_BE0n_CLE, GPMC0_BE1n valid to GPMC0_CSn[x] <sup>(13)</sup> valid    |       | J <sup>(9)</sup> – 2  | J <sup>(9)</sup> + 2  | ns   |
| FA12 | $t_{d(csnV-advnV)}$   | Delay time, GPMC0_CSn[x] <sup>(13)</sup> valid to GPMC0_ADVn_ALE valid                |       | K <sup>(10)</sup> – 2 | K <sup>(10)</sup> + 2 | ns   |
| FA13 | $t_{d(csnV-oenV)}$    | Delay time, GPMC0_CSn[x] <sup>(13)</sup> valid to GPMC0_OEn_REn valid                 |       | L <sup>(11)</sup> – 2 | L <sup>(11)</sup> + 2 | ns   |
| FA16 | $t_{w(aV)}$           | Pulse duration GPMC0_A[26:1] invalid between two successive read and write accesses   |       | G <sup>(7)</sup>      |                       | ns   |
| FA18 | $t_{d(csnV-oenV)}$    | Delay time, GPMC0_CSn[x] <sup>(13)</sup> valid to GPMC0_OEn_REn invalid (Burst read)  |       | I <sup>(8)</sup> – 2  | I <sup>(8)</sup> + 2  | ns   |
| FA20 | $t_{w(av)}$           | Pulse duration, GPMC0_A[27:1] valid - 2nd, 3rd, and 4th accesses                      |       | D <sup>(4)</sup>      |                       | ns   |
| FA25 | $t_{d(csnV-wenV)}$    | Delay time, GPMC0_CSn[x] <sup>(13)</sup> valid to GPMC0_WEn valid                     |       | E <sup>(5)</sup> – 2  | E <sup>(5)</sup> + 2  | ns   |
| FA27 | $t_{d(csnV-wenV)}$    | Delay time, GPMC0_CSn[x] <sup>(13)</sup> valid to GPMC0_WEn invalid                   |       | F <sup>(6)</sup> – 2  | F <sup>(6)</sup> + 2  | ns   |
| FA28 | $t_{d(wenV-dV)}$      | Delay time, GPMC0_WEn valid to GPMC0_AD[31:0] valid                                   |       |                       | 2                     | ns   |
| FA29 | $t_{d(dV-csnV)}$      | Delay time, GPMC0_AD[31:0] valid to GPMC0_CSn[x] <sup>(13)</sup> valid                |       | J <sup>(9)</sup> – 2  | J <sup>(10)</sup> + 2 | ns   |
| FA37 | $t_{d(oenV-aV)}$      | Delay time, GPMC0_OEn_REn valid to GPMC0_AD[31:0] phase end                           |       |                       | 2                     | ns   |

- (1) For single read:  $A = (CSRdOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(14)$   
For single write:  $A = (CSWrOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(14)$   
For burst read:  $A = (CSRdOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(14)$   
For burst write:  $A = (CSWrOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(14)$   
with n being the page burst access number
- (2) For reading:  $B = ((ADVrdOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK(14)$   
For writing:  $B = ((ADVWrOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK(14)$
- (3)  $C = \lfloor ((OEOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \rfloor \times GPMC\_FCLK(14)$
- (4)  $D = PageBurstAccessTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK(14)$
- (5)  $E = \lfloor ((WEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \rfloor \times GPMC\_FCLK(14)$
- (6)  $F = \lfloor ((WEOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \rfloor \times GPMC\_FCLK(14)$
- (7)  $G = Cycle2CycleDelay \times GPMC\_FCLK(14)$
- (8)  $I = \lfloor ((OEOffTime + (n - 1) \times PageBurstAccessTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \rfloor \times GPMC\_FCLK(14)$
- (9)  $J = (CSOnTime \times (TimeParaGranularity + 1) + 0.5 \times CSEExtraDelay) \times GPMC\_FCLK(14)$
- (10)  $K = \lfloor ((ADVOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \rfloor \times GPMC\_FCLK(14)$
- (11)  $L = \lfloor ((OEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \rfloor \times GPMC\_FCLK(14)$
- (12) For single read:  $N = RdCycleTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK(14)$   
For single write:  $N = WrCycleTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK(14)$

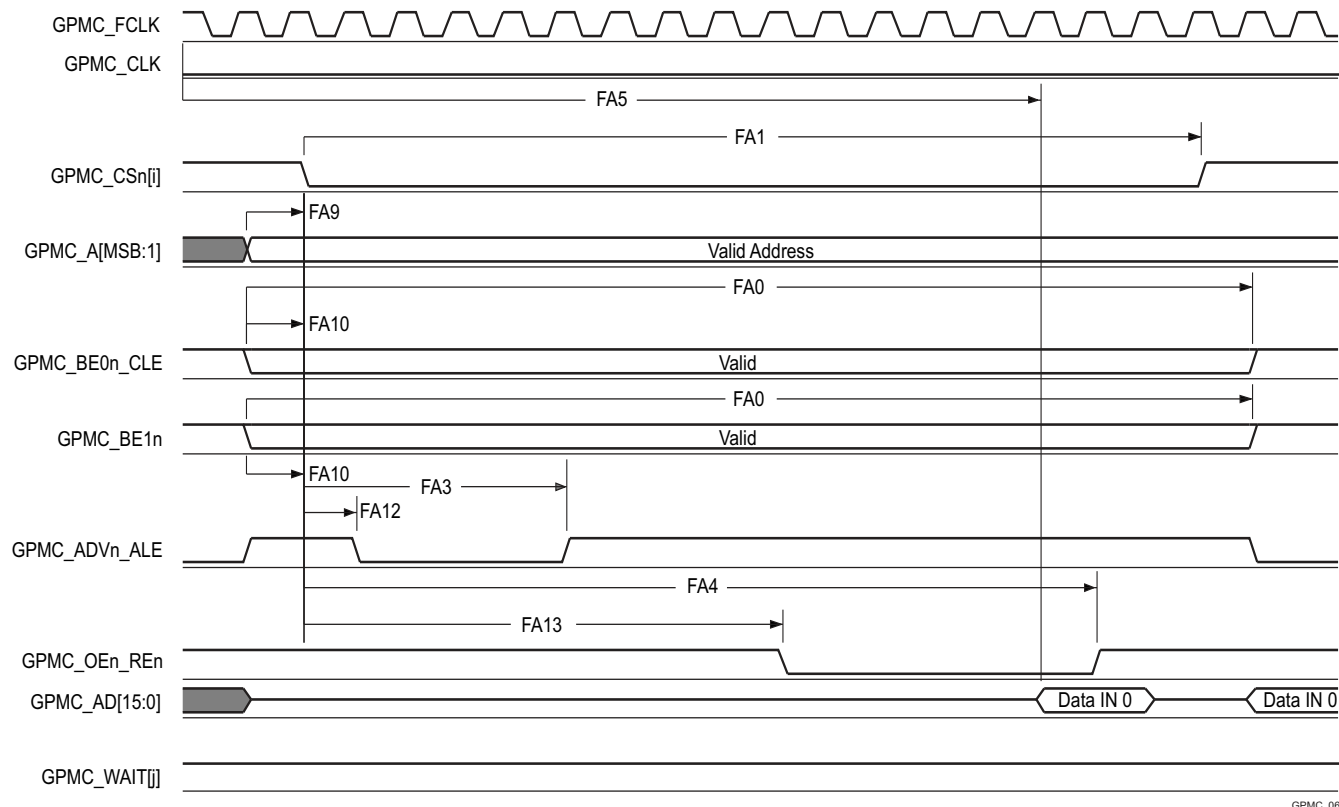
For burst read:  $N = (RdCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(14)$

For burst write:  $N = (WrCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(14)$

(13) In GPMC\_CSn[x], x is equal to 0, 1, 2 or 3.

(14) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.

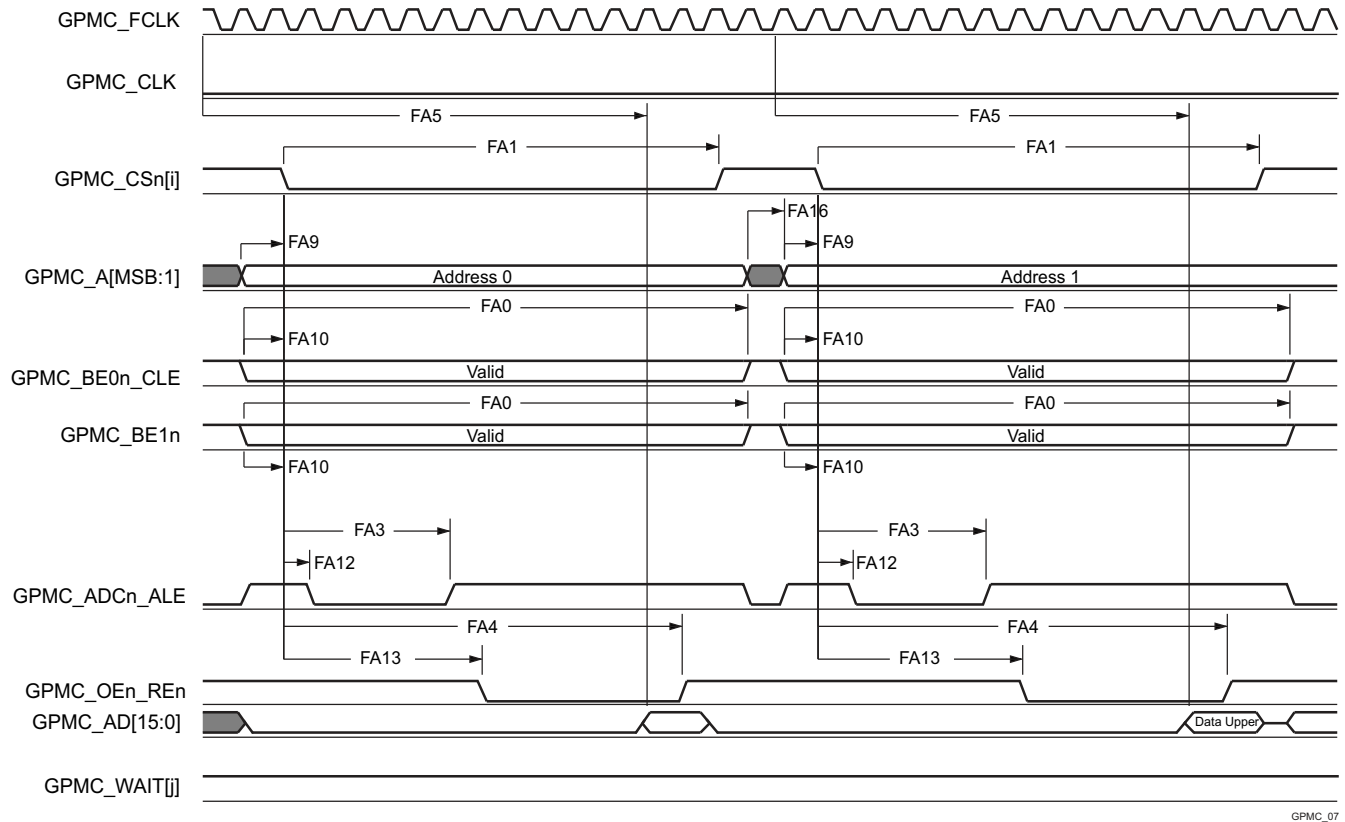
(15) 133MHz GPMC\_FCLK selected - CTRLMMR\_GPMC\_CLKSEL[0] CLK\_SEL = 0 = MAIN\_PLL0\_HSDIV3\_CLKOUT (133/100/80 MHz)



GPMC\_06

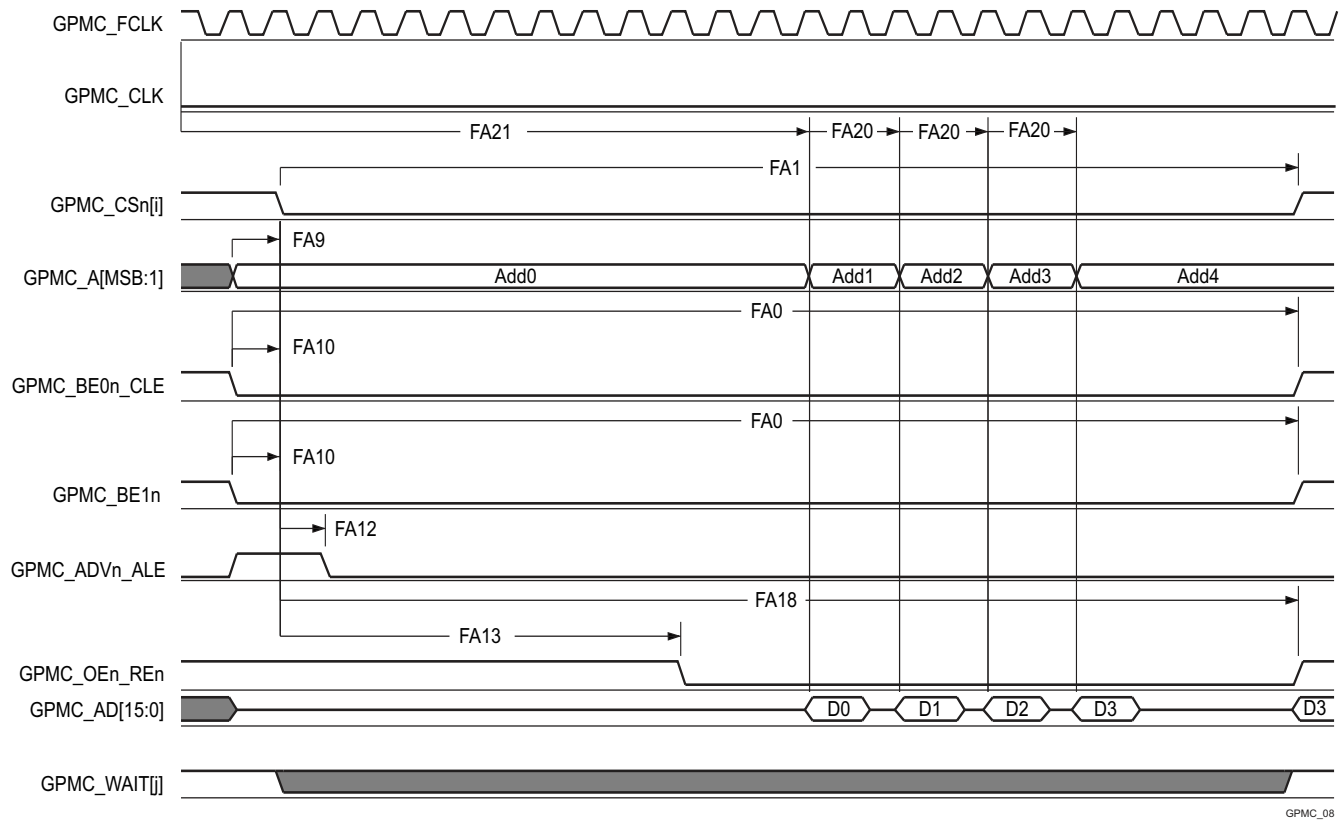
- A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.
- B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- C. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

**Figure 6-30. GPMC and NOR Flash — Asynchronous Read — Single Word**



- A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.
- B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- C. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

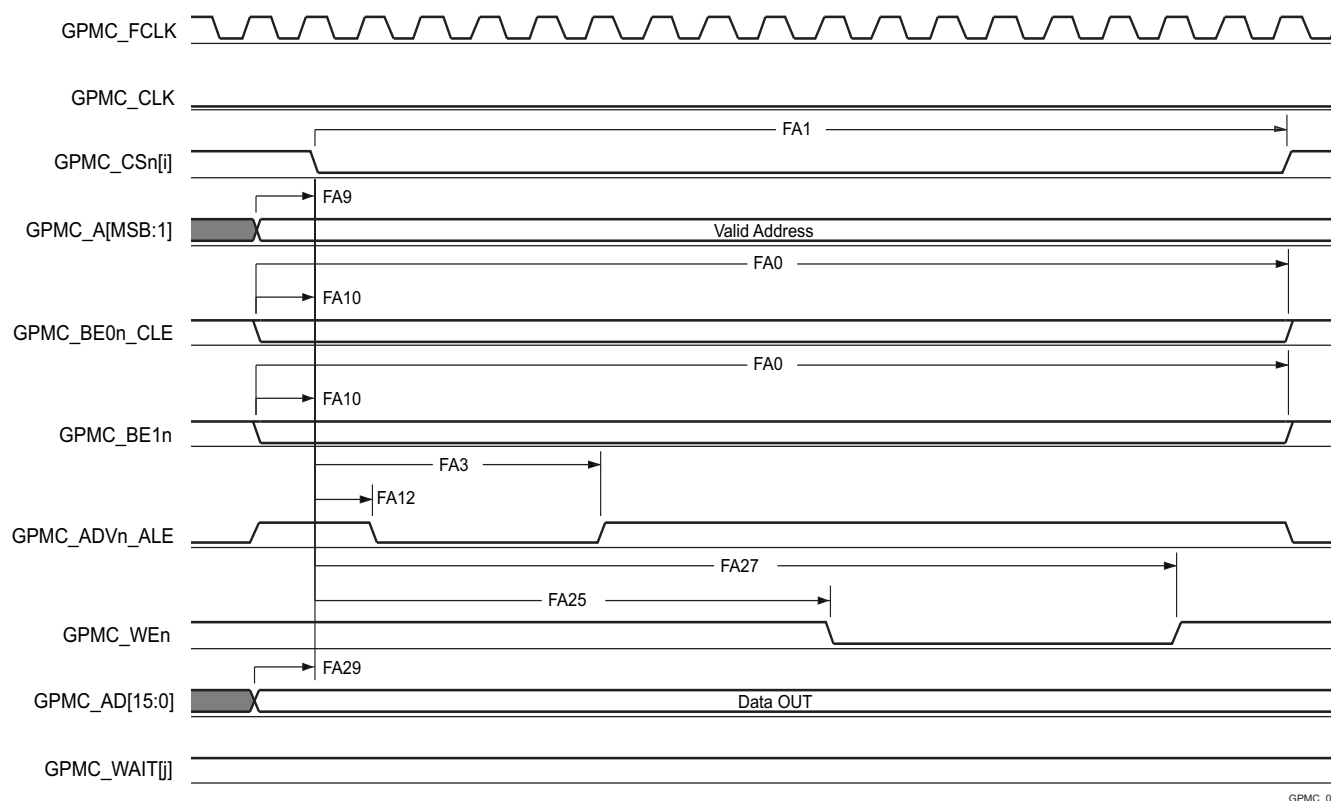
**Figure 6-31. GPMC and NOR Flash — Asynchronous Read — 32-Bit**



GPMC\_08

- In  $\text{GPMC\_CSn}[i]$ ,  $i$  is equal to 0, 1, 2 or 3. In  $\text{GPMC\_WAIT}[j]$ ,  $j$  is equal to 0 or 1.
- FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.
- FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

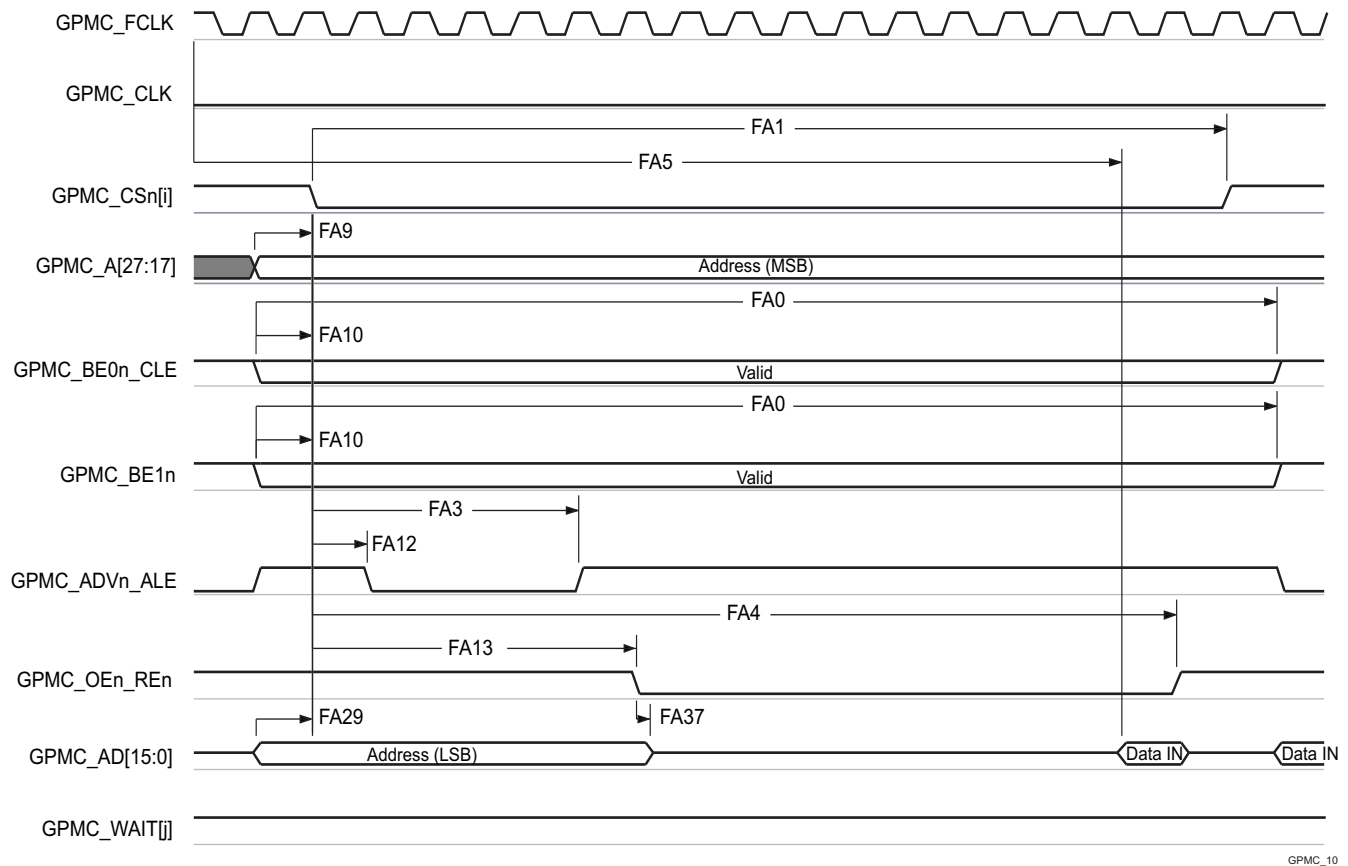
**Figure 6-32. GPMC and NOR Flash — Asynchronous Read — Page Mode 4x16-Bit**



GPMC\_09

A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.

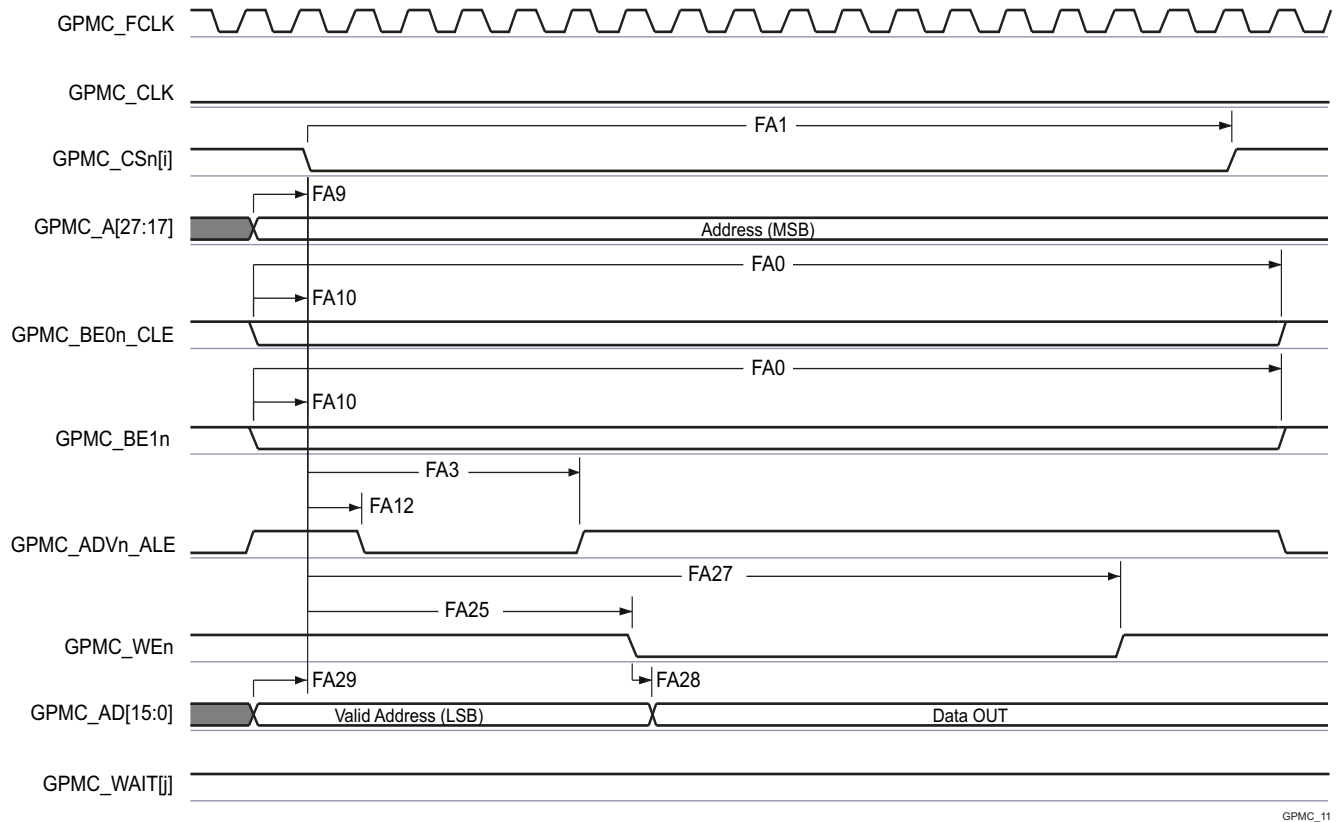
**Figure 6-33. GPMC and NOR Flash — Asynchronous Write — Single Word**



GPMC\_10

- In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.
- FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

**Figure 6-34. GPMC and Multiplexed NOR Flash — Asynchronous Read — Single Word**



GPMC\_11

A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.

**Figure 6-35. GPMC and Multiplexed NOR Flash — Asynchronous Write — Single Word**

#### 6.11.5.7.6 GPMC/NAND Flash Timing Requirements - Asynchronous Mode 100MHz

(4)

| NO.                  | PARAMETER    | DESCRIPTION                                | MIN | MAX              | UNIT |
|----------------------|--------------|--------------------------------------------|-----|------------------|------|
| GNF12 <sup>(1)</sup> | $t_{acc(d)}$ | Access time, GPMC0_AD[31:0] <sup>(3)</sup> |     | J <sup>(2)</sup> | ns   |

- (1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.
- (2)  $J = AccessTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK$ (3)
- (3) GPMC\_FCLK is general-purpose memory controller internal functional clock.
- (4) 133MHz GPMC\_FCLK selected - CTRLMMR\_GPMC\_CLKSEL[0] CLK\_SEL = 0 = MAIN\_PLL0\_HSDIV3\_CLKOUT (133/100/80 MHz)

### 6.11.5.7.7 GPMC/NAND Flash Switching Characteristics - Asynchronous Mode 100MHz

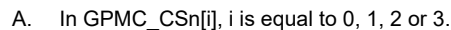
(15)

| NO.   | PARAMETER            | DESCRIPTION                                                              | MIN                   | MAX                   | UNIT |
|-------|----------------------|--------------------------------------------------------------------------|-----------------------|-----------------------|------|
| GNF0  | $t_{w(wenV)}$        | Pulse duration, GPMC0_WEn valid                                          | A <sup>(1)</sup>      |                       | ns   |
| GNF1  | $t_{d(csnV-wenV)}$   | Delay time, GPMC0_CS[n] <sup>(13)</sup> valid to GPMC0_WEn valid         | B <sup>(2)</sup> – 2  | B <sup>(2)</sup> + 2  | ns   |
| GNF2  | $t_{w(cleH-wenV)}$   | Delay time, GPMC0_BE0n_CLE high to GPMC0_WEn valid                       | C <sup>(3)</sup> – 2  | C <sup>(3)</sup> + 2  | ns   |
| GNF3  | $t_{w(wenV-dV)}$     | Delay time, GPMC0_AD[31:0] valid to GPMC0_WEn valid                      | D <sup>(4)</sup> – 2  | D <sup>(4)</sup> + 2  | ns   |
| GNF4  | $t_{w(wenIV-dIV)}$   | Delay time, GPMC0_WEn invalid to GPMC0_AD[31:0] invalid                  | E <sup>(5)</sup> – 2  | E <sup>(5)</sup> + 2  | ns   |
| GNF5  | $t_{w(wenIV-cleIV)}$ | Delay time, GPMC0_WEn invalid to GPMC0_BE0n_CLE invalid                  | F <sup>(6)</sup> – 2  | F <sup>(6)</sup> + 2  | ns   |
| GNF6  | $t_{w(wenIV-csnIV)}$ | Delay time, GPMC0_WEn invalid to GPMC0_CS[n] <sup>(13)</sup> invalid     | G <sup>(7)</sup> – 2  | G <sup>(7)</sup> + 2  | ns   |
| GNF7  | $t_{w(aleH-wenV)}$   | Delay time, GPMC0_ADVn_ALE high to GPMC0_WEn valid                       | C <sup>(3)</sup> – 2  | C <sup>(3)</sup> + 2  | ns   |
| GNF8  | $t_{w(wenIV-aleIV)}$ | Delay time, GPMC0_WEn invalid to GPMC0_ADVn_ALE invalid                  | F <sup>(6)</sup> – 2  | F <sup>(6)</sup> + 2  | ns   |
| GNF9  | $t_{c(wen)}$         | Cycle time, write                                                        |                       | H <sup>(8)</sup>      | ns   |
| GNF10 | $t_{d(csnV-oenV)}$   | Delay time, GPMC0_CS[n] <sup>(13)</sup> valid to GPMC0_OEn_REn valid     | I <sup>(9)</sup> – 2  | I <sup>(9)</sup> + 2  | ns   |
| GNF13 | $t_{w(oenV)}$        | Pulse duration, GPMC0_OEn_REn valid                                      |                       | K <sup>(10)</sup>     | ns   |
| GNF14 | $t_{c(oen)}$         | Cycle time, read                                                         | L <sup>(11)</sup>     |                       | ns   |
| GNF15 | $t_{w(oenIV-csnIV)}$ | Delay time, GPMC0_OEn_REn invalid to GPMC0_CS[n] <sup>(13)</sup> invalid | M <sup>(12)</sup> – 2 | M <sup>(12)</sup> + 2 | ns   |

(1)  $A = (WEOffTime - WEOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK(14)$ (2)  $B = \lfloor ((WEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \rfloor \times GPMC\_FCLK(14)$ (3)  $C = \lfloor ((WEOnTime - ADVOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - ADVExtraDelay)) \rfloor \times GPMC\_FCLK(14)$ (4)  $D = (WEOnTime \times (TimeParaGranularity + 1) + 0.5 \times WEEExtraDelay) \times GPMC\_FCLK(14)$ (5)  $E = \lfloor ((WrCycleTime - WEOffTime) \times (TimeParaGranularity + 1) - 0.5 \times WEEExtraDelay) \rfloor \times GPMC\_FCLK(14)$ (6)  $F = \lfloor ((ADVWrOffTime - WEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - WEEExtraDelay)) \rfloor \times GPMC\_FCLK(14)$ (7)  $G = \lfloor ((CSWrOffTime - WEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - WEEExtraDelay)) \rfloor \times GPMC\_FCLK(14)$ (8)  $H = WrCycleTime \times (1 + TimeParaGranularity) \times GPMC\_FCLK(14)$ (9)  $I = \lfloor ((OEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEEExtraDelay - CSEExtraDelay)) \rfloor \times GPMC\_FCLK(14)$ (10)  $K = (OEOffTime - OEOnTime) \times (1 + TimeParaGranularity) \times GPMC\_FCLK(14)$ (11)  $L = RdCycleTime \times (1 + TimeParaGranularity) \times GPMC\_FCLK(14)$ (12)  $M = \lfloor ((CSRdOffTime - OEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - OEEExtraDelay)) \rfloor \times GPMC\_FCLK(14)$ 

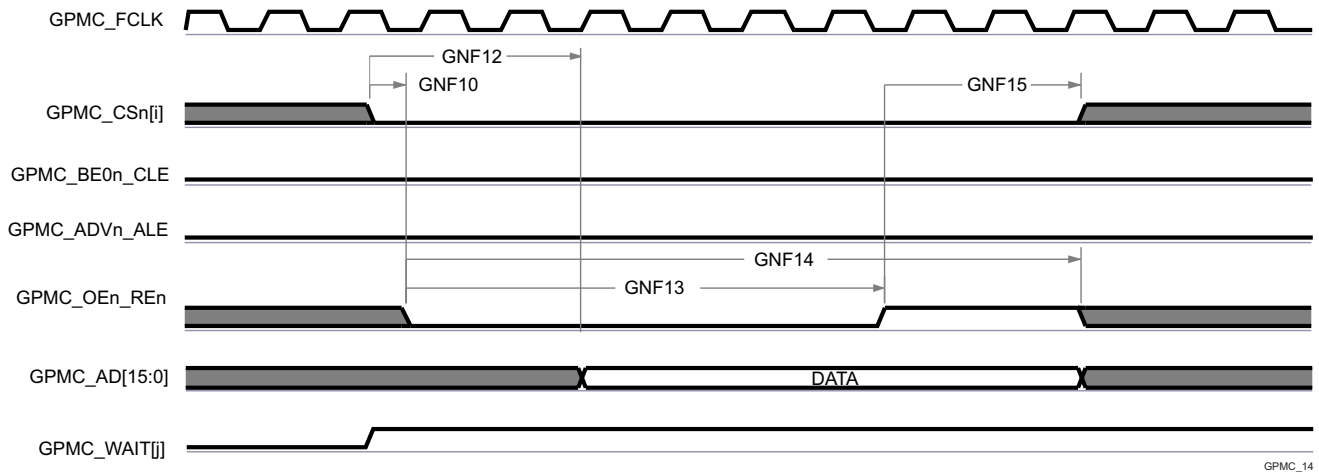
(13) In GPMC\_CS[n], x is equal to 0, 1, 2 or 3.

(14) 133MHz GPMC\_FCLK selected - CTRLMMR\_GPMC\_CLKSEL[0] CLK\_SEL = 0 = MAIN\_PLL0\_HSDIV3\_CLKOUT (133/100/80 MHz)



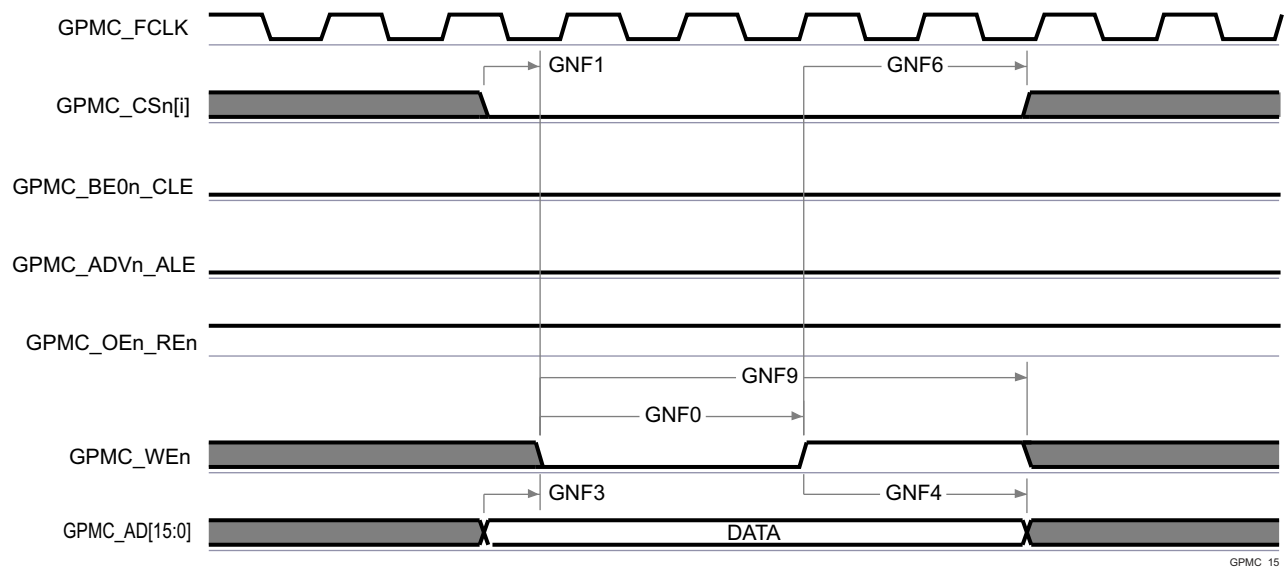
A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3.

Product Folder Links: [AM2634](#) [AM2634-Q1](#) [AM2632](#) [AM2632-Q1](#) [AM2631](#) [AM2631-Q1](#)



- A. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
- B. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.
- C. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.

**Figure 6-38. GPMC and NAND Flash — Data Read Cycle**



- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.

**Figure 6-39. GPMC and NAND Flash — Data Write Cycle**

#### 6.11.5.8 Inter-Integrated Circuit (I<sup>2</sup>C)

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see the *Inter-Integrated Circuit (I2C)* section in the device TRM.

#### 6.11.5.8.1 I2C

The device contains four multicontroller Inter-Integrated Circuit (I2C) controllers. Each I2C controller was designed to be compliant to the Philips I2C-bus™ specification version 2.1. However, the device IOs are not fully compliant to the I2C electrical specification. The speeds supported and exceptions are described per port below:

- I2C1, I2C2, and I2C3
  - Speeds:
    - Standard-mode (up to 100Kbits/s)
      - 3.3V
    - Fast-mode (up to 400Kbits/s)
      - 3.3V
  - Exceptions:
    - The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification because the IOs are implemented with higher performance LVCMOS push-pull IOs that were designed to support other signal functions that could not be implemented with I2C compatible IOs. The LVCMOS IOs being used on these ports are connected so they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.
    - The I2C specification defines a maximum input voltage  $V_{IH}$  of  $(V_{DD_{max}} + 0.5V)$ , which exceeds the absolute maximum ratings for the device IOs. The system must be designed to provide the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this data sheet.
- I2C0
  - Speeds:
    - Standard-mode (up to 100Kbits/s)
      - 3.3V
    - Fast-mode (up to 400Kbits/s)
      - 3.3V
  - Exceptions:
    - The IOs associated with this port were not design to support Hs-mode.
    - The rise and fall times of the I2C signals connected to these ports must not exceed a slew rate of 0.8V/ns (or 8E+7V/s). This limit is more restrictive than the minimum fall time limits defined in the I2C specification. Therefore, it may be necessary to add additional capacitance to the I2C signals to slow the rise and fall times such that the signals do not exceed a slew rate of 0.8V/ns.
    - The I2C specification defines a maximum input voltage  $V_{IH}$  of  $(V_{DD_{max}} + 0.5V)$ , which exceeds the absolute maximum ratings for the device IOs. The system must be designed to make sure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this data sheet.

Refer to the Philips I2C-bus specification version 2.1 for timing details.

For more details about features and additional description information on the device Inter-integrated Circuit, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

### 6.11.5.9 Local Interconnect Network (LIN)

#### Note

The device has multiple LIN modules. LINn is a generic prefix applied to LIN signal names, where n represents the specific LIN module.

For more information, see the *Local Interconnect Network (LIN) Module* section in the device TRM.

#### 6.11.5.9.1 LIN Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 2   | 15  | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 5   | 20  | pF   |

#### 6.11.5.9.2 LIN Timing Requirements

| NO.  | PARAMETER               | DESCRIPTION                                       | MIN | MAX | UNIT |
|------|-------------------------|---------------------------------------------------|-----|-----|------|
| LIN2 | t <sub>d(LINn_RX)</sub> | Delay time, LINn_RX shift register to LINn_RX pin | 0   | 10  | ns   |

#### 6.11.5.9.3 LIN Switching Characteristics

| NO.  | PARAMETER               | DESCRIPTION                                       | MIN | MAX | UNIT |
|------|-------------------------|---------------------------------------------------|-----|-----|------|
| LIN4 | t <sub>d(LINn_TX)</sub> | Delay time, LINn_TX shift register to LINn_TX pin |     | 10  | ns   |

#### 6.11.5.10 Modular Controller Area Network (MCAN)

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

#### Note

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

For more information, see *Controller Area Network (MCAN)* section in the device TRM.

##### 6.11.5.10.1 MCAN Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 2   | 15  | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 5   | 20  | pF   |

##### 6.11.5.10.2 MCAN Switching Characteristics

| NO. | PARAMETER                | DESCRIPTION                                         | MIN | MAX | UNIT |
|-----|--------------------------|-----------------------------------------------------|-----|-----|------|
| M1  | t <sub>d</sub> (MCAN_TX) | Delay time, transmit shift register to MCANn_TX pin |     | 10  | ns   |
| M2  | t <sub>d</sub> (MCAN_RX) | Delay time, MCANn_RX pin to receive shift register  |     | 10  | ns   |

#### 6.11.5.11 Serial Peripheral Interface (SPI)

For more details about features and additional description information on the device Serial Port Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

##### Note

The device has multiple SPI modules. The generic SPI\_ prefix is used to represent the signal names for all SPI instances.

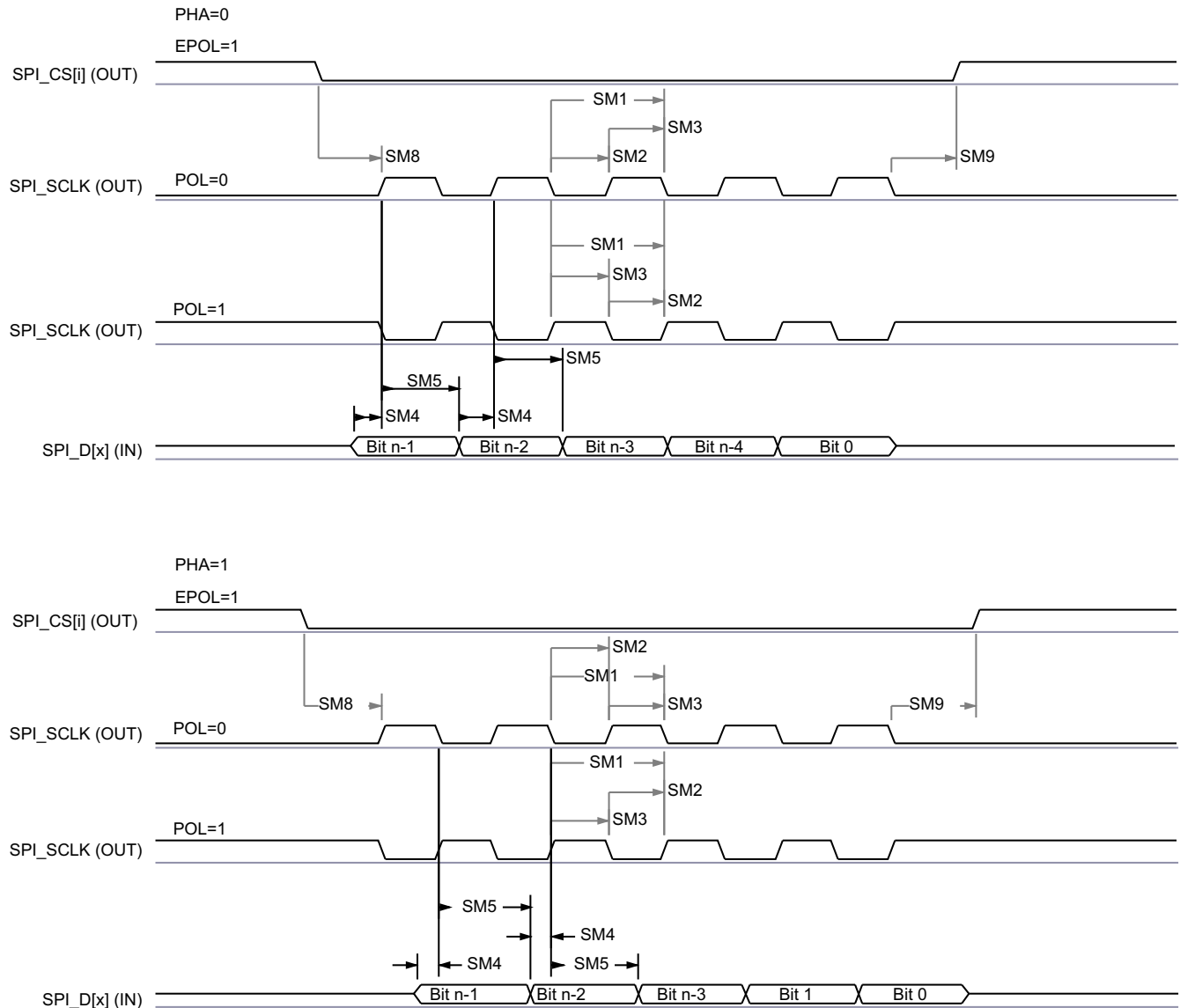
For more information, see the *Serial Peripheral Interface (SPI)* section in the device TRM.

##### 6.11.5.11.1 SPI Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 2   | 8.5 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 2   | 24  | pF   |

##### 6.11.5.11.2 SPI Controller Mode Timing Requirements

| NO.                | PARAMETER                     | DESCRIPTION                                            | MIN | MAX | UNIT |
|--------------------|-------------------------------|--------------------------------------------------------|-----|-----|------|
| <b>Normal Mode</b> |                               |                                                        |     |     |      |
| SM4                | t <sub>su</sub> (MISO-SPICLK) | Setup time, spi_d[x] valid before spi_sclk active edge | 2   |     | ns   |
| SM5                | t <sub>h</sub> (SPICLK-MISO)  | Hold time, spi_d[x] valid after spi_sclk active edge   | 3   |     | ns   |



SPRSP08\_TIMING\_McSPI\_02

**Figure 6-40. SPI Controller Mode Receive Timing**

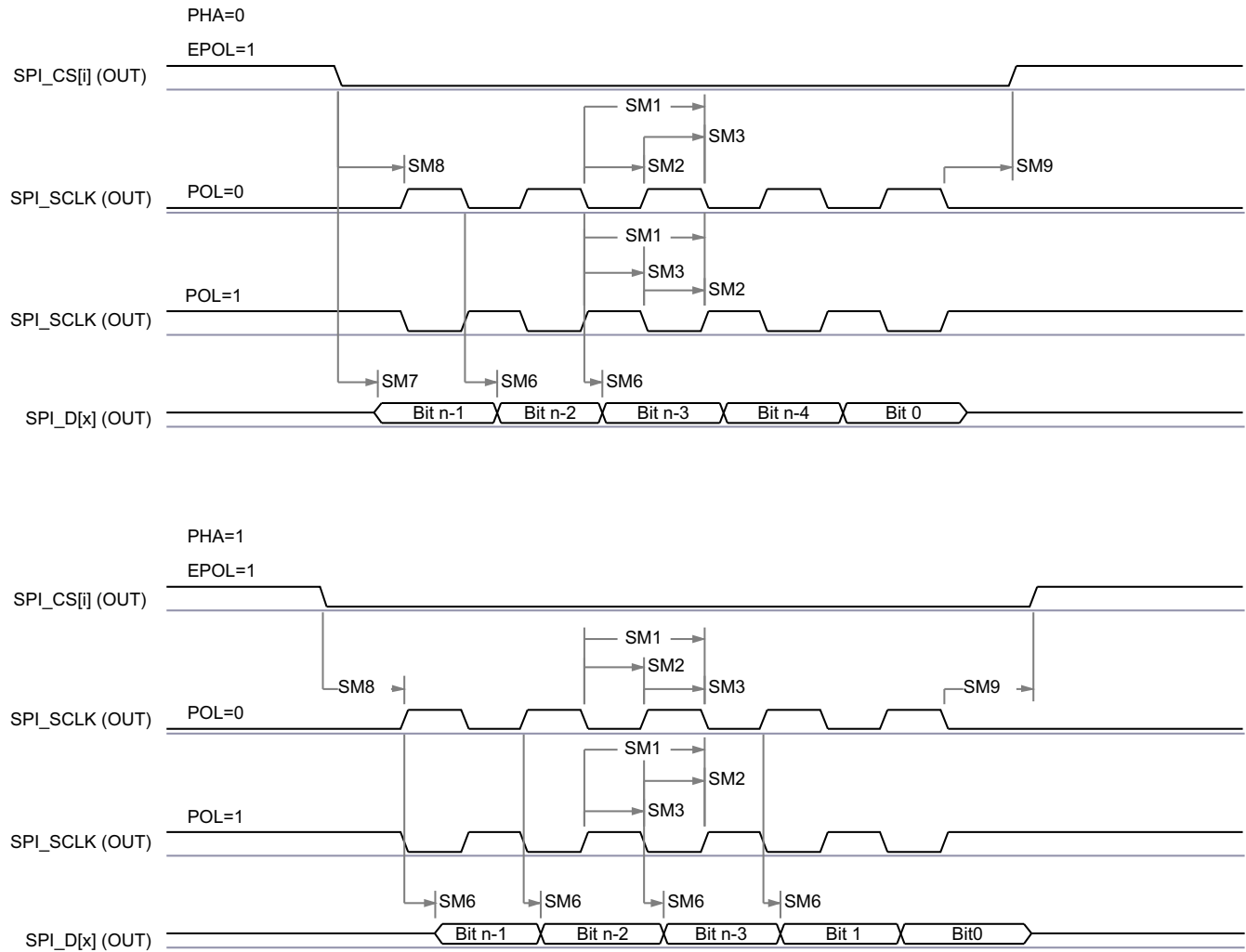
**6.11.5.11.3 SPI Controller Mode Switching Characteristics (Clock Phase = 0)**

| NO.                | PARAMETER                 | DESCRIPTION                                             |         | MIN               | MAX | UNIT |
|--------------------|---------------------------|---------------------------------------------------------|---------|-------------------|-----|------|
| <b>Normal Mode</b> |                           |                                                         |         |                   |     |      |
| SM1                | $t_c(\text{SPICLK})$      | Cycle time, spi_sclk                                    |         | 20                |     | ns   |
| SM2                | $t_w(\text{SPICLK}_L)$    | Typical Pulse duration, spi_sclk low                    |         | $-1 + 0.5P^{(1)}$ |     | ns   |
| SM3                | $t_w(\text{SPICLK}_H)$    | Typical Pulse duration, spi_sclk high                   |         | $-1 + 0.5P^{(1)}$ |     | ns   |
| SM6                | $t_d(\text{SPICLK-SIMO})$ | Delay time, spi_sclk active edge to spi_d[x] transition |         | -3                | 2   | ns   |
| SM7                | $t_{sk}(\text{CS-SIMO})$  | Delay time, spi_cs[x] active to spi_d[x] transition     |         | 5                 |     | ns   |
| SM8                | $t_d(\text{SPICLK-CS})$   | Delay time, spi_cs[x] active to spi_sclk first edge     | PHA = 0 | $-4 + B^{(3)}$    |     | ns   |
|                    |                           |                                                         | PHA = 1 | $-4 + A^{(2)}$    |     | ns   |
| SM9                | $t_d(\text{SPICLK-CS})$   | Delay time, spi_sclk last edge to spi_cs[x] inactive    | PHA = 0 | $-4 + A^{(2)}$    |     | ns   |
|                    |                           |                                                         | PHA = 1 | $-4 + B^{(3)}$    |     | ns   |

(1) P = SPICLK period in ns.

(2) When P = 20.8 ns, A = (TCS + 1) \* TSPICLKREF, where TCS is a bit field of the SPI\_CH(i)CONF register. When P > 20.8 ns, A = (TCS + 0.5) \* Fratio \* TSPICLKREF, where TCS is a bit field of the SPI\_CH(i)CONF register.

(3) B = (TCS + .5) \* TSPICLKREF, where TCS is a bit field of the SPI\_CH(i)CONF register and Fratio = Even >= 2.

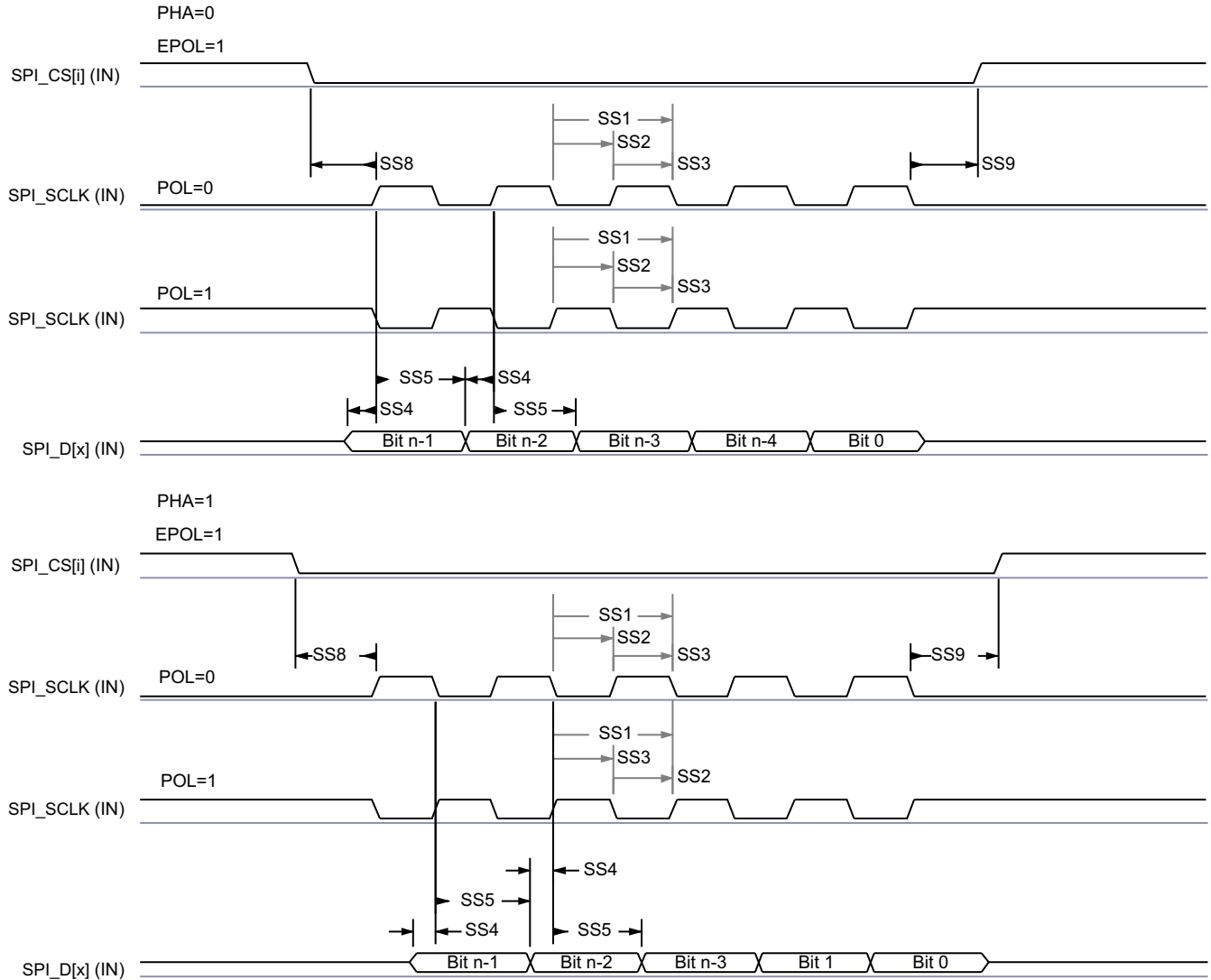


SPRSP08\_TIMING\_McSPI\_01

**Figure 6-41. SPI Controller Mode Transmit Timing****6.11.5.11.4 SPI Peripheral Mode Timing Requirements**

| NO. | PARAMETER                    | DESCRIPTION                                            | MIN                   | MAX | UNIT |
|-----|------------------------------|--------------------------------------------------------|-----------------------|-----|------|
| SS1 | $t_c(\text{SPICLK})$         | Cycle time, spi_sclk                                   | 40                    |     | ns   |
| SS2 | $t_w(\text{SPICLK})$         | Typical Pulse duration, spi_sclk low                   | $0.45 \times P^{(1)}$ |     | ns   |
| SS3 | $t_w(\text{SPICLK})$         | Typical Pulse duration, spi_sclk high                  | $0.45 \times P^{(1)}$ |     | ns   |
| SS4 | $t_{su}(\text{SIMO-SPICLK})$ | Setup time, spi_d[x] valid before spi_sclk active edge | 5                     |     | ns   |
| SS5 | $t_h(\text{SPICLK-SIMO})$    | Hold time, spi_d[x] valid after spi_sclk active edge   | 5                     |     | ns   |
| SS8 | $t_{su}(\text{CS-SPICLK})$   | Setup time, spi_cs[x] valid before spi_sclk first edge | 5                     |     | ns   |
| SS9 | $t_h(\text{SPICLK-CS})$      | Hold time, spi_cs[x] valid after spi_sclk last edge    | 5                     |     | ns   |

(1) P = SPICLK period.

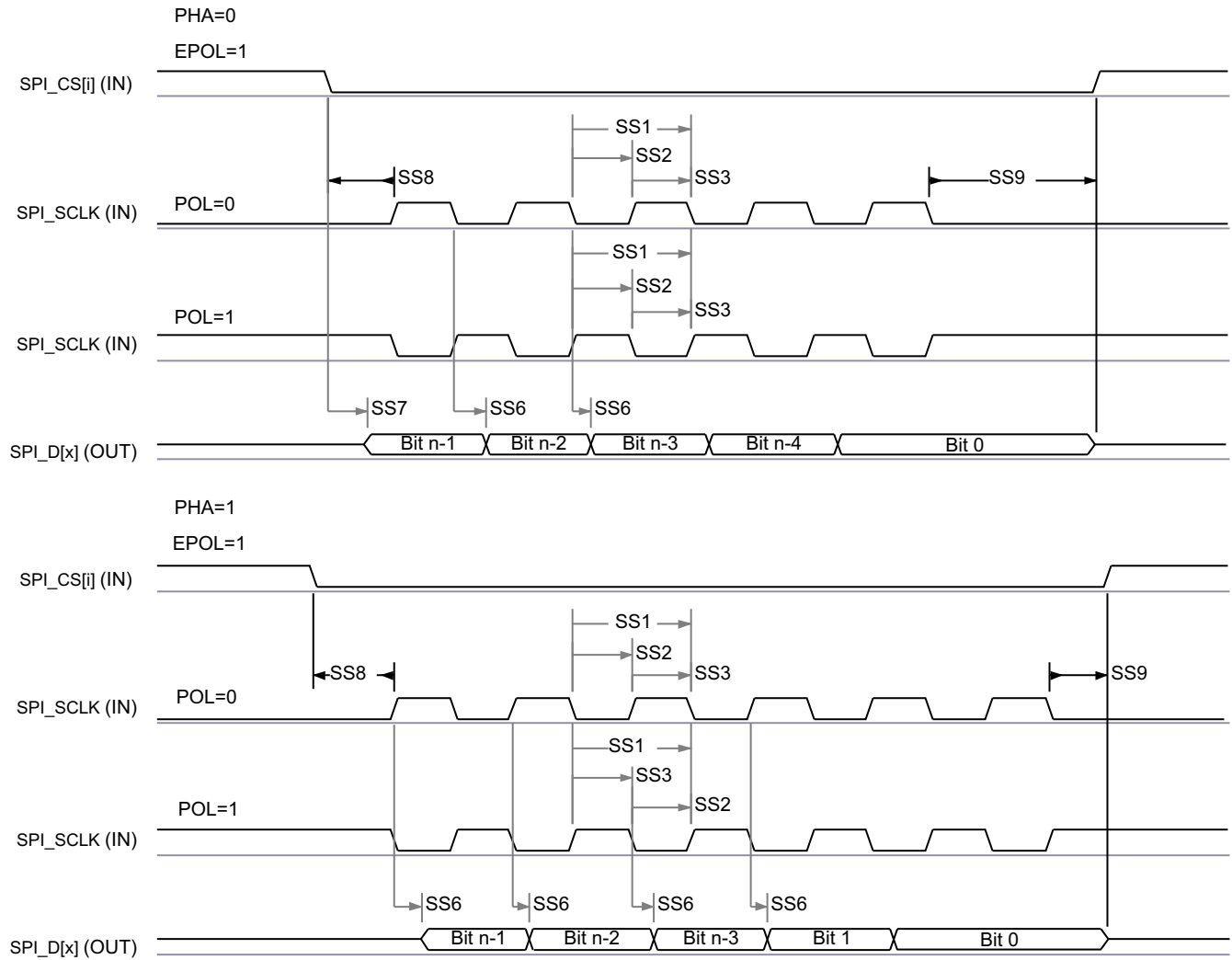


SPRSP08\_TIMING\_McSPI\_04

**Figure 6-42. SPI Peripheral Mode Receive Timing**

#### 6.11.5.11.5 SPI Peripheral Mode Switching Characteristics

| NO.                | PARAMETER            | DESCRIPTION                                                | MIN   | MAX   | UNIT |
|--------------------|----------------------|------------------------------------------------------------|-------|-------|------|
| <b>Normal Mode</b> |                      |                                                            |       |       |      |
| SS6                | $t_{d(SPICLK-SOMI)}$ | Delay time, spi_sclk active edge to mcspi_somi transition  | 2     | 17.12 | ns   |
| SS7                | $t_{sk(CS-SOMI)}$    | Delay time, spi_cs[x] active edge to mcspi_somi transition | 20.95 |       | ns   |



SPRSP08\_TIMING\_McSPI\_03

**Figure 6-43. SPI Peripheral Mode Transmit Timing**

### 6.11.5.12 Multi-Media Card/Secure Digital (MMCSD)

The MMCSD Host Controller provides an interface to embedded Multi-Media Card (MMC) and Secure Digital (SD) devices. The MMCSD Host Controller deals with MMC/SD protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more details about MMCSD interfaces, see the corresponding MMC subsection within *Signal Descriptions* and *Detailed Description* sections.

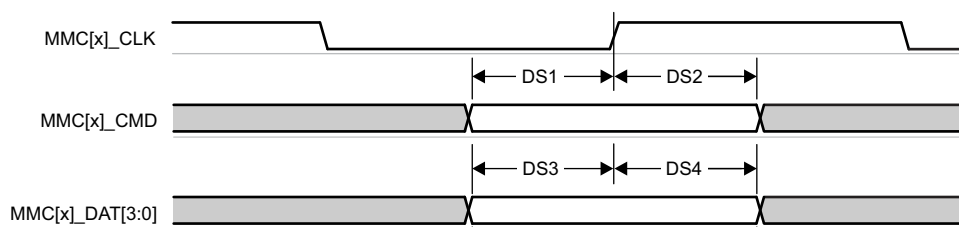
For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

#### 6.11.5.12.1 MMC Timing Conditions

| PARAMETER         |                         | MODE          | MIN  | MAX  | UNIT |
|-------------------|-------------------------|---------------|------|------|------|
| INPUT CONDITIONS  |                         |               |      |      |      |
| SR <sub>I</sub>   | Input Slew Rate         | Default Speed | 0.69 | 2.06 | V/ns |
|                   |                         | High Speed    | 0.69 | 2.06 | V/ns |
| OUTPUT CONDITIONS |                         |               |      |      |      |
| C <sub>L</sub>    | Output Load Capacitance | Default Speed | 1    | 10   | pF   |
|                   |                         | High Speed    | 1    | 10   | pF   |

#### 6.11.5.12.2 MMC Timing Requirements - SD Card Default Speed Mode

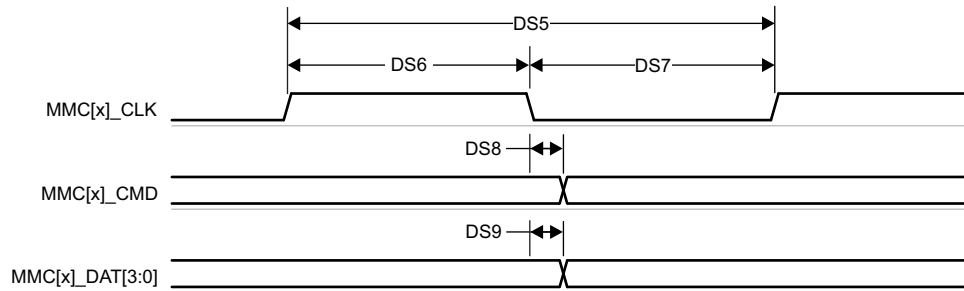
| NO. | PARAMETER                  | DESCRIPTION                                               | MIN   | MAX | UNIT |
|-----|----------------------------|-----------------------------------------------------------|-------|-----|------|
| DS1 | t <sub>su(cmdV-clkH)</sub> | Setup time, MMC_CMD valid before MMC_CLK rising edge      | 2.15  |     | ns   |
| DS2 | t <sub>h(clkH-cmdV)</sub>  | Hold time, MMC_CMD valid after MMC_CLK rising edge        | 19.67 |     | ns   |
| DS3 | t <sub>su(dV-clkH)</sub>   | Setup time, MMC_DAT[3:0] valid before MMC_CLK rising edge | 2.15  |     | ns   |
| DS4 | t <sub>h(clkH-dV)</sub>    | Hold time, MMC_DAT[3:0] valid after MMC_CLK rising edge   | 19.67 |     | ns   |



**Figure 6-44. MMC – Default Speed – Receive Mode**

#### 6.11.5.12.3 MMC Switching Characteristics - SD Card Default Speed Mode

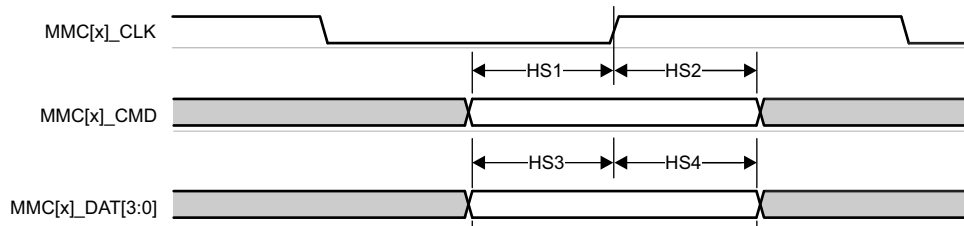
| NO. | PARAMETER                 | DESCRIPTION                                                 | MIN   | MAX  | UNIT |
|-----|---------------------------|-------------------------------------------------------------|-------|------|------|
|     | f <sub>op(clk)</sub>      | Operating frequency, MMC_CLK                                |       | 25   | MHz  |
| DS5 | t <sub>c(clk)</sub>       | Operating period, MMC_CLK                                   |       | 40   | ns   |
| DS6 | t <sub>w(clkH)</sub>      | Pulse duration, MMC_CLK high                                | 18.7  |      | ns   |
| DS7 | t <sub>w(clkL)</sub>      | Pulse duration, MMC_CLK low                                 | 18.7  |      | ns   |
| DS8 | t <sub>d(clkL-cmdV)</sub> | Delay time, MMC_CLK falling edge to MMC_CMD transition      | -14.1 | 14.1 | ns   |
| DS9 | t <sub>d(clkL-dV)</sub>   | Delay time, MMC_CLK falling edge to MMC_DAT[3:0] transition | -14.1 | 14.1 | ns   |



**Figure 6-45. MMC – Default Speed – Transmit Mode**

#### 6.11.5.12.4 MMC Timing Requirements - SD Card High Speed Mode

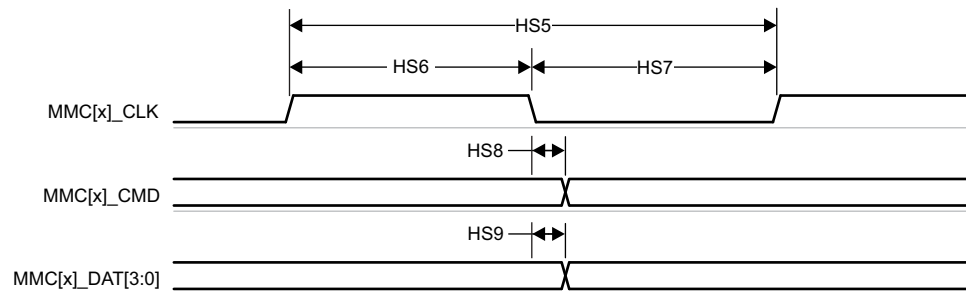
| NO. | PARAMETER           | DESCRIPTION                                               | MIN  | MAX | UNIT |
|-----|---------------------|-----------------------------------------------------------|------|-----|------|
| HS1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC_CMD valid before MMC_CLK rising edge      | 2.15 |     | ns   |
| HS2 | $t_{h(clkH-cmdV)}$  | Hold time, MMC_CMD valid after MMC_CLK rising edge        | 2.67 |     | ns   |
| HS3 | $t_{su(dV-clkH)}$   | Setup time, MMC_DAT[3:0] valid before MMC_CLK rising edge | 2.15 |     | ns   |
| HS4 | $t_{h(clkH-dV)}$    | Hold time, MMC_DAT[3:0] valid after MMC_CLK rising edge   | 2.67 |     | ns   |



**Figure 6-46. MMC – High Speed – Receive Mode**

#### 6.11.5.12.5 MMC Switching Characteristics - SD Card High Speed Mode

| NO. | PARAMETER          | DESCRIPTION                                                 | MIN   | MAX  | UNIT |
|-----|--------------------|-------------------------------------------------------------|-------|------|------|
|     | $f_{op(clk)}$      | Operating frequency, MMC_CLK                                |       | 50   | MHz  |
| HS5 | $t_{c(clk)}$       | Operating period, MMC_CLK                                   |       | 20   | ns   |
| HS6 | $t_{w(clkH)}$      | Pulse duration, MMC_CLK high                                | 9.2   |      | ns   |
| HS7 | $t_{w(clkL)}$      | Pulse duration, MMC_CLK low                                 | 9.2   |      | ns   |
| HS8 | $t_{d(clkL-cmdV)}$ | Delay time, MMC_CLK falling edge to MMC_CMD transition      | -7.35 | 3.35 | ns   |
| HS9 | $t_{d(clkL-dV)}$   | Delay time, MMC_CLK falling edge to MMC_DAT[3:0] transition | -7.35 | 3.35 | ns   |



**Figure 6-47. MMC – High Speed – Transmit Mode**

### 6.11.5.13 Quad Serial Peripheral Interface (QSPI)

For more details about features and additional description information on the device Quad Serial Peripheral Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see *Quad Serial Peripheral Interface (QSPI)* section in the device TRM.

#### 6.11.5.13.1 QSPI Timing Conditions

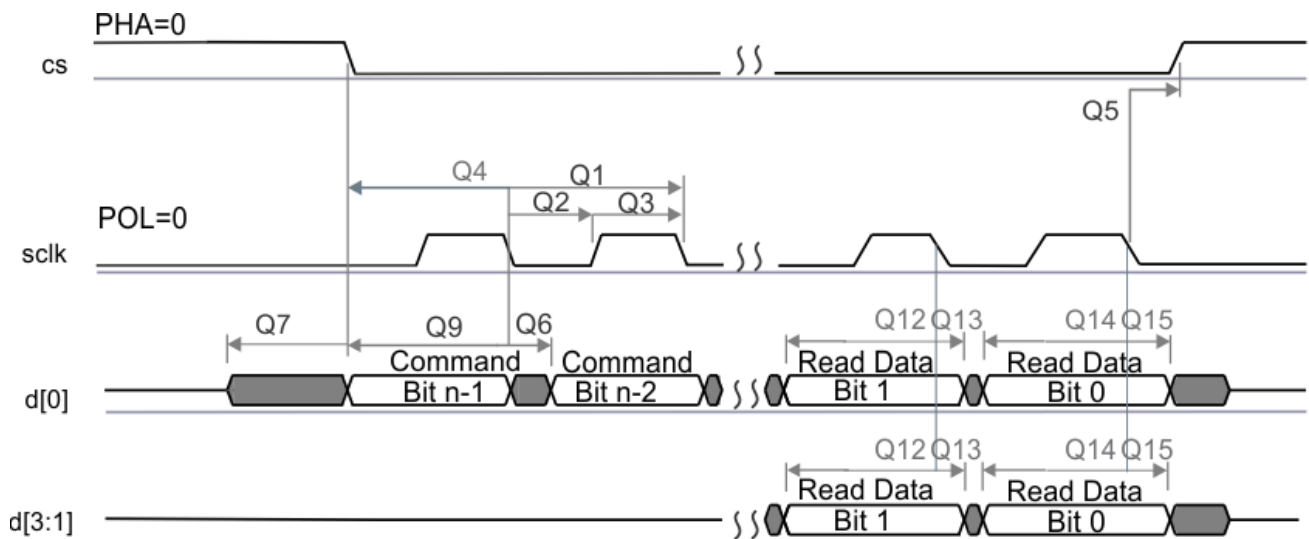
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 2   | 8   | pF   |

#### 6.11.5.13.2 QSPI Timing Requirements

(1) (2)

| NO. | PARAMETER                 | DESCRIPTION                                        | MODE                                 | MIN  | MAX | UNIT |
|-----|---------------------------|----------------------------------------------------|--------------------------------------|------|-----|------|
| Q12 | t <sub>su</sub> (D-RTCLK) | Setup time, d[3:0] valid before falling rtclk edge | Manual IO Timing Modes, Clock Mode 0 | 2.69 |     | ns   |
|     | t <sub>su</sub> (D-SCLK)  | Setup time, d[3:0] valid before falling sclk edge  | Manual IO Timing Modes, Clock Mode 3 | 5.7  |     | ns   |
| Q13 | t <sub>h</sub> (RTCLK-D)  | Hold time, d[3:0] valid after falling rtclk edge   | Manual IO Timing Modes, Clock Mode 0 | -0.1 |     | ns   |
|     | t <sub>h</sub> (SCLK-D)   | Hold time, d[3:0] valid after falling sclk edge    | Manual IO Timing Modes, Clock Mode 3 | 0.1  |     | ns   |

- (1) Clock Modes 1 and 2 are not supported.  
 (2) The device captures data on the falling clock edge in Clock Mode 0 and 3, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Modes 0 and 3.



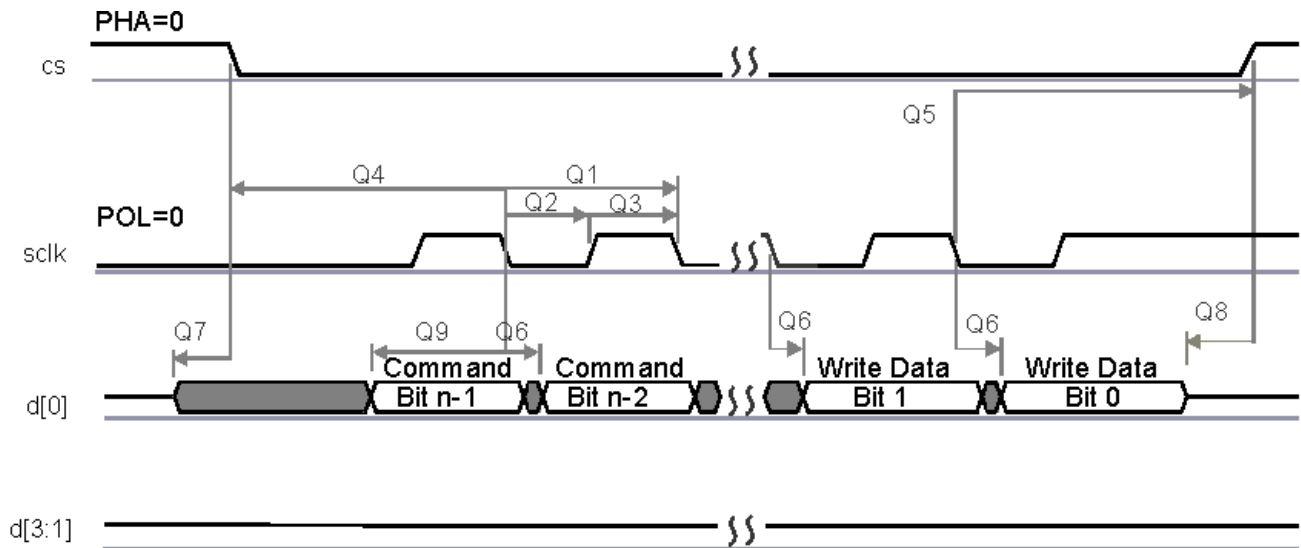
SPRS85v TIMING QSPI1 02

**Figure 6-48. QSPI Timing Requirements**

### 6.11.5.13.3 QSPI Switching Characteristics

| NO. | PARAMETER          | DESCRIPTION                                                  | MODE                                 | MIN                           | MAX                           | UNIT |
|-----|--------------------|--------------------------------------------------------------|--------------------------------------|-------------------------------|-------------------------------|------|
| Q1  | $t_{c(SCLK)}$      | Cycle time, sclk                                             | Manual IO Timing Modes, Clock Mode 0 | 10.41                         |                               | ns   |
|     |                    |                                                              | Manual IO Timing Modes, Clock Mode 3 | 13.02                         |                               | ns   |
| Q2  | $t_{w(SCLKL)}$     | Pulse duration, sclk low                                     | All                                  | $Y^{(4)} \times P^{(1)} - 1$  |                               | ns   |
| Q3  | $t_{w(SCLKH)}$     | Pulse duration, sclk high                                    | All                                  | $Y^{(4)} \times P^{(1)} - 1$  |                               | ns   |
| Q4  | $t_{d(CS-SCLK)}$   | Delay time, sclk falling edge to cs active edge, CS1:0       | Manual IO Timing Modes               | $-M^{(2)} \times P^{(1)} - 2$ | $-M^{(2)} \times P^{(1)} + 2$ | ns   |
| Q5  | $t_{d(SCLK-CS)}$   | Delay time, sclk falling edge to cs inactive edge, CS1:0     | Manual IO Timing Modes               | $N^{(3)} \times P^{(1)} - 2$  | $N^{(3)} \times P^{(1)} + 2$  | ns   |
| Q6  | $t_{d(SCLK-D0)}$   | Delay time, sclk falling edge to d[0] transition             | Manual IO Timing Modes               | -1                            | 2                             | ns   |
| Q7  | $t_{ena(CS-D0LZ)}$ | Enable time, cs active edge to d[0] drive (lo-z)             | All                                  | $-P^{(1)} - 2$                | $-P^{(1)} + 2$                | ns   |
| Q8  | $t_{dis(CS-D0Z)}$  | Disable time, cs active edge to d[0] tri-stated (hi-z)       | All                                  | $-P^{(1)} - 2$                | $-P^{(1)} + 2$                | ns   |
| Q9  | $t_{d(SCLK-D0)}$   | Delay time, sclk first falling edge to first d[0] transition | Manual IO Timing Modes, PHA=0 Only   | $-P^{(1)} - 1$                | $-P^{(1)} + 2$                | ns   |

- (1) P = SCLK period  
(2) M=QSPI\_SPI\_DC\_REG.DDx + 1 when Clock Mode 0. M=QSPI\_SPI\_DC\_REG.DDx when Clock Mode 3.  
(3) N = 2 when Clock Mode 0. N = 3 when Clock Mode 3.  
(4) Y = 0.5 when DCLK\_DIV is 0 or ODD  
Y = (DCLK\_DIV/2)/(DCLK\_DIV+1) when DCLK\_DIV is EVEN



SPRSP74E\_TIMING\_QSPI1.D4

Figure 6-49. QSPI Switching Characteristics

#### 6.11.5.14 Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS)

The device has integrated a single Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS0). The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores in the device.

For more details about features and additional description information on the device PRU-ICSS, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

##### Note

The PRU-ICSS0 supports an internal wrapper multiplexing that expands the device top-level multiplexing.

#### 6.11.5.14.1 PRU-ICSS Programmable Real-Time Unit (PRU)

##### Note

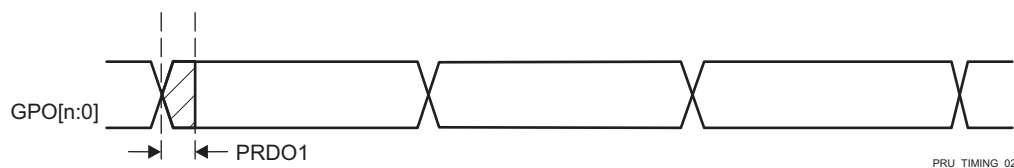
The PRU-ICSS PRU signals have different functionality depending on the mode of operation. The signal naming in this section matches the naming used in the *PRU Module Interface* section in the device TRM.

#### 6.11.5.14.1.1 PRU-ICSS PRU Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 1   | 3   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 2   | 30  | pF   |

#### 6.11.5.14.1.2 PRU-ICSS PRU Switching Characteristics - Direct Output Mode

| NO.   | PARAMETER                 | DESCRIPTION             | MIN | MAX | UNIT |
|-------|---------------------------|-------------------------|-----|-----|------|
| PRDO1 | t <sub>sk</sub> (PRU_GPO) | PRU_GPO (data out) skew |     | 3   | ns   |



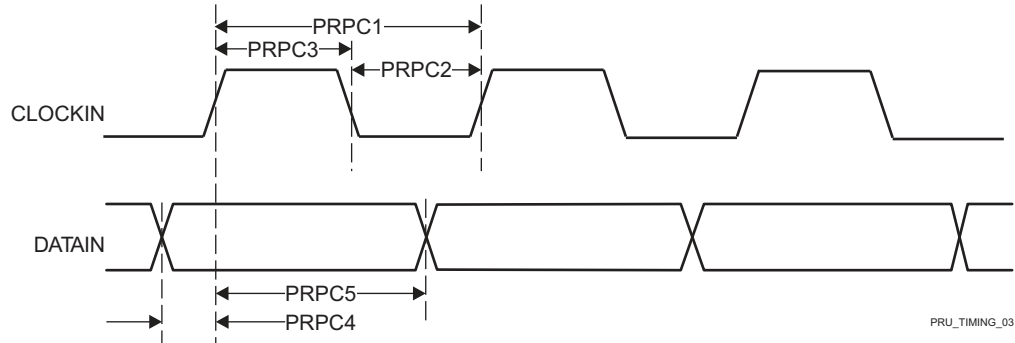
A. n in GPO[n:0] = 19.

**Figure 6-50. PRU-ICSS PRU Direct Output Timing**

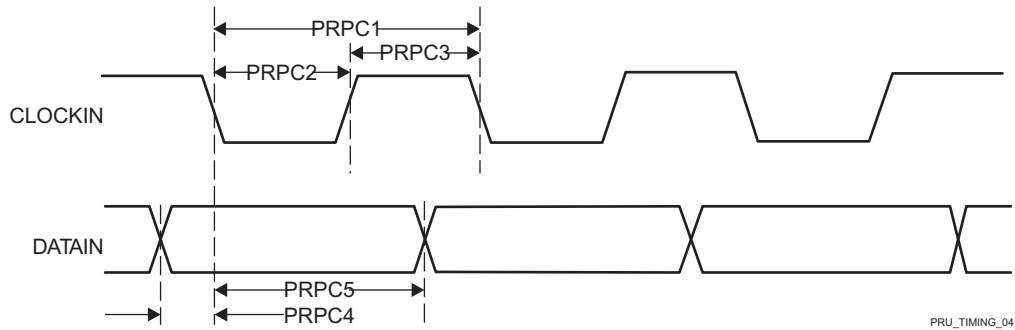
#### 6.11.5.14.1.3 PRU-ICSS PRU Timing Requirements - Parallel Capture Mode

| NO.   | PARAMETER                            | DESCRIPTION                                               | MIN | MAX | UNIT |
|-------|--------------------------------------|-----------------------------------------------------------|-----|-----|------|
| PRPC1 | t <sub>c</sub> (PRU_CLOCK)           | Cycle time, PRU_CLOCK                                     | 20  |     | ns   |
| PRPC2 | t <sub>w</sub> (PRU_CLOCKL)          | Pulse duration, PRU_CLOCK Low                             | 10  |     | ns   |
| PRPC3 | t <sub>w</sub> (PRU_CLOCKH)          | Pulse duration, PRU_CLOCK High                            | 10  |     | ns   |
| PRPC4 | t <sub>su</sub> (PRU_DATAIN-PRU_CLK) | Setup time, PRU_DATAIN valid before PRU_CLOCK active edge | 4   |     | ns   |

| NO.   | PARAMETER                               | DESCRIPTION                                             | MIN | MAX | UNIT |
|-------|-----------------------------------------|---------------------------------------------------------|-----|-----|------|
| PRPC5 | $t_{th}(\text{PRU\_CLOCK-PRU\_DATAIN})$ | Hold time, PRU_DATAIN valid after PRU_CLOCK active edge | 0   |     | ns   |



**Figure 6-51. PRU-ICSS PRU Parallel Capture Timing Requirements – Rising Edge Mode**

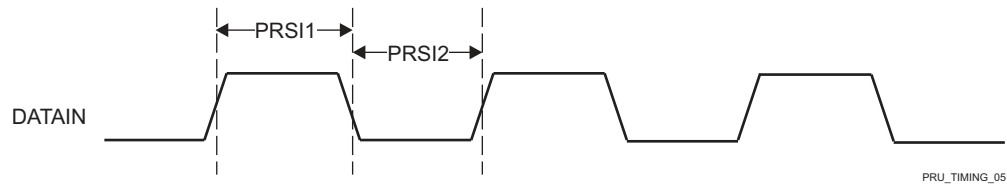


**Figure 6-52. PRU-ICSS PRU Parallel Capture Timing Requirements – Falling Edge Mode**

#### 6.11.5.14.1.4 PRU-ICSS PRU Timing Requirements - Shift In Mode

| NO.   | PARAMETER                  | DESCRIPTION                     | MIN            | MAX | UNIT |
|-------|----------------------------|---------------------------------|----------------|-----|------|
| PRSI1 | $t_w(\text{PRU\_DATAINH})$ | Pulse duration, PRU_DATAIN High | $2 + 2P^{(1)}$ |     | ns   |
| PRSI2 | $t_w(\text{PRU\_DATAINL})$ | Pulse duration, PRU_DATAIN Low  | $2 + 2P^{(1)}$ |     | ns   |

(1) P = Internal shift in clock period, defined by PRU\_GPI\_DIV0 and PRU0\_GPI\_DIV1 bit fields in the GPCFGn register.



**Figure 6-53. PRU-ICSS PRU Shift In Timing**

#### 6.11.5.14.1.5 PRU-ICSS PRU Switching Characteristics - Shift Out Mode

| NO.    | PARAMETER                    | DESCRIPTION                       | MIN                                          | MAX | UNIT |
|--------|------------------------------|-----------------------------------|----------------------------------------------|-----|------|
| PRSO1  | $t_c(\text{PRU\_CLOCKOUT})$  | Cycle time, PRU_CLOCKOUT          | 10                                           |     | ns   |
| PRSO2L | $t_w(\text{PRU\_CLOCKOUTL})$ | Pulse duration, PRU_CLOCKOUT Low  | $-0.3 + 0.475 \times P^{(1)} \times Z^{(2)}$ |     | ns   |
| PRSO2H | $t_w(\text{PRU\_CLOCKOUTH})$ | Pulse duration, PRU_CLOCKOUT High | $-0.3 + 0.475 \times P^{(1)} \times Y^{(3)}$ |     | ns   |

| NO.   | PARAMETER                                | DESCRIPTION                                   | MIN | MAX | UNIT |
|-------|------------------------------------------|-----------------------------------------------|-----|-----|------|
| PRSO3 | $t_d(\text{PRU\_CLOCKOUT-PRU\_DATAOUT})$ | Delay time, PRU_CLOCKOUT to PRU_DATAOUT Valid | 0   | 3   | ns   |

- (1) P = Software programmable shift out clock period, defined by PRU0\_GP0\_Div0 and PRU0\_GPO\_DIV1 bit fields in the GPCFGn register.
- (2) The Z parameter is defined as follows:  
 If PRU0\_GPI\_DIV0 and PRU0\_GPI\_DIV1 are INTEGERS -or- if PRU0\_GPI\_DIV0 is a NON-INTEGER and PRU0\_GPI\_DIV1 is an EVEN INTEGER then,  
 Z equals  $(\text{PRU0\_GPI\_DIV0} * \text{PRU0\_GPI\_DIV1})$ .  
 If PRU0\_GPI\_DIV0 is a NON-INTEGER and PRU0\_GPI\_DIV1 is an ODD INTEGER then,  
 Z equals  $(\text{PRU0\_GPI\_DIV0} * \text{PRU0\_GPI\_DIV1} + 0.5)$ .  
 If PRU0\_GPI\_DIV0 is an INTEGER and PRU0\_GPI\_DIV1 is a NON-INTEGER then,  
 Z equals  $(\text{PRU0\_GPI\_DIV0} * \text{PRU0\_GPI\_DIV1} + 0.5 * \text{PRU0\_GPI\_DIV0})$ .  
 If PRU0\_GPI\_DIV0 and PRU0\_GPI\_DIV1 are NON-INTEGERS then,  
 Z equals  $(\text{PRU0\_GPI\_DIV0} * \text{PRU0\_GPI\_DIV1} + 0.25 * \text{PRU0\_GPI\_DIV0})$ .
- (3) The Y parameter is defined as follows:  
 If PRU0\_GPI\_DIV0 and PRU0\_GPI\_DIV1 are INTEGERS -or- if PRU0\_GPI\_DIV0 is a NON-INTEGER and PRU0\_GPI\_DIV1 is an EVEN INTEGER then,  
 Y equals  $(\text{PRU0\_GPI\_DIV0} * \text{PRU0\_GPI\_DIV1})$ .  
 If PRU0\_GPI\_DIV0 is a NON-INTEGER and PRU0\_GPI\_DIV1 is an ODD INTEGER then,  
 Y equals  $(\text{PRU0\_GPI\_DIV0} * \text{PRU0\_GPI\_DIV1} - 0.5)$ .  
 If PRU0\_GPI\_DIV0 is an INTEGER and PRU0\_GPI\_DIV1 is a NON-INTEGER then,  
 Y equals  $(\text{PRU0\_GPI\_DIV0} * \text{PRU0\_GPI\_DIV1} - 0.5 * \text{PRU0\_GPI\_DIV0})$ .  
 If PRU0\_GPI\_DIV0 and PRU0\_GPI\_DIV1 are NON-INTEGERS then,  
 Y1 equals  $(\text{PRU0\_GPI\_DIV0} * \text{PRU0\_GPI\_DIV1} - 0.25 * \text{PRU0\_GPI\_DIV0})$  and  
 Y2 equals  $(\text{PRU0\_GPI\_DIV0} * \text{PRU0\_GPI\_DIV1} + 0.25 * \text{PRU0\_GPI\_DIV0})$ , where Y1 is the first high pulse and Y2 is the second high pulse.

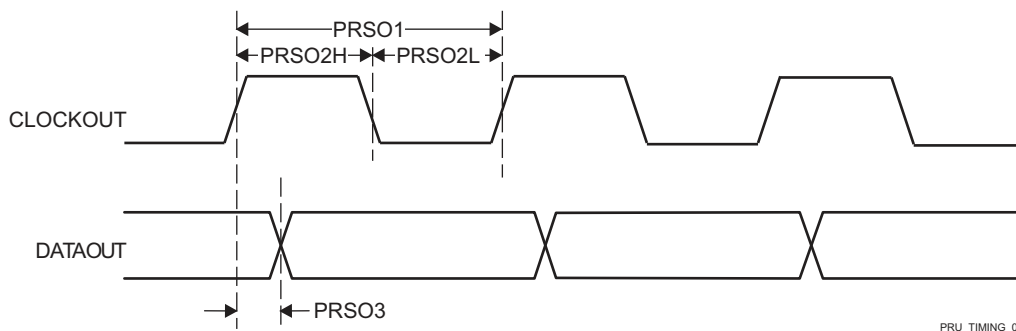


Figure 6-54. PRU-ICSS PRU Shift Out Timing

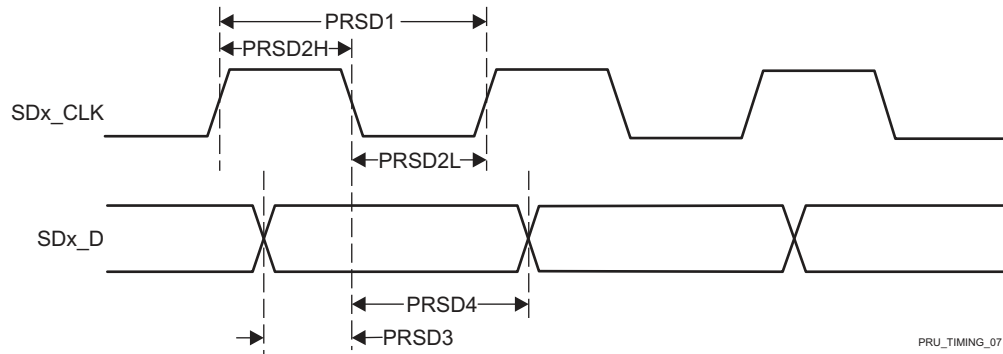
#### 6.11.5.14.2 PRU-ICSS PRU Sigma Delta and Peripheral Interface

##### 6.11.5.14.2.1 PRU-ICSS PRU Sigma Delta and Peripheral Interface Timing Conditions

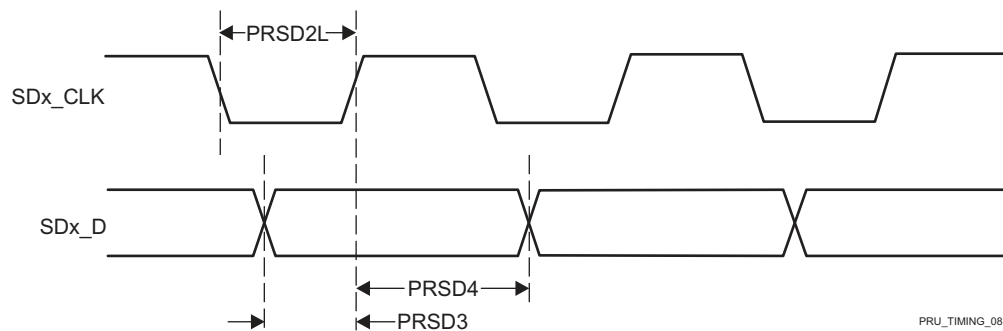
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 1   | 3   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 2   | 18  | pF   |

##### 6.11.5.14.2.2 PRU-ICSS PRU Timing Requirements - Sigma Delta Mode

| NO.    | PARAMETER                    | DESCRIPTION                                      | MIN | MAX | UNIT |
|--------|------------------------------|--------------------------------------------------|-----|-----|------|
| PRSD1  | t <sub>G</sub> (SD_CLK)      | Cycle time, SD_CLK                               | 40  |     | ns   |
| PRSD2L | t <sub>w</sub> (SD_CLKL)     | Pulse duration, SD_CLK Low                       | 20  |     | ns   |
| PRSD2H | t <sub>w</sub> (SD_CLKH)     | Pulse duration, SD_CLK High                      | 20  |     | ns   |
| PRSD3  | t <sub>su</sub> (SD_D-SDCLK) | Setup time, SD_D valid before SD_CLK active edge | 10  |     | ns   |
| PRSD4  | t <sub>su</sub> (SDCLK-SD_D) | Hold time, SD_D valid after SD_CLK active edge   | 5   |     | ns   |



**Figure 6-55. PRU-ICSS PRU SD\_CLK Falling Active Edge**



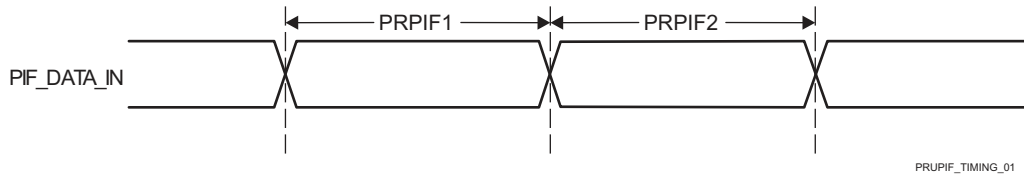
**Figure 6-56. PRU-ICSS PRU SD\_CLK Rising Active Edge**

##### 6.11.5.14.2.3 PRU-ICSS PRU Timing Requirements - Peripheral Interface Mode

| NO.    | PARAMETER                     | DESCRIPTION                      | MIN                                   | MAX | UNIT |
|--------|-------------------------------|----------------------------------|---------------------------------------|-----|------|
| PRPIF1 | t <sub>w</sub> (PIF_DATA_INH) | Pulse duration, PIF_DATA_IN High | $2 + 0.475 \times (4 \times P^{(1)})$ |     | ns   |

| NO.    | PARAMETER               | DESCRIPTION                     | MIN                                   | MAX | UNIT |
|--------|-------------------------|---------------------------------|---------------------------------------|-----|------|
| PRPIF2 | $t_{w(PIF\_DATA\_INL)}$ | Pulse duration, PIF_DATA_IN Low | $2 + 0.475 \times (4 \times P^{(1)})$ |     | ns   |

(1)  $P = 1x$  (or TX) clock period, defined by TX\_DIV\_FACTOR and TX\_DIV\_FACTOR\_FRAC in the CFG\_ED\_P<n>\_TXCFG register.

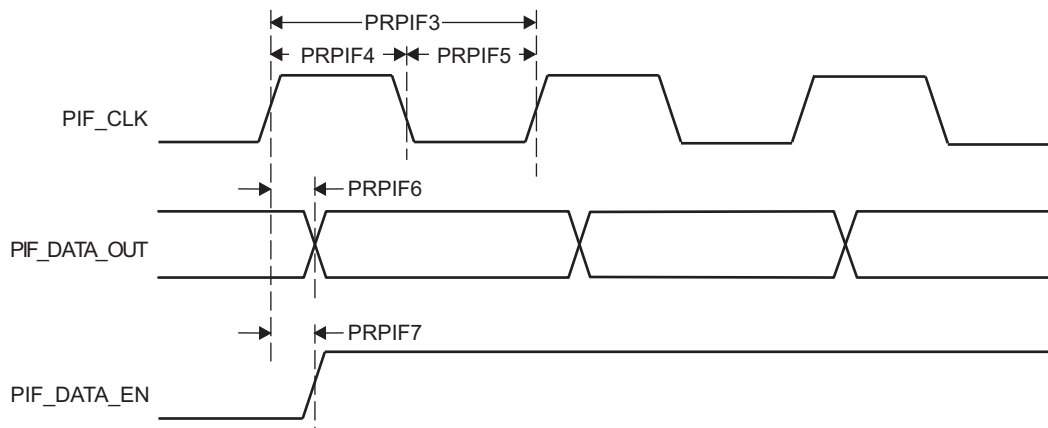


**Figure 6-57. PRU-ICSS PRU Peripheral Interface Timing Requirements**

#### 6.11.5.14.2 PRU-ICSS PRU Switching Characteristics - Peripheral Interface Mode

| NO.    | PARAMETER                        | DESCRIPTION                              | MIN            | MAX | UNIT |
|--------|----------------------------------|------------------------------------------|----------------|-----|------|
| PRPIF3 | $t_{c(PIF\_CLK)}$                | Cycle time, PIF_CLK                      | 30             |     | ns   |
| PRPIF4 | $t_{w(PIF\_CLKH)}$               | Pulse duration, PIF_CLK High             | $0.475P^{(1)}$ |     | ns   |
| PRPIF5 | $t_{w(PIF\_CLKL)}$               | Pulse duration, PIF_CLK Low              | $0.475P^{(1)}$ |     | ns   |
| PRPIF6 | $t_{d(PIF\_CLK-PIF\_DATA\_OUT)}$ | Delay time, PIF_CLK fall to PIF_DATA_OUT | -5             | 5   | ns   |
| PRPIF7 | $t_{d(PIF\_CLK-PIF\_DATA\_EN)}$  | Delay time, PIF_CLK fall to PIF_DATA_EN  | -5             | 5   | ns   |

(1)  $P = 1x$  (or TX) clock period, defined by TX\_DIV\_FACTOR and TX\_DIV\_FACTOR\_FRAC in the CFG\_ED\_P<n>\_TXCFG register.



**Figure 6-58. PRU-ICSS PRU Peripheral Interface Switching Characteristics**

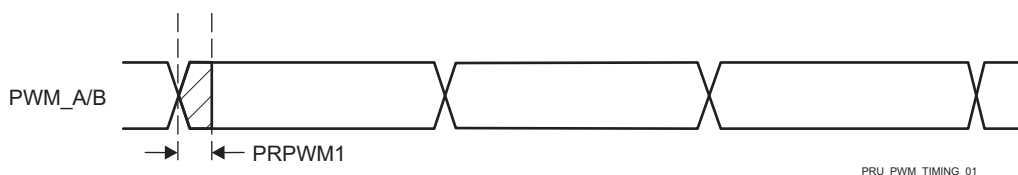
### 6.11.5.14.3 PRU-ICSS Pulse Width Modulation (PWM)

#### 6.11.5.14.3.1 PRU-ICSS PWM Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 2   | 7   | pF   |

#### 6.11.5.14.3.2 PRU-ICSS PWM Switching Characteristics

| NO.    | PARAMETER                 | DESCRIPTION  | MIN | MAX | UNIT |
|--------|---------------------------|--------------|-----|-----|------|
| PRPWM1 | t <sub>sk</sub> (PWM_A/B) | PWM_A/B skew |     | 0   | ns   |



**Figure 6-59. PRU-ICSS PWM Timing**

#### 6.11.5.14.4 PRU-ICSS Industrial Ethernet Peripheral (IEP)

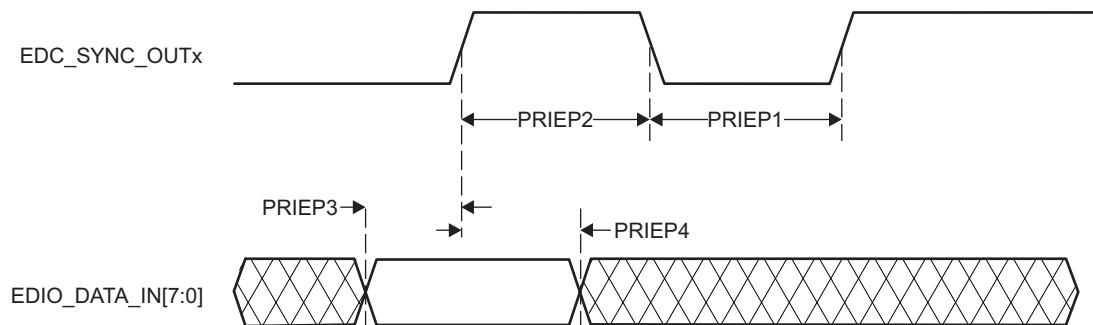
##### 6.11.5.14.4.1 PRU-ICSS IEP Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 1   | 3   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 1   | 7   | pF   |

##### 6.11.5.14.4.2 PRU-ICSS IEP Timing Requirements - Input Validated with SYNCx

| NO.    | PARAMETER                                | DESCRIPTION                                                     | MIN                     | MAX | UNIT |
|--------|------------------------------------------|-----------------------------------------------------------------|-------------------------|-----|------|
| PRIEP1 | $t_{w(EDC\_SYNCx\_OUTL)}$                | Pulse duration, EDC_SYNCx_OUT Low                               | -2 + 20P <sup>(1)</sup> |     | ns   |
| PRIEP2 | $t_{w(EDC\_SYNCx\_OUTH)}$                | Pulse duration, EDC_SYNCx_OUT High                              | -2 + 20P <sup>(1)</sup> |     | ns   |
| PRIEP3 | $t_{su}(EDIO\_DATA\_IN-EDC\_SYNCx\_OUT)$ | Setup time, EDIO_DATA_IN valid before EDC_SYNCx_OUT active edge | 20                      |     | ns   |
| PRIEP4 | $t_h(EDC\_SYNCx\_OUT-EDIO\_DATA\_IN)$    | Hold time, EDIO_DATA_IN valid after EDC_SYNCx_OUT active edge   | 20                      |     | ns   |

(1) P = PRU-ICSS IEP clock source period.



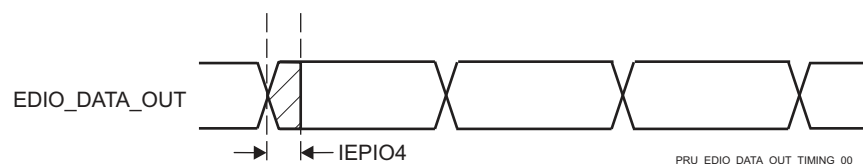
PRU\_IEP\_TIMING\_01

**Figure 6-60. PRU-ICSS IEP SYNC Timing Requirements**

##### 6.11.5.14.4.3 PRU-ICSS IEP Timing Requirements - Digital IOs

| NO.    | PARAMETER                             | DESCRIPTION                                | MIN                     | MAX                | UNIT |
|--------|---------------------------------------|--------------------------------------------|-------------------------|--------------------|------|
| IEPIO1 | $t_{w(EDIO\_OUTVALIDL)}$              | Pulse duration, EDIO_OUTVALID Low          | -2 + 14P <sup>(1)</sup> |                    | ns   |
| IEPIO2 | $t_{w(EDIO\_OUTVALIDH)}$              | Pulse duration, EDIO_OUTVALID High         | -2 + 32P <sup>(1)</sup> |                    | ns   |
| IEPIO3 | $t_d(EDIO\_OUTVALID-EDIO\_DATA\_OUT)$ | Delay time, EDIO_OUTVALID to EDIO_DATA_OUT | 0                       | 18P <sup>(1)</sup> | ns   |
| IEPIO4 | $t_{sk}(EDIO\_DATA\_OUT)$             | EDIO_DATA_OUT skew                         | 6                       |                    | ns   |

(1) P = PRU-ICSS IEP clock source period.



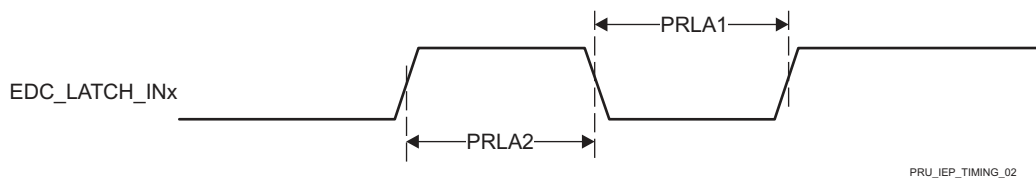
PRU\_EDIO\_DATA\_OUT\_TIMING\_00

**Figure 6-61. PRU-ICSS IEP Digital IOs Timing Requirements**

#### 6.11.5.14.4.4 PRU-ICSS IEP Timing Requirements - LATCHx\_IN

| NO.   | PARAMETER                 | DESCRIPTION                        | MIN            | MAX | UNIT |
|-------|---------------------------|------------------------------------|----------------|-----|------|
| PRLA1 | $t_{w(EDC\_LATCHx\_INL)}$ | Pulse duration, EDC_LATCHx_IN Low  | $2 + 3P^{(1)}$ |     | ns   |
| PRLA2 | $t_{w(EDC\_LATCHx\_INH)}$ | Pulse duration, EDC_LATCHx_IN High | $2 + 3P^{(1)}$ |     | ns   |

(1) P = PRU-ICSS IEP clock source period.



**Figure 6-62. PRU-ICSS IEP LATCH\_INx Timing Requirements**

### 6.11.5.14.5 PRU-ICSS Universal Asynchronous Receiver Transmitter (UART)

#### 6.11.5.14.5.1 PRU-ICSS UART Timing Conditions

| PARAMETER                |                         | MIN  | MAX  | UNIT |
|--------------------------|-------------------------|------|------|------|
| <b>INPUT CONDITIONS</b>  |                         |      |      |      |
| SR <sub>I</sub>          | Input Slew Rate         | 0.01 | 0.33 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |      |      |      |
| C <sub>L</sub>           | Output Load Capacitance | 1    | 30   | pF   |

#### 6.11.5.14.5.2 PRU-ICSS UART Timing Requirements

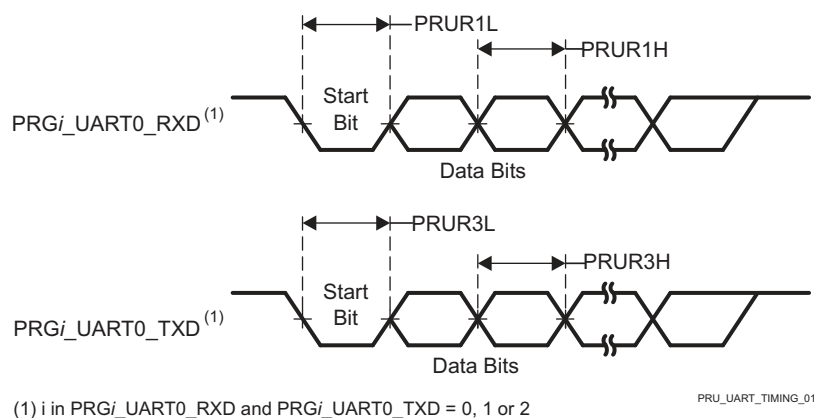
| NO.    | PARAMETER            | DESCRIPTION                                        | MIN                   | MAX | UNIT |
|--------|----------------------|----------------------------------------------------|-----------------------|-----|------|
| PRUR1H | t <sub>w</sub> (RXH) | Pulse duration, Receive start, stop, data bit High | U <sup>(1)</sup>      |     | ns   |
| PRUR1L | t <sub>w</sub> (RXL) | Pulse duration, Receive start, stop, data bit Low  | -2 + U <sup>(1)</sup> |     | ns   |

(1) U = UART baud time = 1/programmed baud rate.

#### 6.11.5.14.5.3 PRU-ICSS UART Switching Characteristics

| NO.    | PARAMETER            | DESCRIPTION                                         | MIN                   | MAX | UNIT |
|--------|----------------------|-----------------------------------------------------|-----------------------|-----|------|
| PRUR2  | f <sub>(baud)</sub>  | Maximum programmable baud rate                      | U <sup>(1)</sup>      |     | ns   |
| PRUR3H | t <sub>w</sub> (TXH) | Pulse duration, Transmit start, stop, data bit High | -2 + U <sup>(1)</sup> |     | ns   |

(1) U = UART baud time = 1/programmed baud rate.



**Figure 6-63. PRU-ICSS UART Timing Requirements and Switching Characteristics**

#### 6.11.5.14.6 PRU-ICSS Enhanced Capture Peripheral (ECAP)

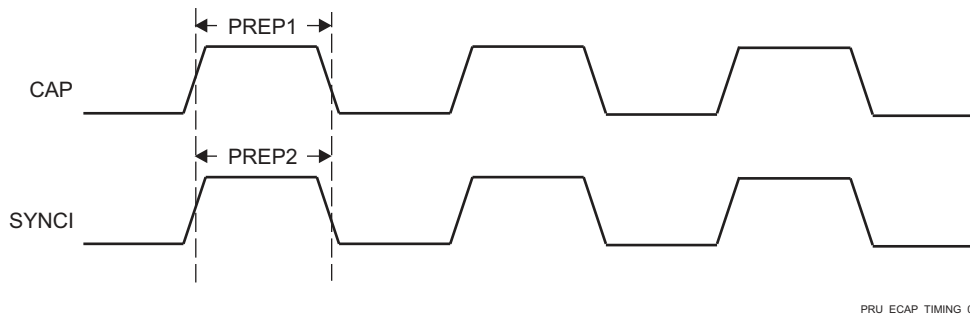
##### 6.11.5.14.6.1 PRU-ICSS ECAP Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 1   | 3   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 2   | 7   | pF   |

##### 6.11.5.14.6.2 PRU-ICSS ECAP Timing Requirements

| NO.   | PARAMETER              | DESCRIPTION                                  | MIN                   | MAX | UNIT |
|-------|------------------------|----------------------------------------------|-----------------------|-----|------|
| PREP1 | t <sub>w</sub> (CAP)   | Pulse duration, Capture input (asynchronous) | 2 + 2P <sup>(1)</sup> |     | ns   |
| PREP2 | t <sub>w</sub> (SYNCl) | Pulse duration, Sync input (asynchronous)    | 2 + 2P <sup>(1)</sup> |     | ns   |

(1) P = core\_clk period

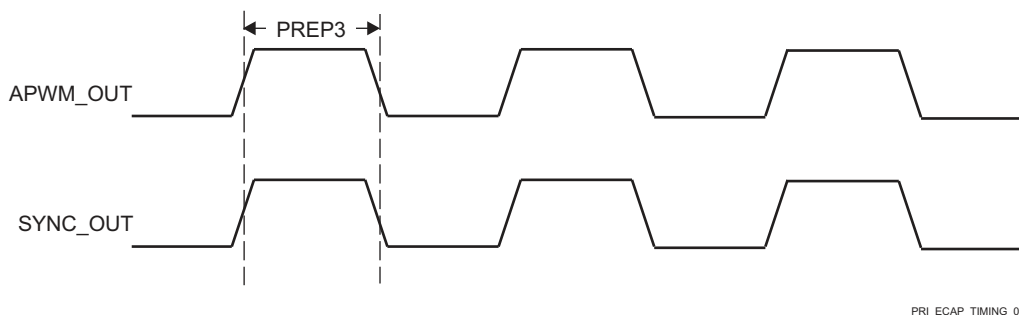


**Figure 6-64. PRU-ICSS ECAP Timing**

##### 6.11.5.14.6.3 PRU-ICSS ECAP Switching Characteristics

| NO.   | PARAMETER              | DESCRIPTION                                          | MIN               | MAX | UNIT |
|-------|------------------------|------------------------------------------------------|-------------------|-----|------|
| PREP3 | t <sub>w</sub> (APWM)  | Pulse duration, Auxiliary PWM (APWM) output high/low | 2P <sup>(1)</sup> |     | ns   |
| PREP4 | t <sub>w</sub> (SYNCO) | Pulse duration, Sync output (asynchronous)           | P <sup>(1)</sup>  |     | ns   |

(1) P = core\_clk period



**Figure 6-65. PRU-ICSS ECAP Switching Characteristics**

#### 6.11.5.14.7 PRU-ICSS MDIO and MII

##### 6.11.5.14.7.1 PRU-ICSS MDIO Timing

###### 6.11.5.14.7.1.1 PRU-ICSS MDIO Timing Conditions

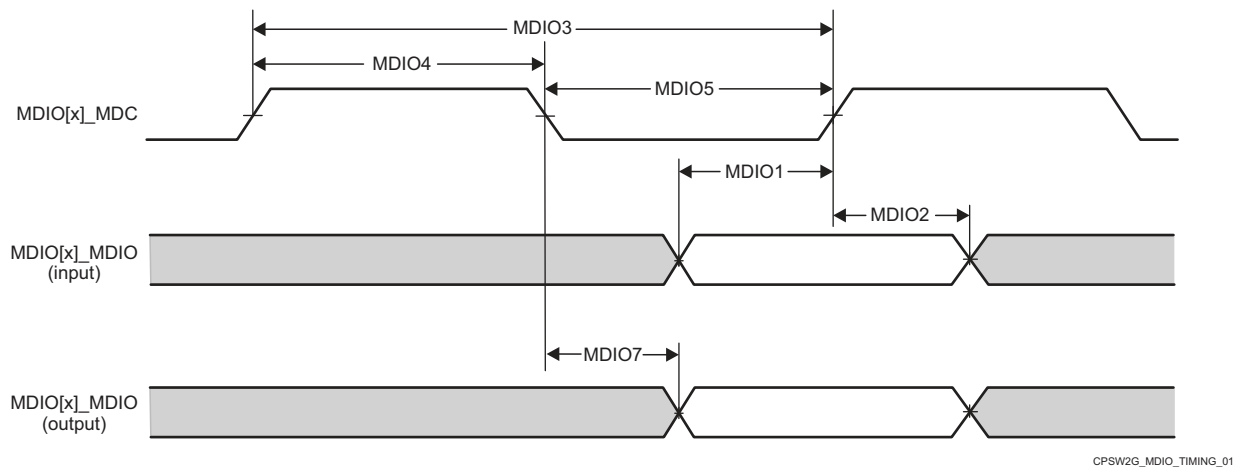
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 0.9 | 3.6 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 10  | 470 | pF   |

###### 6.11.5.14.7.1.2 PRU-ICSS MDIO Timing Requirements

| NO.   | PARAMETER                  | DESCRIPTION                                            | MIN | MAX | UNIT |
|-------|----------------------------|--------------------------------------------------------|-----|-----|------|
| MDIO1 | t <sub>su</sub> (MDIO-MDC) | Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high | 90  |     | ns   |
| MDIO2 | t <sub>h</sub> (MDC-MDIO)  | Hold time, MDIO[x]_MDIO valid from MDIO[x]_MDC high    | 0   |     | ns   |

###### 6.11.5.14.7.1.3 PRU-ICSS MDIO Switching Characteristics

| NO.   | PARAMETER                 | DESCRIPTION                                       | MIN  | MAX | UNIT |
|-------|---------------------------|---------------------------------------------------|------|-----|------|
| MDIO3 | t <sub>c</sub> (MDC)      | Cycle time, MDIO[x]_MDC                           | 400  |     | ns   |
| MDIO4 | t <sub>w</sub> (MDCH)     | Pulse duration, MDIO[x]_MDC high                  | 160  |     | ns   |
| MDIO5 | t <sub>w</sub> (MDCL)     | Pulse duration, MDIO[x]_MDC low                   | 160  |     | ns   |
| MDIO7 | t <sub>d</sub> (MDC-MDIO) | Delay time, MDIO[x]_MDC low to MDIO[x]_MDIO valid | -150 | 150 | ns   |



CPSW2G\_MDIO\_TIMING\_01

Figure 6-66. PRU-ICSS MDIO Timing Requirements and Switching Characteristics

##### 6.11.5.14.7.2 PRU-ICSS MII Timing

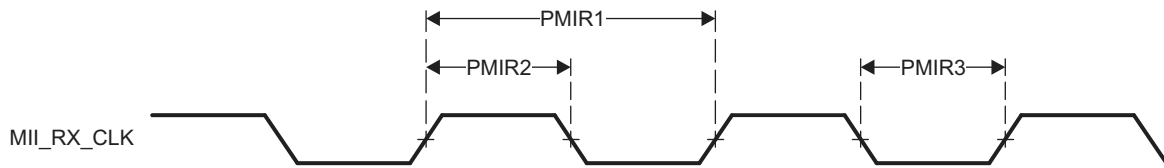
###### 6.11.5.14.7.2.1 PRU-ICSS MII Timing Conditions

| PARAMETER                |                 | MIN | MAX | UNIT |
|--------------------------|-----------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                 |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate | 0.9 | 3.6 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                 |     |     |      |

| PARAMETER |                         | MIN | MAX | UNIT |
|-----------|-------------------------|-----|-----|------|
| $C_L$     | Output Load Capacitance | 2   | 20  | pF   |

#### 6.11.5.14.7.2.2 PRU-ICSS MII Timing Requirements - MII[x]\_RX\_CLK

| NO.   | PARAMETER         | DESCRIPTION                        | MODE    | MIN    | MAX    | UNIT |
|-------|-------------------|------------------------------------|---------|--------|--------|------|
| PMIR1 | $t_{c(RX\_CLK)}$  | Cycle time, MII[x]_RX_CLK          | 10Mbps  | 399.96 | 400.04 | ns   |
|       |                   |                                    | 100Mbps | 39.996 | 40.004 | ns   |
| PMIR2 | $t_{w(RX\_CLKH)}$ | Pulse duration, MII[x]_RX_CLK high | 10Mbps  | 140    | 260    | ns   |
|       |                   |                                    | 100Mbps | 14     | 26     | ns   |
| PMIR3 | $t_{w(RX\_CLKL)}$ | Pulse duration, MII[x]_RX_CLK low  | 10Mbps  | 140    | 260    | ns   |
|       |                   |                                    | 100Mbps | 14     | 26     | ns   |

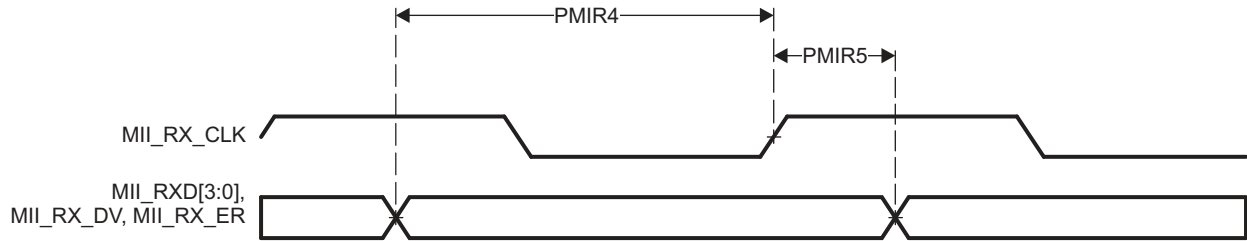


PRU\_MII\_RT\_TIMING\_04

**Figure 6-67. PRU-ICSS MII[x]\_RX\_CLK Timing**

#### 6.11.5.14.7.2.3 PRU-ICSS MII Timing Requirements - MII[x]\_RXD[3:0], MII[x]\_RX\_DV, and MII[x]\_RX\_ER

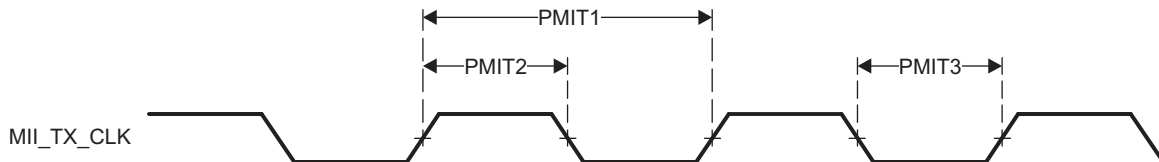
| NO.   | PARAMETER                | DESCRIPTION                                            | MODE     | MIN | MAX | UNIT |
|-------|--------------------------|--------------------------------------------------------|----------|-----|-----|------|
| PMIR4 | $t_{su(RXD-RX\_CLK)}$    | Setup time, MII[x]_RXD[3:0] valid before MII[x]_RX_CLK | 10 Mbps  | 8   |     | ns   |
|       | $t_{su(RX\_DV-RX\_CLK)}$ | Setup time, MII[x]_RX_DV valid before MII[x]_RX_CLK    |          | 8   |     | ns   |
|       | $t_{su(RX\_ER-RX\_CLK)}$ | Setup time, MII[x]_RX_ER valid before MII[x]_RX_CLK    |          | 8   |     | ns   |
|       | $t_{su(RXD-RX\_CLK)}$    | Setup time, MII[x]_RXD[3:0] valid before MII[x]_RX_CLK | 100 Mbps | 8   |     | ns   |
|       | $t_{su(RX\_DV-RX\_CLK)}$ | Setup time, MII[x]_RX_DV valid before MII[x]_RX_CLK    |          | 8   |     | ns   |
|       | $t_{su(RX\_ER-RX\_CLK)}$ | Setup time, MII[x]_RX_ER valid before MII[x]_RX_CLK    |          | 8   |     | ns   |
| PMIR5 | $t_h(RX\_CLK-RXD)$       | Hold time, MII[x]_RXD[3:0] valid after MII[x]_RX_CLK   | 10 Mbps  | 8   |     | ns   |
|       | $t_h(RX\_CLK-RX\_DV)$    | Hold time, MII[x]_RX_DV valid after MII[x]_RX_CLK      |          | 8   |     | ns   |
|       | $t_h(RX\_CLK-RX\_ER)$    | Hold time, MII[x]_RX_ER valid after MII[x]_RX_CLK      |          | 8   |     | ns   |
|       | $t_h(RX\_CLK-RXD)$       | Hold time, MII[x]_RXD[3:0] valid after MII[x]_RX_CLK   | 100 Mbps | 8   |     | ns   |
|       | $t_h(RX\_CLK-RX\_DV)$    | Hold time, MII[x]_RX_DV valid after MII[x]_RX_CLK      |          | 8   |     | ns   |
|       | $t_h(RX\_CLK-RX\_ER)$    | Hold time, MII[x]_RX_ER valid after MII[x]_RX_CLK      |          | 8   |     | ns   |



**Figure 6-68. PRU-ICSS MII[x]\_RXD[3:0], MII[x]\_RX\_DV, and MII[x]\_RX\_ER Timing**

#### 6.11.5.14.7.2.4 PRU-ICSS MII Switching Characteristics - MII[x]\_TX\_CLK

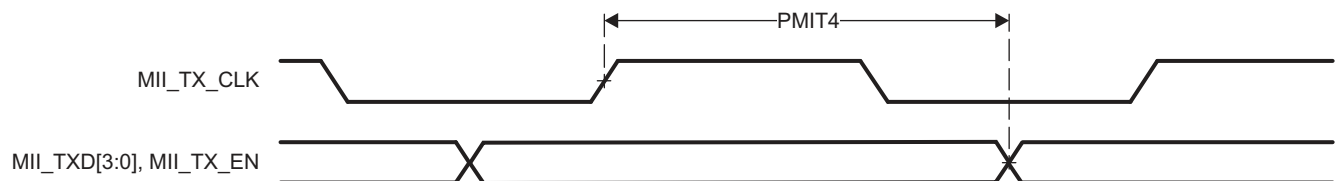
| NO.   | PARAMETER       | DESCRIPTION                        | MODE     | MIN    | MAX    | UNIT |
|-------|-----------------|------------------------------------|----------|--------|--------|------|
| PMIT1 | $t_c(TX\_CLK)$  | Cycle time, MII[x]_TX_CLK          | 10 Mbps  | 399.96 | 400.04 | ns   |
|       |                 |                                    | 100 Mbps | 39.996 | 40.004 | ns   |
| PMIT2 | $t_w(TX\_CLKH)$ | Pulse duration, MII[x]_TX_CLK high | 10 Mbps  | 140    | 260    | ns   |
|       |                 |                                    | 100 Mbps | 14     | 26     | ns   |
| PMIT3 | $t_w(TX\_CLKL)$ | Pulse duration, MII[x]_TX_CLK low  | 10 Mbps  | 140    | 260    | ns   |
|       |                 |                                    | 100 Mbps | 14     | 26     | ns   |



**Figure 6-69. PRU-ICSS MII[x]\_TX\_CLK Timing**

#### 6.11.5.14.7.2.5 PRU-ICSS MII Switching Characteristics - MII[x]\_TXD[3:0] and MII[x]\_TXEN

| NO.   | PARAMETER             | DESCRIPTION                                             | MODE     | MIN | MAX | UNIT |
|-------|-----------------------|---------------------------------------------------------|----------|-----|-----|------|
| PMIT4 | $t_d(TX\_CLK-TXD)$    | Delay time, MII[x]_TX_CLK high to MII[x]_TXD[3:0] valid | 10 Mbps  | 0   | 25  | ns   |
|       | $t_d(TX\_CLK-TX\_EN)$ | Delay time, MII[x]_TX_CLK high to MII[x]_TX_EN valid    |          | 0   | 25  | ns   |
|       | $t_d(TX\_CLK-TXD)$    | Delay time, MII[x]_TX_CLK high to MII[x]_TXD[3:0] valid | 100 Mbps | 0   | 25  | ns   |
|       | $t_d(TX\_CLK-TX\_EN)$ | Delay time, MII[x]_TX_CLK high to MII[x]_TX_EN valid    |          | 0   | 25  | ns   |



**Figure 6-70. PRU-ICSS MII[x]\_TXD[3:0], MII[x]\_TX\_EN Timing**

### 6.11.5.15 Sigma Delta Filter Module (SDFM)

For more information, see *Sigma Delta Filter Module* section in the device TRM.

#### 6.11.5.15.1 SDFM Timing Conditions

| PARAMETER        |                 | MODE   | MIN | MAX | UNIT |
|------------------|-----------------|--------|-----|-----|------|
| INPUT CONDITIONS |                 |        |     |     |      |
| SR <sub>I</sub>  | Input Slew Rate | Mode 0 | 0.5 | 5   | V/ns |

#### 6.11.5.15.2 SDFM Switching Characteristics

(2)

| NO.  | PARAMETER                   | DESCRIPTION                                 | MODE   | MIN               | MAX                 | UNIT |
|------|-----------------------------|---------------------------------------------|--------|-------------------|---------------------|------|
| M0-1 | t <sub>c</sub> (SDC)        | Cycle time, SDx_Cy                          | Mode 0 | 5P <sup>(1)</sup> | 256P <sup>(1)</sup> | ns   |
| M0-2 | t <sub>w</sub> (SDCHL)      | Pulse duration, SDx_Cy (high/low)           | Mode 0 | 2P <sup>(1)</sup> |                     | ns   |
| M0-3 | t <sub>sh</sub> (SDDV-SDCH) | Setup time, SDx_Dy valid before SDx_Cy high | Mode 0 | 2P <sup>(1)</sup> |                     | ns   |
| M0-4 | t <sub>h</sub> (SDCH-SDD)   | Hold time, SDx_Dy wait after SDx_Cy high    | Mode 0 | 2P <sup>(1)</sup> |                     | ns   |

(1) P = SYSCLK period in ns.

(2) Some SDFM signals are pinmuxed with I2C0 SDA and SCL pins. These pins use an alternate open drain voltage buffer and may not meet the specified parameters. Values are pending additional post-silicon validation.

#### 6.11.5.16 Universal Asynchronous Receiver/Transmitter (UART)

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in the device TRM.

##### 6.11.5.16.1 UART Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input Slew Rate         | 0.5 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output Load Capacitance | 1   | 30  | pF   |

##### 6.11.5.16.2 UART Timing Requirements

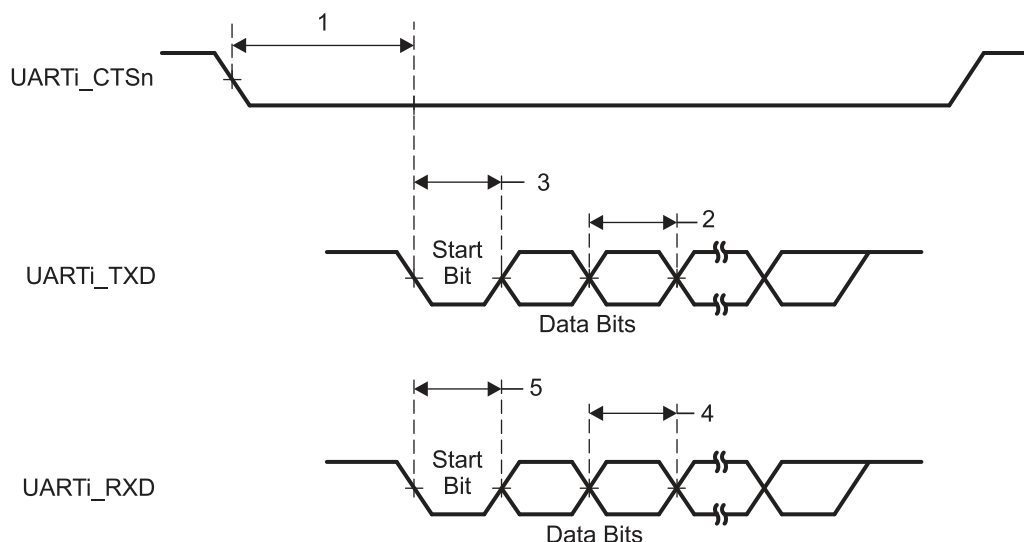
| NO. | PARAMETER           | DESCRIPTION                                 | MIN                  | MAX                  | UNIT |
|-----|---------------------|---------------------------------------------|----------------------|----------------------|------|
| 4   | t <sub>w(RX)</sub>  | Pulse width, receive data bit, high or low  | 0.95U <sup>(1)</sup> | 1.05U <sup>(1)</sup> | ns   |
| 5   | t <sub>w(CTS)</sub> | Pulse width, receive start bit, high or low | 0.95U <sup>(1)</sup> |                      | ns   |

(1) U = UART baud time = 1 / Programmed baud rate.

##### 6.11.5.16.3 UART Switching Characteristics

| NO. | PARAMETER              | DESCRIPTION                                  | MODE  | MIN                    | MAX                    | UNIT |
|-----|------------------------|----------------------------------------------|-------|------------------------|------------------------|------|
|     | f <sub>(baud)</sub>    | Programmable baud rate                       | 15 pF |                        | 12                     | MHz  |
|     |                        |                                              | 30 pF |                        | 0.115                  |      |
| 2   | t <sub>w(TX)</sub>     | Pulse width, transmit data bit, high or low  |       | U <sup>(1)</sup> – 2.2 | U <sup>(1)</sup> + 2.2 | ns   |
| 3   | t <sub>w(RTS)</sub>    | Pulse width, transmit start bit, high or low |       | U <sup>(1)</sup> – 2.2 |                        | ns   |
| 1   | t <sub>d(CTS-TX)</sub> | Delay time, receive CTS bit to transmit data |       | 30                     |                        | ns   |

(1) U = UART baud time = 1 / Programmed baud rate.



**Figure 6-71. UART Timing Requirements and Switching Characteristics**

### 6.11.6 Emulation and Debug

For more details about features and additional description information on the device Trace and JTAG interfaces, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections. For more information, see the *On-Chip Debug* section in the device TRM.

#### 6.11.6.1 JTAG

The acronym stands for the **Joint Test Action Group**, the committee of engineers who defined the boundary-scan standard (IEEE std 1149.1). For more details about features and additional description information on the device JTAG interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

##### 6.11.6.1.1 JTAG Timing Conditions

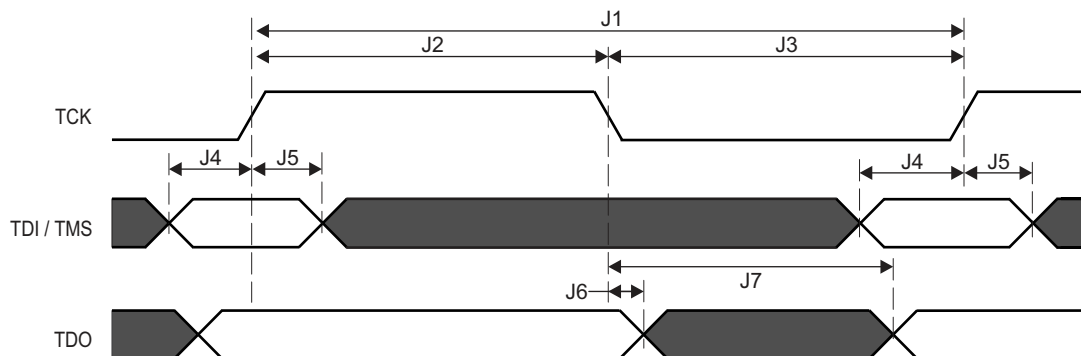
| PARAMETER                |                         | MIN | MAX  | UNIT |
|--------------------------|-------------------------|-----|------|------|
| <b>INPUT CONDITIONS</b>  |                         |     |      |      |
| SR <sub>I</sub>          | Input Slew Rate         | 0.5 | 2.00 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |      |      |
| C <sub>L</sub>           | Output Load Capacitance | 5   | 15   | pF   |

##### 6.11.6.1.2 JTAG Timing Requirements

| NO. | PARAMETER          | DESCRIPTION                              | MIN  | MAX | UNIT |
|-----|--------------------|------------------------------------------|------|-----|------|
| J1  | $t_{c(TCK)}$       | Cycle time, TCK                          | 40   |     | ns   |
| J2  | $t_{w(TCKH)}$      | Pulse width, TCK high                    | 16   |     | ns   |
| J3  | $t_{w(TCKL)}$      | Pulse width, TCK low                     | 16   |     | ns   |
| J4  | $t_{su(TDI-TCKH)}$ | Input setup time, TDI valid to TCK high  | 2    |     | ns   |
|     | $t_{su(TMS-TCKH)}$ | Input setup time, TMS valid to TCK high  | 2    |     |      |
| J5  | $t_h(TCK-TDI)$     | Input hold time, TDI valid from TCK high | 15.9 |     | ns   |
|     | $t_h(TCK-TMS)$     | Input hold time, TMS valid from TCK high | 15.9 |     |      |

##### 6.11.6.1.3 JTAG Switching Characteristics

| NO. | PARAMETER        | DESCRIPTION                        | MIN       | MAX      | UNIT |
|-----|------------------|------------------------------------|-----------|----------|------|
| J6  | $t_d(TCKL-TDOl)$ | Delay time, TCK low to TDO invalid | -0.067005 |          | ns   |
| J7  | $t_d(TCKL-TDOV)$ | Delay time, TCK low to TDO valid   |           | 11.89594 | ns   |



**Figure 6-72. JTAG Timing Requirements and Switching Characteristics**

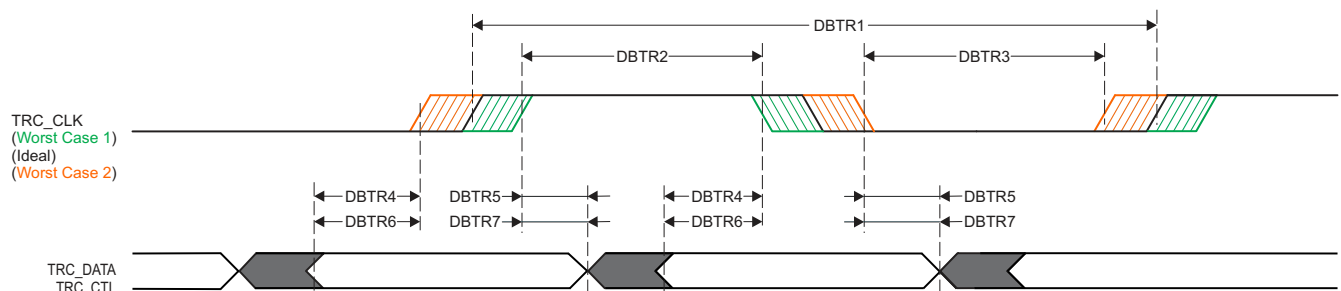
## 6.11.6.2 Trace

### 6.11.6.2.1 Debug Trace Timing Conditions

| PARAMETER                    |                                               | MIN | MAX | UNIT |
|------------------------------|-----------------------------------------------|-----|-----|------|
| <b>OUTPUT CONDITIONS</b>     |                                               |     |     |      |
| $C_L$                        | Output Load Capacitance                       | 2   | 5   | pF   |
| <b>OUTPUT CONDITIONS</b>     |                                               |     |     |      |
| $t_d(\text{Trace Mismatch})$ | Propagation delay mismatch across all traces. |     | 200 | ps   |

### 6.11.6.2.2 Debug Trace Switching Characteristics

| NO.   | PARAMETER                             | DESCRIPTION                                        | MIN  | MAX | UNIT |
|-------|---------------------------------------|----------------------------------------------------|------|-----|------|
| DBTR1 | $t_{c}(\text{TRC\_CLK})$              | Cycle time, TRC_CLK                                | 9.75 |     | ns   |
| DBTR2 | $t_{w}(\text{TRC\_CLKH})$             | Pulse width, TRC_CLK high                          | 4.13 |     | ns   |
| DBTR3 | $t_{w}(\text{TRC\_CLKL})$             | Pulse width, TRC_CLK low                           | 4.13 |     | ns   |
| DBTR4 | $t_{osu}(\text{TRC\_DATAV-TRC\_CLK})$ | Output setup time, TRC_DATA valid to TRC_CLK edge  | 1.22 |     | ns   |
| DBTR5 | $t_{oh}(\text{TRC\_CLK-TRC\_DATAI})$  | Output hold time, TRC_CLK edge to TRC_DATA invalid | 1.22 |     | ns   |
| DBTR6 | $t_{osu}(\text{TRC\_CTLV-TRC\_CLK})$  | Output setup time, TRC_CTL valid to TRC_CLK edge   | 1.22 |     | ns   |
| DBTR7 | $t_{oh}(\text{TRC\_CLK-TRC\_CTLI})$   | Output hold time, TRC_CLK edge to TRC_CTL invalid  | 1.22 |     | ns   |



SPRSP08\_Debug\_01

Figure 6-73. Trace Switching Characteristics

## 6.12 Decoupling Capacitor Requirements

### 6.12.1 Decoupling Capacitor Requirements

| PARAMETER         | DESCRIPTION         | MIN | TYP | MAX | UNIT          |
|-------------------|---------------------|-----|-----|-----|---------------|
| $C_{VDD}$         | Ground (Cap)        |     | 10  |     | $\mu\text{F}$ |
| $C_{VDDS33}$      | 3.3V VDDS (Cap)     |     | 10  |     | $\mu\text{F}$ |
| $C_{VDDA33}$      | 3.3V VDDA (Cap)     |     | 10  |     | $\mu\text{F}$ |
| $C_{VDDS18}$      | 1.8V VDDS (Cap)     |     | 0.1 |     | $\mu\text{F}$ |
| $C_{VDDA18}$      | 1.8V VDDA (Cap)     |     | 0.1 |     | $\mu\text{F}$ |
| $C_{VPP}$         | 1.7V VPP (Cap)      |     | 0.1 |     | $\mu\text{F}$ |
| $C_{VDDS18\_LDO}$ | 1.8V LDO VDDS (Cap) |     | 3.3 |     | $\mu\text{F}$ |
| $C_{VDDA18\_LDO}$ | 1.8V LDO VDDA (Cap) |     | 3.3 |     | $\mu\text{F}$ |
| $C_{ADC\_VREF}$   | ADC VREFHI (Cap)    |     | 4.7 |     | $\mu\text{F}$ |

## 7 Detailed Description

### 7.1 Overview

The AM263x Sitara Arm® Microcontrollers are built to meet the complex real-time processing and control needs of next generation industrial and automotive embedded projects. AM263x uniquely combines advanced compute with industry leading real-time control peripherals to meet the growing performance needs of applications such as HEV/EV (traction inverters, on-board chargers, and DC-DC converters), motor drives, renewable energy, energy storage, and other general real-time constrained systems. AM263x combines up to four Cortex-R5F MCUs, a real-time control subsystem (CONTROLSS), a Hardware Security Module (HSM), and one instance of Sitara's Programmable Real-Time Unit Subsystem (PRU-ICSS), making AM263x designed for advanced motor control and digital power control applications.

For multicore AM263x devices, the R5F cores are arranged in clusters of two Cortex-R5F cores per cluster. Each Cortex-R5F core has 64KB of shared tightly coupled memory (TCM). AM263x has 2MB of shared SRAM spread across 4 banks of 512kB each. The multiple Arm® cores are configured to be in lockstep mode after device reset. They can be optionally programmed by the bootlooder to run in dual core mode instead. Extensive ECC is included with the on-chip memory, peripherals, and interconnect for enhanced reliability. The HSM on AM263x provides cryptographic acceleration, secure boot, and manages granular firewalls, enabling developers to design the most secure systems.

The Real-Time Control Subsystem (CONTROLSS) is a revolutionary subsystem integrated into the device. CONTROLSS contains multiple digital and analog control peripherals including: ADC, CMPSS, EPWM, ECAP, and EQEP, among others to enable efficient execution of critical sense/process/actuate real-time signal chain control loops. The integrated crossbar (XBAR) infrastructure enables flexible configuration and routing of external signals to internal ports and internal signals to external pins.

The PRU-ICSS in AM263x provides the flexible industrial communications capability necessary to run advanced Ethernet protocols such as EtherCAT®, PROFINET®, and Ethernet/IP™, or the PRU-ICSS can be used for standard Ethernet connectivity and custom I/O interfacing. The PRU-ICSS supports two Ethernet Ports at 10/100 Mbit operation. It also enables additional interfaces in the SoC including sigma delta decimation filters and absolute encoder interfaces. In addition to the PRU-ICSS, the Common Platform Switch (CPSW) interface provides two Ethernet ports that can support up to 10/100/1000 Mbit operation and supports standard Ethernet connectivity.

TI provides a complete set of microcontroller software and development tools for the AM263x family of microcontrollers in addition to multiple pin-to-pin compatible devices for scalability and ease of use.

## 7.2 Processor Subsystems

### 7.2.1 Arm Cortex-R5F Subsystem

The R5FSS is a dual-core implementation of the Arm® Cortex®-R5F processor configured for dual-core (split) or lockstep modes of operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™ debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC Aggregators, and various wrappers for protocol conversion and address translation for easy integration into the SoC. The device supports up to two R5FSS modules for a total possible 4x functional cores (dual-core mode) or 2x functional cores (lockstep mode).

---

#### Note

The Arm® Cortex®-R5F processor is a Cortex-R5 processor that includes the optional Floating-point Unit (FPU) extension.

---

For more information, see *R5FSS* section in *Processors and Accelerators* chapter in the device TRM.

## 8 Applications, Implementation, and Layout

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

---

### 8.1 Device Connection and Layout Fundamentals

#### 8.1.1 External Oscillator

For more information about External Oscillators, see the *Clock Specifications* section.

#### 8.1.2 JTAG, EMU, and TRACE

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the [XDS Target Connection Guide](#).

For recommendations on JTAG, EMU, and TRACE routing, see the [Emulation and Trace Headers Technical Reference Manual](#)

#### 8.1.3 Hardware Design Guide

For details regarding creating PCB systems based on the AM263x family of MCU devices, please see the [AM263x Hardware Design Guide](#).

## 9 Device and Documentation Support

### 9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microcontrollers (MCUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, XAM2634AOLFGMZCZQ). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

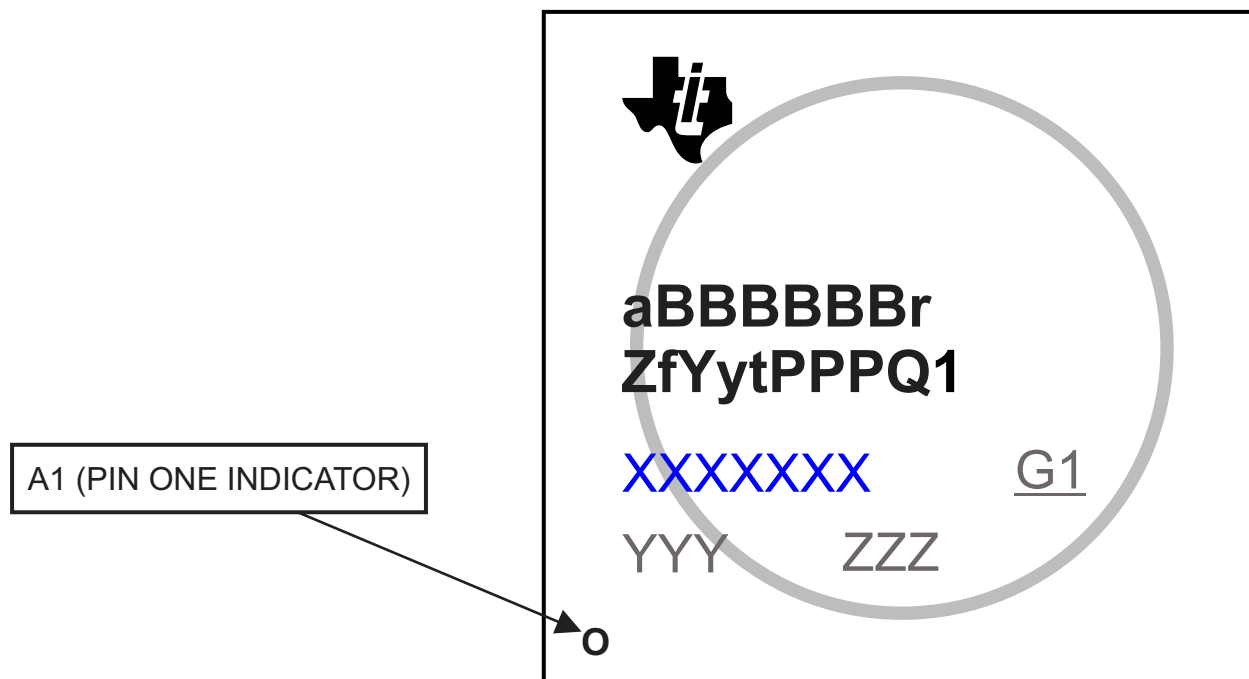
Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM263x devices in the ZCZ package type, see the Package Option Addendum of this document, the TI website ([ti.com](http://ti.com)), or contact your TI sales representative.

### 9.1.1 Standard Package Symbolization

#### Note

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.



**Figure 9-1. Printed Device Reference**

### 9.1.2 Device Naming Convention

**Table 9-1. Nomenclature Description**

| FIELD PARAMETER  | FIELD DESCRIPTION                                               | VALUE                | DESCRIPTION                                                                                                         |
|------------------|-----------------------------------------------------------------|----------------------|---------------------------------------------------------------------------------------------------------------------|
| a <sup>(2)</sup> | Device evolution stage                                          | X                    | Prototype                                                                                                           |
|                  |                                                                 | P                    | Preproduction (production test flow, no reliability data)                                                           |
|                  |                                                                 | BLANK <sup>(1)</sup> | Production                                                                                                          |
| BBBBBB           | Base production part number                                     | AM2634               | See <a href="#">Device Comparison</a> .                                                                             |
|                  |                                                                 | AM2632               |                                                                                                                     |
|                  |                                                                 | AM2631               |                                                                                                                     |
| r                | Device revision                                                 | A                    | SR 1.0                                                                                                              |
|                  |                                                                 | B                    | SR 1.0A                                                                                                             |
|                  |                                                                 | C                    | SR 1.1                                                                                                              |
| Z                | Device Operating Performance Points                             | N                    | See <a href="#">Operating Performance Points</a> .                                                                  |
|                  |                                                                 | O                    |                                                                                                                     |
|                  |                                                                 | P                    |                                                                                                                     |
| f                | Features<br>(see <a href="#">Table 4-1, Device Comparison</a> ) | C                    | PRU Only<br>+ CAN-FD Supported<br>+ Standard Analog                                                                 |
|                  |                                                                 | D                    | PRU-ICSS<br>+ CAN-FD Supported<br>+ Standard Analog                                                                 |
|                  |                                                                 | E                    | PRU-ICSS<br>+ EtherCAT HW Accelerator<br>+ CAN-FD Supported<br>+ Standard Analog                                    |
|                  |                                                                 | F                    | PRU-ICSS<br>+ EtherCAT HW Accelerator<br>+ CAN-FD Supported<br>+ Pre-integrated Stacks Enabled<br>+ Standard Analog |
|                  |                                                                 | J                    | PRU Only<br>+ CAN-FD Supported<br>+ Enhanced Analog                                                                 |
|                  |                                                                 | K                    | PRU-ICSS<br>+ CAN-FD Supported<br>+ Enhanced Analog                                                                 |
|                  |                                                                 | L                    | PRU-ICSS<br>+ EtherCAT HW Accelerator<br>+ CAN-FD Supported<br>+ Enhanced Analog                                    |
|                  |                                                                 | M                    | PRU-ICSS<br>+ EtherCAT HW Accelerator<br>+ CAN-FD Supported<br>+ Pre-integrated Stacks<br>+ Enhanced Analog         |
| Y                | Functional Safety                                               | G                    | Non-Functional Safety (AM2631 only)                                                                                 |
|                  |                                                                 | F                    | Functional Safety                                                                                                   |
| y                | Security                                                        | H                    | Secure                                                                                                              |
| t <sup>(3)</sup> | Junction Temperature<br>(see <a href="#">Section 6.5, ROC</a> ) | A                    | –40°C to 105°C - Industrial                                                                                         |
|                  |                                                                 | I                    | –40°C to 125°C - Automotive                                                                                         |
|                  |                                                                 | M                    | –40°C to 150°C - Extended Automotive                                                                                |
| PPP              | Package Designator                                              | ZCZ                  | ZCZ NFBGA-N324 (15 mm × 15 mm) Package                                                                              |

**Table 9-1. Nomenclature Description (continued)**

| FIELD PARAMETER | FIELD DESCRIPTION     | VALUE | DESCRIPTION                      |
|-----------------|-----------------------|-------|----------------------------------|
| Q1              | Automotive Designator | Q1    | Auto Qualified (AEC-Q100)        |
|                 |                       | BLANK | Standard                         |
| XXXXXXX         |                       |       | Lot Trace Code (LTC)             |
| YYY             |                       |       | Production Code; For TI use only |
| ZZZ             |                       |       | Production Code; For TI use only |
| O               |                       |       | Pin one designator               |
| G1              |                       |       | ECAT - Green package designator  |

- (1) BLANK in the symbol or part number is collapsed so there are no gaps between characters.
- (2) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices. Prototype devices are shipped against the following disclaimer:  
 "This product is still in development and is intended for internal evaluation purposes."  
 Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.
- (3) Applies to device max junction temperature.

## 9.2 Tools and Software

The following products support development for AM263x platforms:

### Development Tools

**Code Composer Studio™ Integrated Development Environment** Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

**SysConfig-PinMux Tool** The SysConfig-PinMux Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI Embedded Processor devices. The tool can be used to automatically calculate the optimal pinmux configuration to satisfy entered system requirements. The tool will generate output C header/code files that can be imported into software development kits (SDKs) and used to configure customer's software to meet custom hardware requirements.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at [ti.com](https://www.ti.com). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

## 9.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents are provided to describe the AM263x device.

**AM263x Silicon Errata** Describes the known exceptions to the functional specifications for the device.

**AM263x Technical Reference Manual** Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM263x family of devices.

**AM263x TRM Register Addendum** Details the memory mapped register information for each peripheral and subsystem in the AM263x family of devices.

## 9.4 Support Resources

**TI E2E™ support forums** are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## 9.5 Trademarks

Ethernet/IP™ is a trademark of ODVA, INC..

Sitara™, Code Composer Studio™, and TI E2E™ are trademarks of Texas Instruments.

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PROFINET® is a registered trademark of PROFINET International.

IO-Link® is a registered trademark of PROFIBUS Nutzerorganisation e.V. eingetragener verein (e.v.) FED REP GERMANY.

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## 9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

### Changes from July 21, 2023 to August 30, 2025 (from Revision D (July 2023) to Revision E (August 2025))

|                                                                                                                                                                                                         | Page |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • (Features): Added support for MII mode.....                                                                                                                                                           | 1    |
| • (Package Information): Updated Package Information table to match TI Standards.....                                                                                                                   | 3    |
| • (Device Comparison): Added Automotive temperature range.....                                                                                                                                          | 6    |
| • (Pin Attributes): Updated SOP pin types from "0" to "I" only.....                                                                                                                                     | 12   |
| • (Pin Connectivity Requirements): Added "(SOP1)" after "QSPI0_D1".....                                                                                                                                 | 63   |
| • (SAFETY_ERRORn Switching Characteristics): Updated table note reference from "RST22" to "SFTY3".....                                                                                                  | 81   |
| • (CPSW MDIO Timing Requirements): Updated MDIO1 MIN value from "90 ns" to "45 ns".....                                                                                                                 | 84   |
| • (CPSW MDIO Switching Characteristics): Updated MDIO MIN value from "-150 ns" to "-10 ns" and MAX value from "150 ns" to "10 ns".....                                                                  | 84   |
| • (CPSW RGMII[x]_TxC, RGMII[x]_TD[3:0], and RGMII[x]_TX_CTL Switching Characteristics - RGMII Mode): Updated table note on internal delay from "always enabled" to "by default enabled after POR."..... | 89   |
| • Removed mentions of TSN.....                                                                                                                                                                          | 149  |
| • Added details about the Ethernet capabilities offered outside of the PRU-ICSS.....                                                                                                                    | 149  |
| • Clarified the architecture of the R5F cores for multicore devices.....                                                                                                                                | 149  |
| • Updated the description that outlined some HSM features.....                                                                                                                                          | 149  |
| • (Device Naming Convention): Added device grade I with Junction temperature of -40°C to 125°C.....                                                                                                     | 154  |

### Changes from November 18, 2022 to July 21, 2023 (from Revision C (November 2022) to Revision D (July 2023))

|                                                                                                                                        | Page |
|----------------------------------------------------------------------------------------------------------------------------------------|------|
| • <b>Global:</b> Changed CPSW3G to CPSW.....                                                                                           | 1    |
| • (Features): Changed "Up to 140 GPIO" to "Up to 139 GPIO".....                                                                        | 1    |
| • (Features): Changed PRU Memory from 12KB to 16KB.....                                                                                | 1    |
| • (Features): Changed from Functional Safety "Targeted" to "Compliant".....                                                            | 1    |
| • (Device Comparison): Added footnote about TCM access to the core.....                                                                | 6    |
| • (Device Comparison): Add footnote about Functional Safety Compliance.....                                                            | 6    |
| • (Device Comparison): Changed "Up to 140" to "Up to 139".....                                                                         | 6    |
| • (Pin Attributes): Updated/Changed all applicable Ball State After Reset values from to "Off / Off / Off" from "Off / On / Down"..... | 12   |
| • (Pin Attributes): Updated QSPI0_CLKLB ball Ball State After Reset values to "On / On / Down".....                                    | 12   |
| • (Pin Attributes): Replaced RSVD_J16 with VDD.....                                                                                    | 12   |
| • (Pin Attributes): Replaced EQEP_S and EQEP_I with EQEP_STROBE and EQEP_INDEX.....                                                    | 12   |
| • (Digital and Analog IO Electrical Characteristics): Changed V_OH to VDDS33 - 0.45V and V_OL to 0.45V.....                            | 68   |
| • (Crystal Oscillator (XTAL) Parameters): Added Duty Cycle.....                                                                        | 82   |
| • (Peripheral Timings ePWM): Added EPWM Characteristics table.....                                                                     | 91   |
| • (SPI): Shanged SS2 and SS3 minimum values from "18.45 x P" to "0.45 x P".....                                                        | 121  |

- 
- (Decoupling Capacitor Requirements): Added  $C_{VPP}$  and  $C_{ADC\_VREF}$  ..... [148](#)
-

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

To learn more about TI packaging, visit the [Packaging information](#) website.

**PACKAGING INFORMATION**

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)          |
|------------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------|
| <a href="#">AM2631CNDGHAZCZR</a>   | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2631C<br>NDGHAZCZ<br>548   |
| AM2631CNDGHAZCZR.B                 | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2631C<br>NDGHAZCZ<br>548   |
| <a href="#">AM2631CNDGHMZCZRQ1</a> | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2631C<br>NDGHMZCZQ1<br>548 |
| AM2631CNDGHMZCZRQ1.B               | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2631C<br>NDGHMZCZQ1<br>548 |
| <a href="#">AM2631CODGHMZCZRQ1</a> | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2631C<br>ODGHMZCZQ1<br>548 |
| AM2631CODGHMZCZRQ1.B               | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2631C<br>ODGHMZCZQ1<br>548 |
| <a href="#">AM2632CNDFHAZCZR</a>   | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2632C<br>NDFHAZCZ<br>548   |
| AM2632CNDFHAZCZR.B                 | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2632C<br>NDFHAZCZ<br>548   |
| <a href="#">AM2632CNEFHAZCZR</a>   | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2632C<br>NEFHAZCZ<br>548   |
| AM2632CNEFHAZCZR.B                 | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2632C<br>NEFHAZCZ<br>548   |
| <a href="#">AM2632CODFHMZCZRQ1</a> | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2632C<br>ODFHMZCZQ1<br>548 |

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)          |
|------------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------|
| AM2632CODFHMZCZRQ1.B               | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2632C<br>ODFHMZCZQ1<br>548 |
| <a href="#">AM2632COKFHAZCZR</a>   | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2632C<br>OKFHAZCZ<br>548   |
| AM2632COKFHAZCZR.B                 | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2632C<br>OKFHAZCZ<br>548   |
| <a href="#">AM2632COKFHMZCZRQ1</a> | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2632C<br>OKFHMZCZQ1<br>548 |
| AM2632COKFHMZCZRQ1.B               | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2632C<br>OKFHMZCZQ1<br>548 |
| <a href="#">AM2632COLFHAZCZR</a>   | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2632C<br>OLFHAZCZ<br>548   |
| AM2632COLFHAZCZR.B                 | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2632C<br>OLFHAZCZ<br>548   |
| <a href="#">AM2632COMFHAZCZR</a>   | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2632C<br>OMFHAZCZ<br>548   |
| AM2632COMFHAZCZR.B                 | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2632C<br>OMFHAZCZ<br>548   |
| <a href="#">AM2632CPDFHMZCZRQ1</a> | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2632C<br>PDFHMZCZQ1<br>548 |
| AM2632CPDFHMZCZRQ1.B               | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2632C<br>PDFHMZCZQ1<br>548 |
| <a href="#">AM2634CODFHAZCZR</a>   | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2634C<br>ODFHAZCZ<br>548   |

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)          |
|------------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------|
| AM2634CODFHAZCZR.B                 | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2634C<br>ODFHAZCZ<br>548   |
| <a href="#">AM2634CODFHMZCZRQ1</a> | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2634C<br>ODFHMZCZQ1<br>548 |
| AM2634CODFHMZCZRQ1.B               | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2634C<br>ODFHMZCZQ1<br>548 |
| <a href="#">AM2634COEFHAZCZR</a>   | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2634C<br>OEFHAZCZ<br>548   |
| AM2634COEFHAZCZR.B                 | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2634C<br>OEFHAZCZ<br>548   |
| <a href="#">AM2634COKFHAZCZR</a>   | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2634C<br>OKFHAZCZ<br>548   |
| AM2634COKFHAZCZR.B                 | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2634C<br>OKFHAZCZ<br>548   |
| <a href="#">AM2634COKFHMZCZRQ1</a> | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2634C<br>OKFHMZCZQ1<br>548 |
| AM2634COKFHMZCZRQ1.B               | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2634C<br>OKFHMZCZQ1<br>548 |
| <a href="#">AM2634COLFHAZCZR</a>   | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2634C<br>OLFHAZCZ<br>548   |
| AM2634COLFHAZCZR.B                 | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2634C<br>OLFHAZCZ<br>548   |
| <a href="#">AM2634COMFHAZCZR</a>   | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2634C<br>OMFHAZCZ<br>548   |

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)           |
|------------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| AM2634COMFHAZCZR.B                 | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 105   | AM2634C<br>OMFHAZCZ<br>548    |
| <a href="#">AM2634CPDFHMZCZRQ1</a> | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2634C<br>PDFHMZCZRQ1<br>548 |
| AM2634CPDFHMZCZRQ1.B               | Active        | Production           | NFBGA (ZCZ)   324 | 1000   LARGE T&R      | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 150   | AM2634C<br>PDFHMZCZRQ1<br>548 |
| <a href="#">XAM2634BOMFHAZCZ</a>   | Active        | Preproduction        | NFBGA (ZCZ)   324 | 1   JEDEC TRAY (5+1)  | -           | Call TI                              | Call TI                           | -40 to 105   |                               |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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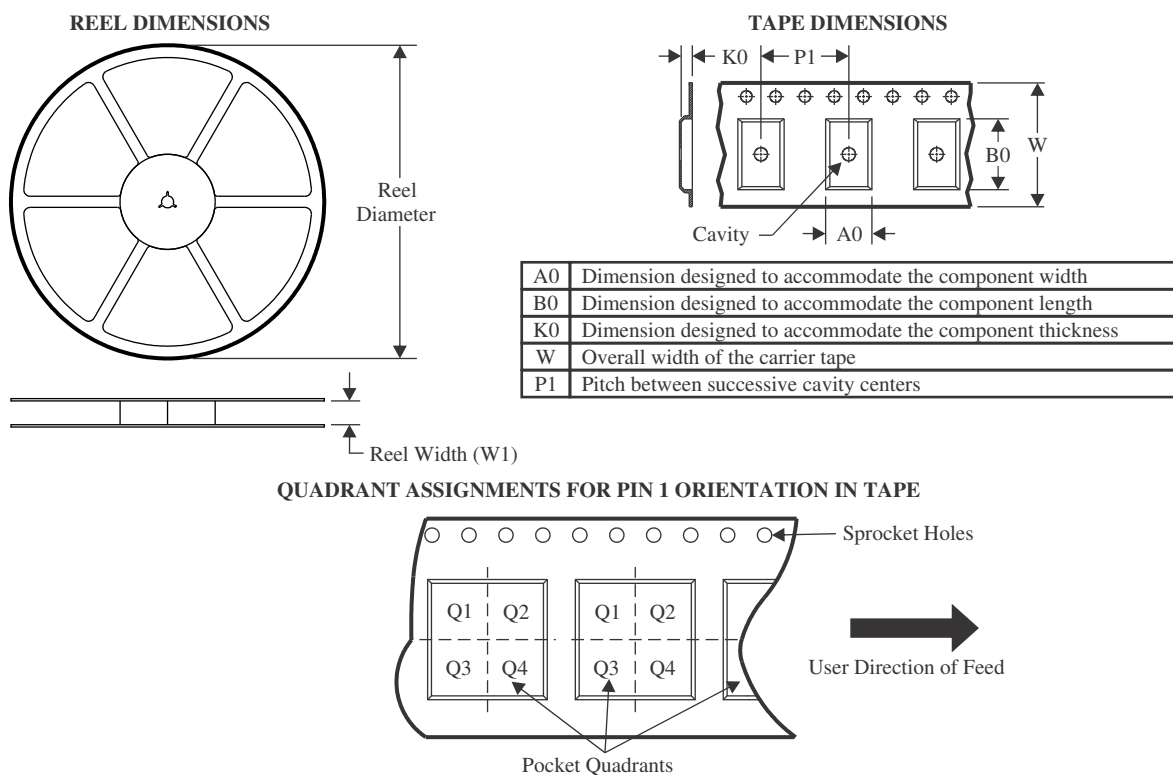
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**OTHER QUALIFIED VERSIONS OF AM2631, AM2631-Q1, AM2632, AM2632-Q1, AM2634, AM2634-Q1 :**

- Catalog : [AM2631](#), [AM2632](#), [AM2634](#)
- Automotive : [AM2631-Q1](#), [AM2632-Q1](#), [AM2634-Q1](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

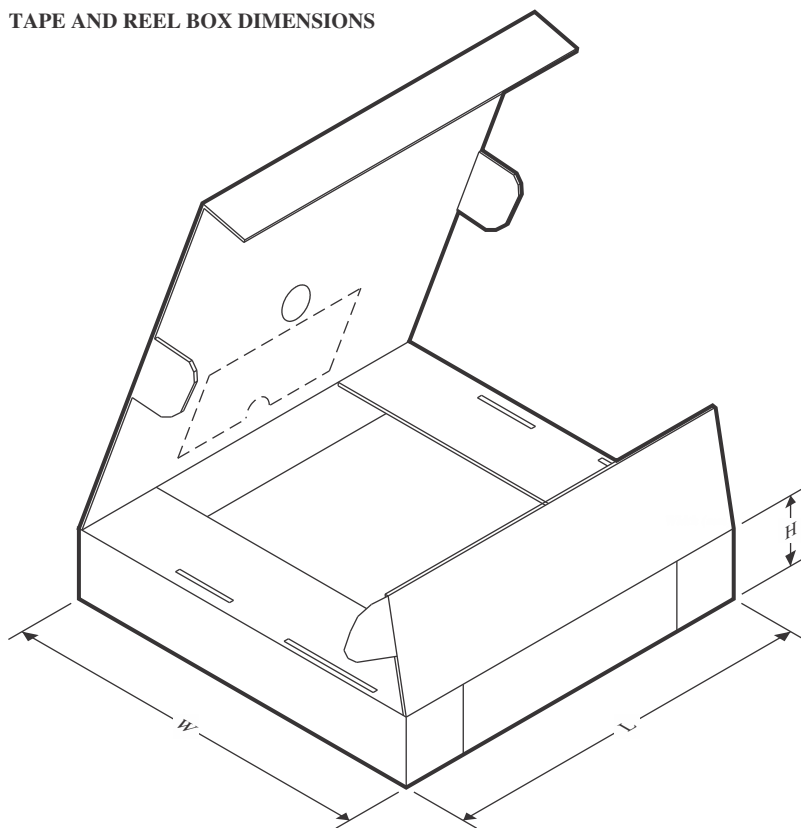
**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| AM2631CNDGHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2631CNDGHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2631CODGHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2632CNDFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2632CNEFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2632CODFHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2632COKFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2632COKFHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2632COLFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2632COMFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2632CPDFHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2634CODFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2634CODFHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2634COEFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2634COKFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2634COKFHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| AM2634COLFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2634COMFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |
| AM2634CPDFHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 330.0              | 24.4               | 15.3    | 15.3    | 2.35    | 20.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

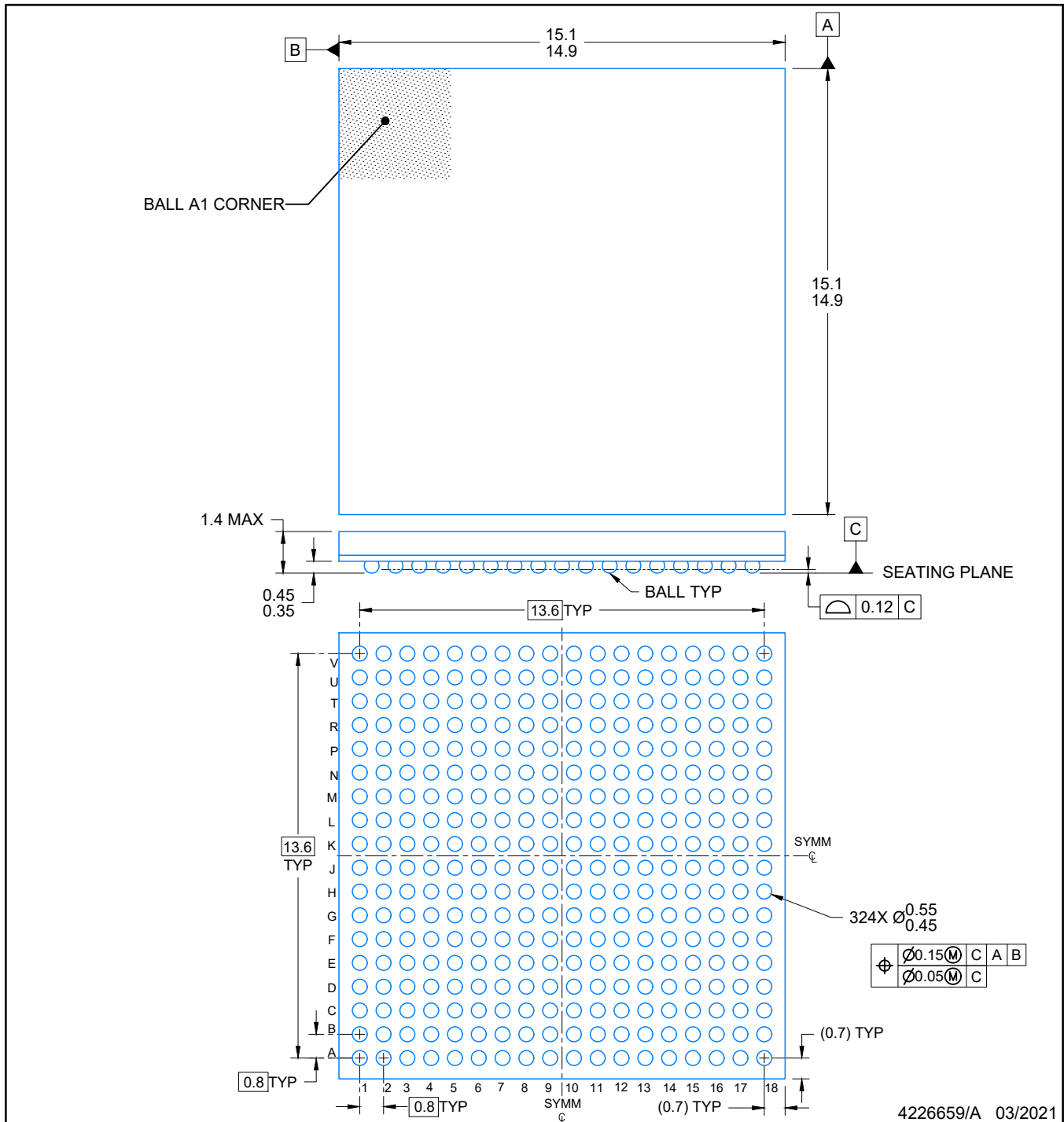


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| AM2631CNDGHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2631CNDGHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2631CODGHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2632CNDFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2632CNEFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2632CODFHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2632COKFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2632COKFHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2632COLFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2632COMFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2632CPDFHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2634CODFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2634CODFHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2634COEFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2634COKFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2634COKFHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2634COLFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |
| AM2634COMFHAZCZR   | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |

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| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| AM2634CPDFHMZCZRQ1 | NFBGA        | ZCZ             | 324  | 1000 | 336.6       | 336.6      | 41.3        |

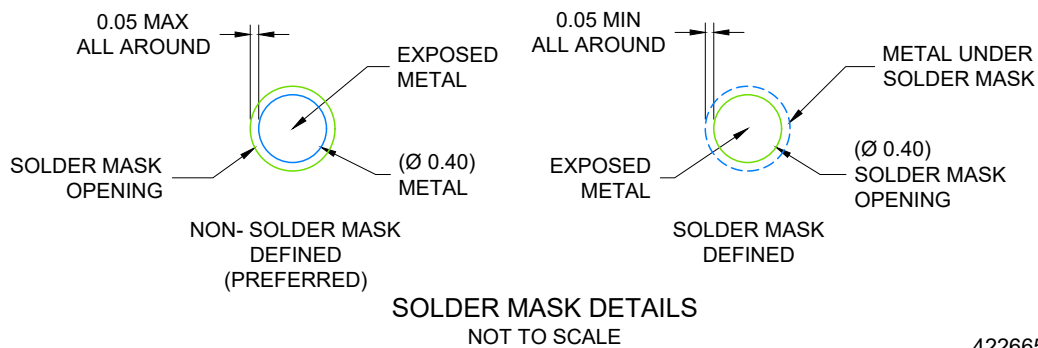
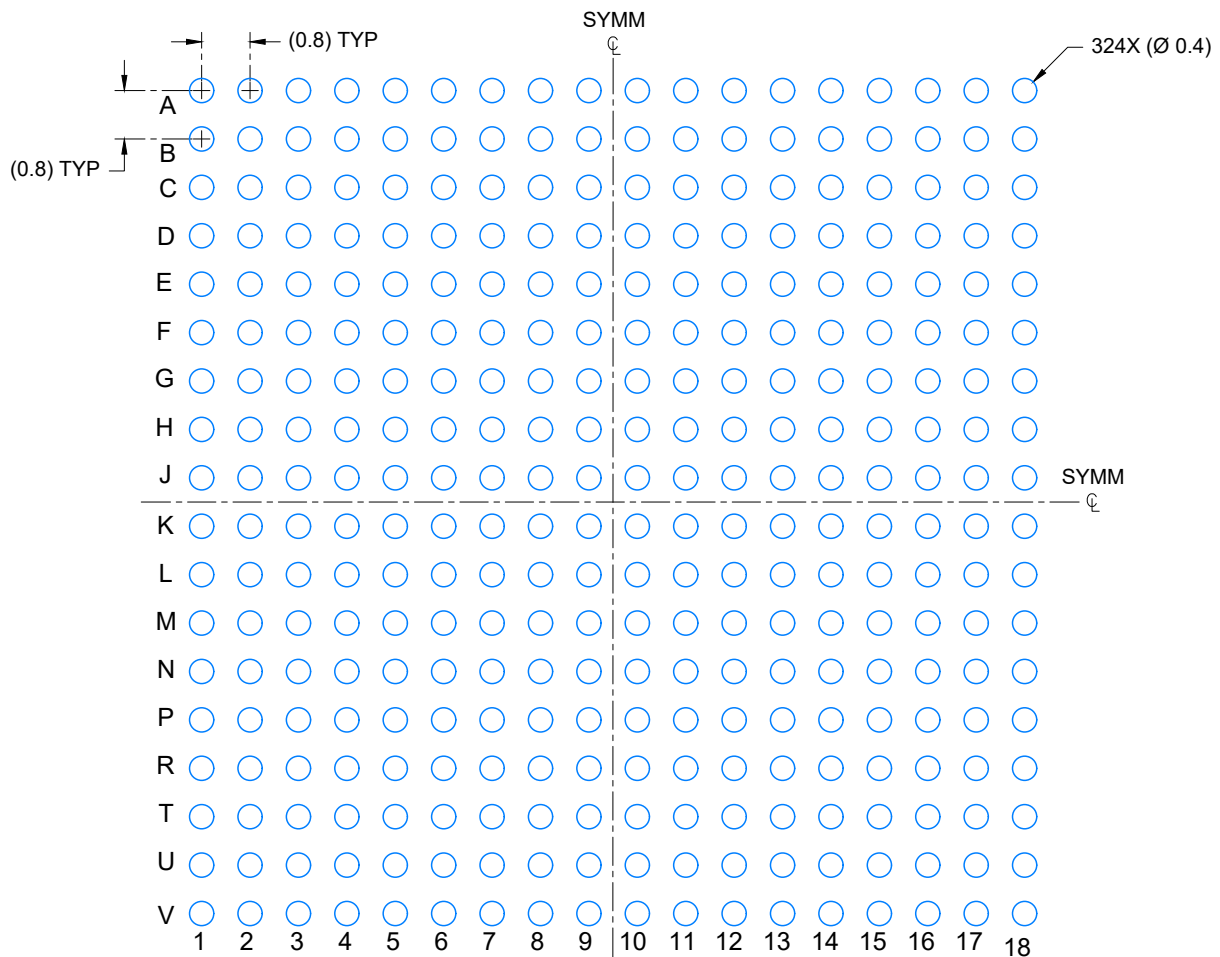


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## NOTES:

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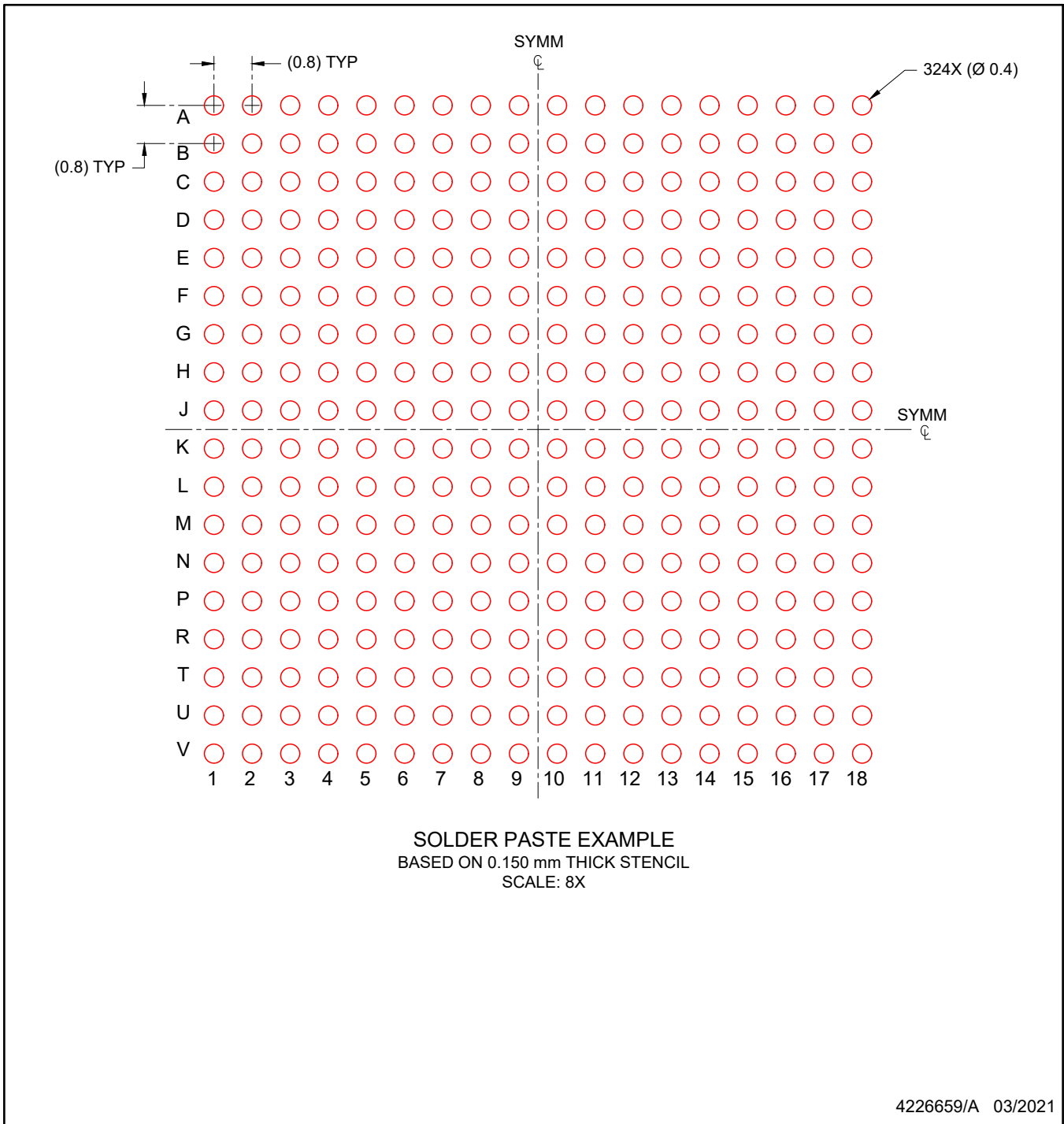
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



4226659/A 03/2021

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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