

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	MP33AB01TR
Manufacturer:	STMicroelectronics
Package:	Tape & Reel (TR)
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/stmicroelectronics/mp33ab01tr.html>

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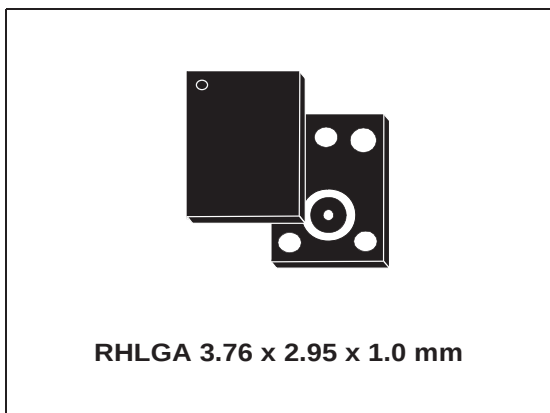
Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

MEMS audio surface-mount bottom-port silicon microphone with analog output

Datasheet - production data



Description

The MP33AB01 is a compact, low-power microphone built with a low-profile sensing element.

The sensing element, capable of detecting acoustic waves, is manufactured using a specialized silicon micromachining process to produce audio sensors.

The MP33AB01 has an acoustic overload point of 125 dB SPL with a 63 dB signal-to-noise ratio.

The MP33AB01 is available in a package compliant with reflow soldering and is guaranteed to operate over an extended temperature range from -30 °C to +100 °C.

Features

- Single supply voltage
- Low power consumption
- Omnidirectional sensitivity
- High signal-to-noise ratio
- High bandwidth
- Package compliant with reflow soldering

Table 1. Device summary

Order code	Temperature range [°C]	Package	Packing
MP33AB01	-30 to +100	RHLGA (3.76 x 2.95 x 1.0) mm	Tray
MP33AB01TR	-30 to +100	RHLGA (3.76 x 2.95 x 1.0) mm	Tape and reel

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1 Pin description

Figure 1. Pin connections

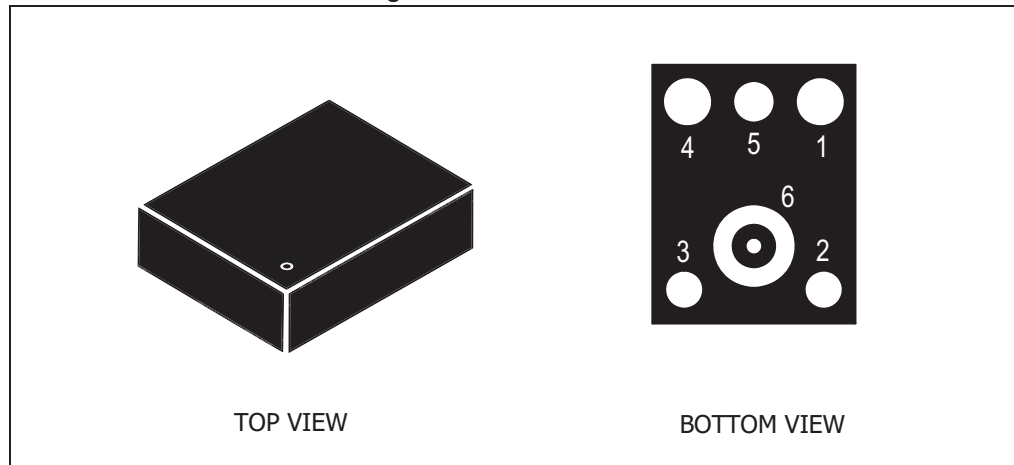


Table 2. Pin description

Pin #	Pin name	Function
1	Output	Analog output
2	GND	0 V supply
3	GND	0 V supply
4	Vdd	Power supply
5	GND	0 V supply
6	GND	0 V supply

2 Acoustic and electrical specifications

2.1 Acoustic and electrical characteristics

The values listed in the table below are specified for $V_{dd} = 2.2 \text{ V}$ unless otherwise noted.

Table 3. Acoustic and electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ. ⁽¹⁾	Max.	Unit
Vdd	Supply voltage		1.5	2.2	3.6	V
Idd	Current consumption	mean value = 2 V			0.25	mA
FR	Frequency range		100		10000	Hz
So	Sensitivity	at 1 kHz (0 dB = 1 V/Pa)	-41	-38	-35	dBV
SNR	Signal-to-noise ratio	at 1 kHz (0 dB = 1 V/Pa)		63		dB
Top	Operating temperature range		-30		+100	°C

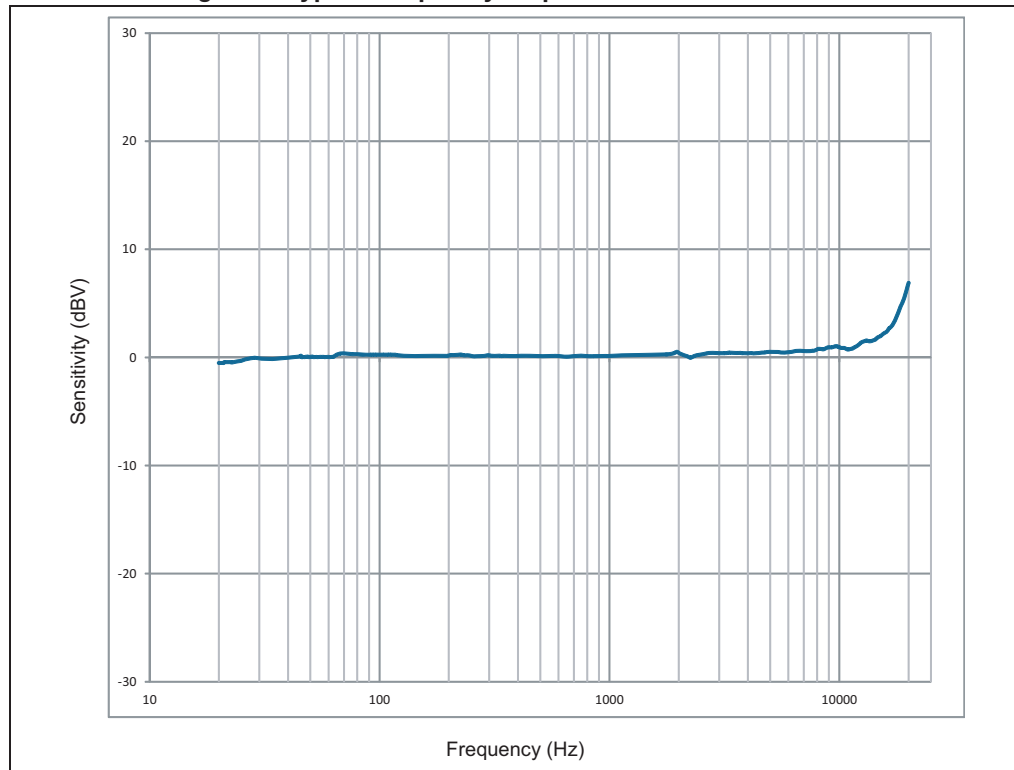
1. Typical specifications are not guaranteed.

Table 4. Distortion specifications at 1 kHz

Parameter	Test condition	Value
Distortion	94 dBSPL	< 1% THD
Distortion	125 dBSPL	10% THD (typ.)

2.2 Frequency response

Figure 2. Typical frequency response normalized at 1 kHz



3 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.5 to 4	V
T _{STG}	Storage temperature range	-40 to +100	°C



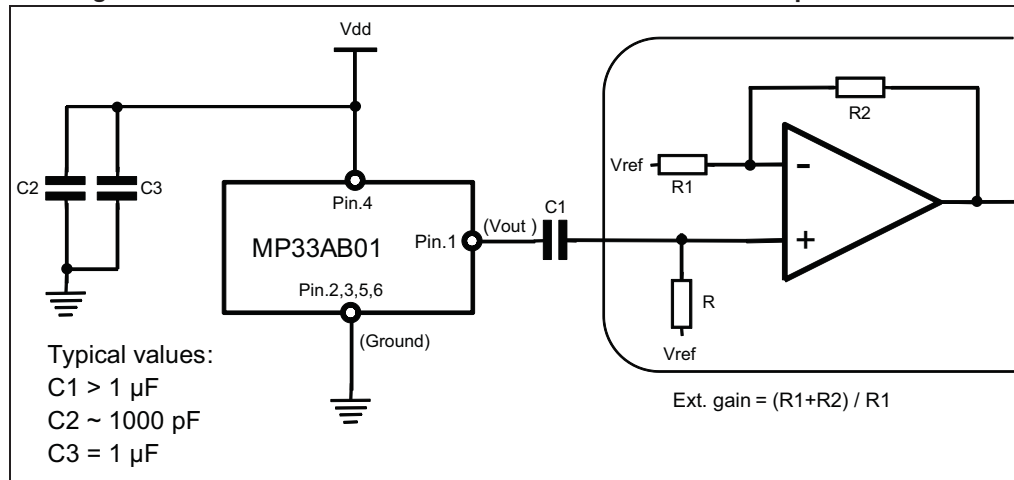
This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is ESD-sensitive, improper handling can cause permanent damage to the part.

4 Application recommendations

Figure 3. MP33AB01 electrical connections and external component values



The DC-blocking capacitor C1 is required on the Vout pin as shown in [Figure 3](#). The C1 value and the input resistance of the interface circuit (R) affect the cut-off frequency of the Audio signal path as:

$$3 \text{ dB cut-off freq} = 1 / 2\pi RC1$$

It's advisable to have a cut-off frequency well below 20 HZ, so for a typical input resistance of about 20 k Ω it is recommended to use a C1 > 1 μF .

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Soldering information

The RHLGA (3.76 x 2.95) mm package is also compliant with the RoHS and “Green” standards and is qualified for soldering heat resistance according to JEDEC J-STD-020.

Land pattern and soldering recommendations are available at www.st.com.

Figure 4. Recommended soldering profile limits

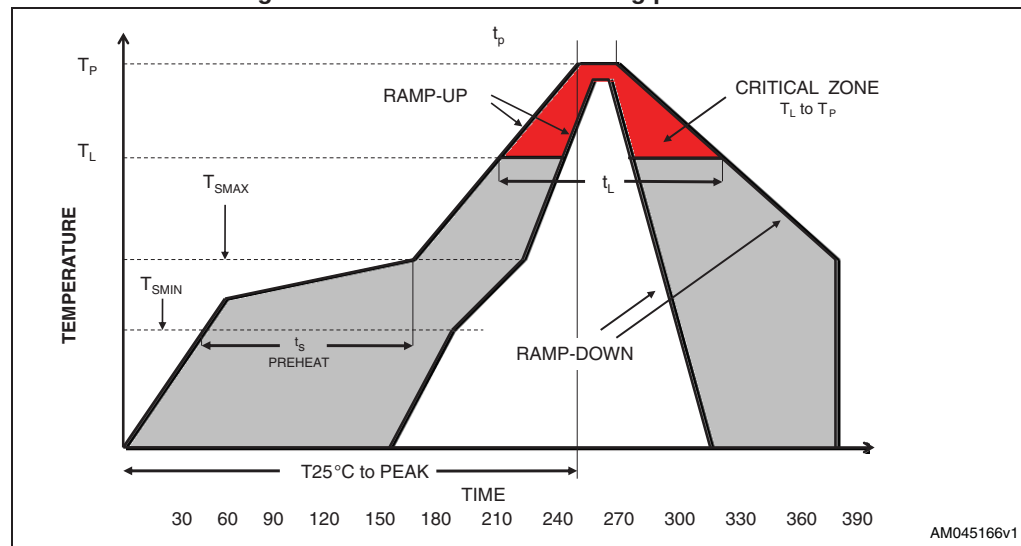


Table 6. Recommended soldering profile limits

Description	Parameter	Pb free
Average ramp rate	T_L to T_P	3 °C/sec max
Preheat		
Minimum temperature	T_{SMIN}	150 °C
Maximum temperature	T_{SMAX}	200 °C
Time (T_{SMIN} to T_{SMAX})	t_s	60 sec to 120 sec
Ramp-up rate	T_{SMAX} to T_L	
Time maintained above liquidous temperature	t_L	60 sec to 150 sec
Liquidous temperature	T_L	217 °C
Peak temperature	T_P	260 °C max
Time within 5 °C of actual peak temperature		20 sec to 40 sec
Ramp-down rate		6 °C/sec max
Time 25 °C ($t_{25\text{ °C}}$) to peak temperature		8 minutes max

Figure 5. RHLGA 3.76 mm x 2.95 mm x 1.0 mm package outline

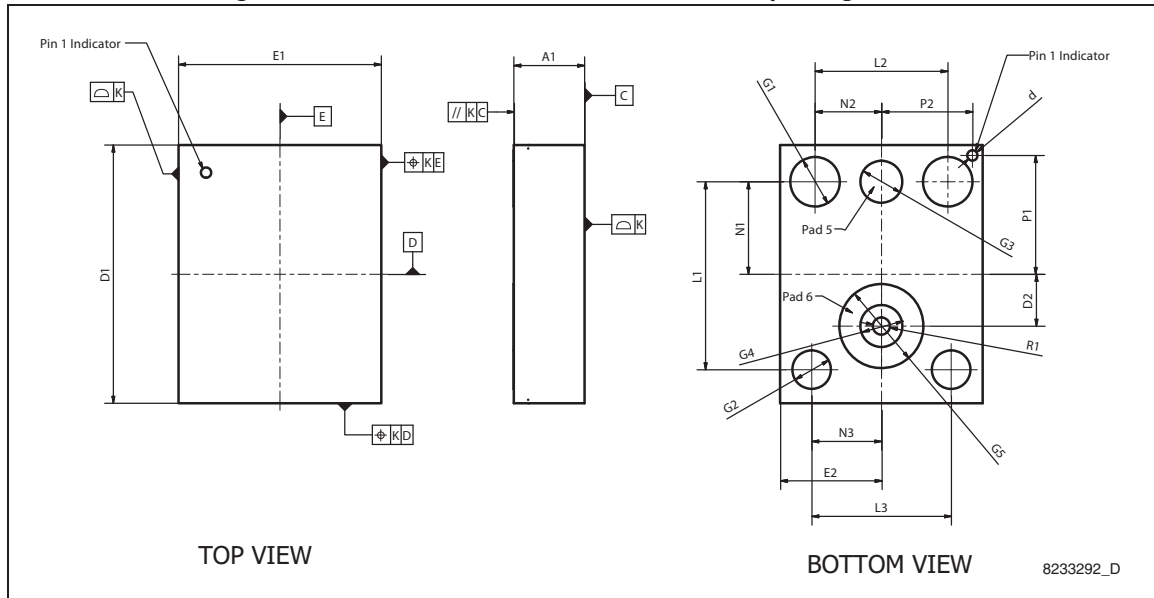


Table 7. RHLGA 3.76 mm x 2.95 mm x 1.0 mm package dimensions

Symbol	mm			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A1	0.900	1.000	1.100	0.0354	0.0394	0.0433
D1	3.660	3.760	3.860	0.1441	0.1480	0.1520
D2	0.600	0.750	0.900	0.0236	0.0295	0.0354
R1	0.200	0.250	0.300	0.0079	0.0098	0.0118
E1	2.850	2.950	3.050	0.1122	0.1161	0.1201
E2	1.325	1.475	1.625	0.0522	0.0581	0.0640
L1	2.690	2.740	2.790	0.1059	0.1079	0.1098
L2	1.882	1.932	1.982	0.0741	0.0761	0.0780
L3	1.981	2.031	2.181	0.0780	0.0800	0.0859
N1	1.300	1.350	1.400	0.0512	0.0531	0.0551
N2	0.916	0.966	1.116	0.0361	0.0380	0.0440
N3	0.965	1.015	1.065	0.0380	0.0400	0.0419
G1	0.673	0.723	0.763	0.0265	0.0285	0.0300
G2	0.512	0.562	0.612	0.0202	0.0221	0.0241
G3	0.562	0.612	0.662	0.0221	0.0241	0.0261
G4	0.562	0.612	0.662	0.0221	0.0241	0.0261
G5	1.174	1.224	1.274	0.0462	0.0482	0.0502
P1	1.680	1.730	1.780	0.0661	0.0681	0.0701
P2	1.275	1.325	1.375	0.0502	0.0522	0.0541

Table 7. RHLGA 3.76 mm x 2.95 mm x 1.0 mm package dimensions (continued)

Symbol	mm			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
d		0.150			0.0059	
K		0.050			0.0020	

Figure 6. Device footprint and PCB land pattern

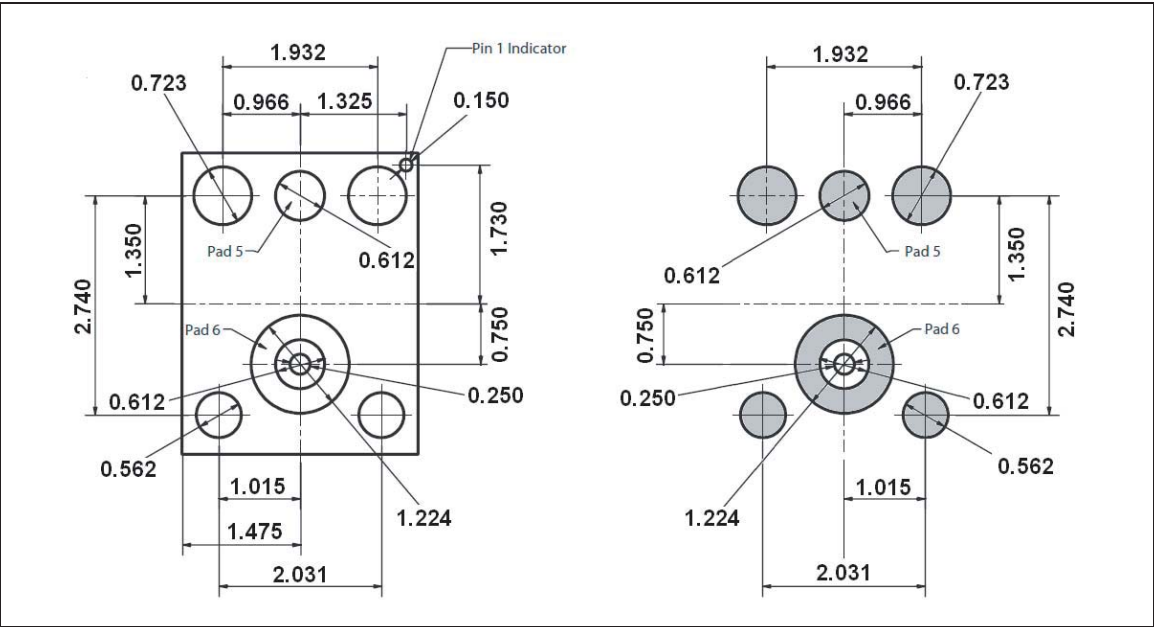
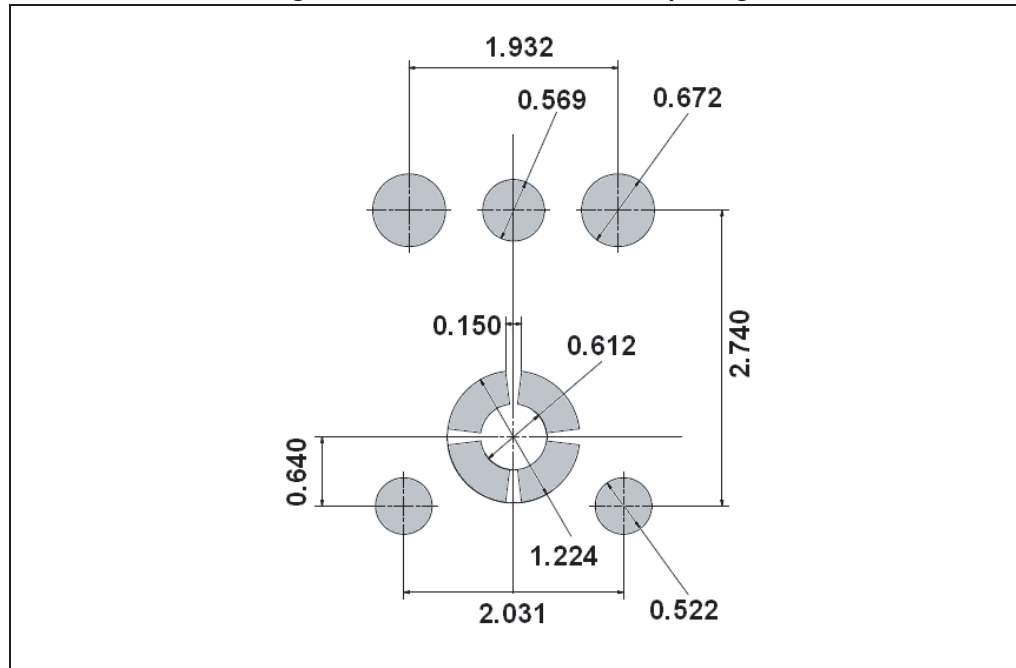


Figure 7. Recommended stencil openings



6 Revision history

Table 8. Document revision history

Date	Revision	Changes
17-Jan-2013	1	Initial release
13-Sep-2013	2	Modified Figure 3 on page 7

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