ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	SI52112-B6-GTR
Manufacturer:	Skyworks Solutions Inc.
Package:	8-TSSOP (0.173", 4.40mm Width)
Availability:	Please confirm with sales

Product Page:

https://antrexco.com/product/details/skyworks-solutions-inc/si52112-b6-gtr.html

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

Si52112-B5/B6

PCI-Express Gen 3 dual Output Clock Generator

Features

- PCI-Express Gen 1, Gen 2, and Gen 3 common clock compliant
- Gen 3 SRNS Compliant
- Low power HCSL differential output buffers
- Supports Serial-ATA (SATA) at 100 MHz
- No termination resistors required
- 25 MHz Crystal Input or Clock input
- Triangular spread spectrum profile for maximum EMI reduction (Si52112-B6)
- Extended Temperature: –40 to 85 °C
- 3.3 V Power supply
- Small packages:
  - 8-pin TDFN (1.4 x 1.6 mm)
  - 10-pin TDFN (3 x 3 mm)
- Si52112-B5 does not support spread spectrum outputs
- Si52112-B6 supports 0.5% down spread outputs

Ordering Information:
See page 13

Patents pending

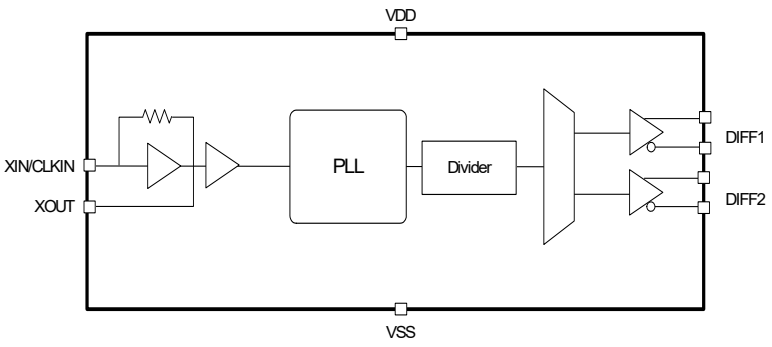
Applications

- Network attached storage
- Multi-function printer
- PCIe Add-on Cards
- Network Interface Cards
- Docking Stations
- Wireless access point
- Routers
- Digital Still Cameras
- Digital Video Cameras

Description

Si52112-B5/B6 is a high-performance, PCIe clock generator that can source two PCIe clocks from a 25 MHz crystal or clock input. The clock outputs are compliant to PCIe Gen 1, Gen 2, Gen 3 common clock, and Gen 3 SRNS specifications. The ultra-small footprint (1.4 x 1.6 mm) and industry leading low power consumption make Si52112-B5/B6 the ideal clock solution for applications with tight board space constraints. Measuring PCIe clock jitter is quick and easy with the Skyworks Solutions PCIe Clock Jitter Tool. Download it for free at https://www.skyworksinc.com/en/Application-Pages/pcie-clock-jitter-tool.

Functional Block Diagram



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1. Electrical Specifications

Table 1. DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	3.3 V ± 5%	3.13	3.30	3.46	V
Operating Supply Current	I_{DD}	Full Active	—	—	17	mA
Input Pin Capacitance	C_{IN}	Input Pin Capacitance	—	3	5	pF
Output Pin Capacitance	C_{OUT}	Output Pin Capacitance	—	—	5	pF

Table 2. AC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal						
Long-term Accuracy	L_{ACC}	Measured at $V_{DD}/2$ differential	—	—	250	ppm
Clock Input						
CLKIN Duty Cycle	T_{DC}	Measured at $V_{DD}/2$	45	—	55	%
CLKIN Rise and Fall Times	T_R/T_F	Measured between 0.2 V_{DD} and 0.8 V_{DD}	0.5	—	4.0	V/ns
CLKIN Cycle-to-Cycle Jitter	T_{CCJ}	Measured at $V_{DD}/2$	—	—	250	ps
CLKIN Long Term Jitter	T_{LTJ}	Measured at $V_{DD}/2$	—	—	350	ps
Input High Voltage	V_{IH}	XIN/CLKIN pin	2	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	XIN/CLKIN pin	—	—	0.8	V
Input High Current	I_{IH}	XIN/CLKIN pin, VIN = V_{DD}	—	—	35	µA
Input Low Current	I_{IL}	XIN/CLKIN pin, 0 < VIN <0.8	–35	—	—	µA
HCSL Clocks						
Duty Cycle	T_{DC}	Measured at 0 V differential	45	—	55	%
Output-to-Output Skew	T_{SKEW}	Measured at 0 V differential	—	—	60	ps
Output Frequency	F_{OUT}		—	100	—	MHz
Frequency Accuracy	F_{ACC}	All output clocks	—	—	100	ppm
Slew Rate	T_R/T_F	Measured differentially from ±150 mV	0.6	—	4.0	V/ns
Cycle-to-Cycle Jitter	T_{CCJ}	Measured at 0 V differential	—	28	70	ps
PCIe Gen 1 Pk-Pk Jitter, Common Clock	$Pk\text{-}Pk_{GEN1}$	PCIe Gen 1	—	24	86	ps
PCIe Gen 2 Phase Jitter, Common Clock	RMS_{GEN2}	10 kHz < F < 1.5 MHz	—	1.35	3.0	ps
		1.5 MHz < F < Nyquist	—	1.4	3.1	ps

Notes:
1. Visit www.pcisig.com for complete PCIe specifications.
2. Download the Skyworks Solutions PCIe Clock Jitter Tool at https://www.skyworksinc.com/en/Application-Pages/pcie-clock-jitter-tool.

Table 2. AC Electrical Specifications (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PCIe Gen 3 Phase Jitter, Common Clock	RMS_{GEN3}	PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	—	0.4	0.7	ps
PCIe Gen 3 Phase Jitter, Separate Reference No Spread, SRNS	RMS_{GEN3_SRNS}	PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	—	0.28	0.71	ps
Crossing Point Voltage	V_{OX}		300	—	550	mV
Voltage High	V_{HIGH}		—	—	1.15	V
Voltage Low	V_{LOW}		–0.3	—	—	V
Spread Range	S_{RNG}	Down Spread, -B6 only	—	–0.5	—	%
Modulation Frequency	F_{MOD}	-B6 only	30	31.5	33	kHz
Enable/Disable and Set-up						
Clock Stabilization from Power-up	T_{STABLE}		—	—	3	ms
Stopclock Set-up Time	T_{SS}		10.0	—	—	ns

Notes:
1. Visit www.pcisig.com for complete PCIe specifications.
2. Download the Skyworks Solutions PCIe Clock Jitter Tool at https://www.skyworksinc.com/en/Application-Pages/pcie-clock-jitter-tool.

Table 3. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature, Storage	T_S	Non-functional	–65	—	150	°C
Temperature, Operating Ambient	T_A	Functional	–40	—	85	°C
Temperature, Junction	T_J	Functional	—	—	125	°C
Dissipation, Junction to Case (8-TDFN)	$Ø_{JC}$	JEDEC (JESD 51) (2-Layers)	—	—	98.8	°C
Dissipation, Junction to Case (10-TDFN)	$Ø_{JC}$	JEDEC (JESD 51) (4-Layers)	—	—	38.3	°C/W
Dissipation, Junction to Case (TSSOP)	$Ø_{JC}$	JEDEC (JESD 51)	—	—	37.0	°C/W
Dissipation, Junction to Ambient (8-TDFN)	$Ø_{JA}$	JEDEC (JESD 51) (2-Layers)	—	—	170.8	°C
Dissipation, Junction to Ambient (10-TDFN)	$Ø_{JA}$	JEDEC (JESD 51) (4-Layers)	—	—	90.4	°C/W
Dissipation, Junction to Ambient (TSSOP)	$Ø_{JA}$	JEDEC (JESD 51)	—	—	124.0	°C/W

Table 4. Absolute Maximum Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main Supply Voltage	$V_{DD\_3.3V}$		—	—	4.6	V
Input Voltage	V_{IN}	Relative to V_{SS}	–0.5	—	4.6	V_{DC}
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22 - A114)	2000	—	—	V
Flammability Rating	UL-94	UL (Class)		V–0		

Note: While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during powerup. Power supply sequencing is not required.

2. Crystal Recommendations

If using a crystal input, the device requires a parallel resonance crystal.

Table 5. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	ESR	Drive	Shunt Cap (max)	Motional (max)	Tolerance (max)	Stability (max)	Aging (max)
25 MHz	AT	Parallel	12–15 pF	<50 Ω	>150 µW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

2.1. Crystal Loading

Crystal loading is critical in achieving low ppm performance. To realize low ppm performance, use the total capacitance the crystal sees to calculate the appropriate capacitive loading (C_L).

Figure 1 shows a typical crystal configuration using two trim capacitors.

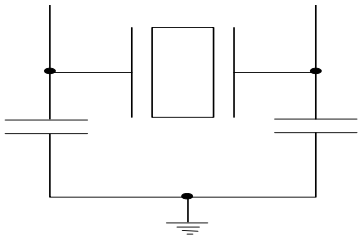

Figure 1. Crystal Capacitive Clarification

2.2. Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. The total capacitance on both sides is twice the specified crystal load capacitance (C_L). Trim capacitors are calculated to provide equal capacitive loading on both sides.

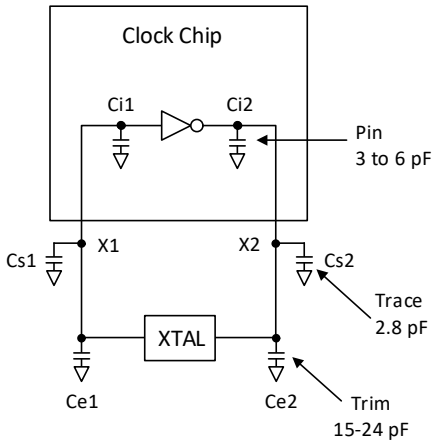

Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 \times CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

- CL: Crystal load capacitance
- CLe: Actual loading seen by crystal using standard value trim capacitors
- Ce: External trim capacitors
- Cs: Stray capacitance (terraced)
- Ci: Internal capacitance (lead frame, bond wires, etc.)

3. Test and Measurement Setup

Figures 3 through 5 show the test load configuration for the differential clock signals.

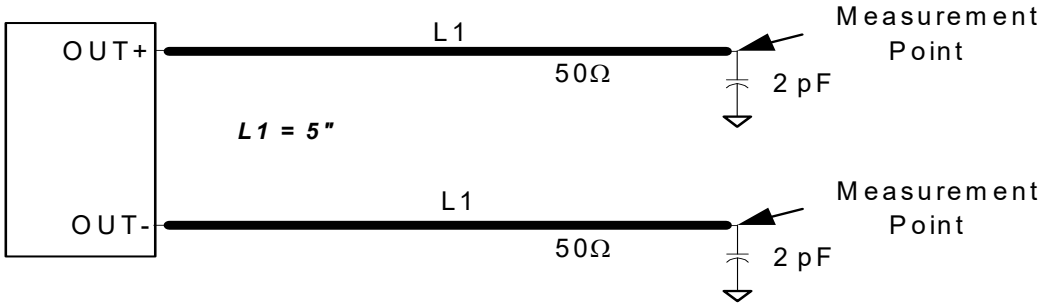

Figure 3. 0.7 V Differential Load Configuration

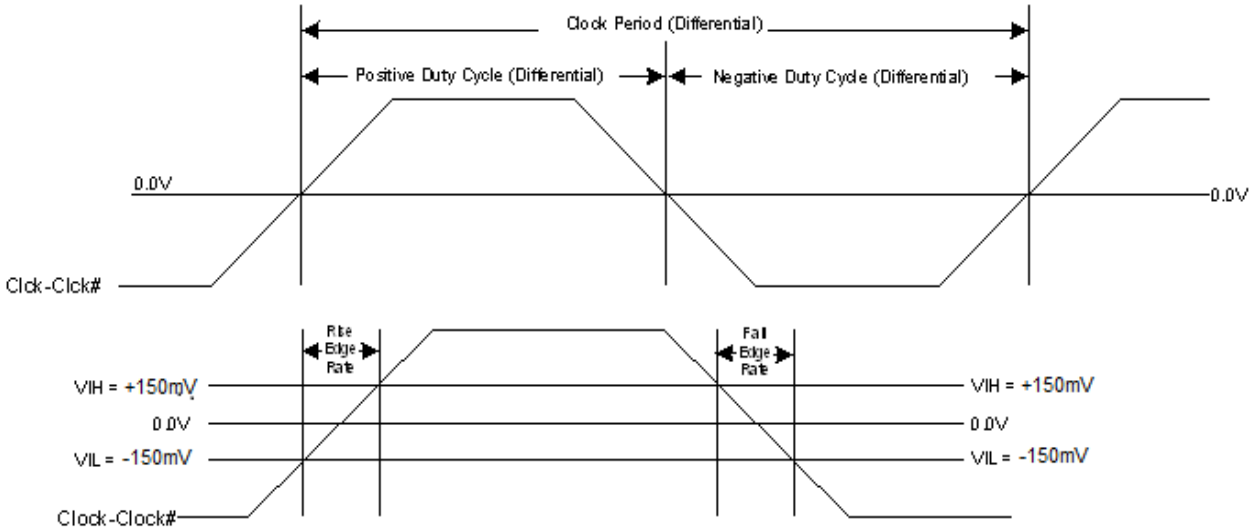

Figure 4. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

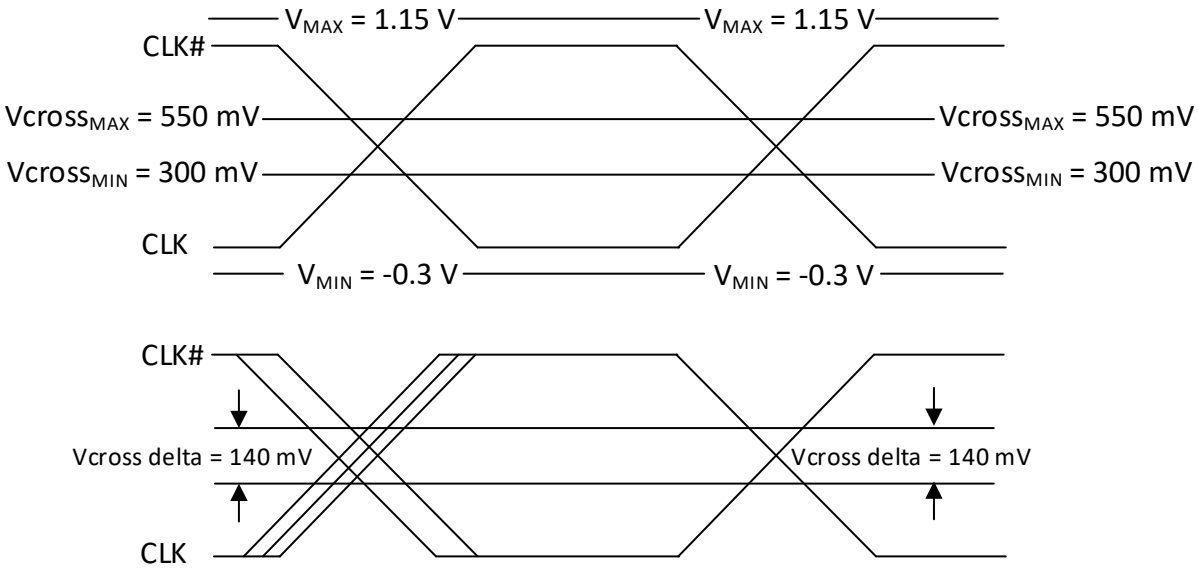

Figure 5. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

4. Pin Descriptions

4.1. 8-Pin TDFN

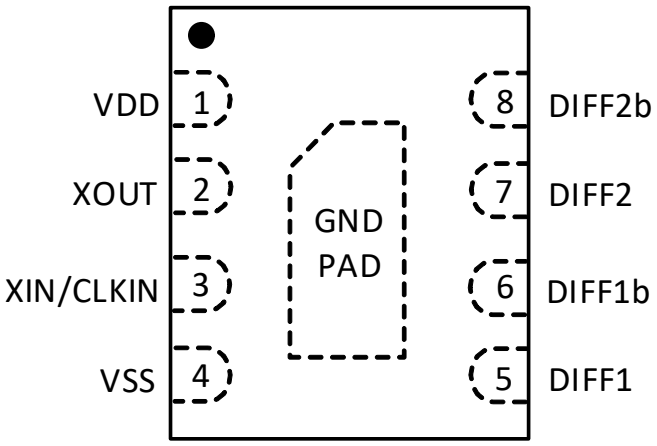

Figure 6. 8-Pin TDFN

Table 6. 8-Pin TDFN Descriptions

Pin #	Name	Type	Description
1	VDD	PWR	3.3 V Power supply.
2	XOUT	O	25.00 MHz crystal output, Float XOUT if using only CLKIN (clock input).
3	XIN/CLKIN	I	25.00 MHz crystal input or 3.3 V, 25 MHz clock Input.
4	VSS	GND	Ground.
5	DIFF1	O, DIF	HCSL DIFF_1, true
6	DIFF1b	O, DIF	HCSL DIFF_1, complementary
7	DIFF2	O, DIF	HCSL DIFF_2, true
8	DIFF2b	O, DIF	HCSL DIFF_2, complementary
	GND PAD	GND	Ground pad. This pad provides an electrical and thermal connection to ground and must be connected for proper operation. Add vias to an internal ground plane as close as possible to the part for optimal thermal dissipation.

4.2. 10-Pin TDFN

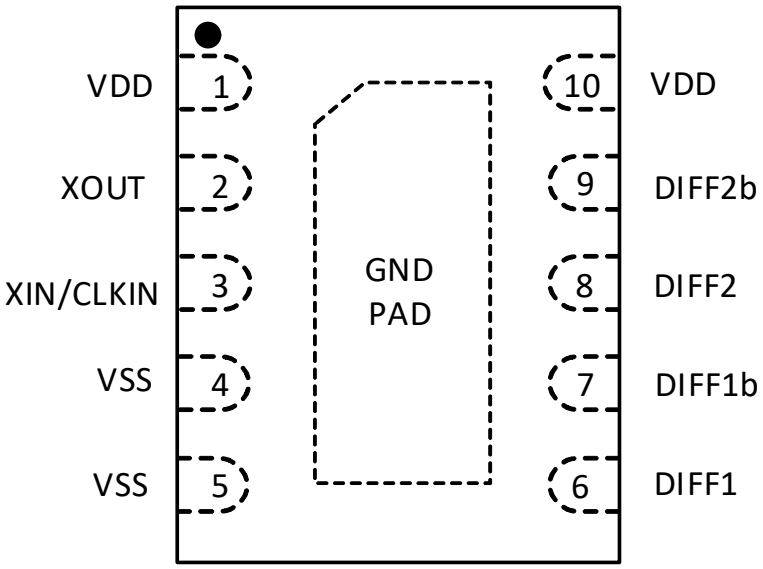

Figure 7. 10-Pin TDFN

Table 7. 10-Pin TDFN Descriptions

Pin #	Name	Type	Description
1	VDD	PWR	3.3 V power supply.
2	XOUT	O	25.00 MHz crystal output, Float XOUT if using only CLKIN (clock input).
3	XIN/CLKIN	I	25.00 MHz crystal input or 3.3 V, 25 MHz clock Input.
4	VSS	GND	Ground.
5	VSS	GND	Ground.
6	DIFF1	O, DIF	HCSL DIFF_1, true
7	DIFF1b	O, DIF	HCSL DIFF_1, complementary
8	DIFF2	O, DIF	HCSL DIFF_2, true
9	DIFF2b	O, DIF	HCSL DIFF_2, complementary
10	VDD	PWR	3.3 V power supply.
	GND PAD	GND	Ground pad. This pad provides an electrical and thermal connection to ground and must be connected for proper operation. Add vias to an internal ground plane as close as possible to the part for optimal thermal dissipation.

4.3. 8-Pin TSSOP

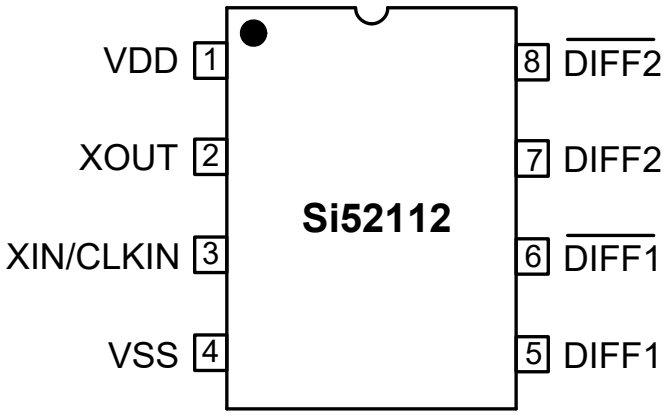

Figure 8. 8-Pin TSSOP

Table 8. 8-Pin TSSOP Descriptions

Pin #	Name	Type	Description
1	VDD	PWR	3.3 V Power supply.
2	XOUT	O	25.00 MHz crystal output, Float XOUT if using only CLKIN (clock input).
3	XIN/CLKIN	I	25.00 MHz crystal input or 3.3 V, 25 MHz clock Input.
4	VSS	GND	Ground.
5	DIFF1	O, DIF	HCSL DIFF_1, true
6	$\overline{\text{DIFF1}}$	O, DIF	HCSL DIFF_1, complementary
7	DIFF2	O, DIF	HCSL DIFF_2, true
8	$\overline{\text{DIFF2}}$	O, DIF	HCSL DIFF_2, complementary

5. Ordering Guide

Part Number	Spread Option	Package Type	Temperature
Si52112-B5-GM2	No Spread	10-pin TDFN	Extended, –40 to 85 °C
Si52112-B5-GM2R	No Spread	10-pin TDFN—Tape and Reel	Extended, –40 to 85 °C
Si52112-B5-GM3	No Spread	8-pin TDFN	Extended, –40 to 85 °C
Si52112-B5-GM3R	No Spread	8-pin TDFN—Tape and Reel	Extended, –40 to 85 °C
Si52112-B5-GT	No Spread	8-pin TSSOP	Extended, –40 to 85 °C
Si52112-B5-GTR	No Spread	8-pin TSSOP - Tape and Reel	Extended, –40 to 85 °C
Si52112-B6-GM3	–0.5% Spread	8-pin TDFN	Extended, –40 to 85 °C
Si52112-B6-GM3R	–0.5% Spread	8-pin TDFN—Tape and Reel	Extended, –40 to 85 °C
Si52112-B6-GM2	–0.5% Spread	10-pin TDFN	Extended, –40 to 85 °C
Si52112-B6-GM2R	–0.5% Spread	10-pin TDFN—Tape and Reel	Extended, –40 to 85 °C
Si52112-B6-GT	–0.5% Spread	8-pin TSSOP	Extended, –40 to 85 °C
Si52112-B6-GTR	–0.5% Spread	8-pin TSSOP - Tape and Reel	Extended, –40 to 85 °C

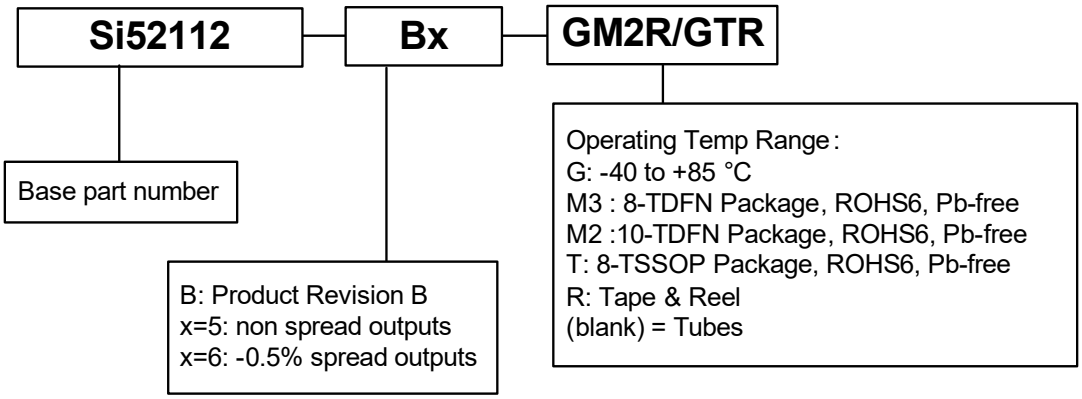

Figure 9. Ordering Information

6. Package Outlines

6.1. 8-Pin TDFN Package

Figure 10 illustrates the package details for the 8-pin TDFN. Table 9 lists the values for the dimensions shown in the illustration.

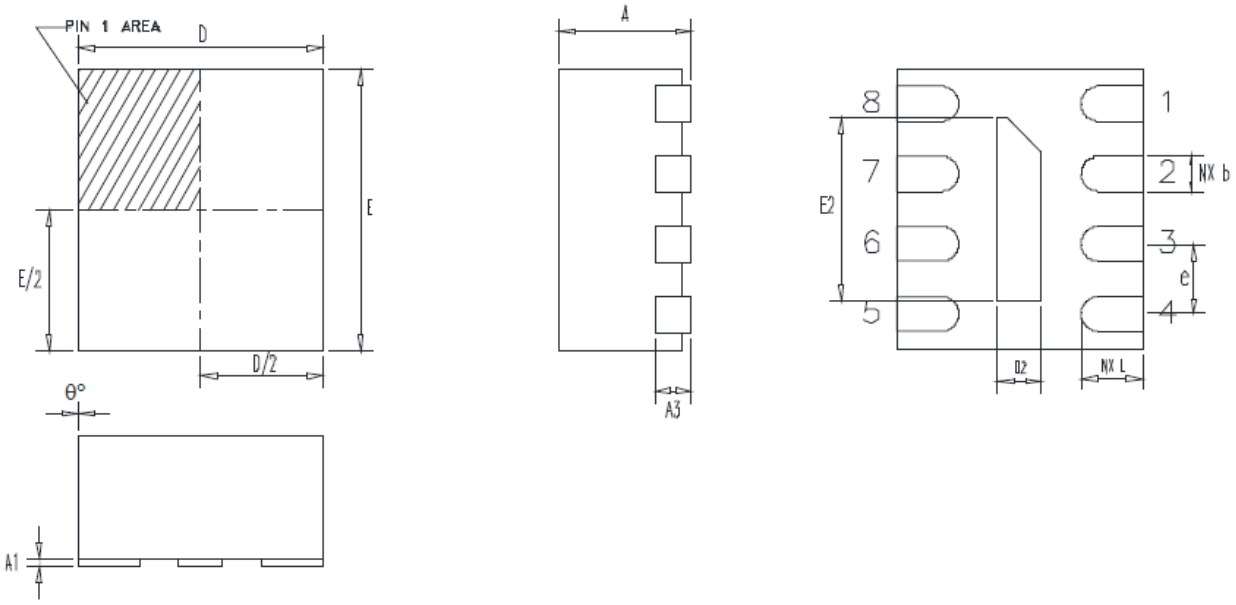

Figure 10. 8-Pin TDFN Package Drawing

Table 9. 8-Pin TDFN Package Diagram Dimensions

Dimension	mm		mils	
Symbol	**Min**	**Max**	**Min**	**Max**
A	0.70	0.80	27.56	31.50
A1	0	0.05	0	1.97
A3	0.175	0.225	6.89	8.86
D	1.3	1.5	51.18	59.06
E	1.5	1.7	59.06	66.93
D2	0.20	0.30	7.87	11.81
E2	1.0	1.1	39.37	43.31
e	0.4 BSC		15.75 BSC	
NX b	0.15	0.25	5.91	9.84
NC L	0.25	0.45	9.84	17.72
0°	0°	4°	0°	4°
ND	0			
NE	4			

Notes:

1. Spade width, lead width and lead thickness exclusive of solder plate.
2. Package outline exclusive of mold flashes and burr dimensions.
3. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall not exceed 0.08 mm.
4. Warpage shall not exceed 0.10 mm.
5. The Terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of Terminal #1 identifier are optional, but must be located within the zone indicated. The Terminal #1 identifier may be either a mold or marked feature.
6. ND and NE refer to the number of terminals on each D and E side respectively.

6.2. 10-Pin TDFN Package

Figure 11 illustrates the package details for the 10-pin TDFN. Table 10 lists the values for the dimensions shown in the illustration.

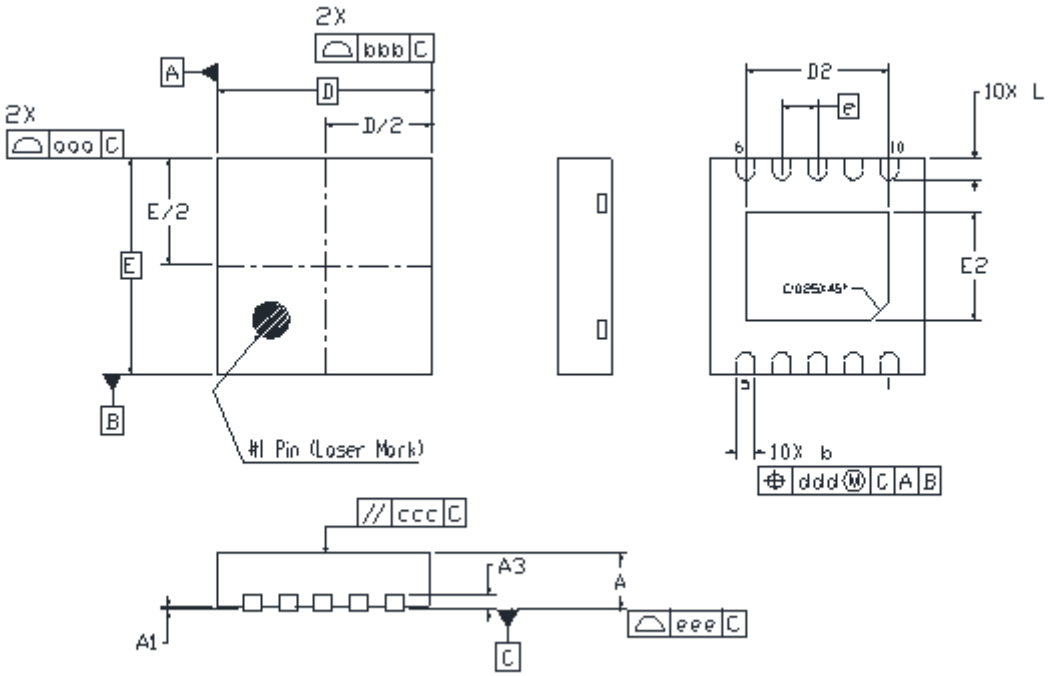

Figure 11. 10-Pin TDFN Package Drawing

Table 10. TDFN Package Diagram Dimensions

Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D		3.00 BSC.	
D2	1.90	2.00	2.10
e		0.50 BSC	
E		3.00 BSC	
E2	1.40	1.50	1.60
L	0.25	0.30	0.35
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.10	
eee		0.08	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
4. This drawing conforms to the JEDEC Solid State Outline MO-229.

6.3. TSSOP Package

Figure 12 illustrates the package details for the 8-pin TSSOP. Table 11 lists the values for the dimensions shown in the illustration.

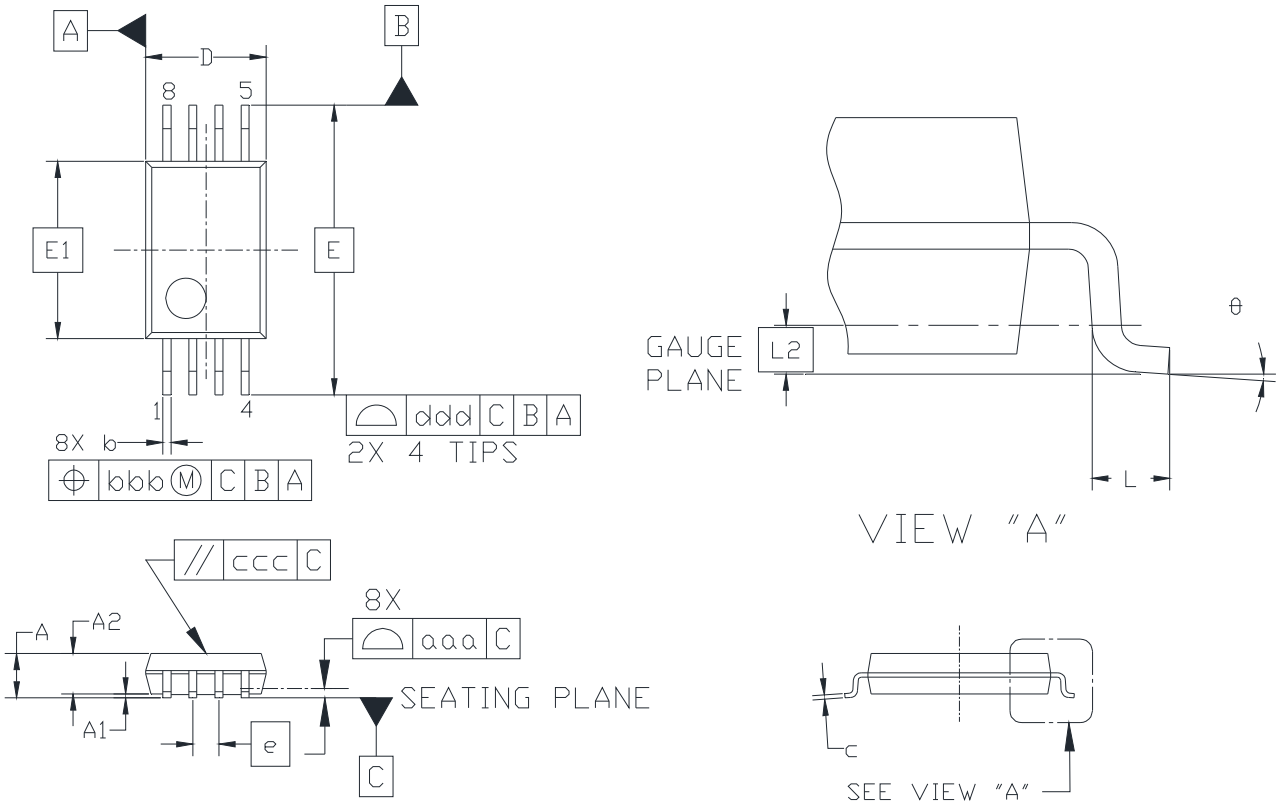

Figure 12. 8-Pin TSSOP Package Drawing

Table 11. TSSOP Package Diagram Dimensions

Symbol	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	0.90	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	2.90	3.00	3.10
E	6.40 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L2	0.25 BSC		
θ	0°	—	8°
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-153, Variation AA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7. Recommended Design Guideline

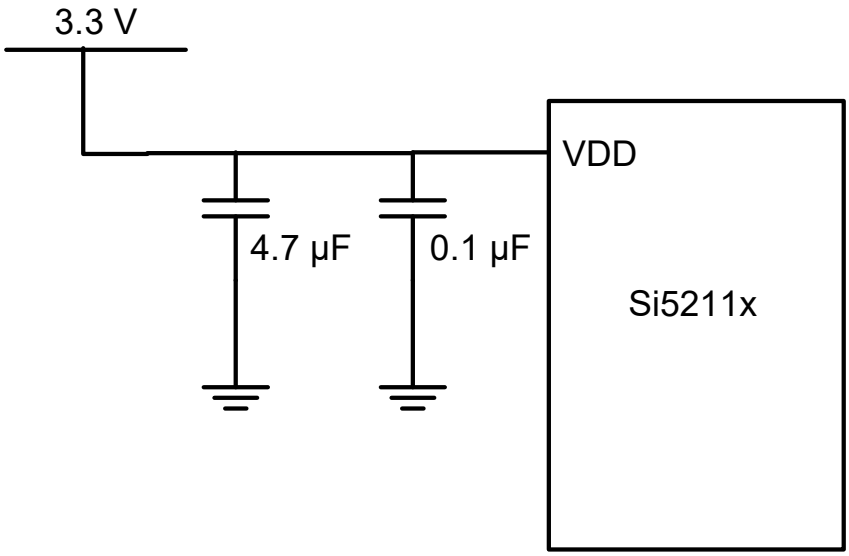

Figure 13. Recommended Power Supply Filtering

Revision History

Revision 1.3

March, 2020

- Added 8-pin TDFN in " Features" on page 1.
- Updated " Applications" on page 1.
- Updated Table 1, “Recommended Operating Conditions,” on page 3.
  - Removed commercial supply voltage spec.
- Updated Table 1, “DC Electrical Specifications,” on page 3.
  - Updated operating voltage spec test condition.
- Updated Table 2, “AC Electrical Specifications,” on page 3.
  - Updated PCIe Gen 3 Phase Jitter, Common Clock max from 1ps to 0.7 ps.
- Added "4.1. 8-Pin TDFN" on page 10.
- Updated "4.2. 10-Pin TDFN" on page 11.
  - Added GND PAD to Pin Descriptions.
- Updated "5. Ordering Guide" on page 13.
  - Added orderable part numbers for 8-Pin TDFN.
- Updated "6.1. 8-Pin TDFN Package" on page 14.

Revision 1.2

November, 2014

- Updated Features on page 1.
- Updated Description on page 1.
- Updated Table 2, “AC Electrical Specifications,” on page 3.

Revision 1.1

July, 2014

- Added “4.3. 8-Pin TSSOP” pin description on page 12.

Revision 1.0

April, 2013

- Initial release.

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