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Electronic Components Sourcing Information

Product Reference Information

Part Number: EFM8BB31F32I-C-QFN24R
Manufacturer: Silicon Labs
Package: 24-VFQFN Exposed Pad
Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/silicon-labs/efm8bb31f32i-c-qfn24r.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

EFM8 Busy Bee Family

EFM8BB3 Data Sheet

The EFM8BB3, part of the Busy Bee family of MCUs, is a performance line of 8-bit microcontrollers with a comprehensive analog and digital feature set in small packages.

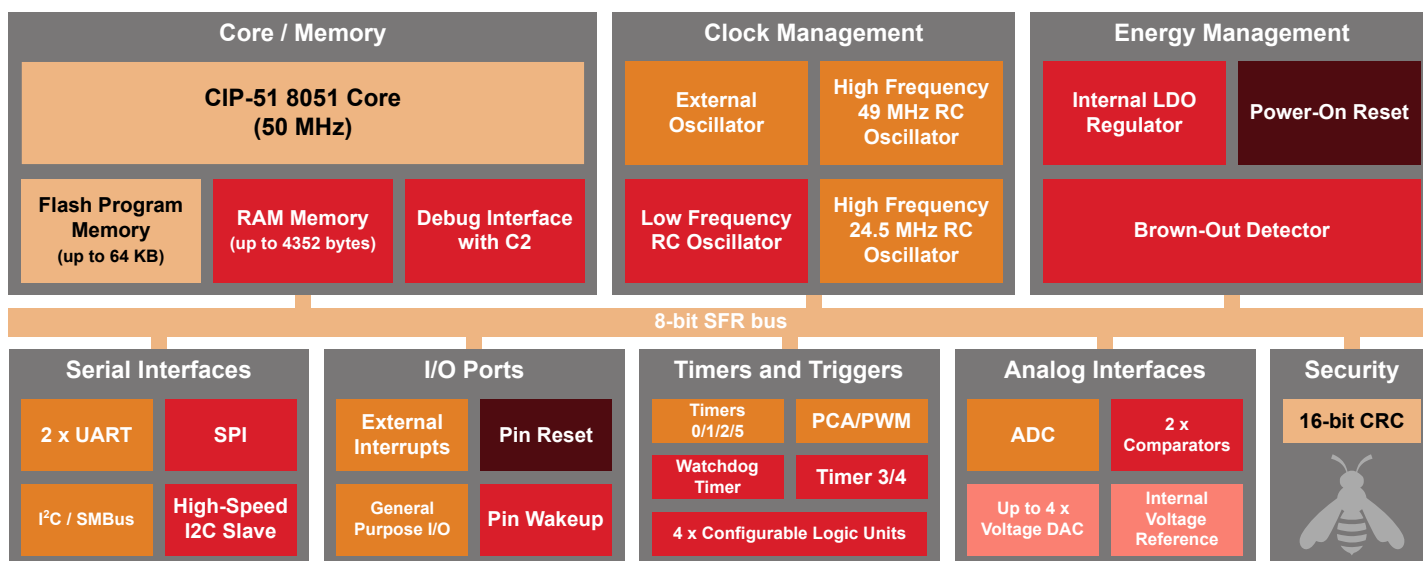
These devices offer state-of-the-art performance by integrating 12-bit ADC, internal temperature sensor, and up to four 12-bit DACs into small packages, making them ideal for general purpose applications. With an efficient, pipelined 8051 core with maximum operating frequency at 50 MHz, various communication interfaces, and four channels of configurable logic, the EFM8BB3 family is optimal for many embedded applications.

EFM8BB3 applications include the following:

- Consumer electronics
- Precision instrumentation
- Power management and control
- Industrial control and automation
- Smart sensors
- Automotive control

KEY FEATURES

- Pipelined 8-bit 8051 MCU Core with 50 MHz operating frequency
- Up to 29 multifunction I/O pins
- One 12-bit/10-bit ADC
- Four 12-bit DACs with synchronization and PWM capabilities
- Two low-current analog comparators with built-in reference DACs
- Internal temperature sensor
- Internal 49 MHz and 24.5 MHz oscillators accurate to $\pm 2\%$
- Four channels of Configurable Logic
- 6-channel PWM / PCA
- Six 16-bit general-purpose timers



Lowest power mode with peripheral operational:

Normal
 Idle
 Suspend
 Snooze
 Shutdown

1. Feature List

The EFM8BB3 device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below.

- Core:
 - Pipelined CIP-51 Core
 - Fully compatible with standard 8051 instruction set
 - 70% of instructions execute in 1-2 clock cycles
 - 50 MHz maximum operating frequency
- Memory:
 - Up to 64 kB flash memory (63 kB user-accessible), in-system re-programmable from firmware in 512-byte sectors
 - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
 - Internal LDO regulator for CPU core voltage
 - Power-on reset circuit and brownout detectors
- I/O: Up to 29 total multifunction I/O pins:
 - Up to 25 pins 5 V tolerant under bias
 - Selectable state retention through reset events
 - Flexible peripheral crossbar for peripheral routing
 - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
 - Internal 49 MHz oscillator with accuracy of $\pm 2\%$
 - Internal 24.5 MHz oscillator with $\pm 2\%$ accuracy
 - Internal 80 kHz low-frequency oscillator
 - External CMOS clock option (up to 25 MHz)
 - External crystal/RC oscillator option up to 25 MHz
- Analog:
 - 12/10-Bit Analog-to-Digital Converter (ADC)
 - Internal temperature sensor
 - 4 x 12-Bit Digital-to-Analog Converters (DAC)
 - 2 x Low-current analog comparators with adjustable reference
- Communications and Digital Peripherals:
 - 2 x UART, up to 3 Mbaud
 - SPI™ Master / Slave, up to 12 Mbps
 - SMBus™/I2C™ Master / Slave, up to 400 kbps
 - I2C High-Speed Slave, up to 3.4 Mbps
 - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
 - 4 Configurable Logic Units
- Timers/Counters and PWM:
 - 6-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes
 - 6 x 16-bit general-purpose timers
 - Independent watchdog timer, clocked from the low frequency oscillator
- On-Chip, Non-Intrusive Debugging
 - Full memory and register inspection
 - Four hardware breakpoints, single-stepping
- Pre-programmed UART bootloader
- Temperature range -40 to 85 °C or -40 to 125 °C
 - Available in commercial, industrial, and automotive variants

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB3 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Device operation is specified from 2.2 V up to a 3.6 V supply. Devices are AEC-Q100 qualified. Both G-grade and I-grade devices are available in 4x4 mm 32-pin QFN, 3x3 mm 24-pin QFN, 32-pin QFP, or 24-pin QSOP packages. A-grade and additional I-grade devices are available in 5x5 mm 32-pin QFN and 4x4 mm 24-pin QFN packages. All package options are lead-free and RoHS compliant.

2. Ordering Information

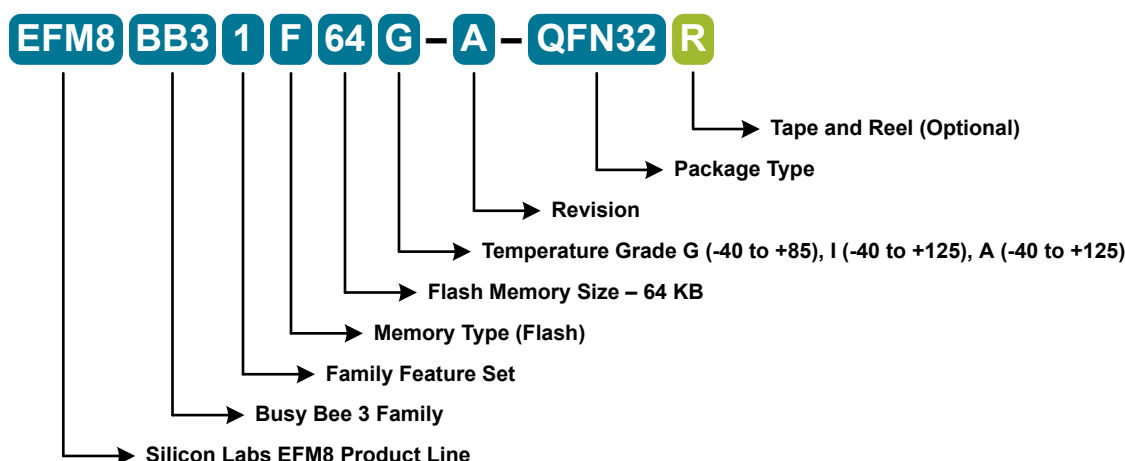


Figure 2.1. EFM8BB3 Part Numbering

All EFM8BB3 family members have the following features:

- CIP-51 Core running up to 49 MHz
- Three Internal Oscillators (49 MHz, 24.5 MHz and 80 kHz)
- SMBus
- I2C Slave
- SPI
- 2 UARTs
- 6-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- Six 16-bit Timers
- Four Configurable Logic Units
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, temperature sensor, channel sequencer, and direct-to-VRAM data transfer
- Two Analog Comparators
- 16-bit CRC Unit
- AEC-Q100 qualified
- Pre-loaded UART bootloader

In addition to these features, each part number in the EFM8BB3 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Voltage DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Package
EFM8BB31F64G-D-QFN32	64	4352	29	4	20	10	9	Yes	QFN32-GI
EFM8BB31F64G-D-QFP32	64	4352	28	4	20	10	9	Yes	QFP32
EFM8BB31F64G-D-QFN24	64	4352	20	4	12	6	6	Yes	QFN24-GI

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Voltage DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Package
EFM8BB31F64G-D-QSOP24 ¹	64	4352	21	4	13	6	7	Yes	QSOP24
EFM8BB31F32G-D-QFN32	32	2304	29	2 ²	20	10	9	Yes	QFN32-GI
EFM8BB31F32G-D-QFP32	32	2304	28	2 ²	20	10	9	Yes	QFP32
EFM8BB31F32G-D-QFN24	32	2304	20	2 ²	12	6	6	Yes	QFN24-GI
EFM8BB31F32G-D-QSOP24 ¹	32	2304	21	2 ²	13	6	7	Yes	QSOP24
EFM8BB31F16G-D-QFN32	16	2304	29	2 ²	20	10	9	Yes	QFN32-GI
EFM8BB31F16G-D-QFP32 ³	16	2304	28	2 ²	20	10	9	Yes	QFP32
EFM8BB31F16G-D-QFN24	16	2304	20	2 ²	12	6	6	Yes	QFN24-GI
EFM8BB31F16G-D-QSOP24 ¹	16	2304	21	2 ²	13	6	7	Yes	QSOP24
EFM8BB31F64I-D-QFN32	64	4352	29	4	20	10	9	Yes	QFN32-GI
EFM8BB31F64I-D-QFP32 ³	64	4352	28	4	20	10	9	Yes	QFP32
EFM8BB31F64I-D-QFN24	64	4352	20	4	12	6	6	Yes	QFN24-GI
EFM8BB31F64I-D-QSOP24 ¹	64	4352	21	4	13	6	7	Yes	QSOP24
EFM8BB31F64I-D-5QFN32 ³	64	4352	29	4	20	10	9	Yes	QFN32-AI
EFM8BB31F64I-D-4QFN24	64	4352	20	4	12	6	6	Yes	QFN24-AI
EFM8BB31F32I-D-QFN32 ³	32	2304	29	2 ²	20	10	9	Yes	QFN32-GI
EFM8BB31F32I-D-QFP32 ³	32	2304	28	2 ²	20	10	9	Yes	QFP32
EFM8BB31F32I-D-QFN24 ³	32	2304	20	2 ²	12	6	6	Yes	QFN24-GI
EFM8BB31F32I-D-QSOP24 ¹	32	2304	21	2 ²	13	6	7	Yes	QSOP24
EFM8BB31F32I-D-5QFN32 ³	32	2304	29	2 ²	20	10	9	Yes	QFN32-AI
EFM8BB31F32I-D-4QFN24	32	2304	20	2 ²	12	6	6	Yes	QFN24-AI
EFM8BB31F16I-D-QFN32 ³	16	2304	29	2 ²	20	10	9	Yes	QFN32-GI
EFM8BB31F16I-D-QFP32	16	2304	28	2 ²	20	10	9	Yes	QFP32
EFM8BB31F16I-D-QFN24 ³	16	2304	20	2 ²	12	6	6	Yes	QFN24-GI
EFM8BB31F16I-D-QSOP24 ¹	16	2304	21	2 ²	13	6	7	Yes	QSOP24
EFM8BB31F16I-D-5QFN32	16	2304	29	2 ²	20	10	9	Yes	QFN32-AI
EFM8BB31F16I-D-4QFN24 ³	16	2304	20	2 ²	12	6	6	Yes	QFN24-AI
EFM8BB31F64A-D-5QFN32	64	4352	29	4	20	10	9	Yes	QFN32-AI
EFM8BB31F64A-D-4QFN24 ³	64	4352	20	4	12	6	6	Yes	QFN24-AI
EFM8BB31F32A-D-5QFN32	32	2304	29	2 ²	20	10	9	Yes	QFN32-AI

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Voltage DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Package
EFM8BB31F32A-D-4QFN24 ³	32	2304	20	2 ²	12	6	6	Yes	QFN24-AI
EFM8BB31F16A-D-5QFN32	16	2304	29	2 ²	20	10	9	Yes	QFN32-AI
EFM8BB31F16A-D-4QFN24	16	2304	20	2 ²	12	6	6	Yes	QFN24-AI

Note:

1. End of life.
2. DAC0 and DAC1 are enabled on devices with 2 DACs available.
3. Not recommended for new designs (NRND).

The A-grade (i.e. EFM8BB31F64A-C-5QFN32 or EFM8BB31F64A-C-4QFN24) devices receive full automotive quality production status, including AEC-Q100 qualification, registration with International Material Data System (IMDS), and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at www.silabs.com with a registered and NDA approved user account.

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13.9 Revision 0.488

13.10 Revision 0.388

13.11 Revision 0.289

13.12 Revision 0.189

3. System Overview

3.1 Introduction

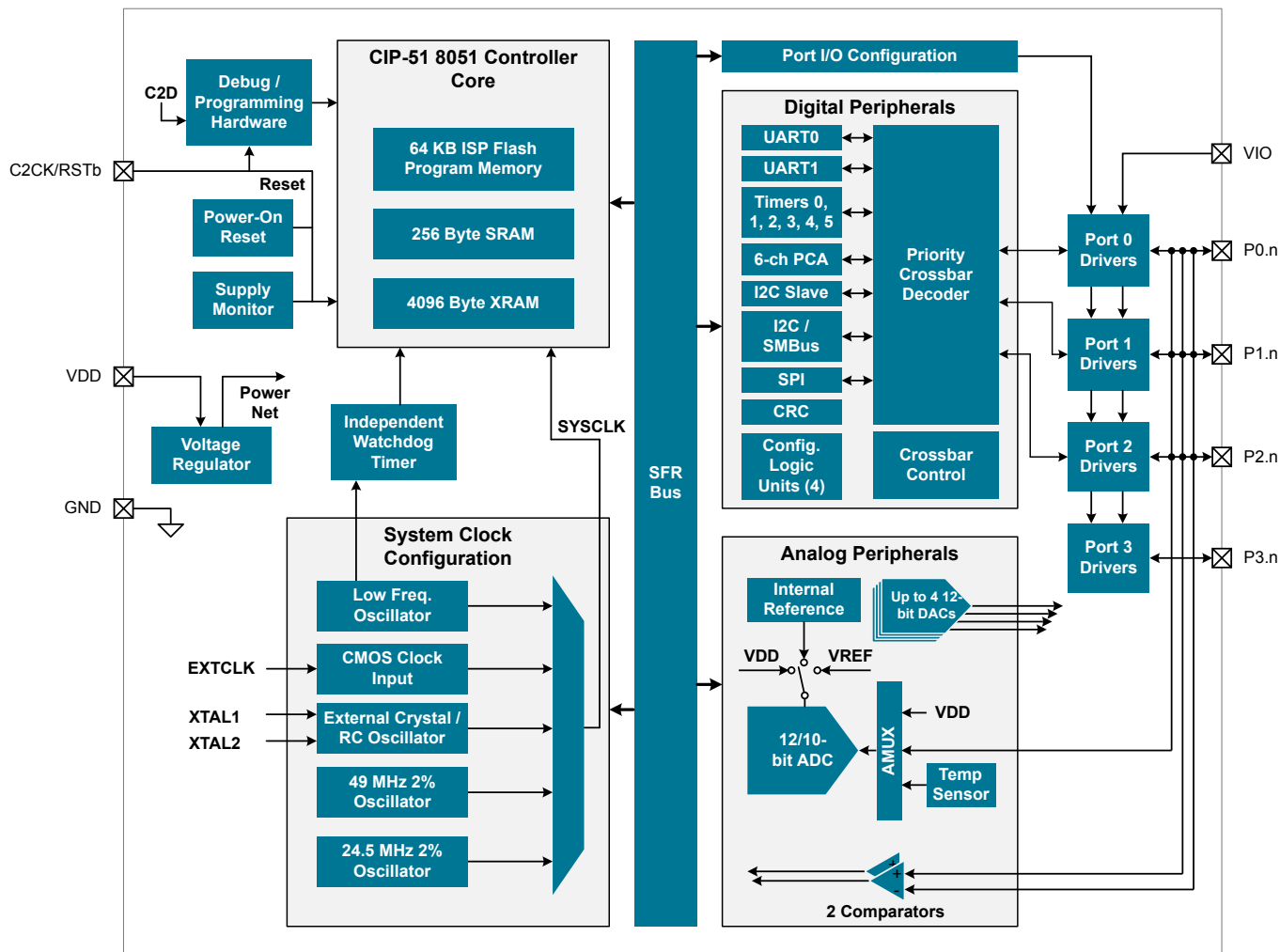


Figure 3.1. Detailed EFM8BB3 Block Diagram

This section describes the EFM8BB3 family at a high level.

For more information on the device packages and pinout, electrical specifications, and typical connection diagrams, see the EFM8BB3 Data Sheet. For more information on each module including register definitions, see the EFM8BB3 Reference Manual. For more information on any errata, see the EFM8BB3 Errata.

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational		
Idle	- Core halted - All peripherals clocked and fully operational - Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Suspend	- Core and peripheral clocks halted - HFOSC0 and HFOSC1 oscillators stopped - Regulator in normal bias mode for fast wake - Timer 3 and 4 may clock from LFOSC0 - Code resumes execution on wake event	- Switch SYSCLK to HFOSC0 - Set SUSPEND bit in PCON1	- Timer 4 Event - SPI0 Activity - I2C0 Slave Activity - Port Match Event - Comparator 0 Falling Edge - CLUn Interrupt-Enabled Event
Stop	- All internal power nets shut down - Pins retain state - Exit on any reset source	- Clear STOPCF bit in REG0CN - Set STOP bit in PCON0	Any reset source
Snooze	- Core and peripheral clocks halted - HFOSC0 and HFOSC1 oscillators stopped - Regulator in low bias current mode for energy savings - Timer 3 and 4 may clock from LFOSC0 - Code resumes execution on wake event	- Switch SYSCLK to HFOSC0 - Set SNOOZE bit in PCON1	- Timer 4 Event - SPI0 Activity - I2C0 Slave Activity - Port Match Event - Comparator 0 Falling Edge - CLUn Interrupt-Enabled Event
Shutdown	- All internal power nets shut down - Pins retain state - Exit on pin or power-on reset	- Set STOPCF bit in REG0CN - Set STOP bit in PCON0	- RSTb pin reset - Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.3 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.4 to P3.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 or P3.7, depending on the package option.

The port control block offers the following features:

- Up to 29 multi-function I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- State retention feature allows pins to retain configuration through most reset sources.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 24 direct-pin interrupt sources with shared interrupt vector (Port Match).

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

The clock control system offers the following features:

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to $\pm 2\%$ over supply and temperature corners.
- 49 MHz internal oscillator (HFOSC1), accurate to $\pm 2\%$ over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External RC, and CMOS clock options (EXTCLK and EXTOSC).
- Clock divider with eight settings for flexible clock scaling:
 - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.
 - HFOSC0 and HFOSC1 include 1.5x pre-scalers for further flexibility.

3.5 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to six independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0 or comparator 1

Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- Clock sources for all timers include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8
- LFOSC0 divided by 8 may be used to clock Timer 3 and Timer 4 in active or suspend/snooze power modes
- Timer 4 is a low-power wake source, and can be chained together with Timer 3
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- External pin capture
- LFOSC0 capture
- Comparator 0 capture
- Configurable Logic output capture

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- Programmable timeout interval
- Runs from the low-frequency oscillator
- Lock-out feature to prevent any modification until a system reset

3.6 Communications and Other Digital Peripherals

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- Single-byte FIFO on transmit and receive.

Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions
- Dedicated baud rate generator supports baud rates up to $\text{SYSCLK}/2$ (transmit) or $\text{SYSCLK}/8$ (receive)
- 5, 6, 7, 8, or 9 bit data
- Automatic start and stop generation
- Automatic parity generation and checking
- Single-byte buffer on transmit and receive
- Auto-baud detection
- LIN break and sync field detection
- CTS / RTS hardware flow control

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a main (clock driver) or secondary (clock receiver) interface in both 3-wire or 4-wire modes, and supports multiple main/secondary devices on a single SPI bus. The chip-select (NSS) signal can be configured as an input to select the SPI in secondary mode, or to disable main mode operation in an environment with multiple main interfaces, avoiding contention on the SPI bus when more than one main device attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in main interface mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple secondary devices.

- Supports 3- or 4-wire main or secondary modes
- Supports external clock frequencies up to 12 Mbps in main or secondary mode
- Support for all clock phase and polarity modes
- 8-bit programmable clock rate (main)
- Programmable receive timeout (secondary)
- Two byte FIFO on transmit and receive
- Can operate in suspend or snooze modes and wake the CPU on reception of a byte
- Support for multiple masters on the same data lines

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I²C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- Support for leader, follower, and multi-leader modes
- Hardware synchronization and arbitration for multi-leader mode
- Clock low extending (clock stretching) to interface with faster leader devices
- Hardware support for 7-bit follower and general call address recognition
- Firmware support for 10-bit follower address decoding
- Ability to inhibit all follower states
- Programmable data setup/hold times
- Transmit and receive FIFOs (one byte) to help increase throughput in faster applications

I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- Support for slave mode only
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave address recognition
- Transmit and receive FIFOs (two byte) to help increase throughput in faster applications
- Hardware support for multiple slave addresses with the option to save the matching address in the receive FIFO

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

Configurable Logic Units (CLU0, CLU1, CLU2, and CLU3)

The Configurable Logic block consists of multiple Configurable Logic Units (CLUs). CLUs are flexible logic functions which may be used for a variety of digital functions, such as replacing system glue logic, aiding in the generation of special waveforms, or synchronizing system event triggers.

- Four configurable logic units (CLUs), with direct-pin and internal logic connections
- Each unit supports 256 different combinatorial logic functions (AND, OR, XOR, muxing, etc.) and includes a clocked flip-flop for synchronous operations
- Units may be operated synchronously or asynchronously
- May be cascaded together to perform more complicated logic functions
- Can operate in conjunction with serial peripherals such as UART and SPI or timing peripherals such as timers and PCA channels
- Can be used to synchronize and trigger multiple on-chip resources (ADC, DAC, Timers, etc.)
- Asynchronous output may be used to wake from low-power states

3.7 Analog

12/10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12- and 10-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs
- Single-ended 12-bit and 10-bit modes
- Supports an output update rate of up to 350 ksp/s in 12-bit mode
- Channel sequencer logic with direct-to-XDATA output transfers
- Operation in a low power mode at lower conversion speeds
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Conversion complete and window compare interrupts supported
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.65 V reference and an on-chip precision 2.4 / 1.2 V reference, with support for using the supply as the reference, an external reference and signal ground
- Integrated temperature sensor

12-Bit Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)

The DAC modules are 12-bit Digital-to-Analog Converters with the capability to synchronize multiple outputs together. The DACs are fully configurable under software control. The voltage reference for the DACs is selectable between internal and external reference sources.

- Voltage output with 12-bit performance
- Supports an update rate of 200 ksp/s
- Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Outputs may be configured to persist through reset and maintain output state to avoid system disruption
- Multiple DAC outputs can be synchronized together
- DAC pairs (DAC0 and 1 or DAC2 and 3) support complementary output waveform generation
- Outputs may be switched between two levels according to state of configurable logic / PWM input trigger
- Flexible input data formatting
- Supports references from internal supply, on-chip precision reference, or external VREF pin

Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- Up to 10 (CMP0) or 9 (CMP1) external positive inputs
- Up to 10 (CMP0) or 9 (CMP1) external negative inputs
- Additional input options:
 - Internal connection to LDO output
 - Direct connection to GND
 - Direct connection to VDD
 - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and ± 20 mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset

3.9 Debugging

The EFM8BB3 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

Silicon Labs recommends the bootloader be disabled and the flash memory locked after the production programming step in applications where code security is a concern. More information about the factory bootloader protocol, usage, customization and best practices can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [Application Notes] tile.

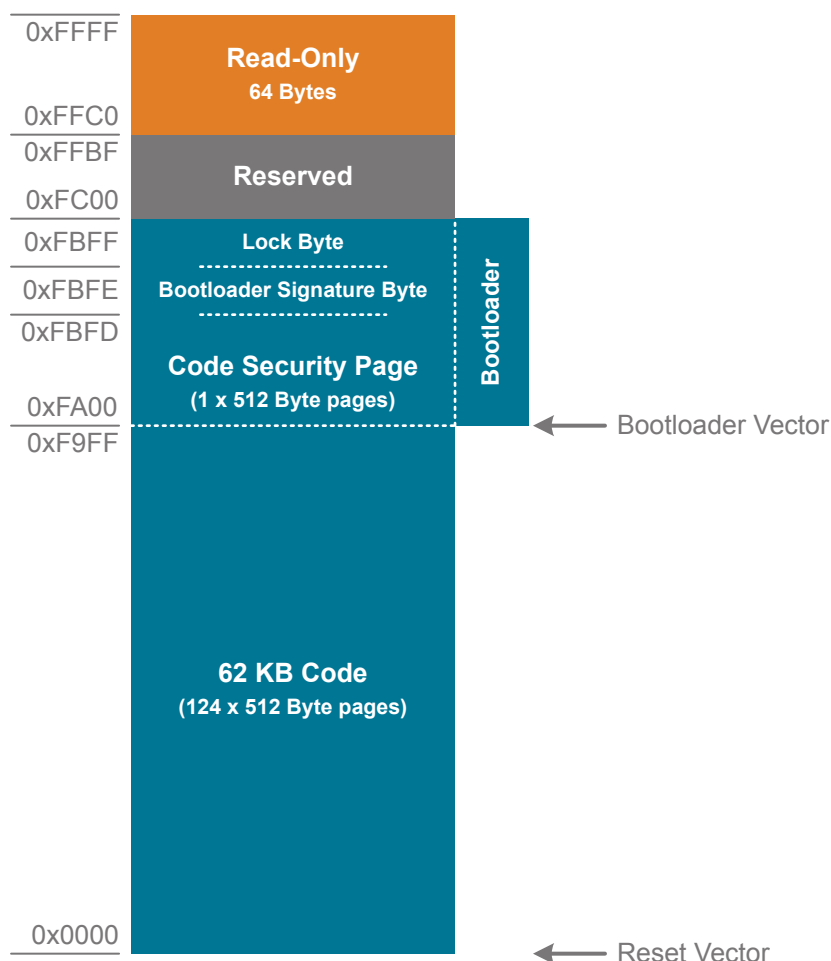


Figure 3.2. Flash Memory Map with Bootloader — 62.5 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5

Table 3.3. Summary of Pins for Bootload Mode Entry

Device Package	Pin for Bootload Mode Entry
all QFN32 packages	P3.7 / C2D
QFP32	P3.7 / C2D
all QFN24 packages	P3.0 / C2D
QSOP24	P3.0 / C2D

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions on page 19](#), unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V _{DD}		2.2	—	3.6	V
Operating Supply Voltage on VIO ²	V _{IO}		2.2	—	V _{DD}	V
System Clock Frequency	f _{SYSCLK}		0	—	50	MHz
Operating Ambient Temperature	T _A	G-grade devices	−40	—	85	°C
		I-grade or A-grade devices	−40	—	125	°C

Note:

1. All voltages with respect to GND
2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.
3. I/O have reduced current drive/sink capabilities at lower VIO levels. See [4.1.16 Port I/O](#) for additional information.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current (G-grade devices, -40 °C to +85 °C)						
Normal Mode-Full speed with code executing from flash	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²	—	5	14.4	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²	—	4.2	5	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²	—	625	820	μA
		F _{SYSCLK} = 80 kHz ³	—	155	310	μA
Idle Mode-Core halted with peripherals running	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²	—	3.8	11.8	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²	—	3.14	3.8	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²	—	520	725	μA
		F _{SYSCLK} = 80 kHz ³	—	135	315	μA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off.	I _{DD}	LFO Running	—	125	320	μA
		LFO Stopped	—	120	300	μA
Snooze Mode-Core halted and high frequency clocks stopped. Regulator in low-power state, Supply monitor off.	I _{DD}	LFO Running	—	23	190	μA
		LFO Stopped	—	19	186	μA
Stop Mode—Core halted and all clocks stopped, Internal LDO On, Supply monitor off.	I _{DD}		—	120	300	μA
Shutdown Mode—Core halted and all clocks stopped, Internal LDO Off, Supply monitor off.	I _{DD}		—	0.2	0.91	μA
Digital Core Supply Current (I-grade or A-grade devices, -40 °C to +125 °C)						
Normal Mode-Full speed with code executing from flash	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²	—	5	14.4	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²	—	4.2	5.2	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²	—	625	1280	μA
		F _{SYSCLK} = 80 kHz ³	—	155	765	μA
Idle Mode-Core halted with peripherals running	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²	—	3.8	11.8	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²	—	3.14	4.1	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²	—	520	1175	μA
		F _{SYSCLK} = 80 kHz ³	—	135	750	μA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off.	I _{DD}	LFO Running	—	125	775	μA
		LFO Stopped	—	120	755	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Snooze Mode—Core halted and high frequency clocks stopped. Regulator in low-power state, Supply monitor off.	I _{DD}	LFO Running	—	23	615	μA
		LFO Stopped	—	19	610	μA
Stop Mode—Core halted and all clocks stopped, Internal LDO On, Supply monitor off.	I _{DD}		—	120	740	μA
Shutdown Mode—Core halted and all clocks stopped, Internal LDO Off, Supply monitor off.	I _{DD}		—	0.2	4.5	μA
Analog Peripheral Supply Currents (-40 °C to +125 °C)						
High-Frequency Oscillator 0	I _{HFOSC0}	Operating at 24.5 MHz, T _A = 25 °C	—	120	135	μA
High-Frequency Oscillator 1	I _{HFOSC1}	Operating at 49 MHz, T _A = 25 °C	—	770	1200	μA
Low-Frequency Oscillator	I _{LFOSC}	Operating at 80 kHz, T _A = 25 °C	—	3.7	6	μA
ADC0 ⁴	I _{ADC}	High Speed Mode 1 Msps, 10-bit conversions Normal bias settings V _{DD} = 3.0 V	—	1210	1600	μA
		Low Power Mode 350 ksps, 12-bit conversions Low power bias settings V _{DD} = 3.0 V	—	415	560	μA
Internal ADC0 Reference ⁵	I _{VREFFS}	High Speed Mode	—	700	790	μA
		Low Power Mode	—	170	210	μA
On-chip Precision Reference	I _{VREFP}		—	75	—	μA
Temperature Sensor	I _{TSENSE}		—	68	120	μA
Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3) ⁶	I _{DAC}		—	125	—	μA
Comparators (CMP0, CMP1)	I _{CMP}	CPMD = 11	—	0.5	—	μA
		CPMD = 10	—	3	—	μA
		CPMD = 01	—	10	—	μA
		CPMD = 00	—	25	—	μA
Comparator Reference ⁷	I _{CPREF}		—	24	—	μA
Voltage Supply Monitor (VMON0)	I _{VMON}		—	15	20	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount. 2. Includes supply current from internal LDO regulator, supply monitor, and High Frequency Oscillator. 3. Includes supply current from internal LDO regulator, supply monitor, and Low Frequency Oscillator. 4. ADC0 power excludes internal reference supply current. 5. The internal reference is enabled as-needed when operating the ADC in low power mode. Total ADC + Reference current will depend on sampling rate. 6. DAC supply current for each enabled DA and not including external load on pin. 7. This value is the current sourced from the pin or supply selected as the full-scale reference to the comparator DAC.						

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}		1.95	2.05	2.15	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on VDD	—	1.4	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t_{RMP}	Time to $V_{DD} > 2.2$ V	10	—	—	μ s
Reset Delay from POR	t_{POR}	Relative to $V_{DD} > V_{POR}$	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	50	—	μ s
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	μ s
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{SYSCLK} > 1$ MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7.5	13.5	kHz
VDD Supply Monitor Turn-On Time	t_{MON}		—	2	—	μ s

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time ^{1,2}	t _{WRITE}	One Byte, F _{SYSClk} = 24.5 MHz	19	20	21	μs
Erase Time ^{1,2}	t _{ERASE}	One Page, F _{SYSClk} = 24.5 MHz	5.2	5.35	5.5	ms
V _{DD} Voltage During Programming ³	V _{PROG}		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	N _{WE}		20k	100k	—	Cycles
CRC Calculation Time	t _{CRC}	One 256-Byte Block SYSClk = 49 MHz	—	5.5	—	μs

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSClk cycles.
2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t _{IDLEWK}		2	—	3	SYSClks
Suspend Mode Wake-up Time	t _{SUS- PENDWK}	SYSClk = HFOSC0 CLKDIV = 0x00	—	170	—	ns
Snooze Mode Wake-up Time	t _{SLEEPWK}	SYSClk = HFOSC0 CLKDIV = 0x00	—	12	—	μs

4.1.6 Internal Oscillators

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	$\text{PSS}_{\text{HFOSC0}}$	$T_A = 25\text{ }^{\circ}\text{C}$	—	0.5	—	%/V
Temperature Sensitivity	$\text{TS}_{\text{HFOSC0}}$	$V_{\text{DD}} = 3.0\text{ V}$	—	40	—	ppm/ $^{\circ}\text{C}$
High Frequency Oscillator 1 (49 MHz)						
Oscillator Frequency	f_{HFOSC1}	Full Temperature and Supply Range	48.02	49	49.98	MHz
Power Supply Sensitivity	$\text{PSS}_{\text{HFOSC1}}$	$T_A = 25\text{ }^{\circ}\text{C}$	—	300	—	ppm/V
Temperature Sensitivity	$\text{TS}_{\text{HFOSC1}}$	$V_{\text{DD}} = 3.0\text{ V}$	—	103	—	ppm/ $^{\circ}\text{C}$
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	$\text{PSS}_{\text{LFOSC}}$	$T_A = 25\text{ }^{\circ}\text{C}$	—	0.05	—	%/V
Temperature Sensitivity	TS_{LFOSC}	$V_{\text{DD}} = 3.0\text{ V}$	—	65	—	ppm/ $^{\circ}\text{C}$

4.1.7 External Clock Input

Table 4.7. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	50	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns

4.1.8 External Oscillator

Table 4.8. External Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}		0.02	—	25	MHz
Crystal Drive Current	I_{XTAL}	XFCN = 000	—	0.5	—	μA
		XFCN = 001	—	1.5	—	μA
		XFCN = 010	—	4.8	—	μA
		XFCN = 011	—	14	—	μA
		XFCN = 100	—	40	—	μA
		XFCN = 101	—	120	—	μA
		XFCN = 110	—	550	—	μA
		XFCN = 111	—	2.6	—	mA
Frequency Range (resonators and RC oscillators)	f_{EXTOSC}	XFCN = 000	0.02	—	25	kHz
		XFCN = 001	25	—	50	kHz
		XFCN = 010	50	—	100	kHz
		XFCN = 011	100	—	200	kHz
		XFCN = 100	200	—	400	kHz
		XFCN = 101	400	—	800	kHz
		XFCN = 110	800	—	1600	kHz
		XFCN = 111	1.6	—	3.2	MHz

4.1.9 ADC

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N _{bits}	12 Bit Mode	12			Bits
		10 Bit Mode	10			Bits
Throughput Rate (High Speed Mode)	f _S	10 Bit Mode	—	—	1.125	Msp/s
Throughput Rate (Low Power Mode)	f _S	12 Bit Mode	—	—	340	ksps
		10 Bit Mode	—	—	360	ksps
Tracking Time	t _{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t _{PWR}		1.2	—	—	μs
SAR Clock Frequency	f _{SAR}	High Speed Mode	—	—	18	MHz
		Low Power Mode	—	—	12.25	MHz
Conversion Time ¹	t _{CNV}	12-Bit Conversion, SAR Clock = 6.125 MHz, System Clock = 49 MHz	2.0			μs
		10-Bit Conversion, SAR Clock = 16.33 MHz, System Clock = 49 MHz	0.658			μs
Sample/Hold Capacitor	C _{SAR}	Gain = 1	—	5.2	—	pF
		Gain = 0.75	—	3.9	—	pF
		Gain = 0.5	—	2.6	—	pF
		Gain = 0.25	—	1.3	—	pF
Input Pin Capacitance	C _{IN}		—	20	—	pF
Input Mux Impedance	R _{MUX}		—	550	—	Ω
Voltage Reference Range	V _{REF}		1	—	V _{IO}	V
Input Voltage Range ²	V _{IN}		0	—	V _{REF} / Gain	V
Power Supply Rejection Ratio	PSRR _{ADC}	At 1 kHz	—	66	—	dB
		At 1 MHz	—	43	—	dB
DC Performance						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Integral Nonlinearity	INL	12 Bit Mode	-1.9	-0.35 / +1	1.9	LSB
		10 Bit Mode	-0.6	±0.2	0.6	LSB
		T _A = -40 °C to 85 °C				
		10 Bit Mode	-0.7	±0.2	0.7	LSB
		T _A = -40 °C to 125 °C (I-grade or A-grade parts only)				
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	-0.9	±0.3	0.9	LSB
		T _A = -40 °C to 85 °C				
		12 Bit Mode	-1.02	±0.3	1.02	LSB
		T _A = -40 °C to 125 °C (I-grade or A-grade parts only)				
		10 Bit Mode	-0.5	±0.2	0.5	LSB
Offset Error ³	E _{OFF}	12 Bit Mode	-2	0	2	LSB
		T _A = -40 °C to 85 °C				
		12 Bit Mode	-3	0	3	LSB
		T _A = -40 °C to 125 °C (I-grade or A-grade parts only)				
		10 Bit Mode	-1	0	1	LSB
		T _A = -40 °C to 85 °C				
		10 Bit Mode	-1	0	1.3	LSB
		T _A = -40 °C to 125 °C (I-grade or A-grade parts only)				
Offset Temperature Coefficient	TC _{OFF}		—	0.011	—	LSB/°C
Slope Error	E _M	12 Bit Mode	-2.5	—	2.5	LSB
		T _A = -40 °C to 85 °C				
		12 Bit Mode	-2.6	—	2.6	LSB
		T _A = -40 °C to 125 °C (I-grade or A-grade parts only)				
		10 Bit Mode	-1.1	—	1.1	LSB
Dynamic Performance 10 kHz Sine Wave Input 1 dB below full scale, Max throughput, using AGND pin						
Signal-to-Noise	SNR	12 Bit Mode	64	68	—	dB
		10 Bit Mode	59	61	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	64	68	—	dB
		10 Bit Mode	59	61	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	-72	—	dB
		10 Bit Mode	—	-69	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	74	—	dB
		10 Bit Mode	—	71	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: - Conversion Time does not include Tracking Time. Total Conversion Time is: Total Conversion Time = $[RPT \times (ADTK + NUMBITS + 1) \times T(SARCLK)] + (T(ADCCLK) \times 4)$ where RPT is the number of conversions represented by the ADRPT field and ADCCLK is the clock selected for the ADC. - Absolute input pin voltage is limited by the V_{IO} supply. - The offset is determined using curve fitting since the specification is measured using linear search where the intercept is always positive. - Production test uses a 2.4 V external reference and external ground.						

4.1.10 Voltage Reference

Table 4.10. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}		1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	μs
Power Supply Rejection	$PSRR_{\text{REFFS}}$		—	400	—	ppm/V
On-chip Precision Reference						
Valid Supply Range	V_{DD}	1.2 V Output	2.2	—	3.6	V
		2.4 V Output	2.7	—	3.6	V
Output Voltage	V_{REFP}	1.2 V Output, $V_{\text{DD}} = 3.3 \text{ V}$, $T = 25 \text{ °C}$	1.195	1.2	1.205	V
		1.2 V Output	1.18	1.2	1.22	V
		2.4 V Output, $V_{\text{DD}} = 3.3 \text{ V}$, $T = 25 \text{ °C}$	2.39	2.4	2.41	V
		2.4 V Output	2.36	2.4	2.44	V
Turn-on Time, settling to 0.5 LSB	t_{VREFP}	4.7 μF tantalum + 0.1 μF ceramic bypass on VREF pin	—	3	—	ms
		0.1 μF ceramic bypass on VREF pin	—	100	—	μs
Load Regulation	LR_{VREFP}	$V_{\text{REF}} = 2.4 \text{ V}$, Load = 0 to 200 μA to GND	—	8	—	μV/μA
		$V_{\text{REF}} = 1.2 \text{ V}$, Load = 0 to 200 μA to GND	—	5	—	μV/μA
Load Capacitor	C_{VREFP}	Load = 0 to 200 μA to GND	0.1	—	—	μF
Short-circuit current	ISC_{VREFP}		—	—	8	mA
Power Supply Rejection	$PSRR_{\text{VREFP}}$		—	75	—	dB
External Reference						
Input Current	I_{EXTREF}	ADC Sample Rate = 800 ksps; $V_{\text{REF}} = 3.0 \text{ V}$	—	5	—	μA

4.1.11 Temperature Sensor

Table 4.11. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	751	—	mV
Offset Error ¹	E_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	19	—	mV
Slope	M		—	2.82	—	mV/ $^{\circ}\text{C}$
Slope Error ¹	E_M		—	29	—	$\mu\text{V}/^{\circ}\text{C}$
Linearity	LIN	$T = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	—	± 0.4	—	$^{\circ}\text{C}$
		$T = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ (I-grade or A-grade parts only)	—	-0.6 to 1.2	—	$^{\circ}\text{C}$
Turn-on Time	t_{ON}		—	3.5	—	μs
Note: 1. Represents one standard deviation from the mean.						

4.1.12 1.8 V Internal LDO Voltage Regulator

Table 4.12. 1.8V Internal LDO Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage	$V_{OUT_1.8V}$		1.79	1.84	1.88	V

4.1.13 DACs

Table 4.13. DACs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage	V_{OUT}		0	—	V_{DD}	V
Output Current	I_{OUT}		-2	—	2	mA
Resolution	N_{bits}		12			Bits
Throughput Rate	f_S		—	—	200	ksps
Integral Nonlinearity	INL	DAC0 and DAC2 $T_A = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ (I-grade or A-grade parts only)	-11.5	-1.77 / 1.56	11.5	LSB
		DAC1 and DAC3 $T_A = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ (I-grade or A-grade parts only)	-13.5	-2.73 / 1.11	13.5	LSB
Differential Nonlinearity	DNL		-1	—	1	LSB
Output Noise	V_{NOISE}	$V_{REF} = 2.4\text{ V}$ $f_S = 0.1\text{ Hz}$ to 300 kHz	—	110	—	μV_{RMS}
Slew Rate	SLEW		—	± 1	—	$\text{V}/\mu\text{s}$
Output Settling Time to 1% Full-scale	t_{SETTLE}	V_{OUT} change between 25% and 75% Full Scale	—	2.6	5	μs
Power-on Time	t_{PWR}		—	—	10	μs
Voltage Reference Range	V_{REF}		1.15	—	V_{DD}	V
Power Supply Rejection Ratio	PSRR	DC, $V_{OUT} = 50\%$ Full Scale	—	78	—	dB
Total Harmonic Distortion	THD	$V_{OUT} = 10\text{ kHz}$ sine wave, 10% to 90%	54	—	—	dB
Offset Error	E_{OFF}	$V_{REF} = 2.4\text{ V}$	-8	0	8	LSB
Full-Scale Error	E_{FS}	$V_{REF} = 2.4\text{ V}$	-13	± 5	13	LSB
External Load Impedance	R_{LOAD}		2	—	—	k Ω
External Load Capacitance ¹	C_{LOAD}		—	—	100	pF

Note:

1. No minimum external load capacitance is required. However, under low loading conditions, it is possible for the DAC output to glitch during start-up. If smooth start-up is required, the minimum loading capacitance at the pin should be a minimum of 10 pF.

4.1.14 Comparators

Table 4.14. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		-100 mV Differential	—	150	—	ns
Response Time, CPMD = 11 (Low- est Power)	t_{RESP3}	+100 mV Differential	—	1.5	—	μs
		-100 mV Differential	—	3.5	—	μs
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	-8	—	mV
		CPHYN = 10	—	-16	—	mV
		CPHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	-6	—	mV
		CPHYN = 10	—	-12	—	mV
		CPHYN = 11	—	-24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	-4.5	—	mV
		CPHYN = 10	—	-9	—	mV
		CPHYN = 11	—	-18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS _{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V _{IN}		-0.25	—	V _{IO} +0.25	V
Input Pin Capacitance	C _{CP}		—	7.5	—	pF
Internal Reference DAC Resolution	N _{bits}		6			bits
Common-Mode Rejection Ratio	CMRR _{CP}		—	70	—	dB
Power Supply Rejection Ratio	PSRR _{CP}		—	72	—	dB
Input Offset Voltage	V _{OFF}	T _A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC _{OFF}		—	3.5	—	μV/°

4.1.15 Configurable Logic

Table 4.15. Configurable Logic

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation Delay	t _{DLY}	Through single CLU Using an external pin	—	—	35.3	ns
		Through single CLU Using an internal connection	—	3	—	ns
Clocking Frequency	F _{CLK}	1 or 2 CLUs Cascaded	—	—	73.5	MHz
		3 or 4 CLUs Cascaded	—	—	36.75	MHz

4.1.16 Port I/O

Table 4.16. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	V_{OH}	$I_{OH} = -7 \text{ mA}$, $V_{IO} \geq 3.0 \text{ V}$	$V_{IO} - 0.7$	—	—	V
		$I_{OH} = -3.3 \text{ mA}$, $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	$V_{IO} \times 0.8$	—	—	V
		$I_{OH} = -1.8 \text{ mA}$, $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output Low Voltage (High Drive)	V_{OL}	$I_{OL} = 13.5 \text{ mA}$, $V_{IO} \geq 3.0 \text{ V}$	—	—	0.6	V
		$I_{OL} = 7 \text{ mA}$, $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	—	—	$V_{IO} \times 0.2$	V
		$I_{OL} = 3.6 \text{ mA}$, $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output High Voltage (Low Drive)	V_{OH}	$I_{OH} = -4.75 \text{ mA}$, $V_{IO} \geq 3.0 \text{ V}$	$V_{IO} - 0.7$	—	—	V
		$I_{OH} = -2.25 \text{ mA}$, $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	$V_{IO} \times 0.8$	—	—	V
		$I_{OH} = -1.2 \text{ mA}$, $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output Low Voltage (Low Drive)	V_{OL}	$I_{OL} = 6.5 \text{ mA}$, $V_{IO} \geq 3.0 \text{ V}$	—	—	0.6	V
		$I_{OL} = 3.5 \text{ mA}$, $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	—	—	$V_{IO} \times 0.2$	V
		$I_{OL} = 1.8 \text{ mA}$, $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Input High Voltage	V_{IH}		$0.7 \times V_{IO}$	—	—	V
Input Low Voltage	V_{IL}		—	—	$0.3 \times V_{IO}$	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current ($V_{IN} = 0 \text{ V}$)	I_{PU}	$V_{DD} = 3.6$	-30	-20	-10	μA
Input Leakage (Pullups off or Analog)	I_{LK}	$GND < V_{IN} < V_{IO}$ (G-grade and I-grade devices)	-1.1	—	4	μA
		$GND < V_{IN} < V_{IO}$ (A-grade devices only)	-1.1	—	1.1	μA
Input Leakage Current with V_{IN} above V_{IO}	I_{LK}	$V_{IO} < V_{IN} < V_{IO} + 2.5 \text{ V}$ Any pin except P3.0, P3.1, P3.2, or P3.3	0	5	150	μA

4.1.17 SMBus

Table 4.17. SMBus Peripheral Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70 ²	kHz
SMBus Operating Frequency	f_{SMB}		40 ¹	—	70 ²	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	μs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	μs
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	μs
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	μs
Data Hold Time	$t_{HD:DAT}$		275 ³	—	—	ns
Data Setup Time	$t_{SU:DAT}$		300 ³	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	μs
Clock High Period	t_{HIGH}		9.4	—	50 ⁴	μs
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	256 ²	kHz
SMBus Operating Frequency	f_{SMB}		40 ¹	—	256 ²	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	μs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	μs
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	μs
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	μs
Data Hold Time	$t_{HD:DAT}$		275 ³	—	—	ns
Data Setup Time	$t_{SU:DAT}$		300 ³	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	μs
Clock High Period	t_{HIGH}		2.6	—	50 ⁴	μs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications.
3. Data setup and hold timing at 40 MHz or lower with EXTHOLD set to 1. The DLYEXT bit can be used to adjust the data setup and hold times.
4. SMBus has a maximum requirement of 50 μ s for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 μ s. I2C can support periods longer than 50 μ s.

Table 4.18. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	$f_{CSO} / 3$
Bus Free Time Between STOP and START Conditions	t_{BUF}	$2 / f_{CSO}$
Hold Time After (Repeated) START Condition	$t_{HD:STA}$	$1 / f_{CSO}$
Repeated START Condition Setup Time	$t_{SU:STA}$	$2 / f_{CSO}$
STOP Condition Setup Time	$t_{SU:STO}$	$2 / f_{CSO}$
Clock Low Period	t_{LOW}	$1 / f_{CSO}$
Clock High Period	t_{HIGH}	$2 / f_{CSO}$

Note:

1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

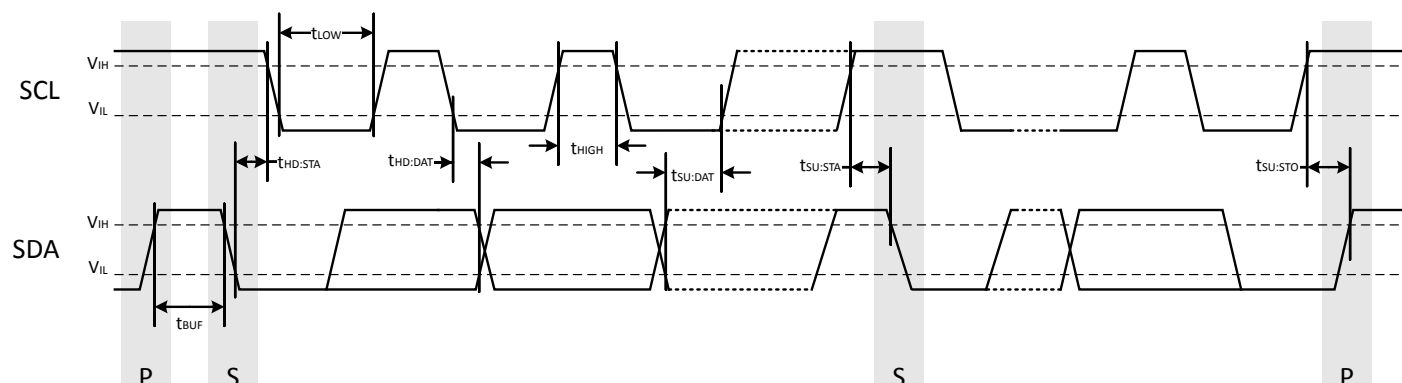
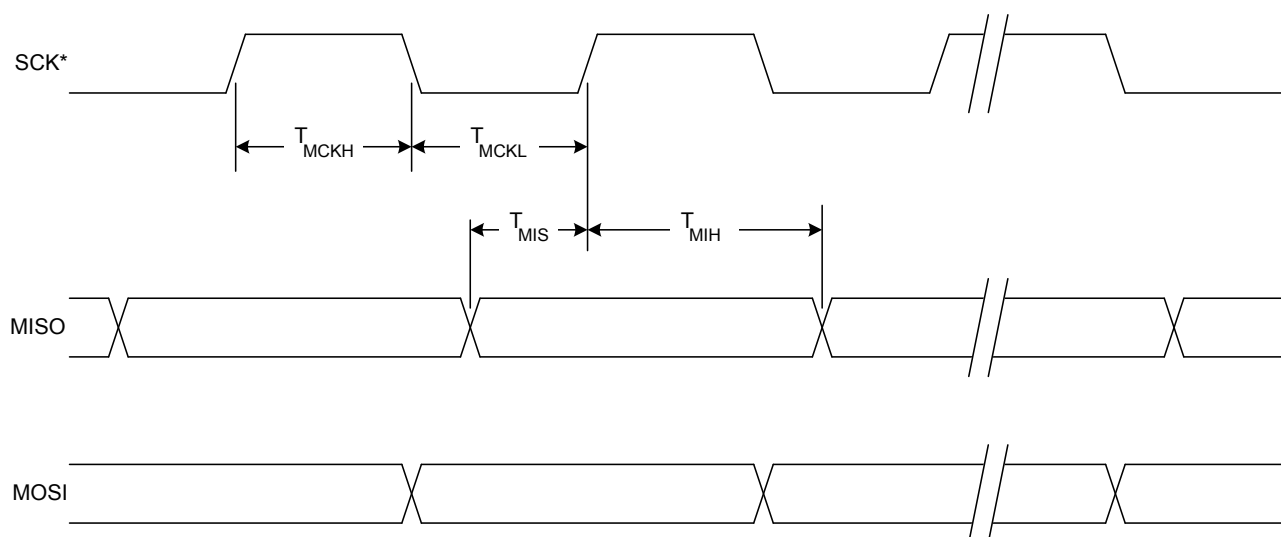


Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.1.18 SPI

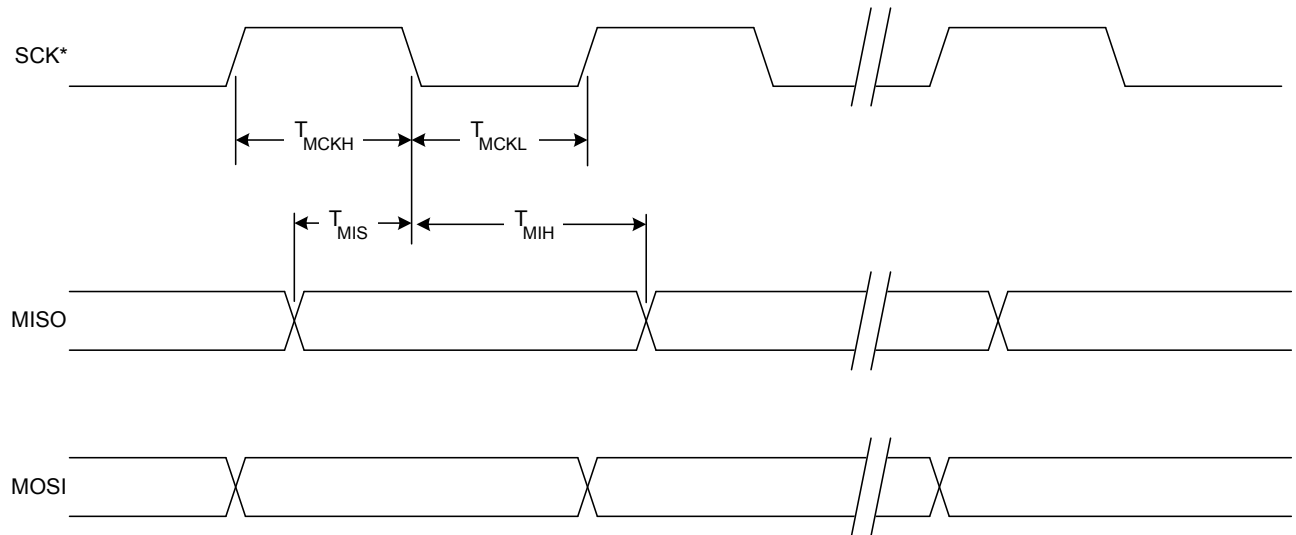
Table 4.19. SPI Timing Parameters

Parameter	Description	Min	Max	Units
Master Mode Timing				
T_{MCKH}	SCK High Time	$1 \times T_{SYSCLK}$	—	ns
T_{MCKL}	SCK Low Time	$1 \times T_{SYSCLK}$	—	ns
T_{MIS}	MISO Valid to SCK Sample Edge	20	—	ns
T_{MIH}	SCK Sample Edge to MISO Change	5	—	ns
Slave Mode Timing				
T_{SE}	NSS Falling to First SCK Edge	5	—	ns
T_{SD}	Last SCK Edge to NSS Rising	5	—	ns
T_{SEZ}	NSS Falling to MISO Valid	—	20	ns
T_{SDZ}	NSS Rising to MISO High-Z	—	20	ns
T_{CKH}	SCK High Time	40	—	ns
T_{CKL}	SCK Low Time	40	—	ns
T_{SIS}	MOSI Valid to SCK Sample Edge	20	—	ns
T_{SIH}	SCK Sample Edge to MOSI Change	5	—	ns
T_{SOH}	SCK Shift Edge to MISO Change	—	20	ns
Note: 1. T_{SYSCLK} is equal to one period of the device system clock (SYSCLK).				



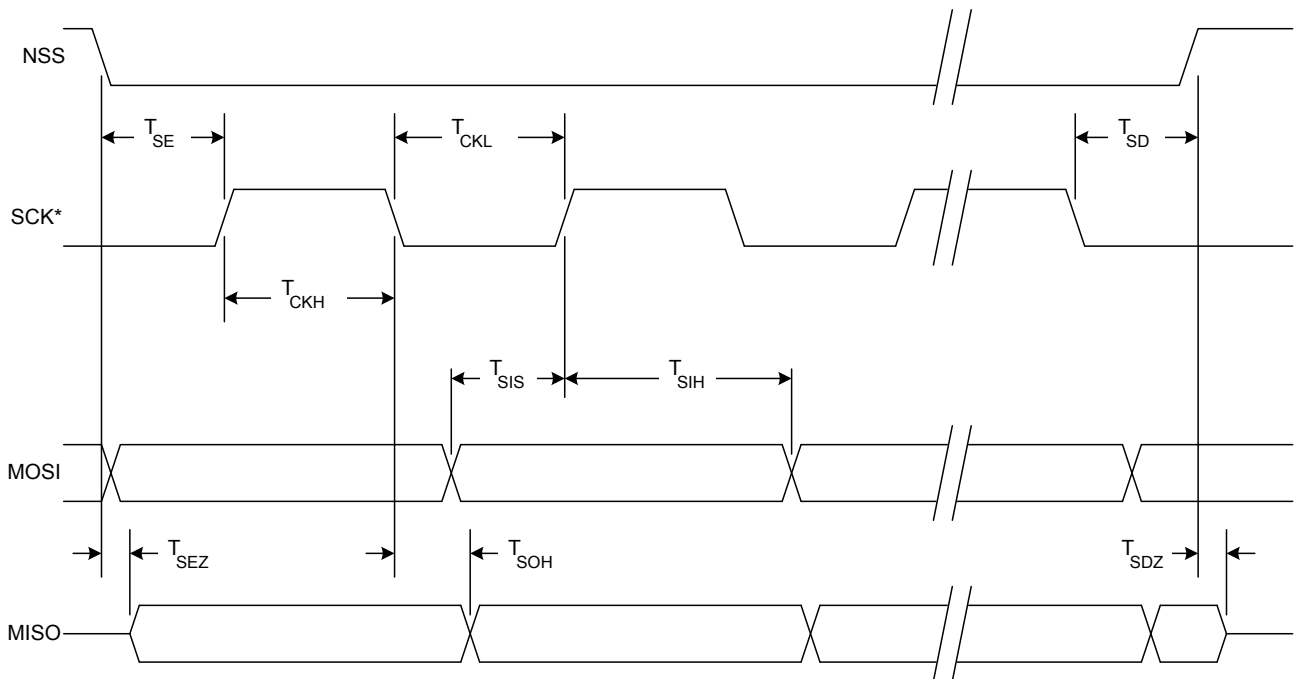
* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 4.2. SPI Master Timing (CKPHA = 0)



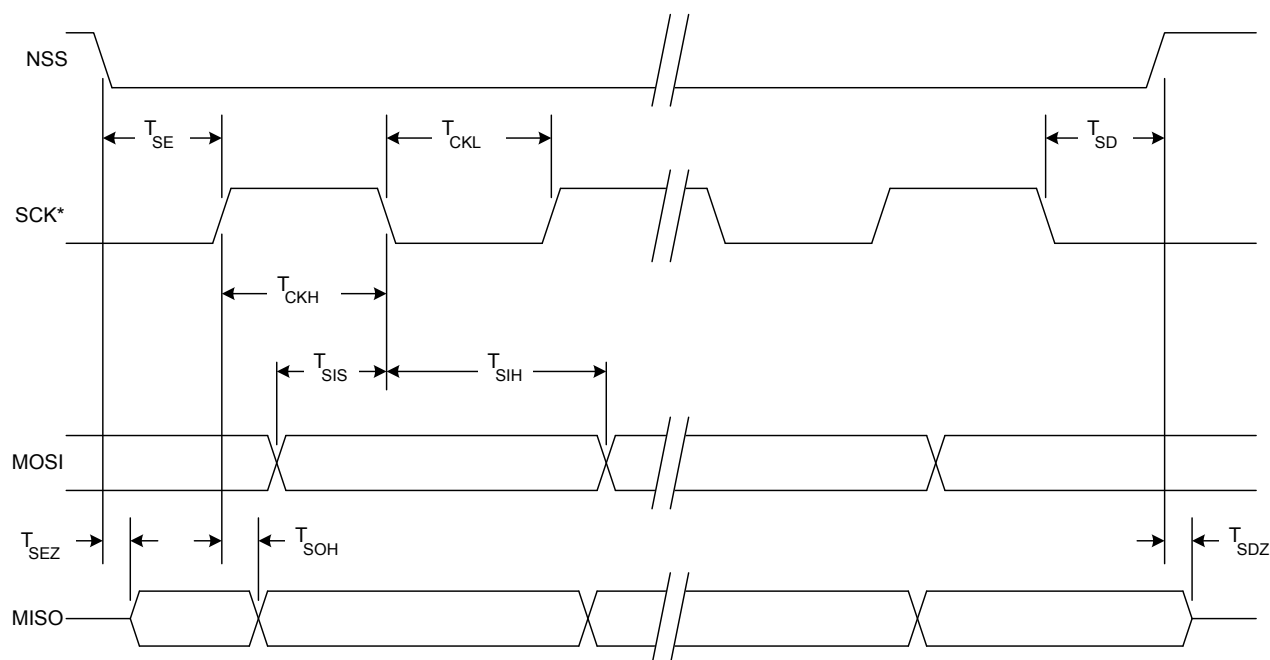
* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 4.3. SPI Master Timing (CKPHA = 1)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 4.4. SPI Slave Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 4.5. SPI Slave Timing (CKPHA = 1)

4.2 Thermal Conditions

Table 4.20. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	θ_{JA}	QFN24-GI Packages	—	30	—	°C/W
		QFN24-AI Packages	—	TBD	—	°C/W
		QFN32-GI Packages	—	26	—	°C/W
		QFN32-AI Packages	—	TBD	—	°C/W
		QFP32 Packages	—	80	—	°C/W
		QSOP24 Packages	—	65	—	°C/W

Note:

1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

4.3 Absolute Maximum Ratings

Stresses above those listed in [Table 4.21 Absolute Maximum Ratings on page 40](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

Table 4.21. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		-55	125	°C
Storage Temperature	T_{STG}		-65	150	°C
Voltage on VDD	V_{DD}		GND-0.3	4.2	V
Voltage on VIO ²	V_{IO}		GND-0.3	$V_{DD}+0.3$	V
Voltage on I/O pins or RSTb, excluding P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	V_{IN}	$V_{IO} > 3.3\text{ V}$	GND-0.3	5.8	V
		$V_{IO} < 3.3\text{ V}$	GND-0.3	$V_{IO}+2.5$	V
Voltage on P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	V_{IN}		GND-0.3	$V_{DD}+0.3$	V
Total Current Sunk into Supply Pin	I_{VDD}		—	200	mA
Total Current Sourced out of Ground Pin	I_{GND}		200	—	mA
Current Sourced or Sunk by any I/O Pin or RSTb	I_{IO}		-100	100	mA
Operating Junction Temperature	T_J	$T_A = -40\text{ °C to }85\text{ °C}$	-40	105	°C
		$T_A = -40\text{ °C to }125\text{ °C}$ (I-grade or A-grade parts only)	-40	130	°C

Note:

1. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Power Connection Diagram on page 41 shows a typical connection diagram for the power pins of the device.

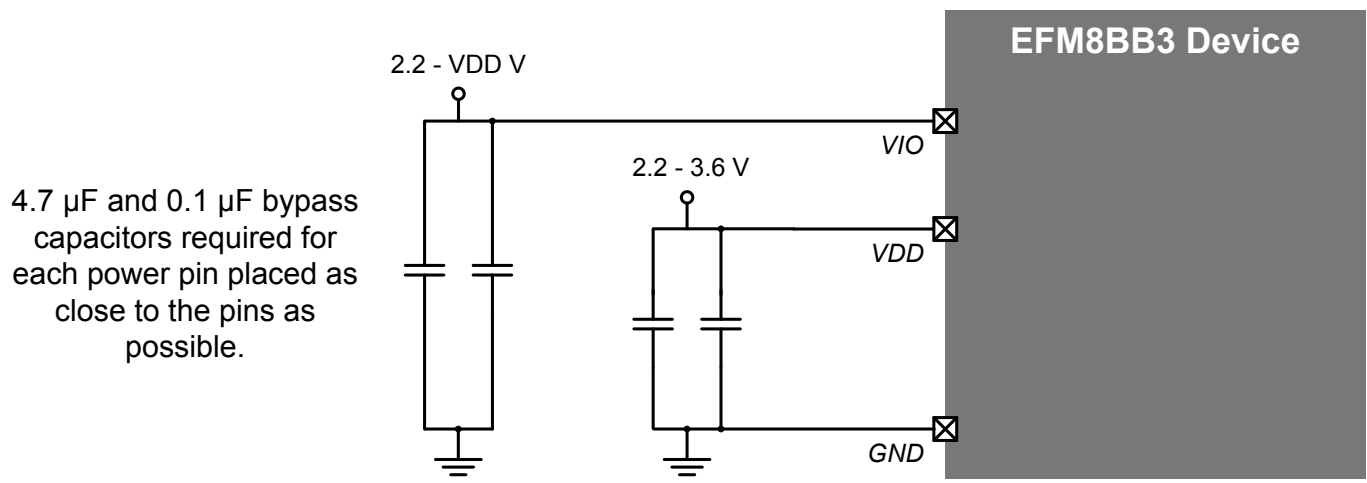


Figure 5.1. Power Connection Diagram

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in *AN124: Pin Sharing Techniques for the C2 Interface*. Application notes can be found on the Silicon Labs website (<http://www.silabs.com/8bit-appnotes>) or in Simplicity Studio.

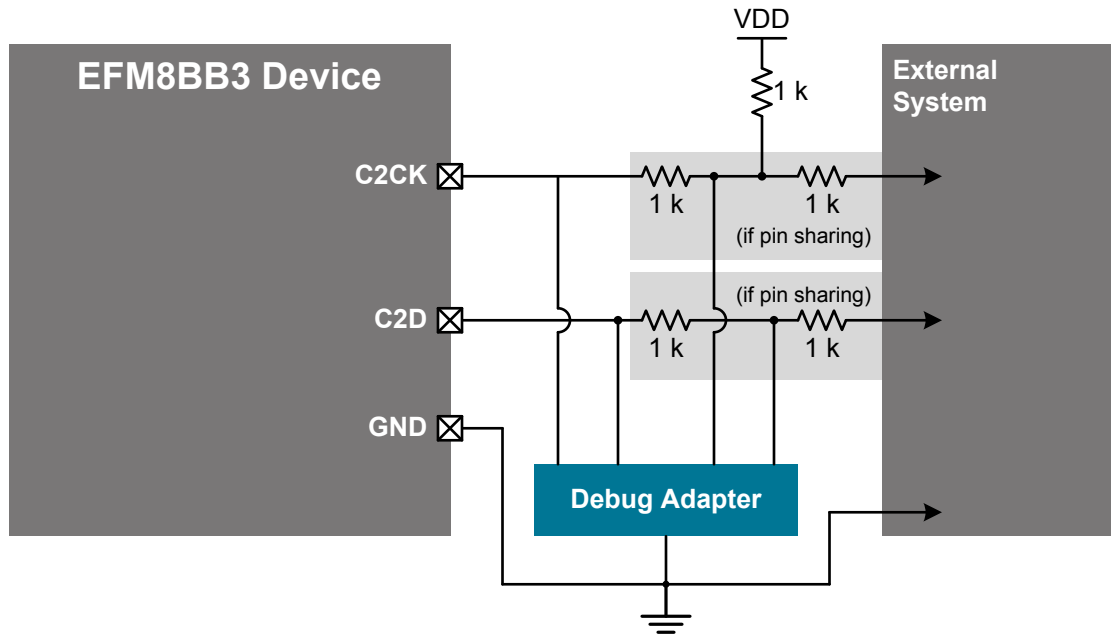


Figure 5.2. Debug Connection Diagram

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN203: "8-bit MCU Printed Circuit Board Design Notes" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

6. Pin Definitions

6.1 EFM8BB3x-QFN32 and EFM8BB3x-5QFN32 Pin Definitions

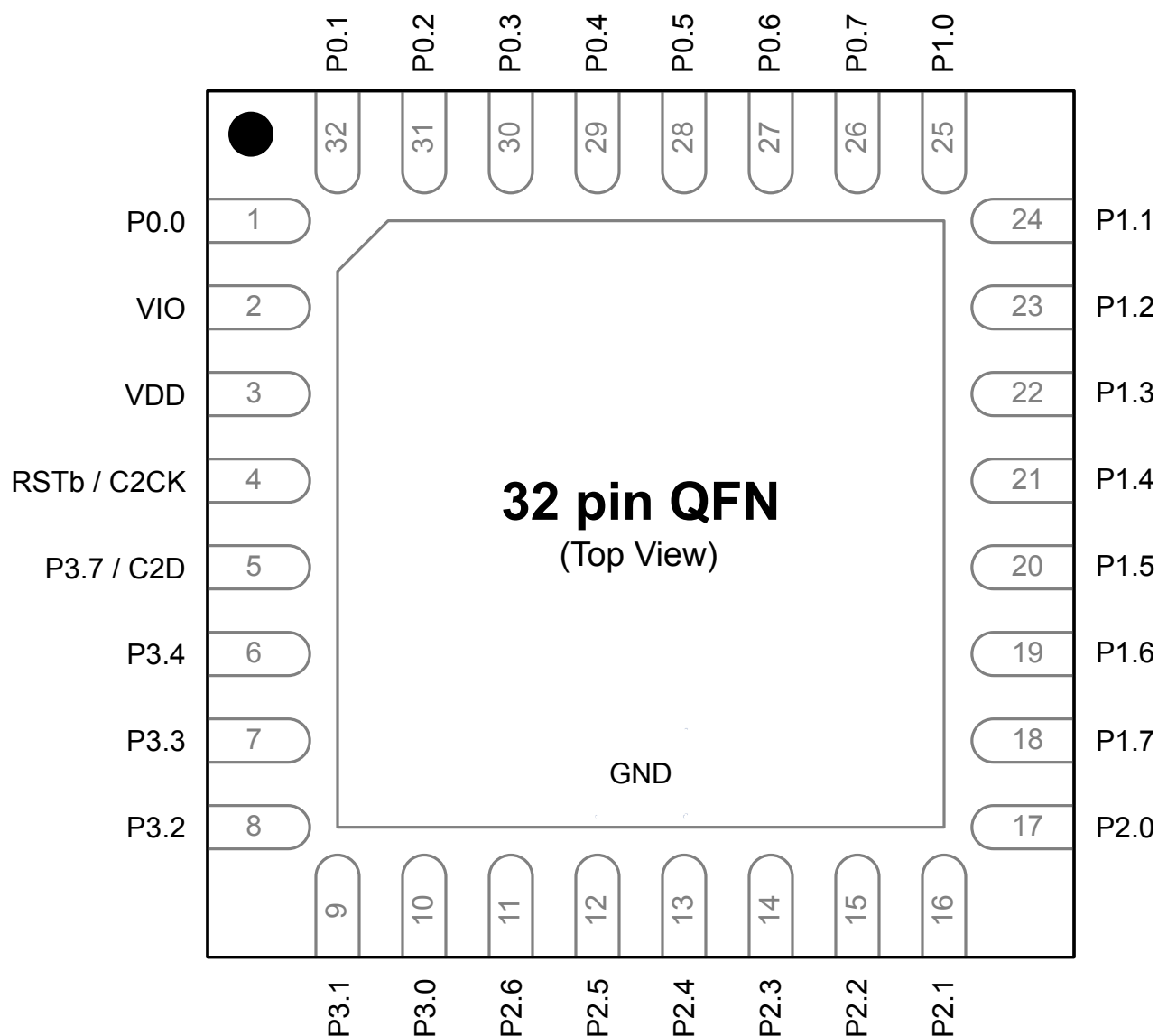


Figure 6.1. EFM8BB3x-QFN32 (QFN32-GI) and EFM8BB3x-5QFN32 (QFN32-AI) Pinout

Table 6.1. Pin Definitions for EFM8BB3x-QFN32 (QFN32-GI) and EFM8BB3x-5QFN32 (QFN32-AI)

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
2	VIO	I/O Supply Power Input			
3	VDD	Supply Power Input			
4	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
5	P3.7 / C2D	Multifunction I/O / C2 Debug Data			
6	P3.4	Multifunction I/O			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19 CMP1P.8 CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18 CMP1P.7 CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17 CMP1P.6 CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	ADC0.16 CMP1P.5 CMP1N.5

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7 CMP0P.7 CMP0N.7
25	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU1OUT CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6 CMP0P.6 CMP0N.6 CMP1P.1 CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.0 CMP1N.0
27	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
28	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.3 CMP0P.3 CMP0N.3
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	EXTOSC
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
Center	GND	Ground			

6.2 EFM8BB3x-QFP32 Pin Definitions

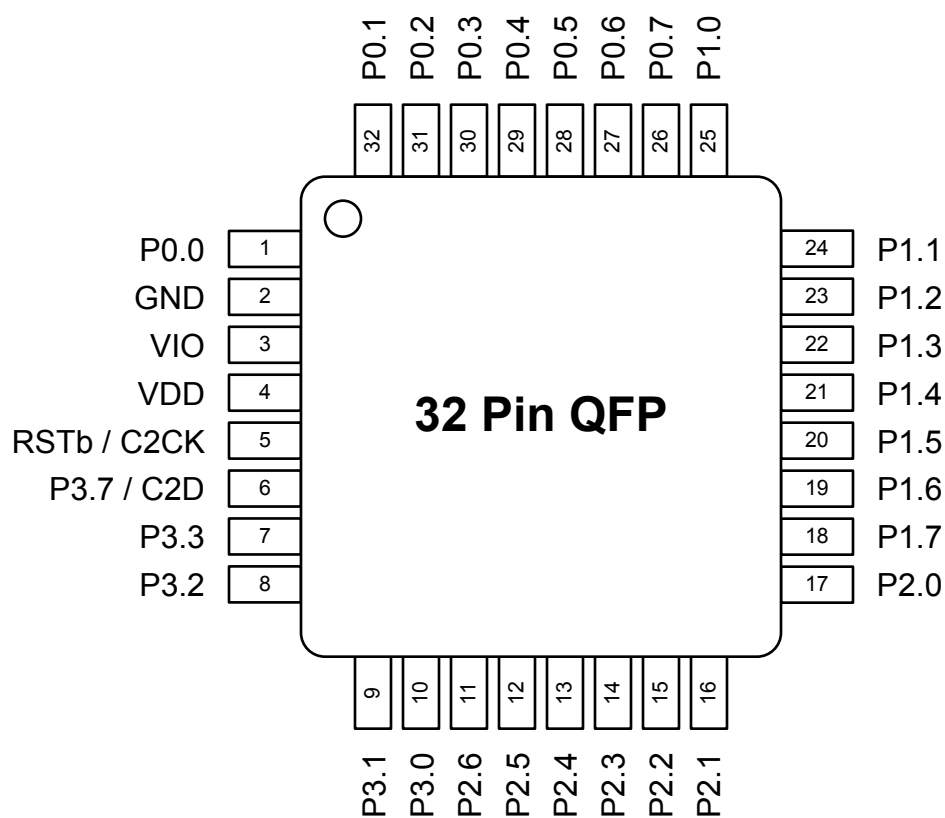


Figure 6.2. EFM8BB3x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8BB3x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
2	GND	Ground			
3	VIO	I/O Supply Power Input			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
6	P3.7 / C2D	Multifunction I/O / C2 Debug Data			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19 CMP1P.8 CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18 CMP1P.7 CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17 CMP1P.6 CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	ADC0.16 CMP1P.5 CMP1N.5
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7 CMP0P.7 CMP0N.7

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
25	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU1OUT CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6 CMP0P.6 CMP0N.6 CMP1P.1 CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.0 CMP1N.0
27	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4
28	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.3 CMP0P.3 CMP0N.3
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	EXTOSC
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

6.3 EFM8BB3x-QFN24 and EFM8BB3x-4QFN24 Pin Definitions

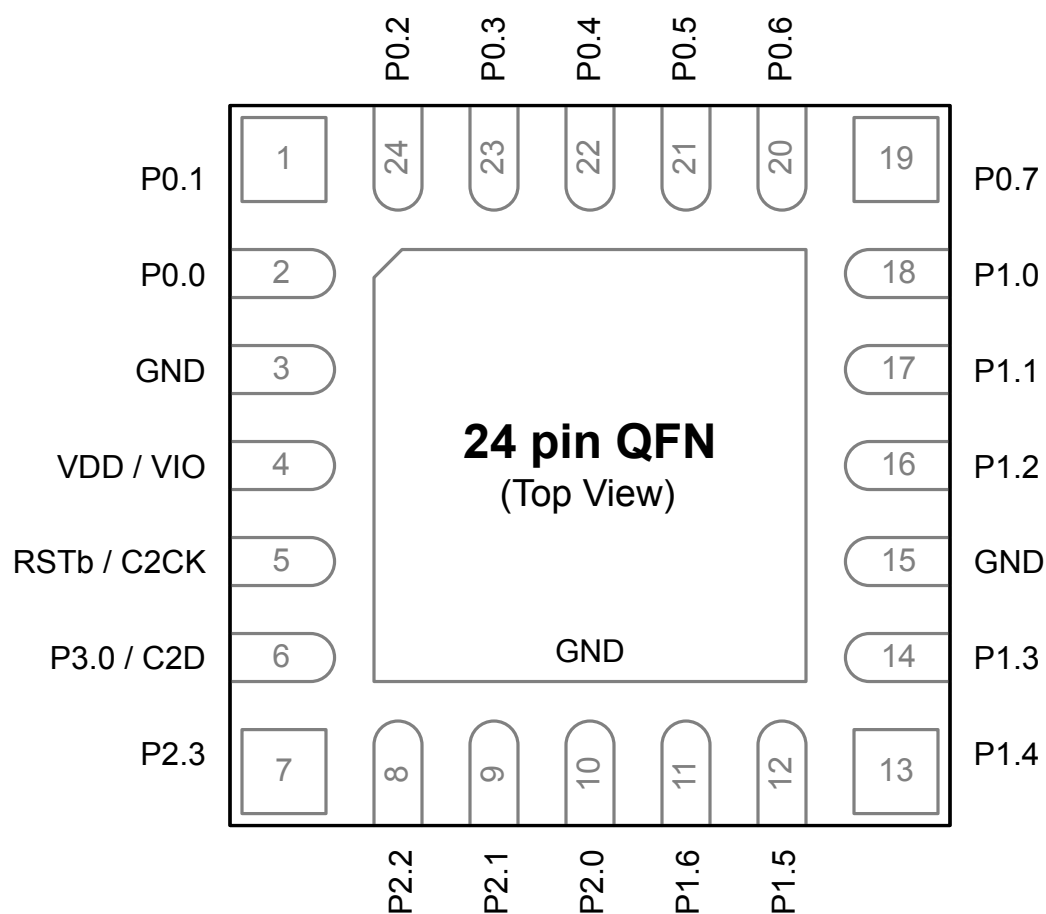


Figure 6.3. EFM8BB3x-QFN24 (QFN24-GI) and EFM8BB3x-4QFN24 (QFN24-AI) Pinout

Table 6.3. Pin Definitions for EFM8BB3x-QFN24 (QFN24-GI) and EFM8BB3x-4QFN24 (QFN24-AI)

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
3	GND	Ground			
4	VDD / VIO	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
6	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
7	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	DAC3
8	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU1A.15 CLU2B.14 CLU3A.14	DAC2
9	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	DAC1
10	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	DAC0
11	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU3OUT CLU0A.15 CLU1B.12 CLU2A.12	ADC0.11 CMP1P.5 CMP1N.5

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
12	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU2OUT CLU0B.14 CLU1A.13 CLU2B.13	ADC0.10 CMP1P.4 CMP1N.4
13	P1.4	Multifunction I/O	Yes	P1MAT.4 I2C0_SCL CLU0A.14 CLU1A.12 CLU2B.12	ADC0.9 CMP1P.3 CMP1N.3
14	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SDA CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	CMP1P.2 CMP1N.2
15	GND	Ground			
16	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8
17	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7
18	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU1OUT CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.1 CMP1N.1
20	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4 CMP1P.0 CMP1N.0
21	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.3 CMP0P.3 CMP0N.3
22	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2
23	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	EXTOSC

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
24	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	ADC0.1 CMP0P.1 CMP0N.1
Center	GND	Ground			

6.4 EFM8BB3x-QSOP24 Pin Definitions

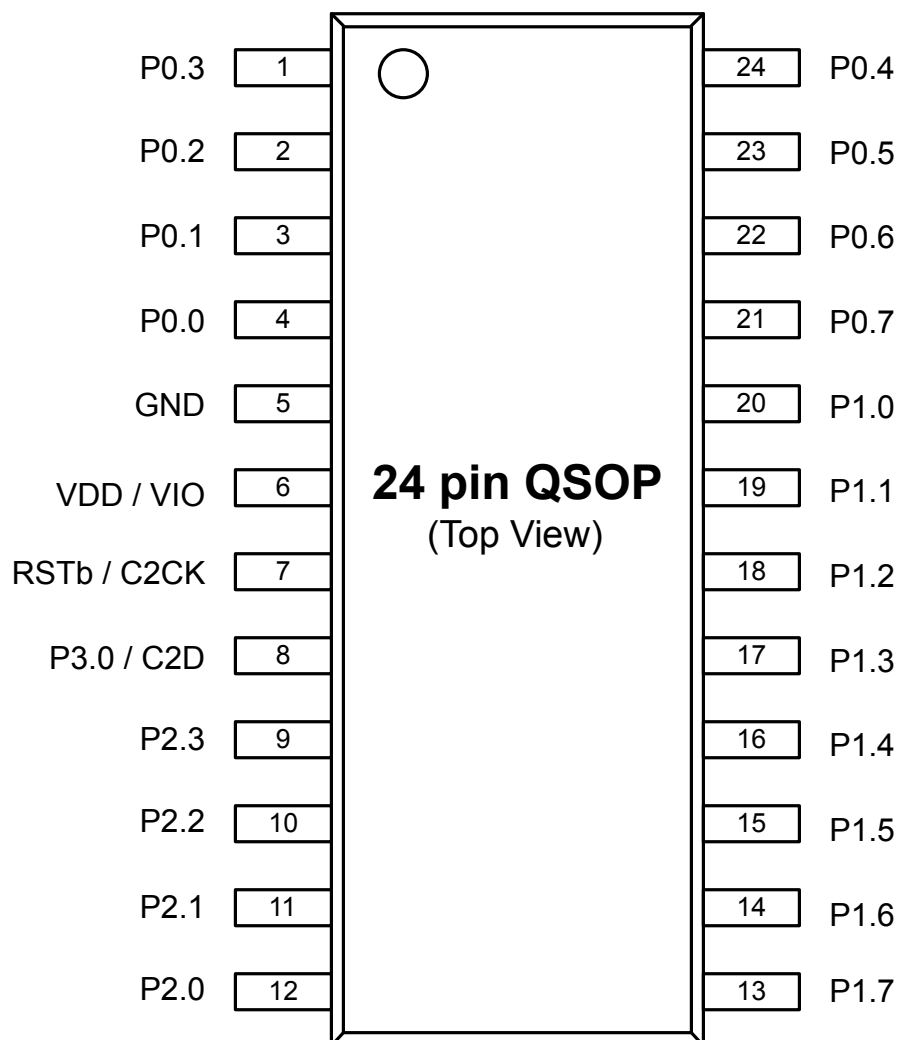


Figure 6.4. EFM8BB3x-QSOP24 Pinout

Table 6.4. Pin Definitions for EFM8BB3x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	EXTOSC

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	ADC0.1 CMP0P.1 CMP0N.1
3	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
4	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
5	GND	Ground			
6	VDD / VIO	Supply Power Input			
7	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
8	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
9	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	DAC3
10	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU1A.15 CLU2B.14 CLU3A.14	DAC2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
11	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	DAC1
12	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	DAC0
13	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.12 CMP1P.6 CMP1N.6
14	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU3OUT CLU0A.15 CLU1B.12 CLU2A.12	ADC0.11 CMP1P.5 CMP1N.5
15	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU2OUT CLU0B.14 CLU1A.13 CLU2B.13	ADC0.10 CMP1P.4 CMP1N.4
16	P1.4	Multifunction I/O	Yes	P1MAT.4 I2C0_SCL CLU0A.14 CLU1A.12 CLU2B.12	ADC0.9 CMP1P.3 CMP1N.3
17	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SDA CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	CMP1P.2 CMP1N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8
19	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7
20	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6
21	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU1OUT CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.1 CMP1N.1
22	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4 CMP1P.0 CMP1N.0

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
23	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.3 CMP0P.3 CMP0N.3
24	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2

7. QFN32-GI Package Specifications

7.1 QFN32-GI Package Dimensions

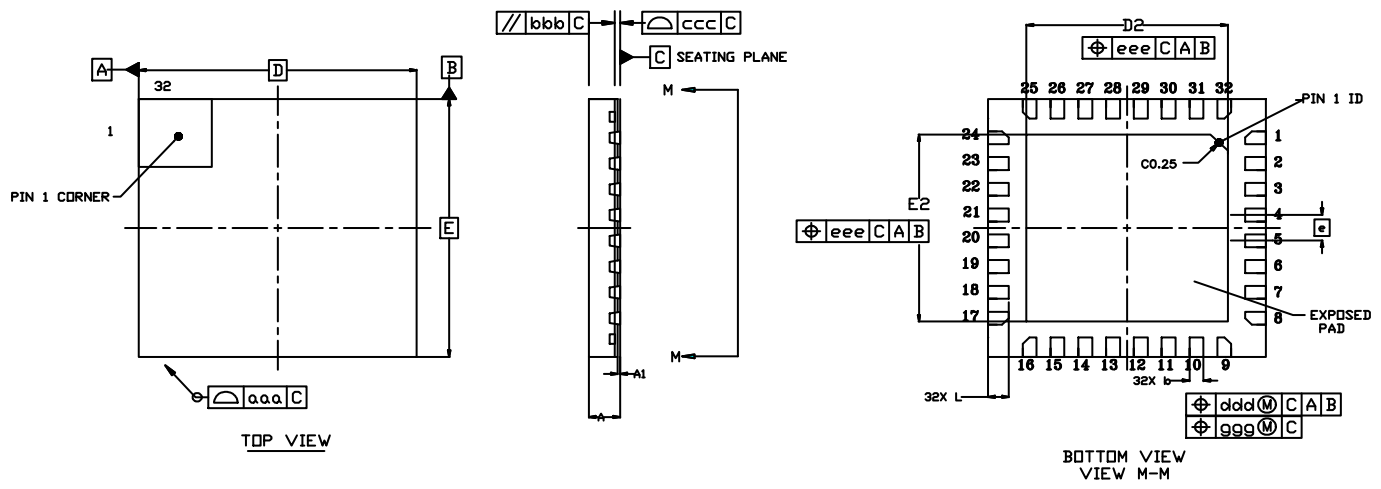


Figure 7.1. Package Drawing

Table 7.1. Package Dimensions

Dimension	Min	Typ	Max
A	0.45	0.50	0.55
A1	0.00	0.035	0.05
b	0.15	0.20	0.25
D	4.00 BSC.		
D2	2.80	2.90	3.00
e	0.40 BSC.		
E	4.00 BSC.		
E2	2.80	2.90	3.00
L	0.20	0.30	0.40
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10
ggg	—	—	0.05

Dimension	Min	Typ	Max
Note: - All dimensions shown are in millimeters (mm) unless otherwise noted. - Dimensioning and Tolerancing per ANSI Y14.5M-1994. - This drawing conforms to JEDEC Solid State Outline MO-220. - Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.			

7.2 QFN32-GI PCB Land Pattern

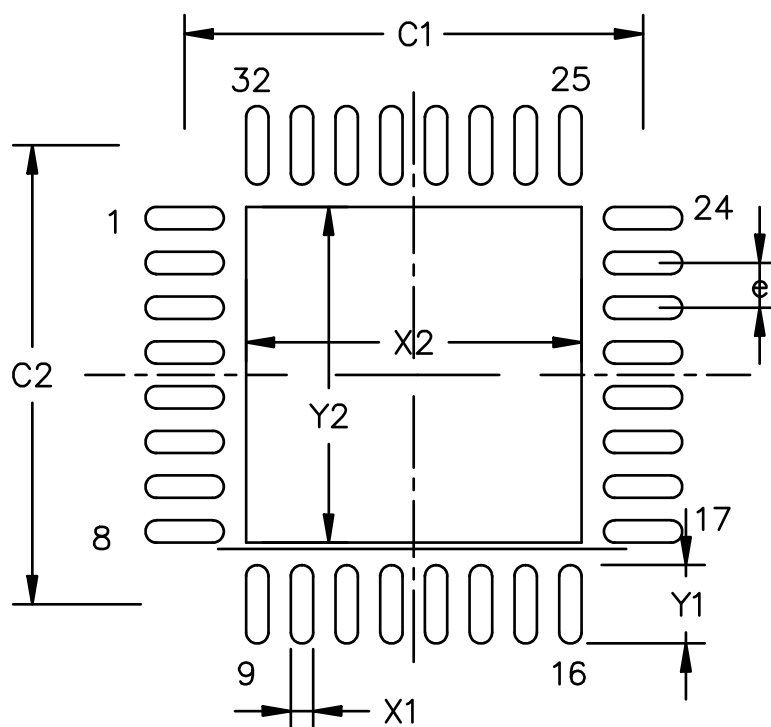


Figure 7.2. PCB Land Pattern Drawing

Table 7.2. PCB Land Pattern Dimensions

Dimension	Min	Max
C1	—	4.10
C2	—	4.10
X1	—	0.2
X2	—	3.0
Y1	—	0.7
Y2	—	3.0
e	—	0.4

Dimension	Min	Max
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification. 3. This Land Pattern Design is based on the IPC-7351 guidelines. 4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm. 5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. 6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 7. The stencil thickness should be 0.125 mm (5 mils). 8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 9. A 2 x 2 array of 1.10 mm square openings on a 1.30 mm pitch should be used for the center pad. 10. A No-Clean, Type-3 solder paste is recommended. 11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.		

7.3 QFN32-GI Package Marking

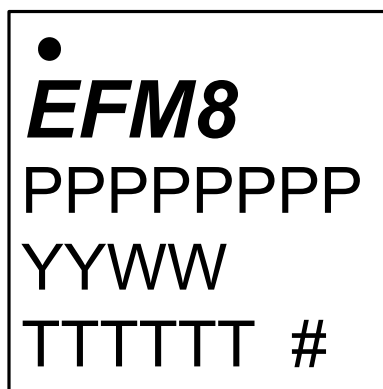


Figure 7.3. Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

8. QFN32-AI Package Specifications

8.1 QFN32-AI Package Dimensions

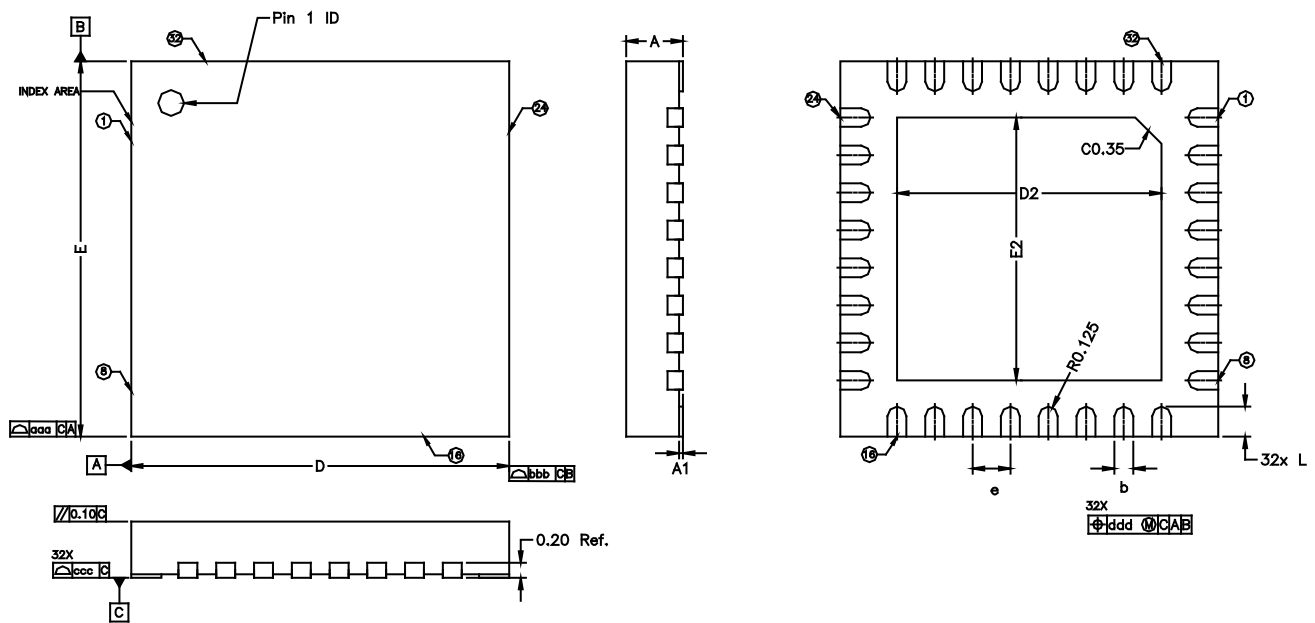


Figure 8.1. Package Drawing

Table 8.1. Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
D	5.00 BSC		
D2	3.40	3.50	3.60
e	0.50 BSC		
E	5.00 BSC		
E2	3.40	3.50	3.60
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.10		

Dimension	Min	Typ	Max
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.			

8.2 QFN32-AI PCB Land Pattern

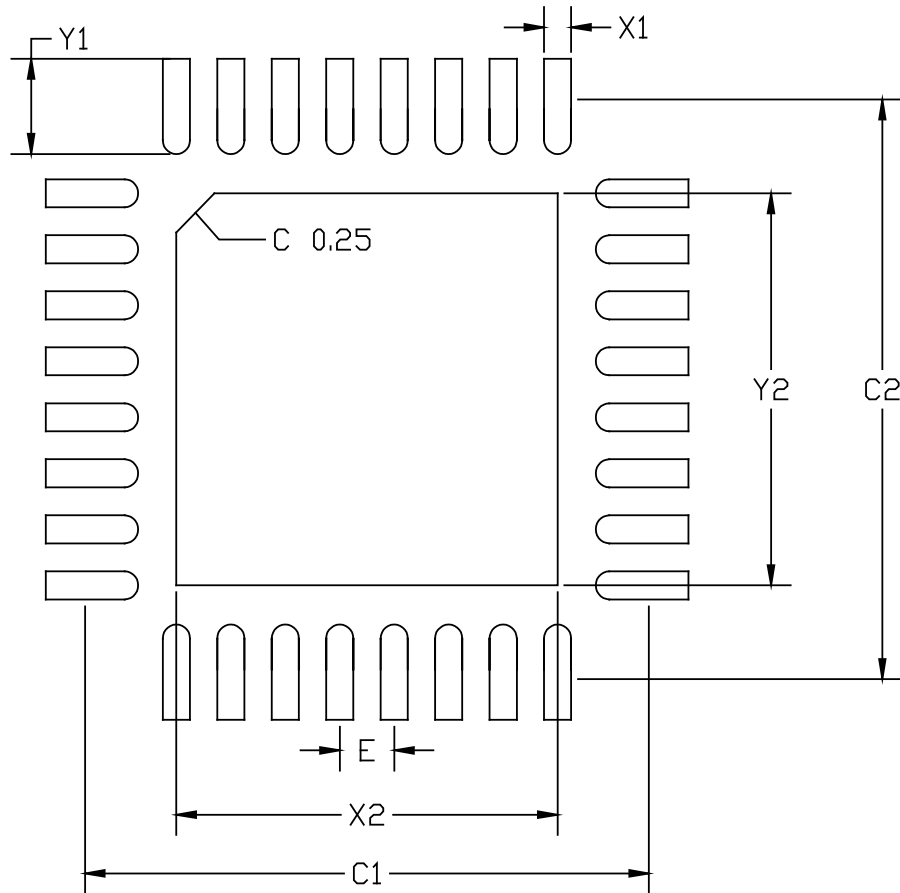


Figure 8.2. PCB Land Pattern Drawing

Table 8.2. PCB Land Pattern Dimensions

Dimension	mm
C1	4.90
C2	4.90
E	0.50
X1	0.30
Y1	0.85
X2	3.60
Y2	3.60

Dimension	mm
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This land pattern design is based on the IPC-7351 guidelines. 3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. 4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 5. The stencil thickness should be 0.125 mm (5 mils). 6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 7. A 2x2 array of 0.9 mm square openings on 1.2 mm pitch should be used for the center ground pad. 8. A No-Clean, Type-3 solder paste is recommended. 9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.	

8.3 QFN32-AI Package Marking

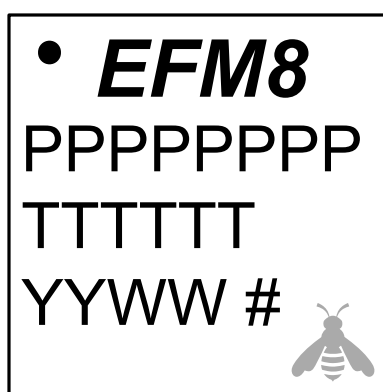


Figure 8.3. Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

9. QFP32 Package Specifications

9.1 QFP32 Package Dimensions

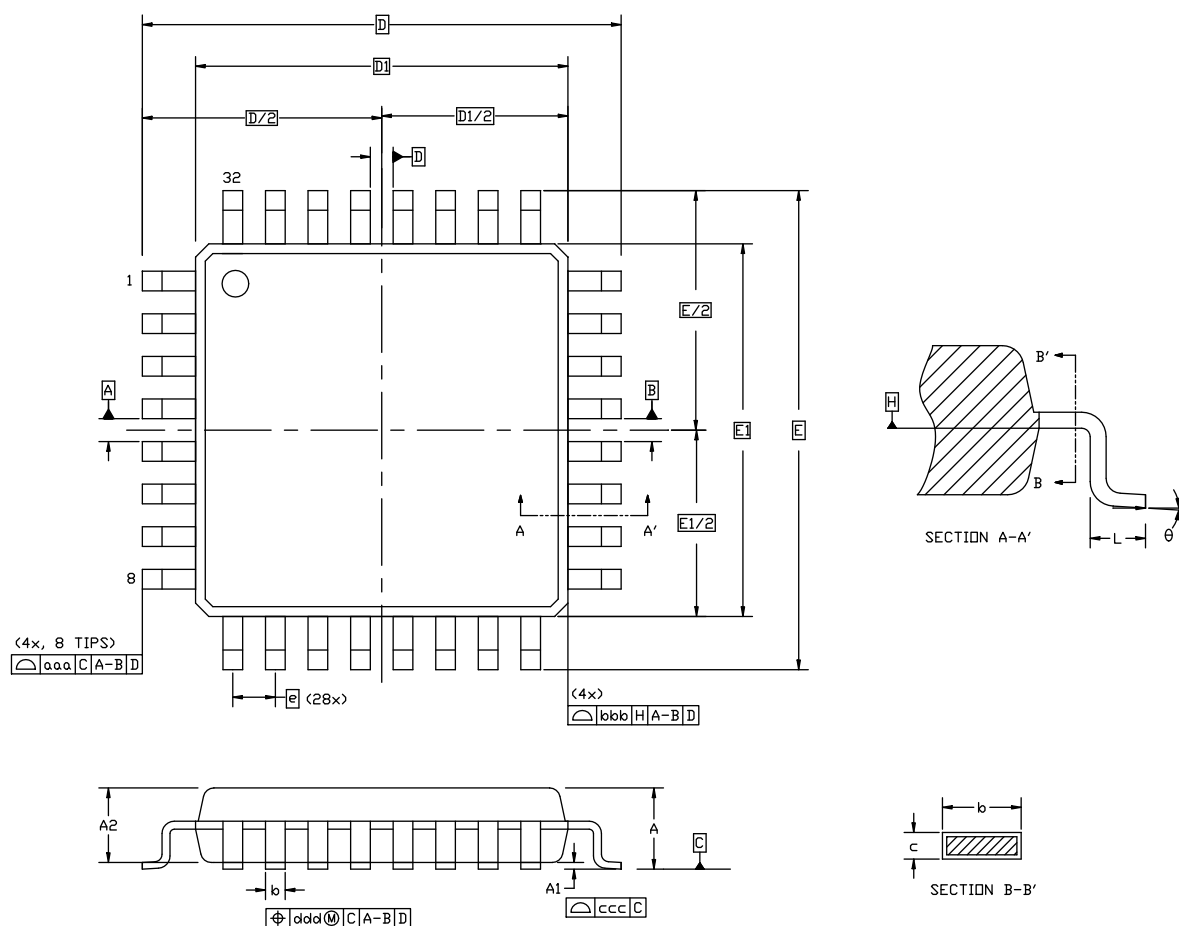


Figure 9.1. Package Drawing

Table 9.1. Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.30	0.37	0.45
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.80 BSC		
E	9.00 BSC		

Dimension	Min	Typ	Max
E1	7.00 BSC		
L	0.50	0.60	0.70
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
theta	0°	3.5°	7°
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 3. This drawing conforms to JEDEC outline MS-026. 4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.			

9.2 QFP32 PCB Land Pattern

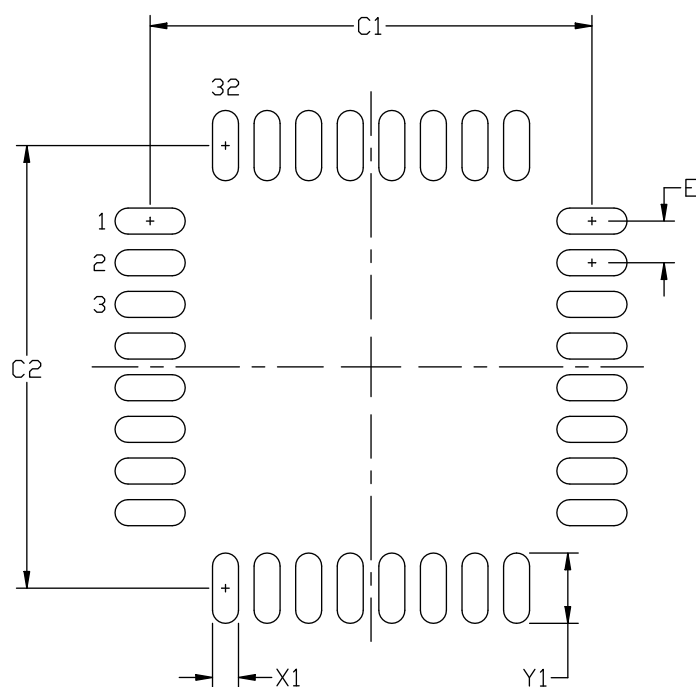


Figure 9.2. PCB Land Pattern Drawing

Table 9.2. PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.55	
Y1	1.5	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.3 QFP32 Package Marking

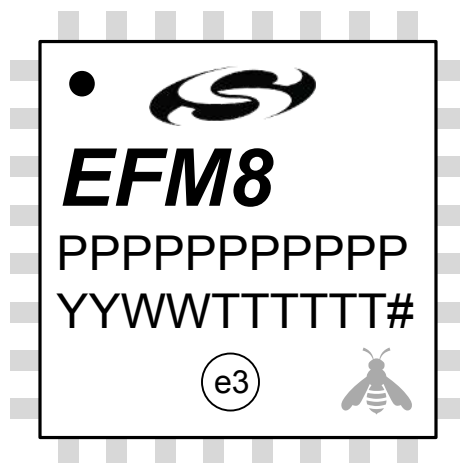


Figure 9.3. Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

10. QFN24-GI Package Specifications

10.1 QFN24-GI Package Dimensions

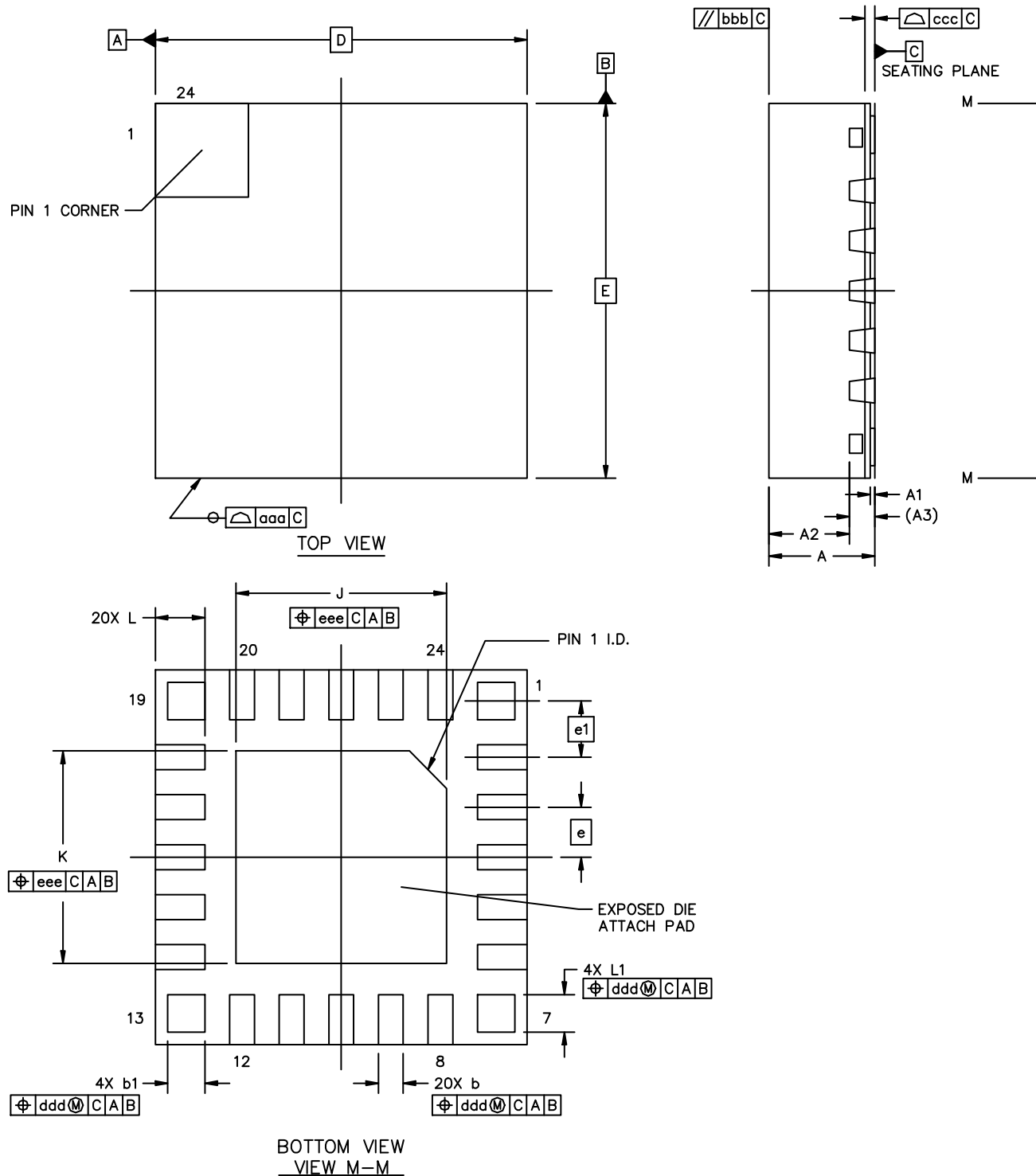


Table 10.1. Package Dimensions

Dimension	Min	Typ	Max
A	0.8	0.85	0.9
A1	0.00	—	0.05
A2	—	0.65	—
A3	0.203 REF		
b	0.15	0.2	0.25
b1	0.25	0.3	0.35
D	3.00 BSC		
E	3.00 BSC		
e	0.40 BSC		
e1	0.45 BSC		
J	1.60	1.70	1.80
K	1.60	1.70	1.80
L	0.35	0.40	0.45
L1	0.25	0.30	0.35
aaa	—	0.10	—
bbb	—	0.10	—
ccc	—	0.08	—
ddd	—	0.1	—
eee	—	0.1	—

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-248 but includes custom features which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2 QFN24 PCB Land Pattern

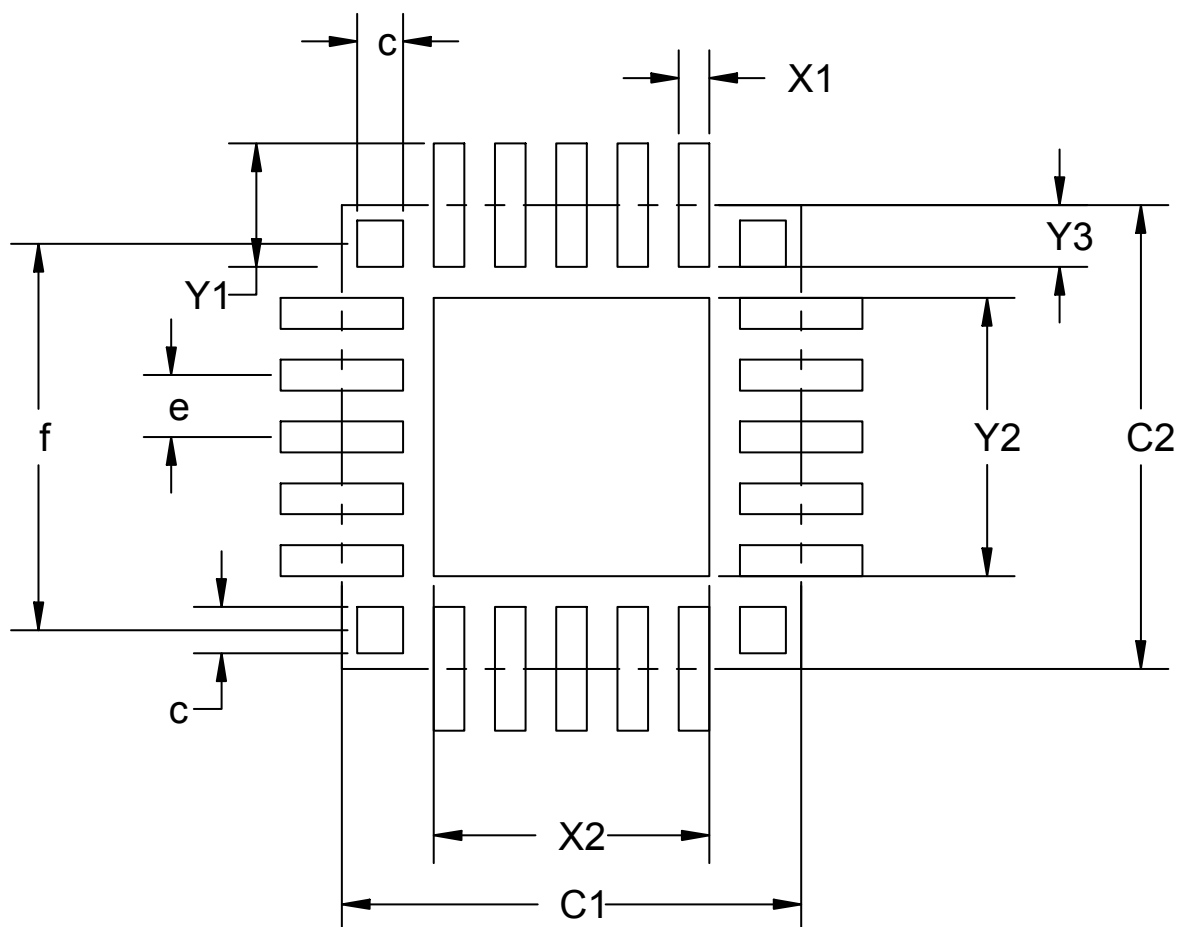


Figure 10.2. PCB Land Pattern Drawing

Table 10.2. PCB Land Pattern Dimensions

Dimension	Min	Max
C1		3.00
C2		3.00
e		0.4 REF
X1		0.20
X2		1.80
Y1		0.80
Y2		1.80
Y3		0.4
f		2.50 REF

Dimension	Min	Max
c	0.25	0.35

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-SM-782 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
8. A 2 x 1 array of 0.7 mm x 1.6 mm openings on a 0.9 mm pitch should be used for the center pad.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.3 QFN24 Package Marking

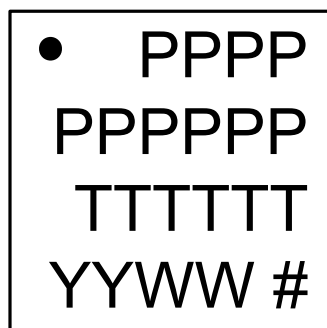


Figure 10.3. Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

11. QFN24-AI Package Specifications

11.1 QFN24 Package Dimensions

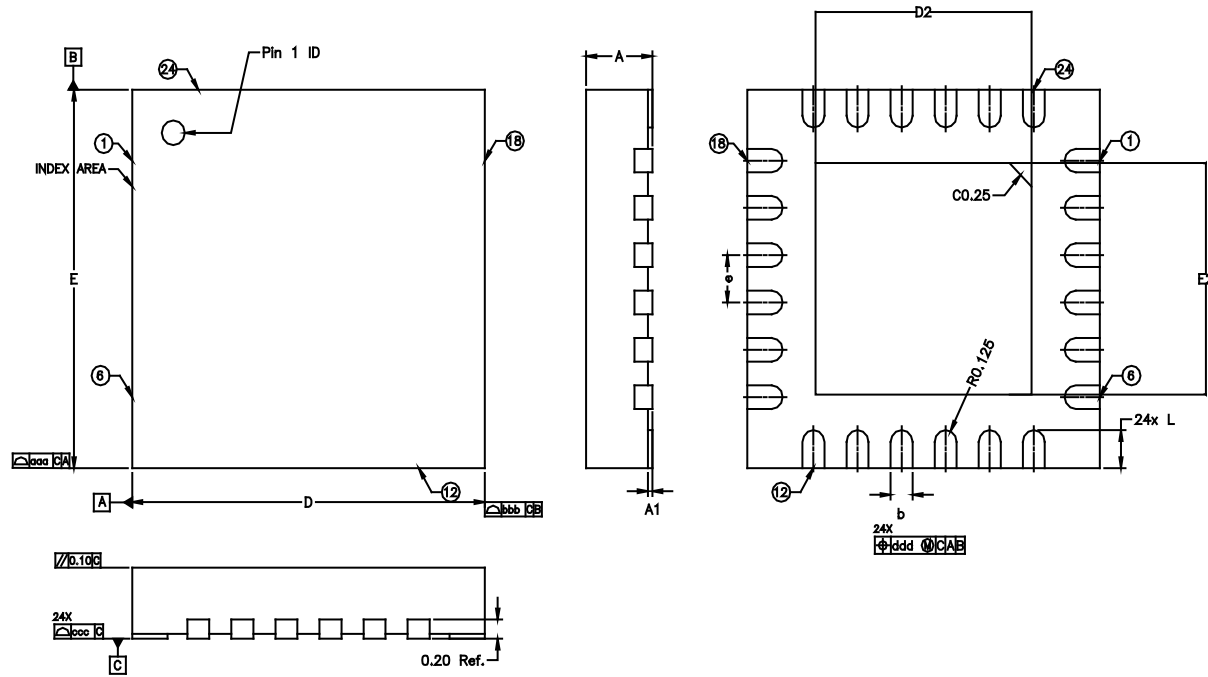


Figure 11.1. Package Drawing

Table 11.1. Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
D	4.00 BSC		
D2	2.35	2.45	2.55
e	0.50 BSC		
E	4.00 BSC		
E2	2.35	2.45	2.55
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.10		

Dimension	Min	Typ	Max
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.			

11.2 QFN24 PCB Land Pattern

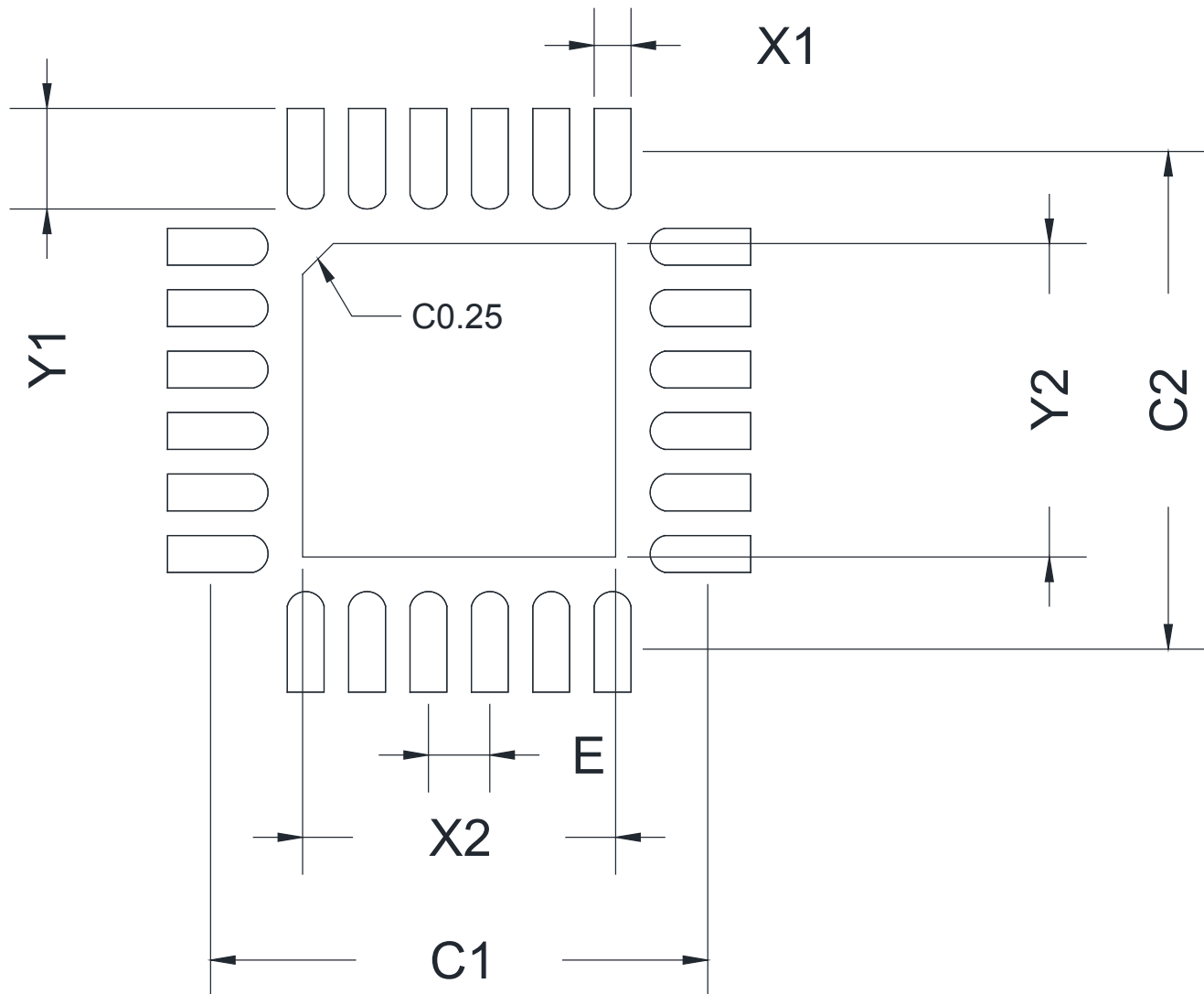


Figure 11.2. PCB Land Pattern Drawing

Table 11.2. PCB Land Pattern Dimensions

Dimension	Min	Max
C1		3.90
C2		3.90
E		0.50
X1		0.30
X2		2.55
Y1		0.85
Y2		2.55

Dimension	Min	Max
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This Land Pattern Design is based on the IPC-7351 guidelines. 3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. 4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 5. The stencil thickness should be 0.125 mm (5 mils). 6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 7. A 2 x 2 array of 0.9 mm square openings on a 1.2 mm pitch should be used for the center pad. 8. A No-Clean, Type-3 solder paste is recommended. 9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.		

11.3 QFN24 Package Marking



Figure 11.3. Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

12. QSOP24 Package Specifications

12.1 QSOP24 Package Dimensions

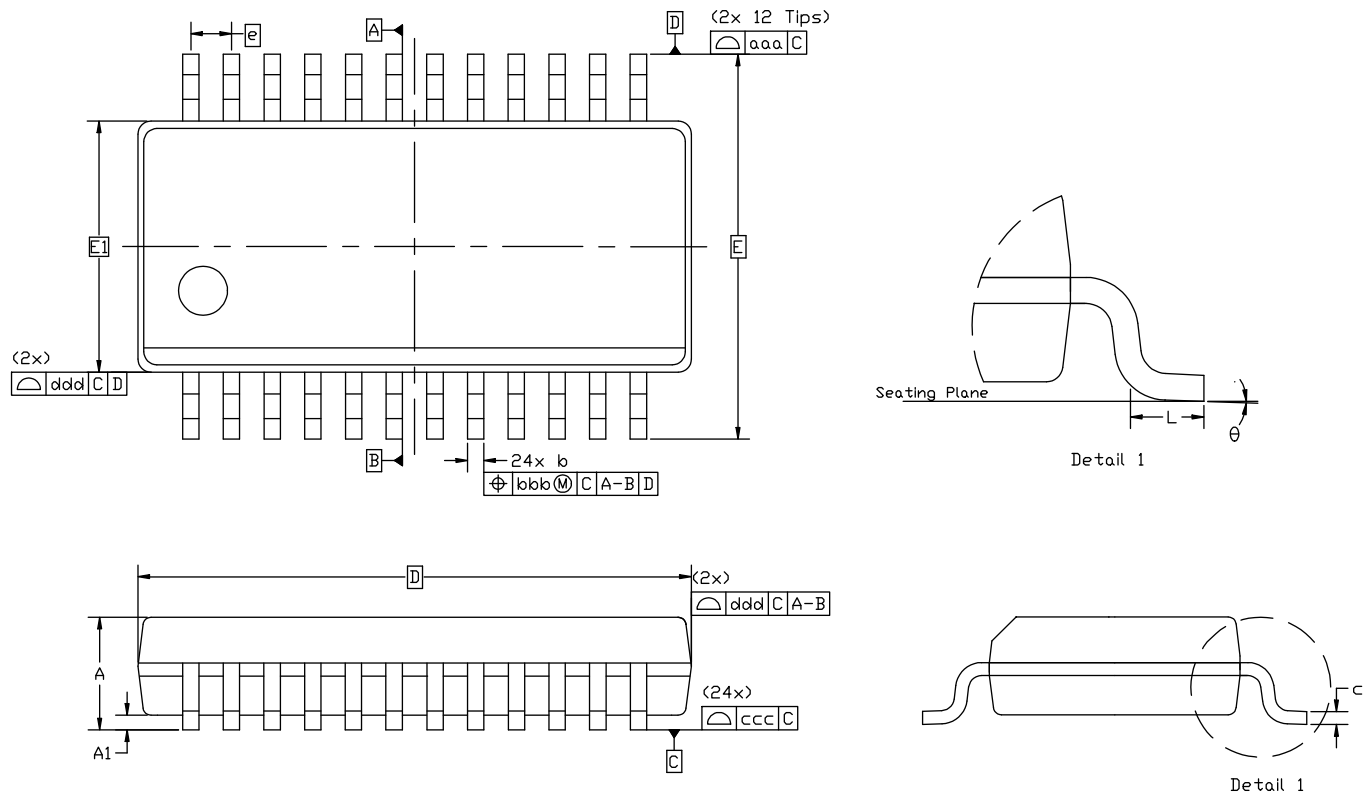


Figure 12.1. Package Drawing

Table 12.1. Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27

Dimension	Min	Typ	Max
theta	0°	—	8°
aaa	0.20		
bbb	0.18		
ccc	0.10		
ddd	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12.2 QSOP24 PCB Land Pattern

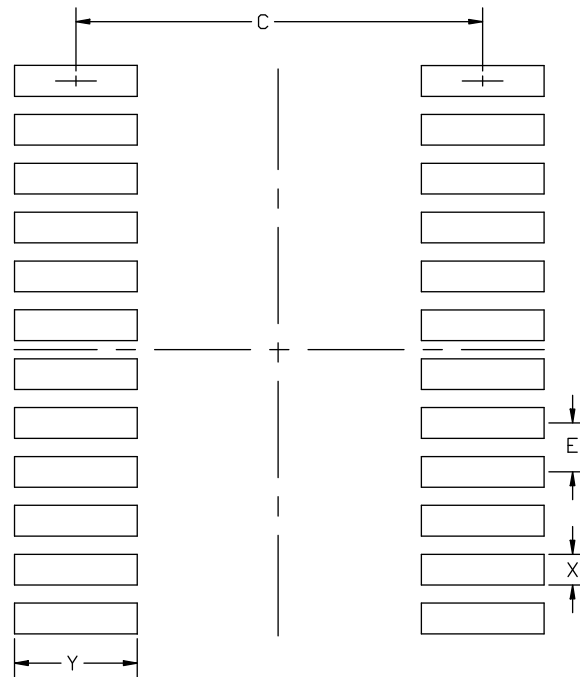


Figure 12.2. PCB Land Pattern Drawing

Table 12.2. PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12.3 QSOP24 Package Marking



Figure 12.3. Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

13. Revision History

13.1 Revision 1.6

October, 2025

- Moved select parts to NRND in [Table 2.1 Product Selection Guide on page 3](#).

13.2 Revision 1.5

March, 2024

- Noted that all QSOP Package OPNs are EOL.
- Added missing [4.1.18 SPI](#) electrical specifications.

13.3 Revision 1.4

October, 2020

- Updated ordering part numbers to revision D.
- Restored crystal oscillator in [1. Feature List](#), [Figure 3.1 Detailed EFM8BB3 Block Diagram on page 9](#), and [3.4 Clocking](#) as it is again available on revision D.
- Restored crystal frequency and current specifications to [Table 4.8 External Oscillator on page 25](#).
- Added Input Leakage (Pullups off or Analog) current for A-grade devices and I- and G-grade devices in [Table 4.16 Port I/O on page 34](#).
- Corrected typos and made minor edits throughout the document.

13.4 Revision 1.3

December, 2018

- Updated ordering part numbers to revision C.
- Updated [1. Feature List](#), [Figure 3.1 Detailed EFM8BB3 Block Diagram on page 9](#), and [3.4 Clocking](#) to removed external crystal oscillator as clock source.
- Updated [Table 4.8 External Oscillator on page 25](#) for RC oscillator specifications.
- Updated [3.1 Introduction](#) to mention all device documentation.
- Updated [4.1.1 Recommended Operating Conditions](#) to remove the "GPIO levels are undefined whenever VIO is less than 1 V" note, added a new minimum for VIO, and added a note referencing [4.1.16 Port I/O](#).
- Updated [3.10 Bootloader](#) recommendations for production programming.
- Added more information about documentation to the [3.1 Introduction](#) section.
- Removed all references to XTAL and renamed it to EXTOSC.

13.5 Revision 1.2

June, 2017

- Added A-grade devices and additional I-grade devices.
- Added the packages for the A-grade and new I-grade devices (QFN24-AI and QFN32-AI).
- Renamed the existing QFN24 and QFN32 packages to QFN24-GI and QFN32-GI.
- Added a note to [Table 4.2 Power Consumption on page 20](#) providing more information about the Comparator Reference specification.

13.6 Revision 1.1

March, 2017

- Added [4.1.12 1.8 V Internal LDO Voltage Regulator](#).
- Updated the Integral Nonlinearity second row conditions to "DAC1 and DAC3" instead of "DAC0 and DAC3" in [4.1.13 DACs](#).
- Fixed the Symbol and Test Condition values for Output Noise in [4.1.13 DACs](#).
- Added a note to [4.1.9 ADC](#) specifying the production test VREF and ground setup.
- Added Output Voltage and Output Current specifications to [4.1.13 DACs](#).
- Updated the language in [1. Feature List](#) to clarify the package offerings for each of the different temperature grades.
- Updated the minimum VIO displayed in [Figure 5.1 Power Connection Diagram on page 41](#) to match the specification in [4.1.1 Recommended Operating Conditions](#).
- Added a note to [3.1 Introduction](#) referencing the Reference Manual.
- Corrected the application note number for *AN124: Pin Sharing Techniques for the C2 Interface* in [5.2 Debug](#).
- Adjusted the Data Hold and Data Setup Times in [4.1.17 SMBus](#) and added a note referring to the DLYEXT bit.

13.7 Revision 1.01

October, 2016

- Updated [Figure 2.1 EFM8BB3 Part Numbering on page 3](#) to include the I-grade description.
- Updated QFN24 center pad stencil description.

13.8 Revision 1.0

September, 2016

- Filled in all TBD values in [4. Electrical Specifications](#).
- Added a note regarding which DACs are available to [Table 2.1 Product Selection Guide on page 3](#).
- Added specifications for [4.1.17 SMBus](#).
- Added bootloader pinout information to [3.10 Bootloader](#).
- Added CRC Calculation Time to [4.1.4 Flash Memory](#).

13.9 Revision 0.4

May, 2016

- Filled in TBD values for DAC Integral Nonlinearity in [Table 4.13 DACs on page 31](#).
- Added I-grade devices.
- Adjusted the Total Current Sunk into Supply Pin and Total Current Sourced out of Ground Pin specifications in [4.3 Absolute Maximum Ratings](#).
- Added Operating Junction Temperature specification to [4.3 Absolute Maximum Ratings](#).

13.10 Revision 0.3

February, 2016

- Added EFM8831F16G-A-QFN24 to [Table 2.1 Product Selection Guide on page 3](#).
- Updated [Figure 5.2 Debug Connection Diagram on page 42](#) to move the pull-up resistor on C2D / RSTb to after the series resistor instead of before.
- Added mention of the pre-programmed bootloader in [1. Feature List](#).
- Added a reference to *AN945: EFM8 Factory Bootloader User Guide* in [3.10 Bootloader](#).
- Updated all part numbers to revision B.
- Adjusted C1, C2, X2, Y2, and Y1 maximums for [7.2 QFN32-GI PCB Land Pattern](#).
- Adjusted package markings for QFN32 and QSOP24 packages.
- Filled in TBD minimum and maximum values for DAC Differential Nonlinearity in [Table 4.13 DACs on page 31](#).

13.11 Revision 0.2

September, 2017

- Added information on the bootloader to [3.10 Bootloader](#).
- Updated some characterization TBD values.

13.12 Revision 0.1

April, 2015

- Initial release.

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