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Product Reference Information

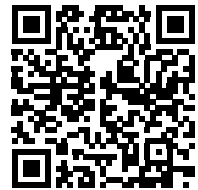
Part Number: EFM8BB21F16G-B-QSOP24
Manufacturer: Silicon Labs
Package: 24-SSOP (0.154", 3.90mm Width)
Availability: Please confirm with sales

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

EFM8 Busy Bee Family

EFM8BB2 Data Sheet

The EFM8BB2, part of the Busy Bee family of MCUs, is a multi-purpose line of 8-bit microcontrollers with a comprehensive feature set in small packages.

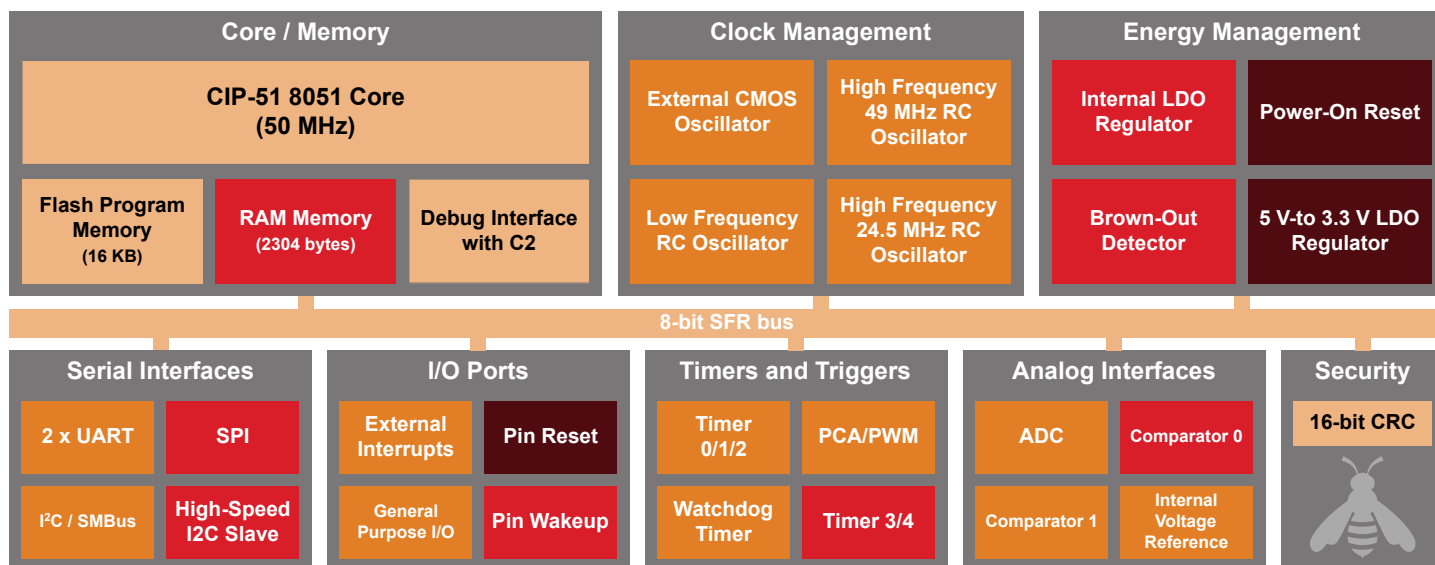
These devices offer high-value by integrating advanced analog and enhanced high-speed communication peripherals into small packages, making them ideal for space-constrained applications. With an efficient 8051 core, enhanced pulse-width modulation, and precision analog, the EFM8BB2 family is also optimal for embedded applications.

EFM8BB2 applications include the following:

- Motor control
- Consumer electronics
- Sensor controllers
- Medical equipment
- Lighting systems
- High-speed communication hub

KEY FEATURES

- Pipelined 8-bit C8051 core with 50 MHz maximum operating frequency
- Up to 22 multifunction, 5 V tolerant I/O pins
- One 12-bit Analog to Digital converter (ADC)
- Two Low-current analog comparators with build-in DAC as reference input
- Integrated temperature sensor
- 3-channel PWM / PCA with special hardware kill/safe state capability
- Five 16-bit timers
- Two UARTs, SPI, SMBus/I2C master/slave and I2C slave
- Priority crossbar for flexible pin mapping



Lowest power mode with peripheral operational:

Normal
 Idle
 Suspend
 Snooze
 Shutdown

1. Feature List

The EFM8BB2 highlighted features are listed below.

- Core:
 - Pipelined CIP-51 Core
 - Fully compatible with standard 8051 instruction set
 - 70% of instructions execute in 1-2 clock cycles
 - 50 MHz maximum operating frequency
- Memory:
 - Up to 16 KB flash memory, in-system re-programmable from firmware, including 1 KB of 64-byte sectors and 15 KB of 512-byte sectors.
 - Up to 2304 bytes RAM (including 256 bytes standard 8051 RAM and 2048 bytes on-chip XRAM)
- Power:
 - 5 V-input LDO regulator
 - Internal LDO regulator for CPU core voltage
 - Power-on reset circuit and brownout detectors
- I/O: Up to 22 total multifunction I/O pins:
 - All pins 5 V tolerant under bias
 - Flexible peripheral crossbar for peripheral routing
 - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
 - Internal 49 MHz oscillator with accuracy of $\pm 1.5\%$
 - Internal 24.5 MHz oscillator with $\pm 2\%$ accuracy
 - Internal 80 kHz low-frequency oscillator
 - External CMOS clock option
- Timers/Counters and PWM:
 - 3-channel Programmable Counter Array (PCA) supporting PWM, capture/compare, and frequency output modes
 - 5 x 16-bit general-purpose timers
 - Independent watchdog timer, clocked from the low frequency oscillator
- Communications and Digital Peripherals:
 - 2 x UART, up to 3 Mbaud
 - SPI™ Master / Slave, up to 12 Mbps
 - SMBus™/I2C™ Master / Slave, up to 400 kbps
 - I2C High-Speed Slave, up to 3.4 Mbps
 - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
- Analog:
 - 12-Bit Analog-to-Digital Converter (ADC)
 - 2 x Low-current analog comparators with adjustable reference
- On-Chip, Non-Intrusive Debugging
 - Full memory and register inspection
 - Four hardware breakpoints, single-stepping
- Pre-loaded UART bootloader
- Temperature range -40 to 85 °C or -40 to 125 °C
 - Automotive grade available (requires PPAP)
- Single power supply of 2.2 to 3.6 V or 3.0 to 5.25 V
- QFN28, QSOP24, and QFN20 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB2 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Each device is specified for 2.2 to 3.6 V operation (or up to 5.25 V with the 5 V regulator option). Both the G-grade and I-grade devices are available in 28-pin QFN, 20-pin QFN, or 24-pin QSOP packages, and A-grade devices are available in 28-pin QFN or 20-pin QFN packages. All package options are lead-free and RoHS compliant.

2. Ordering Information

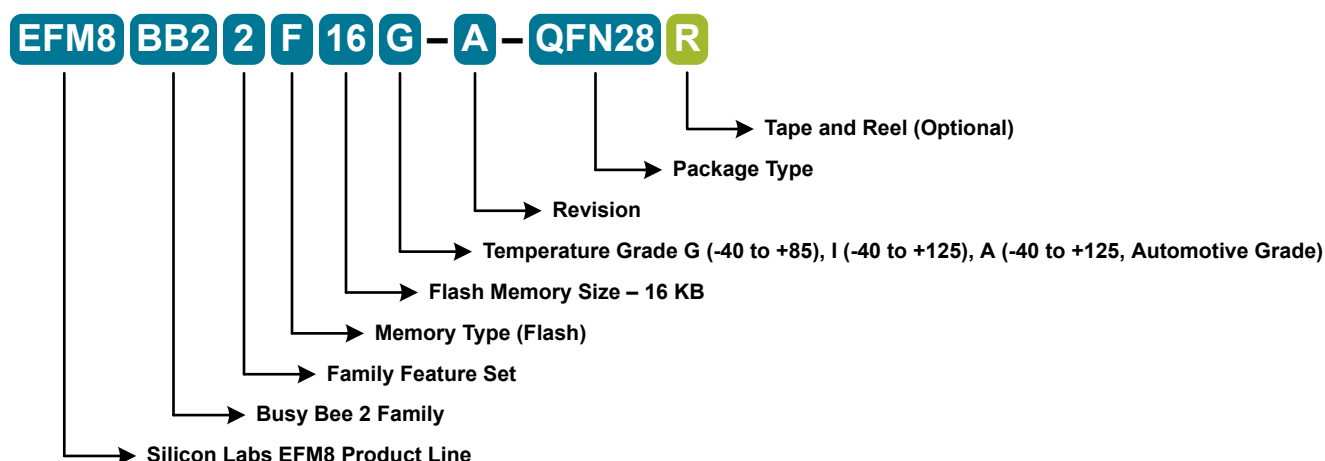


Figure 2.1. EFM8BB2 Part Numbering

All EFM8B2 family members have the following features:

- CIP-51 Core running up to 50 MHz
- Three Internal Oscillators (49 MHz, 24.5 MHz and 80 kHz)
- SMBus
- I2C Slave
- SPI
- 2 UARTs
- 3-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 5 16-bit Timers
- 2 Analog Comparators
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, and temperature sensor
- 16-bit CRC Unit
- AEC-Q100 qualified
- Pre-loaded UART bootloader

In addition to these features, each part number in the EFM8BB2 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (KB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	5-to-3.3 V Regulator	Temperature Range	Package
EFM8BB22F16G-C-QFN28	16	2304	22	20	10	12	Yes	Yes	-40 to +85 °C	QFN28
EFM8BB21F16G-C-QSOP24 ¹	16	2304	21	20	10	12	Yes	—	-40 to +85 °C	QSOP24
EFM8BB21F16G-C-QFN20	16	2304	16	15	10	7	Yes	—	-40 to +85 °C	QFN20
EFM8BB22F16I-C-QFN28	16	2304	22	20	10	12	Yes	Yes	-40 to +125 °C	QFN28

Ordering Part Number	Flash Memory (KB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	5-to-3.3 V Regulator	Temperature Range	Package
EFM8BB21F16I-C-QSOP24 ¹	16	2304	21	20	10	12	Yes	—	-40 to +125 °C	QSOP24
EFM8BB21F16I-C-QFN20	16	2304	16	15	10	7	Yes	—	-40 to +125 °C	QFN20
EFM8BB22F16A-C-QFN28 ²	16	2304	22	20	10	12	Yes	Yes	-40 to +125 °C	QFN28
EFM8BB21F16A-C-QFN20	16	2304	16	15	10	7	Yes	—	-40 to +125 °C	QFN20

Note:

1. End of life.
2. Not recommended for new designs (NRND).

The A-grade (i.e. EFM8BB21F16A-C-QFN20) devices receive full automotive quality production status, including AEC-Q100 qualification, registration with International Material Data System (IMDS), and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at www.silabs.com with a registered and NDA approved user account.

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3. System Overview

3.1 Introduction

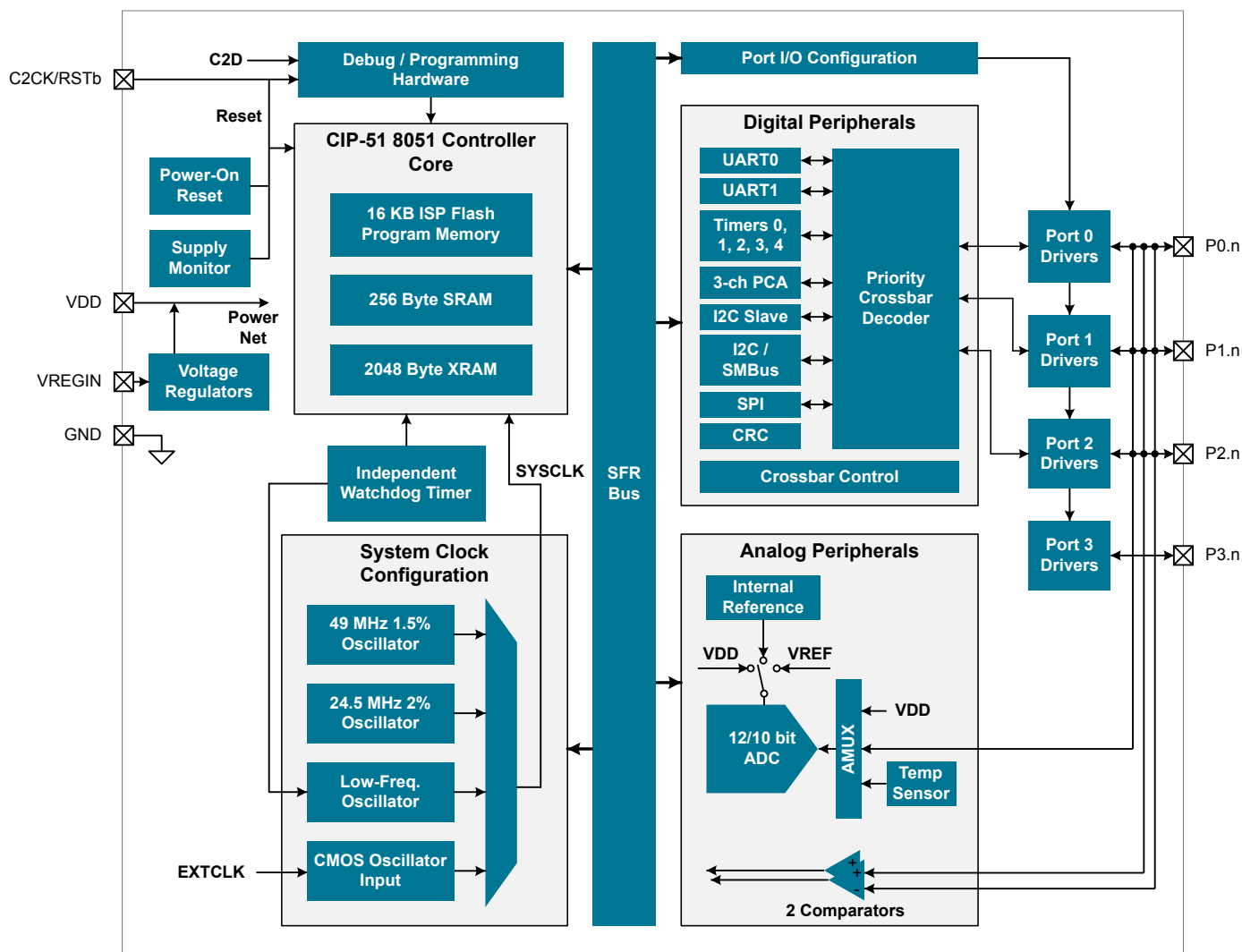


Figure 3.1. Detailed EFM8BB2 Block Diagram

This section describes the EFM8BB2 family at a high level.

For more information on the device packages and pinout, electrical specifications, and typical connection diagrams, see the EFM8BB2 Data Sheet. For more information on each module including register definitions, see the EFM8BB2 Reference Manual. For more information on any errata, see the EFM8BB2 Errata.

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	- Core halted - All peripherals clocked and fully operational - Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Suspend	- Core and peripheral clocks halted - HFOSC0 and HFOSC1 oscillators stopped - Regulators in normal bias mode for fast wake - Timer 3 and 4 may clock from LFOSC0 - Code resumes execution on wake event	- Switch SYSCLK to HFOSC0 - Set SUSPEND bit in PCON1	- Timer 4 Event - SPI0 Activity - I2C0 Slave Activity - Port Match Event - Comparator 0 Falling Edge
Stop	- All internal power nets shut down 5 V regulator remains active (if enabled) - Internal 1.8 V LDO on - Pins retain state - Exit on any reset source	- Clear STOPCF bit in REG0CN - Set STOP bit in PCON0	Any reset source
Snooze	- Core and peripheral clocks halted - HFOSC0 and HFOSC1 oscillators stopped - Regulators in low bias current mode for energy savings - Timer 3 and 4 may clock from LFOSC0 - Code resumes execution on wake event	- Switch SYSCLK to HFOSC0 - Set SNOOZE bit in PCON1	- Timer 4 Event - SPI0 Activity - I2C0 Slave Activity - Port Match Event - Comparator 0 Falling Edge
Shutdown	- All internal power nets shut down 5 V regulator remains active (if enabled) - Internal 1.8 V LDO off to save energy - Pins retain state - Exit on pin or power-on reset	- Set STOPCF bit in REG0CN - Set STOP bit in PCON0	- RSTb pin reset - Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.3 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P3.0 and P3.1 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0.

The port control block offers the following features:

- Up to 22 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 20 direct-pin interrupt sources with shared interrupt vector (Port Match).

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

The clock control system offers the following features:

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to $\pm 2\%$ over supply and temperature corners.
- 49 MHz internal oscillator (HFOSC1), accurate to $\pm 1.5\%$ over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External CMOS clock input (EXTCLK).
- Clock divider with eight settings for flexible clock scaling:
 - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.
 - HFOSC0 and HFOSC1 include 1.5x pre-scalers for further flexibility.

3.5 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to three independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0

Timers (Timer 0, Timer 1, Timer 2, Timer 3, and Timer 4)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3 and Timer 4 are 16-bit timers including the following features:

- Clock sources for all timers include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8.
- LFOSC0 divided by 8 may be used to clock Timer 3 and Timer 4 in active or suspend/snooze power modes.
- Timer 4 is a low-power wake source, and can be chained together with Timer 3
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- External pin capture
- LFOSC0 capture
- Comparator 0 capture

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- Programmable timeout interval
- Runs from the low-frequency oscillator
- Lock-out feature to prevent any modification until a system reset

3.6 Communications and Other Digital Peripherals

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- Single-byte FIFO on transmit and receive.

Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions.
- Dedicated baud rate generator supports baud rates up to $\text{SYSCLK}/2$ (transmit) or $\text{SYSCLK}/8$ (receive).
- 5, 6, 7, 8, or 9 bit data.
- Automatic start and stop generation.
- Automatic parity generation and checking.
- Four byte FIFO on transmit and receive.
- Auto-baud detection.
- LIN break and sync field detection.
- CTS / RTS hardware flow control.

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a main (clock driver) or secondary (clock receiver) interface in both 3-wire or 4-wire modes, and supports multiple main/secondary devices on a single SPI bus. The chip-select (NSS) signal can be configured as an input to select the SPI in secondary mode, or to disable main mode operation in an environment with multiple main interfaces, avoiding contention on the SPI bus when more than one main device attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in main interface mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple secondary devices.

- Supports 3- or 4-wire main or secondary modes
- Supports external clock frequencies up to 12 Mbps in main or secondary mode
- Support for all clock phase and polarity modes
- 8-bit programmable clock rate (main)
- Programmable receive timeout (secondary)
- Four byte FIFO on transmit and receive
- Can operate in suspend or snooze modes and wake the CPU on reception of a byte
- Support for multiple masters on the same data lines

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I²C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- Support for leader, follower, and multi-leader modes
- Hardware synchronization and arbitration for multi-leader mode
- Clock low extending (clock stretching) to interface with faster leader devices
- Hardware support for 7-bit follower and general call address recognition
- Firmware support for 10-bit follower address decoding
- Ability to inhibit all follower states
- Programmable data setup/hold times
- Transmit and receive FIFOs (one byte) to help increase throughput in faster applications

I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- Support for slave mode only
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave address recognition
- Transmit and receive FIFOs (two bytes) to help increase throughput in faster applications

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

3.7 Analog

12-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12-, 10-, and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs.
- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 200 ksps samples per second in 12-bit mode or 800 ksps samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal fast-settling reference with two levels (1.65 V and 2.4 V) and support for external reference and signal ground.
- Integrated temperature sensor.

Low Current Comparators (CMP0, CMP1)

Analog comparators are used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- Up to 10 (CMP0) or 12 (CMP1) external positive inputs
- Up to 10 (CMP0) or 12 (CMP1) external negative inputs
- Additional input options:
 - Internal connection to LDO output
 - Direct connection to GND
 - Direct connection to VDD
 - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and ± 20 mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset

3.9 Debugging

The EFM8BB2 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

3.10 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in the code security page and last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

Silicon Labs recommends the bootloader be disabled and the flash memory locked after the production programming step in applications where code security is a concern. More information about the factory bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [Application Notes] tile.

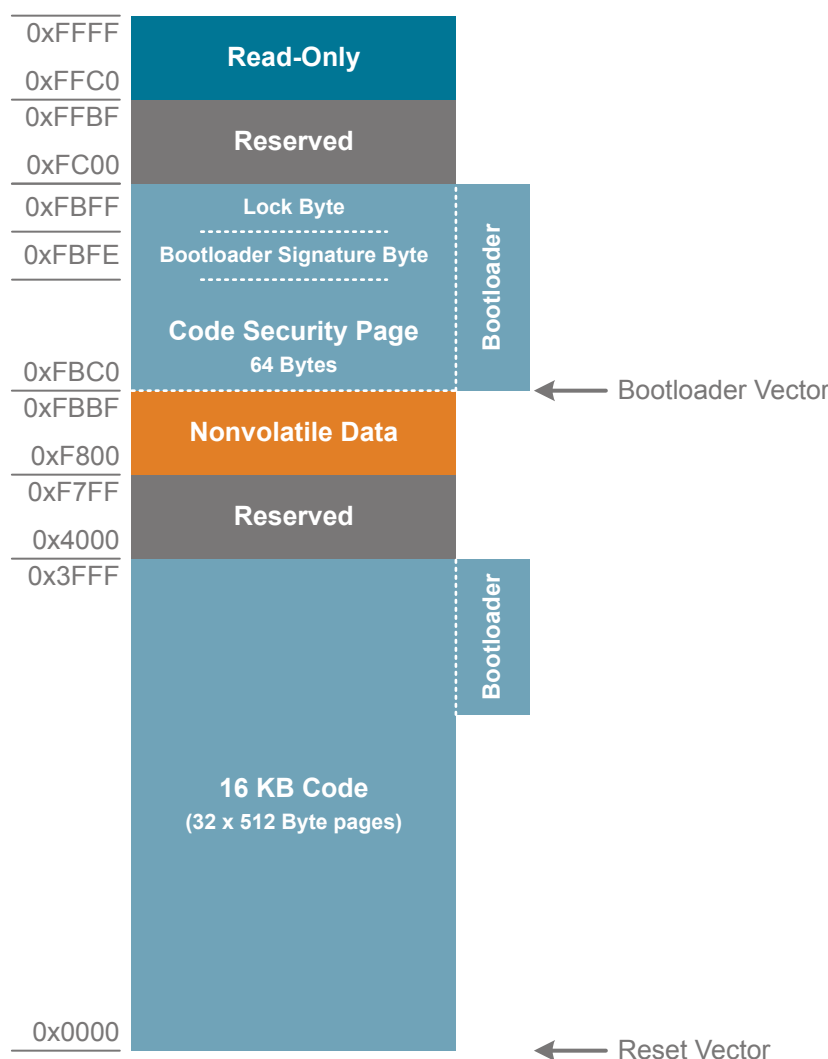


Figure 3.2. Flash Memory Map with Bootloader—16 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5

Table 3.3. Summary of Pins for Bootload Mode Entry

Device Package	Pin for Bootload Mode Entry
QFN28	P3.0 / C2D
QSOP24	P3.0 / C2D
QFN20	P2.0 / C2D

4. Electrical Characteristics

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions on page 16](#), unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V _{DD}		2.2	—	3.6	V
Operating Supply Voltage on VREGIN	V _{REGIN}		3.0	—	5.25	V
System Clock Frequency	f _{SYSCLK}		0	—	50	MHz
Operating Ambient Temperature	T _A	G-grade devices	-40	—	85	°C
		I-grade or A-grade devices	-40	—	125	°C
Note: 1. All voltages with respect to GND. 2. GPIO levels are undefined whenever VDD is less than 1 V.						

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current (G-grade devices, -40 °C to +85 °C)						
Normal Mode-Full speed with code executing from flash	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²	—	9.4	10.1	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²	—	4.5	5.2	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²	—	600	900	μA
		F _{SYSCLK} = 80 kHz ³	—	145	410	μA
Idle Mode-Core halted with peripherals running	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²	—	6.3	6.8	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²	—	2.9	3.3	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²	—	440	750	μA
		F _{SYSCLK} = 80 kHz ³	—	130	420	μA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off.	I _{DD}	LFO Running	—	125	400	μA
		LFO Stopped	—	120	390	μA
Snooze Mode-Core halted and high frequency clocks stopped. Regulator in low-power state, Supply monitor off.	I _{DD}	LFO Running	—	25	300	μA
		LFO Stopped	—	20	290	μA
Stop Mode—Core halted and all clocks stopped, Internal LDO On, Supply monitor off.	I _{DD}		—	120	390	μA
Shutdown Mode—Core halted and all clocks stopped, Internal LDO Off, Supply monitor off.	I _{DD}		—	0.2	3	μA
Digital Core Supply Current (I-grade or A-grade devices, -40 °C to +125 °C)						
Normal Mode-Full speed with code executing from flash	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²	—	9.4	10.9	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²	—	4.5	5.6	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²	—	600	1555	μA
		F _{SYSCLK} = 80 kHz ³	—	145	1070	μA
Idle Mode-Core halted with peripherals running	I _{DD}	F _{SYSCLK} = 49 MHz (HFOSC1) ²	—	6.3	7.4	mA
		F _{SYSCLK} = 24.5 MHz (HFOSC0) ²	—	2.9	3.9	mA
		F _{SYSCLK} = 1.53 MHz (HFOSC0) ²	—	440	1400	μA
		F _{SYSCLK} = 80 kHz ³	—	130	1050	μA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off.	I _{DD}	LFO Running	—	125	1050	μA
		LFO Stopped	—	120	1045	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Snooze Mode—Core halted and high frequency clocks stopped. Regulator in low-power state, Supply monitor off.	I _{DD}	LFO Running	—	25	950	μA
		LFO Stopped	—	20	940	μA
Stop Mode—Core halted and all clocks stopped, Internal LDO On, Supply monitor off.	I _{DD}		—	120	1045	μA
Shutdown Mode—Core halted and all clocks stopped, Internal LDO Off, Supply monitor off.	I _{DD}		—	0.2	15	μA
Analog Peripheral Supply Currents (-40 °C to +125 °C)						
High-Frequency Oscillator 0	I _{HFOSC0}	Operating at 24.5 MHz, T _A = 25 °C	—	105	—	μA
High-Frequency Oscillator 1	I _{HFOSC1}	Operating at 49 MHz, T _A = 25 °C	—	865	940	μA
Low-Frequency Oscillator	I _{LFOSC}	Operating at 80 kHz, T _A = 25 °C	—	4	—	μA
ADC0 Always-on ⁴	I _{ADC}	800 ksps, 10-bit conversions or 200 ksps, 12-bit conversions Normal bias settings V _{DD} = 3.0 V	—	820	1200	μA
		250 ksps, 10-bit conversions or 62.5 ksps 12-bit conversions Low power bias settings V _{DD} = 3.0 V	—	405	580	μA
ADC0 Burst Mode, 10-bit single conversions, external reference	I _{ADC}	200 ksps, V _{DD} = 3.0 V	—	370	—	μA
		100 ksps, V _{DD} = 3.0 V	—	185	—	μA
		10 ksps, V _{DD} = 3.0 V	—	20	—	μA
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I _{ADC}	200 ksps, V _{DD} = 3.0 V	—	485	—	μA
		100 ksps, V _{DD} = 3.0 V	—	245	—	μA
		10 ksps, V _{DD} = 3.0 V	—	25	—	μA
ADC0 Burst Mode, 12-bit single conversions, external reference	I _{ADC}	100 ksps, V _{DD} = 3.0 V	—	505	—	μA
		50 ksps, V _{DD} = 3.0 V	—	255	—	μA
		10 ksps, V _{DD} = 3.0 V	—	50	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Burst Mode, 12-bit single conversions, internal reference	I_{ADC}	100 ksp/s, $V_{DD} = 3.0\text{ V}$, Normal bias	—	950	—	μA
		50 ksp/s, $V_{DD} = 3.0\text{ V}$, Low power bias	—	415	—	μA
		10 ksp/s, $V_{DD} = 3.0\text{ V}$, Low power bias	—	80	—	μA
Internal ADC0 Reference, Always-on ⁵	I_{VREFFS}	Normal Power Mode	—	680	790	μA
		Low Power Mode	—	160	210	μA
Temperature Sensor	I_{TSENSE}		—	70	120	μA
Comparator 0 (CMP0, CMP1)	I_{CMP}	CPMD = 11	—	0.5	—	μA
		CPMD = 10	—	3	—	μA
		CPMD = 01	—	8.5	—	μA
		CPMD = 00	—	22.5	—	μA
Comparator Reference ⁶	I_{CPREF}		—	1.2	—	μA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	20	μA
5V Regulator	I_{VREG}	Normal Mode (SUSEN = 0, BIASENB = 0)	—	245	340	μA
		Suspend Mode (SUSEN = 1, BIASENB = 0)	—	60	100	μA
		Bias Disabled (BIASENB = 1)	—	2.5	10	μA
		Disabled (BIASENB = 1, REG1ENB = 1)	—	2.5	—	nA

Note:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal LDO regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal LDO regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.
6. This value is the current sourced from the pin or supply selected as the full-scale reference to the comparator DAC.

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V _{VDDM}		1.95	2.05	2.15	V
Power-On Reset (POR) Threshold	V _{POR}	Rising Voltage on VDD	—	1.2	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t _{RMP}	Time to V _{DD} > 2.2 V	10	—	—	μs
Reset Delay from POR	t _{POR}	Relative to V _{DD} > V _{POR}	3	10	31	ms
Reset Delay from non-POR source	t _{RST}	Time between release of reset source and code execution	—	50	—	μs
RST Low Time to Generate Reset	t _{RSTL}		15	—	—	μs
Missing Clock Detector Response Time (final rising edge to reset)	t _{MCD}	F _{SYSClk} > 1 MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F _{MCD}		—	7.5	13.5	kHz
VDD Supply Monitor Turn-On Time	t _{MON}		—	2	—	μs

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time ^{1,2}	t _{WRITE}	One Byte, F _{SYSClk} = 24.5 MHz	19	20	21	μs
Erase Time ^{1,2}	t _{ERASE}	One Page, F _{SYSClk} = 24.5 MHz	5.2	5.35	5.5	ms
V _{DD} Voltage During Programming ³	V _{PROG}		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	N _{WE}		20k	100k	—	Cycles
CRC Calculation Time	t _{CRC}	One 256-Byte Block SYSClk = 49 MHz	—	5.5	—	μs

Note:

- Does not include sequencing time before and after the write/erase operation, which may be multiple SYSClk cycles.
- The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
- Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
- Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t_{IDLEWK}		2	—	3	SYSCCLKs
Suspend Mode Wake-up Time	$t_{SUS-PENDWK}$	SYSCCLK = HFOSC0 CLKDIV = 0x00	—	170	—	ns
Snooze Mode Wake-up Time	$t_{SLEEPWK}$	SYSCCLK = HFOSC0 CLKDIV = 0x00	—	12	—	μ s

4.1.6 Internal Oscillators

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	PSS_{HFOSC0}	$T_A = 25\text{ }^{\circ}\text{C}$	—	0.5	—	%/V
Temperature Sensitivity	TS_{HFOSC0}	$V_{DD} = 3.0\text{ V}$	—	40	—	ppm/ $^{\circ}\text{C}$
High Frequency Oscillator 1 (49 MHz)						
Oscillator Frequency	f_{HFOSC1}	Full Temperature and Supply Range	48.25	49	49.75	MHz
Power Supply Sensitivity	PSS_{HFOSC1}	$T_A = 25\text{ }^{\circ}\text{C}$	—	0.02	—	%/V
Temperature Sensitivity	TS_{HFOSC1}	$V_{DD} = 3.0\text{ V}$	—	45	—	ppm/ $^{\circ}\text{C}$
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	PSS_{LFOSC}	$T_A = 25\text{ }^{\circ}\text{C}$	—	0.05	—	%/V
Temperature Sensitivity	TS_{LFOSC}	$V_{DD} = 3.0\text{ V}$	—	65	—	ppm/ $^{\circ}\text{C}$

4.1.7 External Clock Input

Table 4.7. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	50	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns

4.1.8 ADC

Table 4.8. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N _{bits}	12 Bit Mode	12			Bits
		10 Bit Mode	10			Bits
Throughput Rate (High Speed Mode)	f _S	12 Bit Mode	—	—	200	ksps
		10 Bit Mode	—	—	800	ksps
Throughput Rate (Low Power Mode)	f _S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t _{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t _{PWR}		1.2	—	—	μs
SAR Clock Frequency	f _{SAR}	High Speed Mode, Reference is 2.4 V internal	—	—	6.25	MHz
		High Speed Mode, Reference is not 2.4 V internal	—	—	12.5	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t _{CNV}	10-Bit Conversion, SAR Clock = 12.25 MHz, System Clock = 24.5 MHz.	1.1			μs
Sample/Hold Capacitor	C _{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C _{IN}		—	20	—	pF
Input Mux Impedance	R _{MUX}		—	550	—	Ω
Voltage Reference Range	V _{REF}		1	—	V _{DD}	V
Input Voltage Range ¹	V _{IN}	Gain = 1	0	—	V _{REF}	V
		Gain = 0.5	0	—	2xV _{REF}	V
Power Supply Rejection Ratio	PSRR _{ADC}		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±2.3	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	-1	±0.7	1.9	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
Offset Error	E _{OFF}	12 Bit Mode, V _{REF} = 1.65 V	-3	0	3	LSB
		10 Bit Mode, V _{REF} = 1.65 V	-2	0	2	LSB
Offset Temperature Coefficient	TC _{OFF}		—	0.004	—	LSB/°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slope Error	E _M	12 Bit Mode	—	±0.02	±0.1	%
		10 Bit Mode	—	±0.06	±0.24	%
Dynamic Performance 10 kHz Sine Wave Input 1 dB below full scale, Max throughput, using AGND pin						
Signal-to-Noise	SNR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	71	—	dB
		10 Bit Mode	—	70	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	-79	—	dB
		10 Bit Mode	—	-70	—	dB
Note: 1. Absolute input pin voltage is limited by the V _{DD} supply.						

4.1.9 Voltage Reference

Table 4.9. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}	1.65 V Setting	1.62	1.65	1.68	V
		2.4 V Setting, $V_{DD} > 2.6$ V	2.35	2.4	2.45	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	μs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 800 ksps; $V_{REF} = 3.0$ V	—	8	—	μA

4.1.10 Temperature Sensor

Table 4.10. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	757	—	mV
Offset Error ¹	E_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	17	—	mV
Slope	M		—	2.85	—	mV/ $^{\circ}\text{C}$
Slope Error ¹	E_M		—	70	—	$\mu\text{V}/^{\circ}$
Linearity			—	0.5	—	$^{\circ}\text{C}$
Turn-on Time			—	1.8	—	μs

Note:

1. Represents one standard deviation from the mean.

4.1.11 1.8 V Internal LDO Voltage Regulator

Table 4.11. 1.8V Internal LDO Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage	$V_{OUT_1.8V}$		1.78	1.85	1.92	V

4.1.12 5 V Voltage Regulator

Table 4.12. 5 V Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range ¹	V_{REGIN}		3.0	—	5.25	V
Output Voltage on VDD ²	V_{REGOUT}	Output Current = 1 to 100 mA Regulation range ($V_{REGIN} \geq 4.1\text{ V}$)	3.1	3.3	3.6	V
		Output Current = 1 to 100 mA Dropout range ($V_{REGIN} < 4.1\text{ V}$)	—	$V_{REGIN} - V_{DROPOUT}$	—	V
Output Current ²	I_{REGOUT}		—	—	100	mA
Dropout Voltage	$V_{DROPOUT}$	Output Current = 100 mA	—	—	0.8	V

Note:

1. Input range to meet the Output Voltage on VDD specification. If the 5V voltage regulator is not used, V_{REGIN} should be tied to VDD.
2. Output current is total regulator output, including any current required by the device.

4.1.13 Comparators

Table 4.13. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential, $V_{CM} = 1.65$ V	—	110	—	ns
		-100 mV Differential, $V_{CM} = 1.65$ V	—	160	—	ns
Response Time, CPMD = 11 (Low- est Power)	t_{RESP3}	+100 mV Differential, $V_{CM} = 1.65$ V	—	1.2	—	μ s
		-100 mV Differential, $V_{CM} = 1.65$ V	—	4.5	—	μ s
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	-8	—	mV
		CPHYN = 10	—	-16	—	mV
		CPHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V_{IN}		-0.25	—	$V_{DD}+0.25$	V
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Internal Reference DAC Resolution	N_{bits}		6			bits
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	70	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	$T_A = 25$ °C	-10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	μ V/°

4.1.14 Port I/O

Table 4.14. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive) ¹	V _{OH}	I _{OH} = -7 mA, V _{DD} ≥ 3.0 V	V _{DD} - 0.7	—	—	V
		I _{OH} = -3.3 mA, 2.2 V ≤ V _{DD} < 3.0 V	V _{DD} × 0.8	—	—	V
Output Low Voltage (High Drive) ¹	V _{OL}	I _{OL} = 13.5 mA, V _{DD} ≥ 3.0 V	—	—	0.6	V
		I _{OL} = 7 mA, 2.2 V ≤ V _{DD} < 3.0 V	—	—	V _{DD} × 0.2	V
Output High Voltage (Low Drive) ¹	V _{OH}	I _{OH} = -4.75 mA, V _{DD} ≥ 3.0 V	V _{DD} - 0.7	—	—	V
		I _{OH} = -2.25 mA, 2.2 V ≤ V _{DD} < 3.0 V	V _{DD} × 0.8	—	—	V
Output Low Voltage (Low Drive) ¹	V _{OL}	I _{OL} = 6.5 mA, V _{DD} ≥ 3.0 V	—	—	0.6	V
		I _{OL} = 3.5 mA, 2.2 V ≤ V _{DD} < 3.0 V	—	—	V _{DD} × 0.2	V
Input High Voltage	V _{IH}		V _{DD} - 0.6	—	—	V
Input Low Voltage	V _{IL}		—	—	0.6	V
Pin Capacitance	C _{IO}		—	7	—	pF
Weak Pull-Up Current (V _{IN} = 0 V)	I _{PU}	V _{DD} = 3.6	-30	-20	-10	μA
Input Leakage (Pullups off or Analog)	I _{LK}	GND < V _{IN} < V _{DD}	-1.1	—	1.1	μA
Input Leakage Current with V _{IN} above V _{DD}	I _{LK}	V _{DD} < V _{IN} < V _{DD} +2.0 V	0	5	150	μA

Note:

1. See [Figure 4.7 Typical V_{OH} Curves on page 34](#) and [Figure 4.8 Typical V_{OL} Curves on page 34](#) for more information.

4.1.15 SMBus

Table 4.15. SMBus Peripheral Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70 ²	kHz
SMBus Operating Frequency	f_{SMB}		40 ¹	—	70 ²	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	μs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	μs
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	μs
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	μs
Data Hold Time	$t_{HD:DAT}$		275 ³	—	—	ns
Data Setup Time	$t_{SU:DAT}$		300 ³	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	μs
Clock High Period	t_{HIGH}		9.4	—	50 ⁴	μs
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	255 ²	kHz
SMBus Operating Frequency	f_{SMB}		40 ¹	—	255 ²	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	μs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	μs
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	μs
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	μs
Data Hold Time	$t_{HD:DAT}$		275 ³	—	—	ns
Data Setup Time	$t_{SU:DAT}$		300 ³	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	μs
Clock High Period	t_{HIGH}		2.6	—	50 ⁴	μs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications. The maximum frequency cannot be achieved with all combinations of oscillators and dividers available, but the effective frequency must not exceed 256 kHz.
3. Data setup and hold timing at 40 MHz or lower with EXTHOLD set to 1.
4. SMBus has a maximum requirement of 50 μ s for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 μ s. I2C can support periods longer than 50 μ s.

Table 4.16. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	$f_{CSO} / 3$
Bus Free Time Between STOP and START Conditions	t_{BUF}	$2 / f_{CSO}$
Hold Time After (Repeated) START Condition	$t_{HD:STA}$	$1 / f_{CSO}$
Repeated START Condition Setup Time	$t_{SU:STA}$	$2 / f_{CSO}$
STOP Condition Setup Time	$t_{SU:STO}$	$2 / f_{CSO}$
Clock Low Period	t_{LOW}	$1 / f_{CSO}$
Clock High Period	t_{HIGH}	$2 / f_{CSO}$

Note:

1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

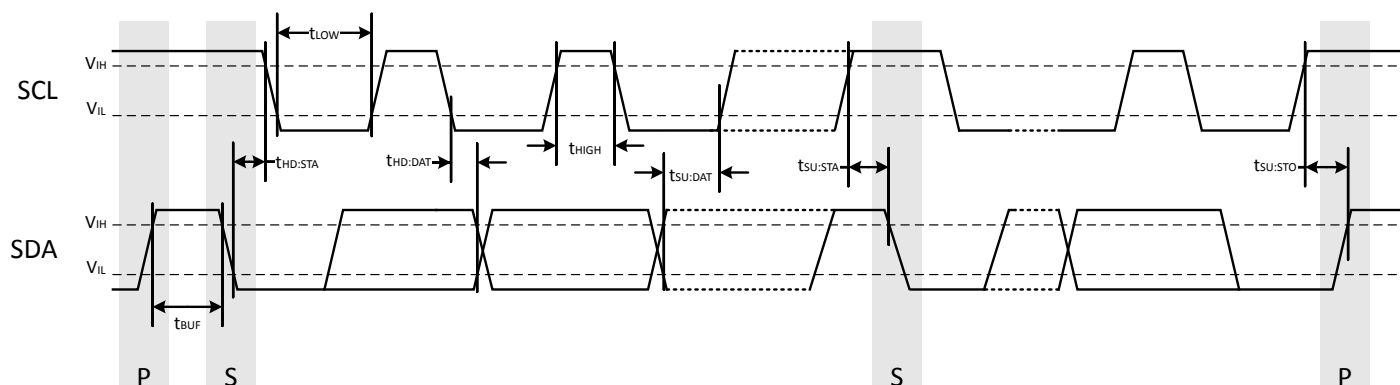


Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.2 Thermal Conditions

Table 4.17. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{JA}	QFN-20 Packages	—	60	—	°C/W
		QFN-28 Packages	—	26	—	°C/W
		QSOP-24 Packages	—	65	—	°C/W
Thermal Resistance (Junction to Case)	θ_{JC}	QFN-20 Packages	—	28.86	—	°C/W
		QFN-28 Packages	—	18.8	—	°C/W
Thermal Characterization Parameter (Junction to Top)	Ψ_{JT}	QFN-20 Package	—	0.88	—	°C/W
		QFN-28 Packages	—	0.3	—	°C/W
Note: 1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

4.3 Absolute Maximum Ratings

Stresses above those listed in [Table 4.18 Absolute Maximum Ratings on page 30](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

Table 4.18. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T _{BIAS}		-55	125	°C
Storage Temperature	T _{STG}		-65	150	°C
Voltage on VDD	V _{DD}		GND-0.3	4.2	V
Voltage on VREGIN	V _{REGIN}		GND-0.3	5.8	V
Voltage on I/O pins or RSTb	V _{IN}	V _{DD} > 3.3 V	GND-0.3	5.8	V
		V _{DD} < 3.3 V	GND-0.3	V _{DD} +2.5	V
Total Current Sunk into Supply Pin	I _{VDD}		—	200	mA
Total Current Sourced out of Ground Pin	I _{GND}		200	—	mA
Current Sourced or Sunk by any I/O Pin or RSTb	I _{IO}		-100	100	mA
Operating Junction Temperature	T _J	T _A = -40 °C to 85 °C	−40	105	°C
		T _A = -40 °C to 125 °C (I-grade or A-grade parts only)	−40	130	°C
Note: 1. Exposure to maximum rating conditions for extended periods may affect device reliability.					

4.4 Typical Performance Curves

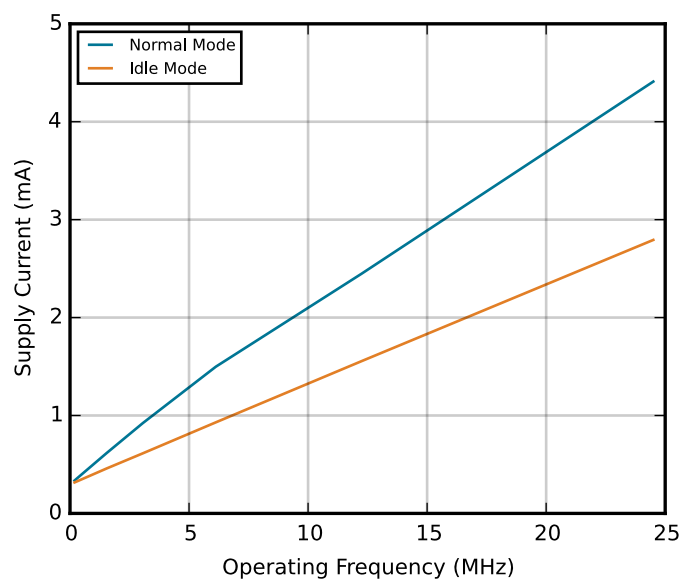


Figure 4.2. Typical Operating Supply Current using HFOSC0

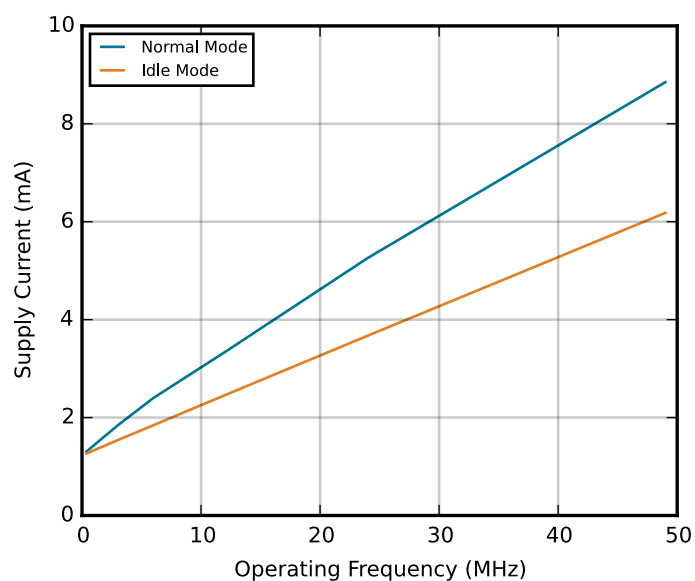


Figure 4.3. Typical Operating Supply Current using HFOSC1

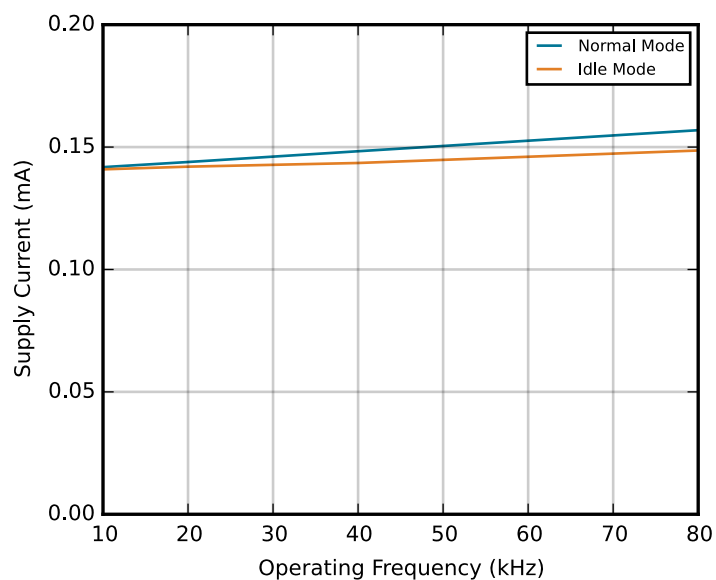


Figure 4.4. Typical Operating Supply Current using LFOSC

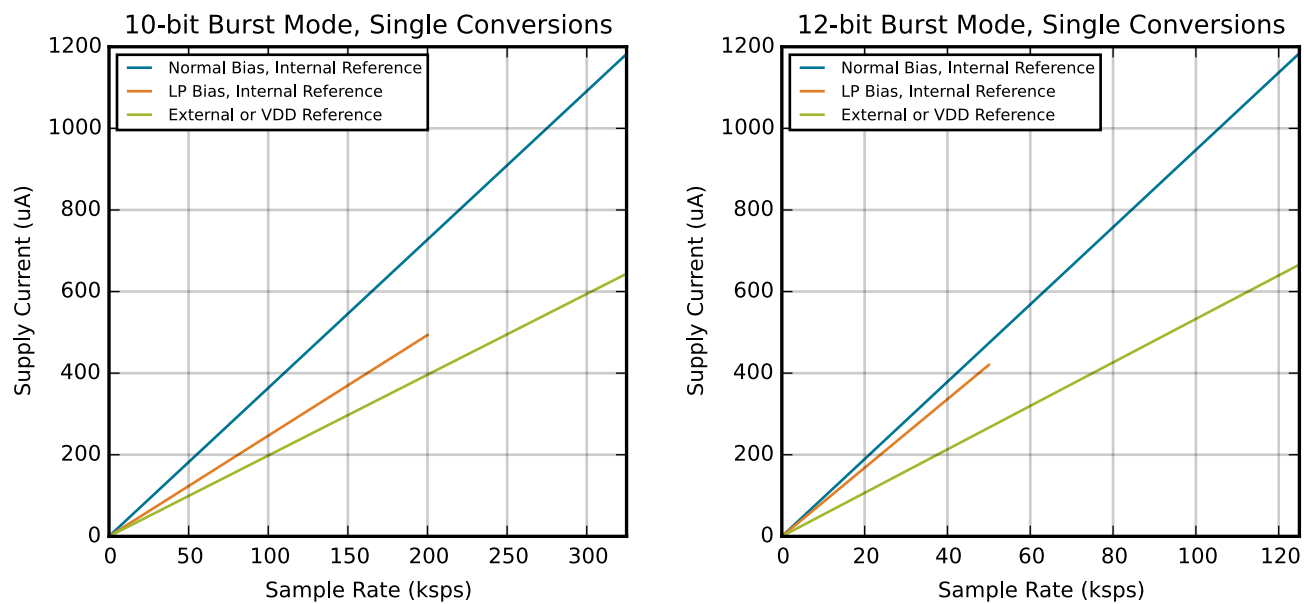


Figure 4.5. Typical ADC0 and Internal Reference Supply Current in Burst Mode

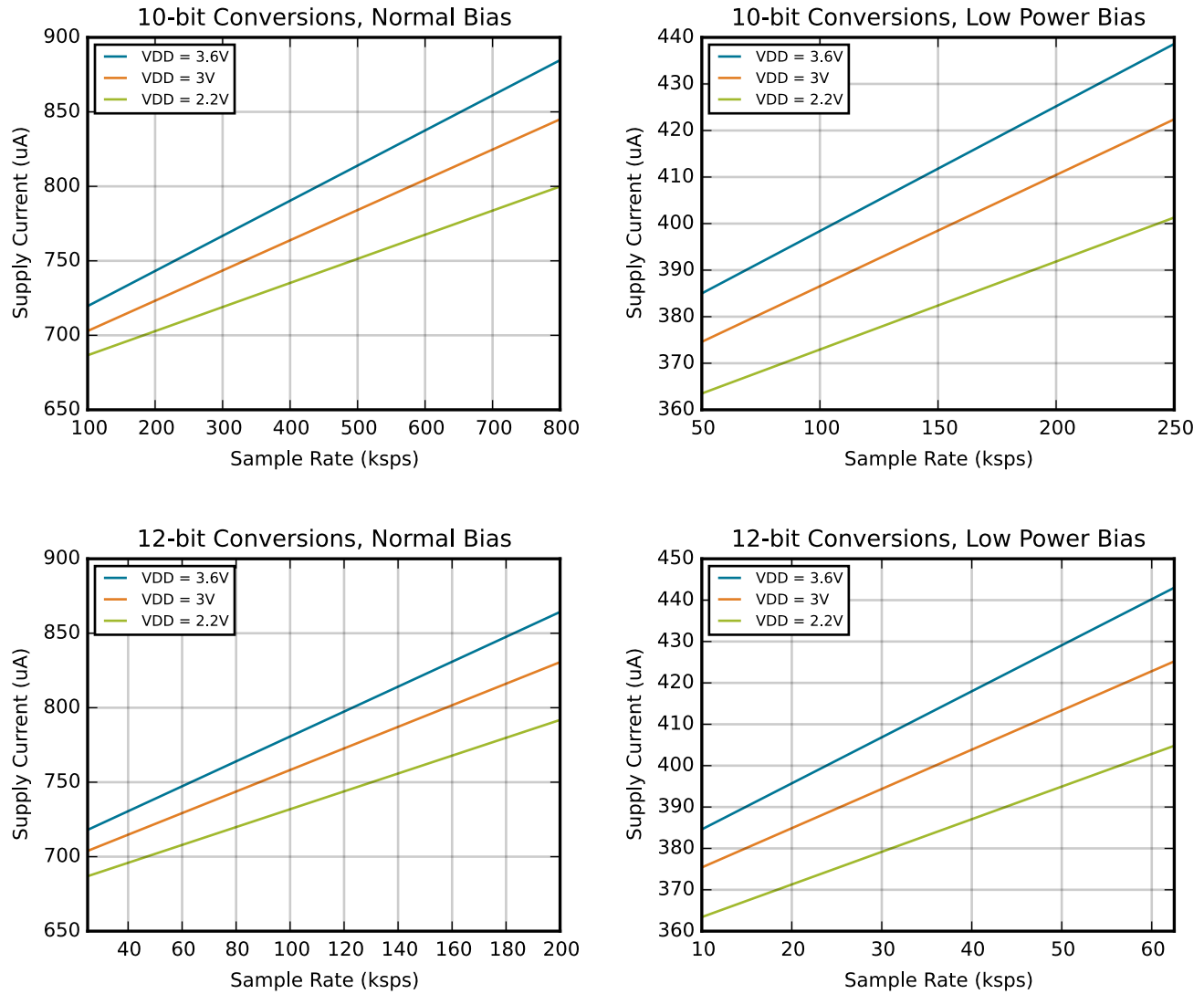


Figure 4.6. Typical ADC0 Supply Current in Normal (always-on) Mode

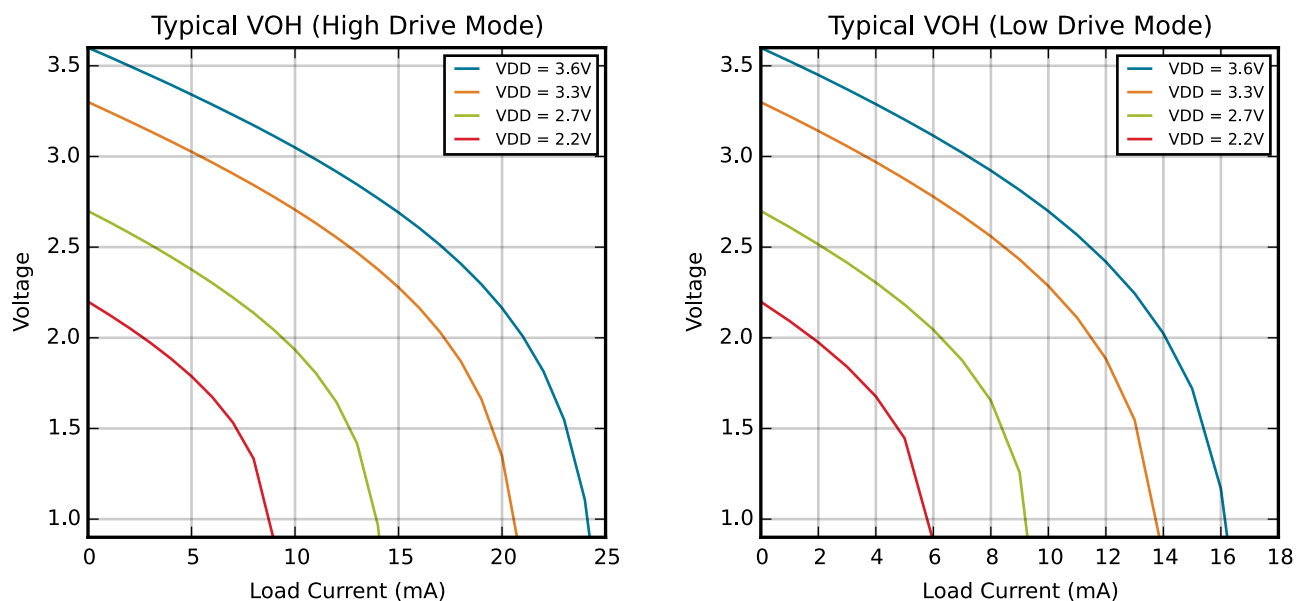


Figure 4.7. Typical V_{OH} Curves

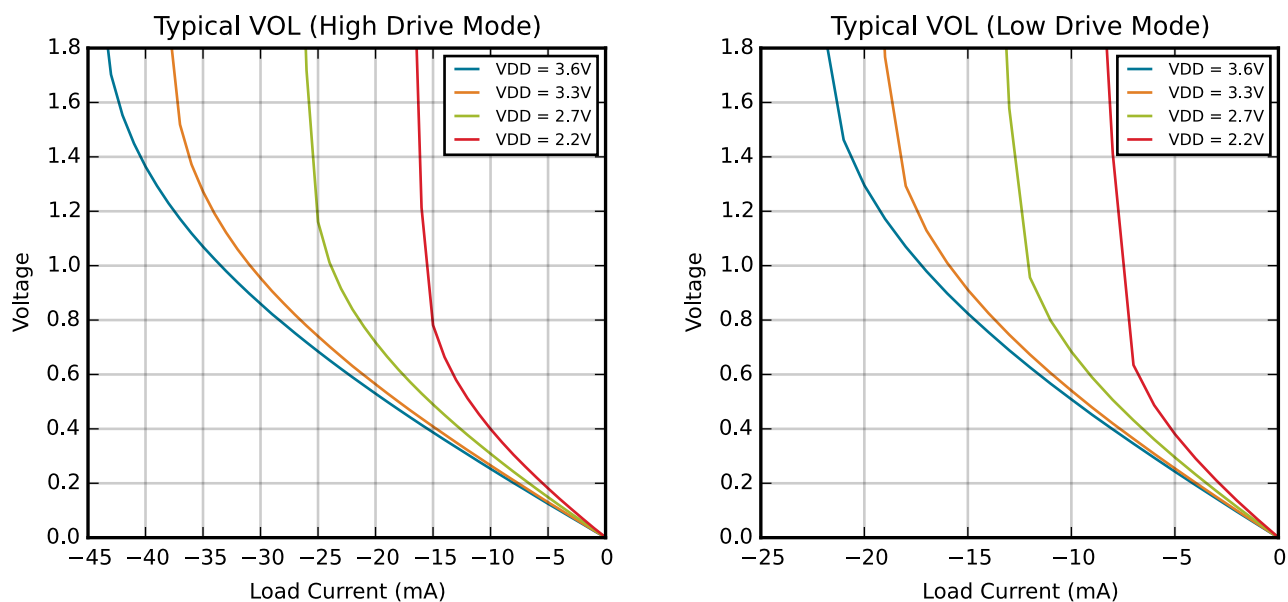


Figure 4.8. Typical V_{OL} Curves

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Connection Diagram with Voltage Regulator Used on page 35 shows a typical connection diagram for the power pins of the EFM8BB2 devices when the 5 V-to-3.3 V regulator is in use.

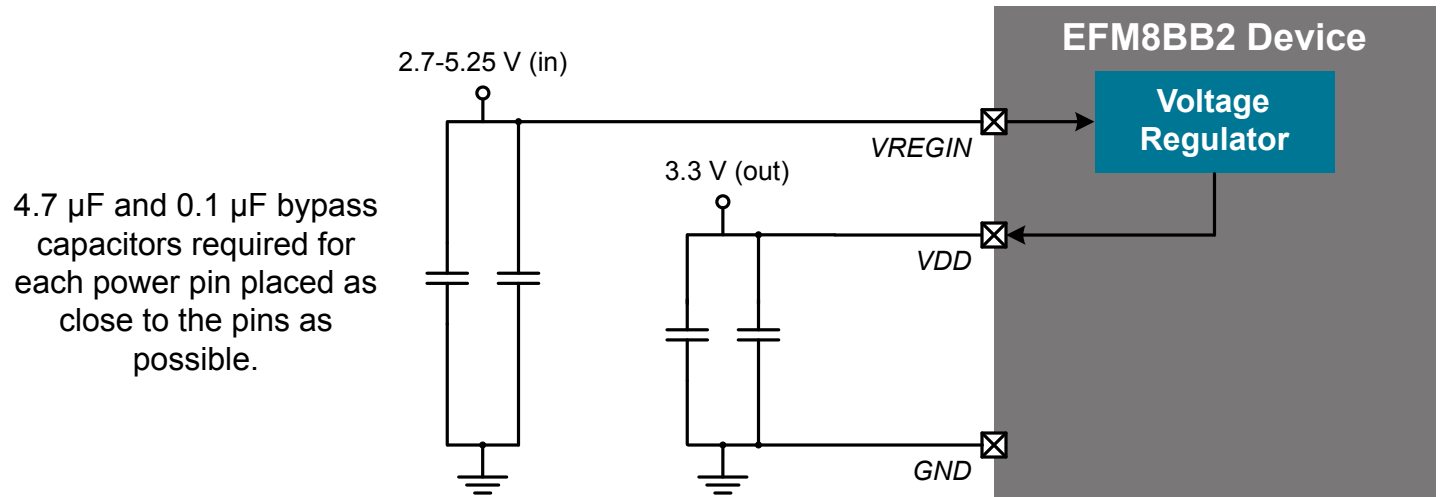


Figure 5.1. Connection Diagram with Voltage Regulator Used

Figure 5.2 Connection Diagram with Voltage Regulator Not Used on page 35 shows a typical connection diagram for the power pins of the EFM8BB2 devices when the internal 5 V-to-3.3 V regulator is not used.

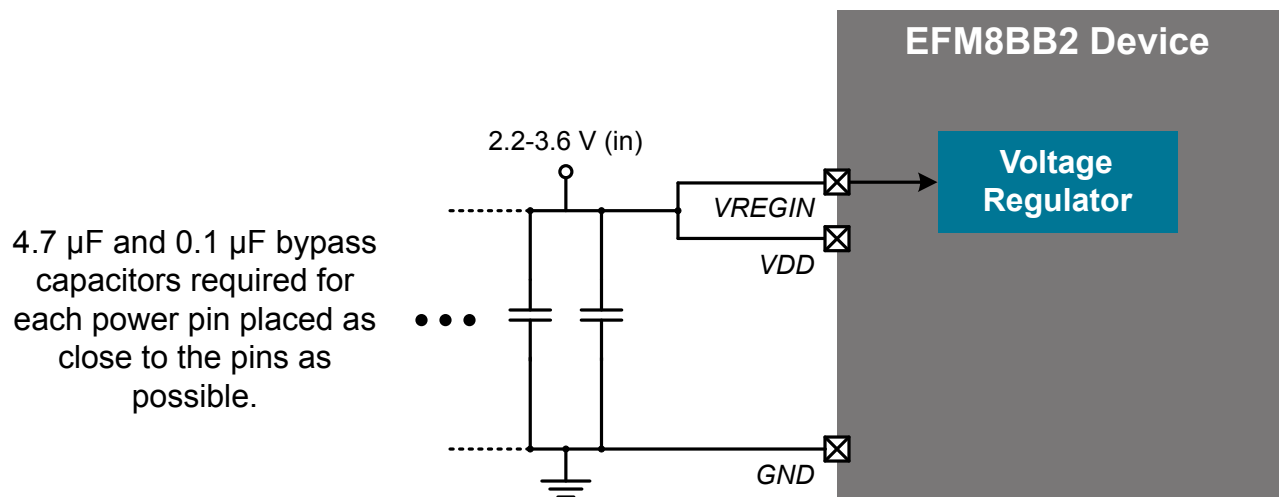


Figure 5.2. Connection Diagram with Voltage Regulator Not Used

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in *AN124: Pin Sharing Techniques for the C2 Interface*. Application notes can be found on the Silicon Labs website (<http://www.silabs.com/8bit-appnotes>) or in Simplicity Studio.

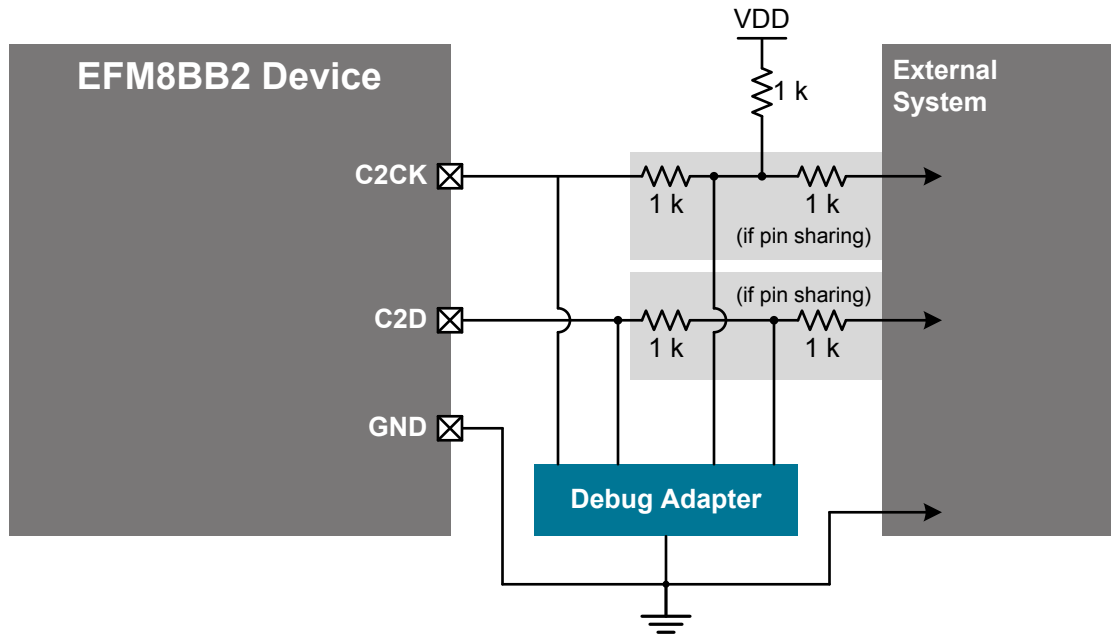


Figure 5.3. Debug Connection Diagram

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note *AN203: 8-bit MCU Printed Circuit Board Design Notes* contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

6. Pin Definitions

6.1 EFM8BB2x-QFN28 Pin Definitions

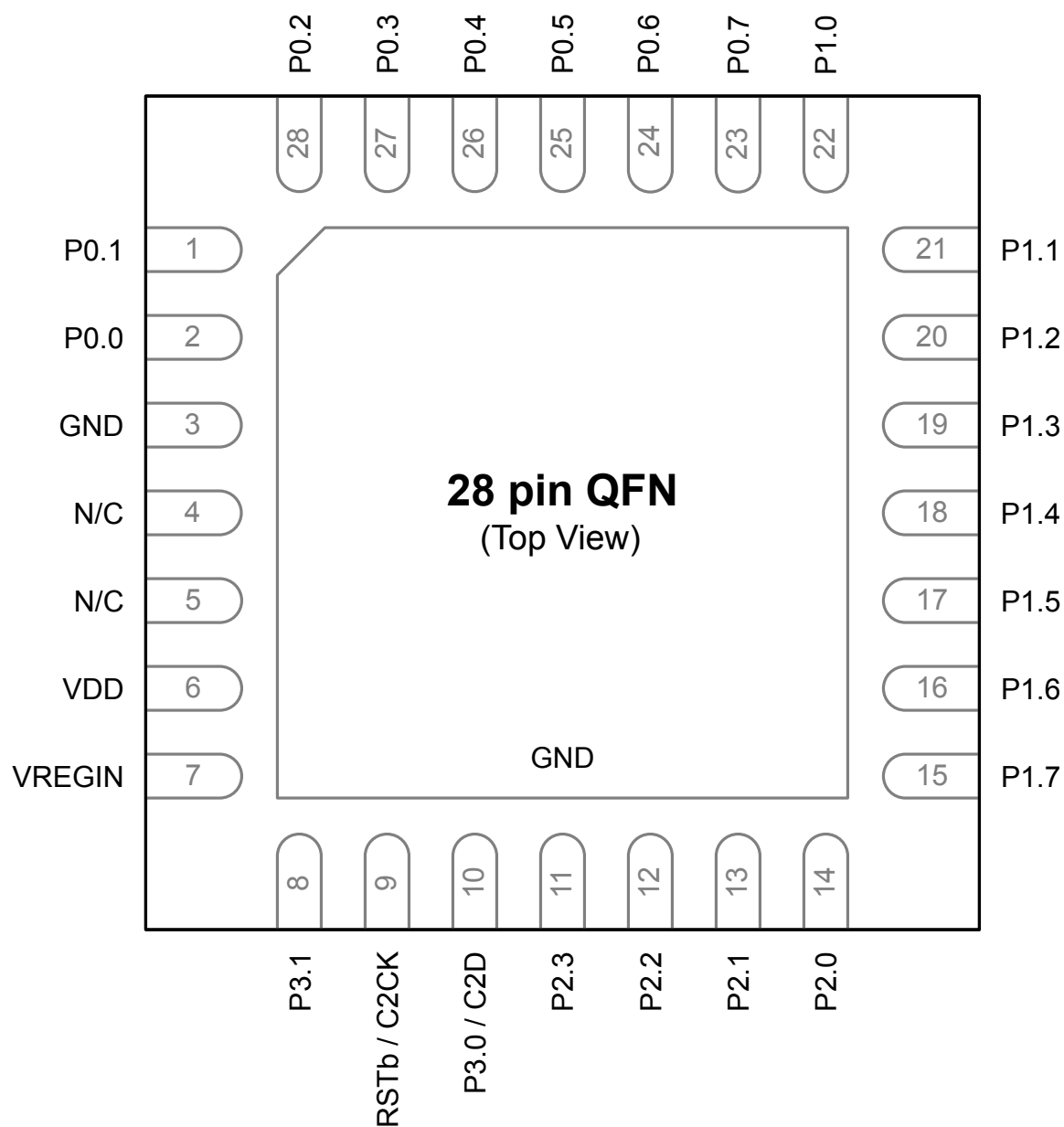


Figure 6.1. EFM8BB2x-QFN28 Pinout

Table 6.1. Pin Definitions for EFM8BB2x-QFN28

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF
3	GND	Ground			
4	N/C	No Connection			
5	N/C	No Connection			
6	VDD	Supply Power Input / 5V Regulator Output			
7	VREGIN	5V Regulator Input			
8	P3.1	Multifunction I/O			
9	RST / C2CK	Active-low Reset / C2 Debug Clock			
10	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
11	P2.3	Multifunction I/O	Yes	P2MAT.3	ADC0.23 CP1P.12 CP1N.12
12	P2.2	Multifunction I/O	Yes	P2MAT.2	ADC0.22 CP1P.11 CP1N.11
13	P2.1	Multifunction I/O	Yes	P2MAT.1	ADC0.21 CP1P.10 CP1N.10
14	P2.0	Multifunction I/O	Yes	P2MAT.0	ADC0.20 CP1P.9 CP1N.9
15	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.15 CP1P.7 CP1N.7

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
16	P1.6	Multifunction I/O	Yes	P1MAT.6 I2C0_SCL	ADC0.14 CP1P.6 CP1N.6
17	P1.5	Multifunction I/O	Yes	P1MAT.5 I2C0_SDA	ADC0.13 CP1P.5 CP1N.5
18	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CP1P.4 CP1N.4
19	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CP1P.3 CP1N.3
20	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CP1P.2 CP1N.2
21	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CP1P.1 CP1N.1 CMP0P.10 CMP0N.10
22	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CP1P.0 CP1N.0 CMP0P.9 CMP0N.9
23	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP0P.7 CMP0N.7
24	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.6 CMP0N.6
25	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX	ADC0.5 CMP0P.5 CMP0N.5

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
26	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX	ADC0.4 CMP0P.4 CMP0N.4
27	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3
28	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2
Center	GND	Ground			

6.2 EFM8BB2x-QSOP24 Pin Definitions

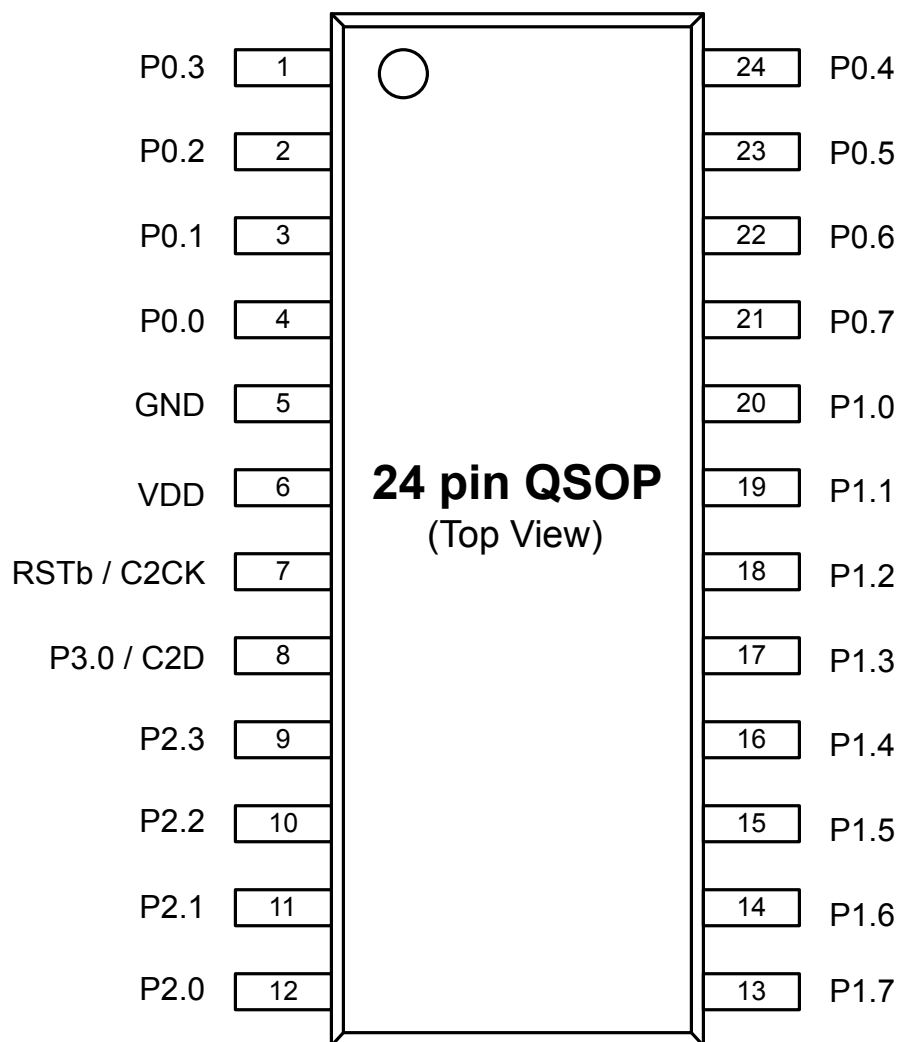


Figure 6.2. EFM8BB2x-QSOP24 Pinout

Table 6.2. Pin Definitions for EFM8BB2x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3
2	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND
4	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF
5	GND	Ground			
6	VDD	Supply Power Input			
7	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
8	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
9	P2.3	Multifunction I/O	Yes	P2MAT.3	ADC0.23 CMP1P.12 CMP1N.12
10	P2.2	Multifunction I/O	Yes	P2MAT.2	ADC0.22 CMP1P.11 CMP1N.11
11	P2.1	Multifunction I/O	Yes	P2MAT.1	ADC0.21 CMP1P.10 CMP1N.10
12	P2.0	Multifunction I/O	Yes	P2MAT.0	ADC0.20 CMP1P.9 CMP1N.9
13	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.15 CMP1P.7 CMP1N.7
14	P1.6	Multifunction I/O	Yes	P1MAT.6 I2C0_SCL	ADC0.14 CMP1P.6 CMP1N.6
15	P1.5	Multifunction I/O	Yes	P1MAT.5 I2C0_SDA	ADC0.13 CMP1P.5 CMP1N.5

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
16	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.4 CMP1N.4
17	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.3 CMP1N.3
18	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2
19	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1 CMP0P.10 CMP0N.10
20	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.0 CMP1N.0 CMP0P.9 CMP0N.9
21	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP0P.7 CMP0N.7
22	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.6 CMP0N.6
23	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX	ADC0.5 CMP0P.5 CMP0N.5
24	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX	ADC0.4 CMP0P.4 CMP0N.4

6.3 EFM8BB2x-QFN20 Pin Definitions

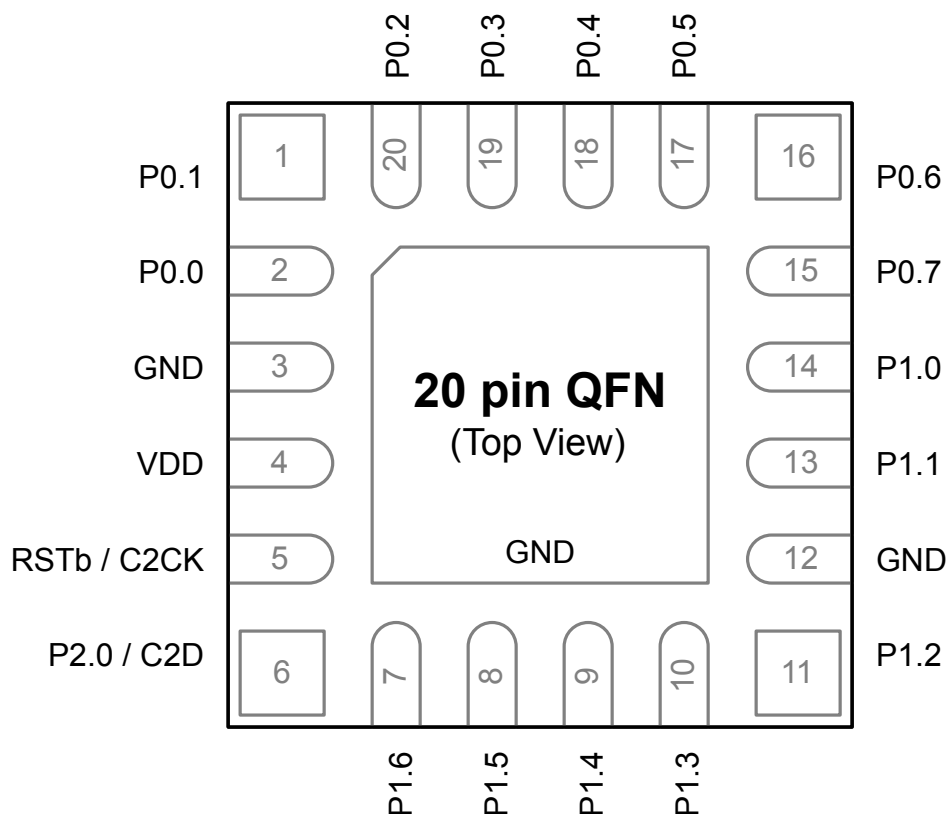


Figure 6.3. EFM8BB2x-QFN20 Pinout

Table 6.3. Pin Definitions for EFM8BB2x-QFN20

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	GND	Ground			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
6	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
7	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.14 CMP1P.6 CMP1N.6
8	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CMP1P.5 CMP1N.5
9	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.4 CMP1N.4
10	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SCL	ADC0.11 CMP1P.3 CMP1N.3
11	P1.2	Multifunction I/O	Yes	P1MAT.2 I2C0_SDA	ADC0.10 CMP1P.2 CMP1N.2
12	GND	Ground			
13	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1 CMP0P.10 CMP0N.10
14	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.0 CMP1N.0 CMP0P.9 CMP0N.9
15	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP0P.7 CMP0N.7

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
16	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.6 CMP0N.6
17	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX	ADC0.5 CMP0P.5 CMP0N.5
18	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX	ADC0.4 CMP0P.4 CMP0N.4
19	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3
20	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2
Center	GND	Ground			

7. QFN28 Package Specifications

7.1 QFN28 Package Dimensions

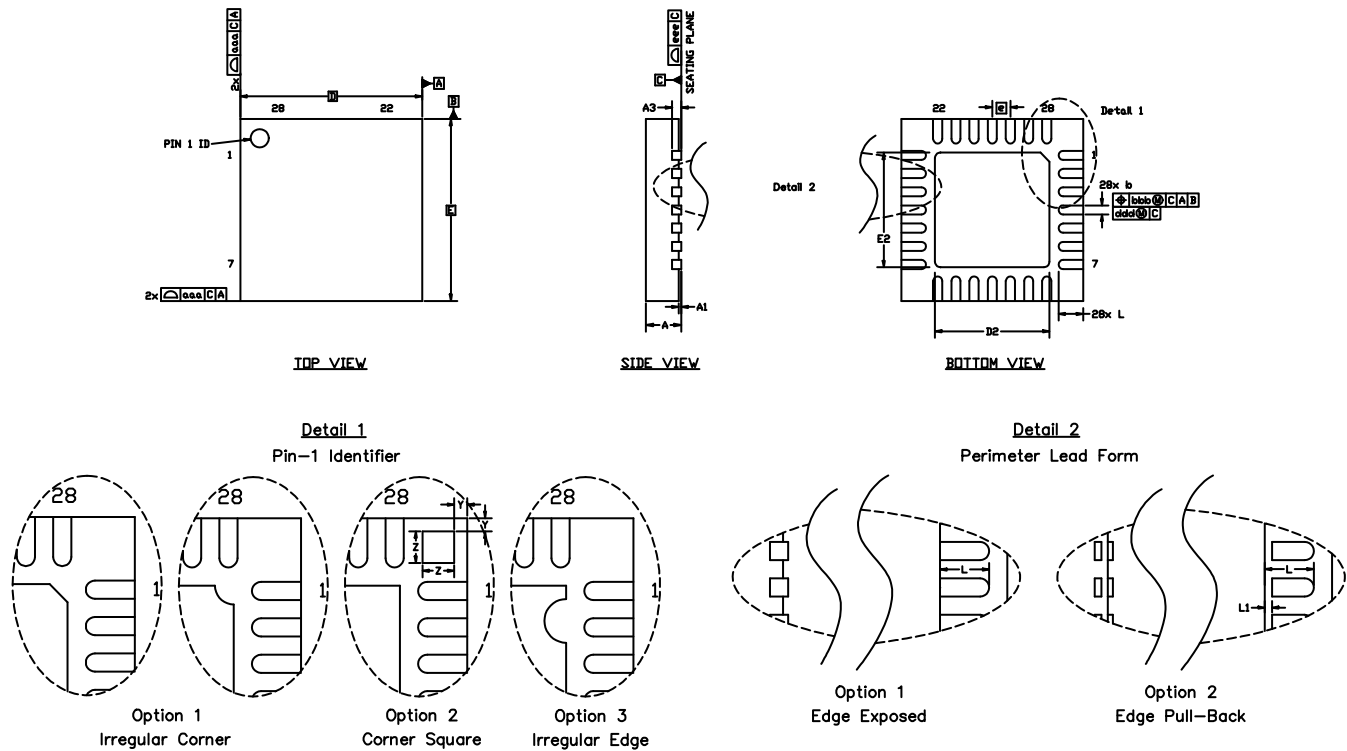


Figure 7.1. QFN28 Package Drawing

Table 7.1. QFN28 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	5.00 BSC		
D2	3.15	3.25	3.35
e	0.50 BSC		
E	5.00 BSC		
E2	3.15	3.25	3.35
L	0.45	0.55	0.65
aaa	0.10		
bbb	0.10		
ddd	0.05		

Dimension	Min	Typ	Max
eee		0.08	
Z		0.44	
Y		0.18	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220 except for custom features D2, E2, L, Z, and Y which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 QFN28 PCB Land Pattern

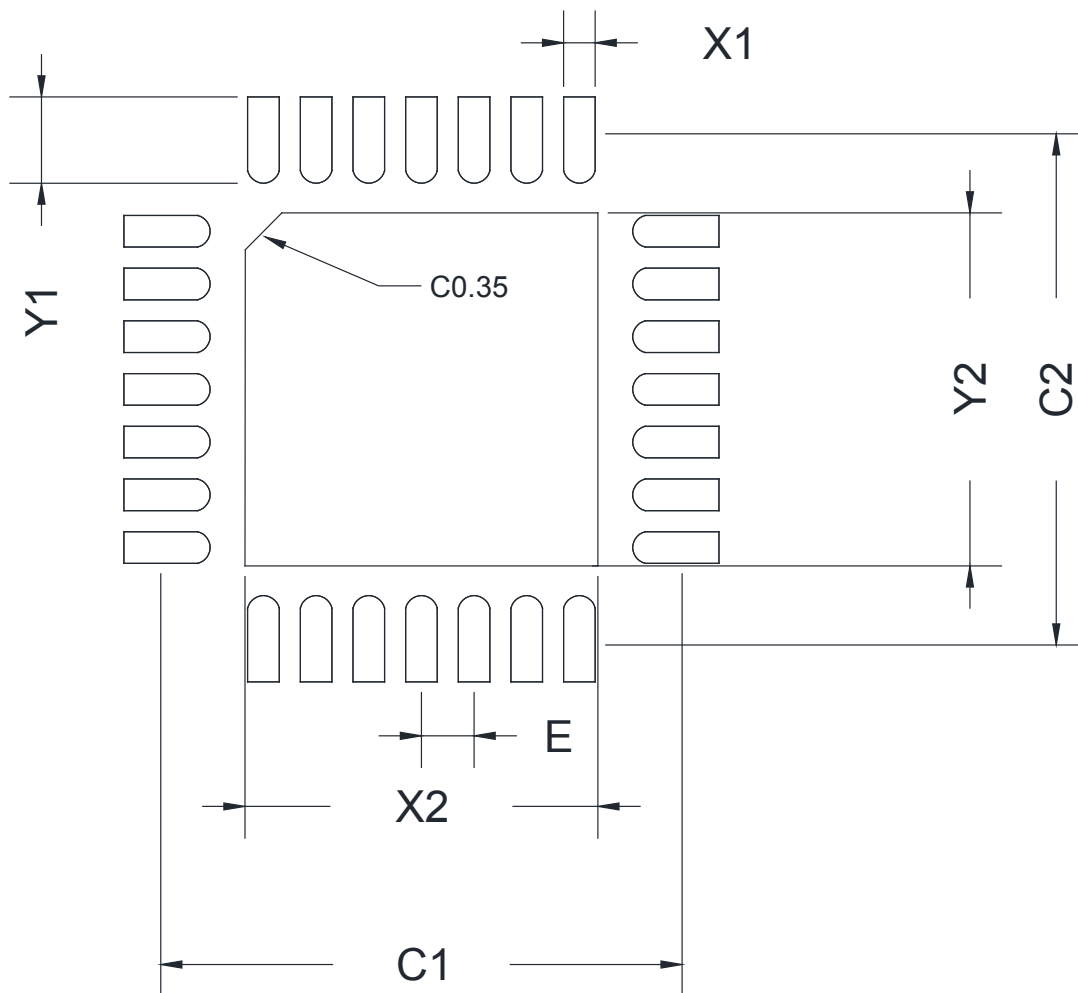


Figure 7.2. QFN28 PCB Land Pattern Drawing

Table 7.2. QFN28 PCB Land Pattern Dimensions

Dimension	Min	Max
C1		4.80
C2		4.80
E		0.50
X1		0.30
X2		3.35
Y1		0.95
Y2		3.35

Dimension	Min	Max
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This Land Pattern Design is based on the IPC-7351 guidelines. 3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. 4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 5. The stencil thickness should be 0.125 mm (5 mils). 6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 7. A 2 x 2 array of 1.2 mm square openings on a 1.5 mm pitch should be used for the center pad. 8. A No-Clean, Type-3 solder paste is recommended. 9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.		

7.3 QFN28 Package Marking

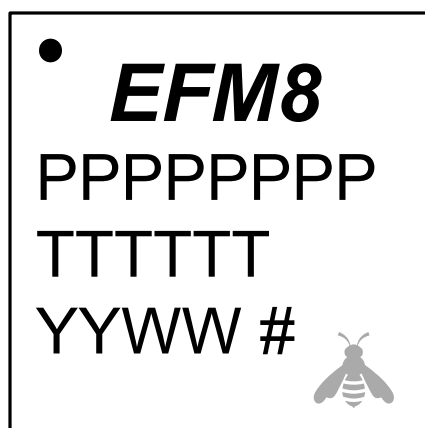


Figure 7.3. QFN28 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

Note: Firmware revision is not part of the package marking.

8. QSOP24 Package Specifications

8.1 QSOP24 Package Dimensions

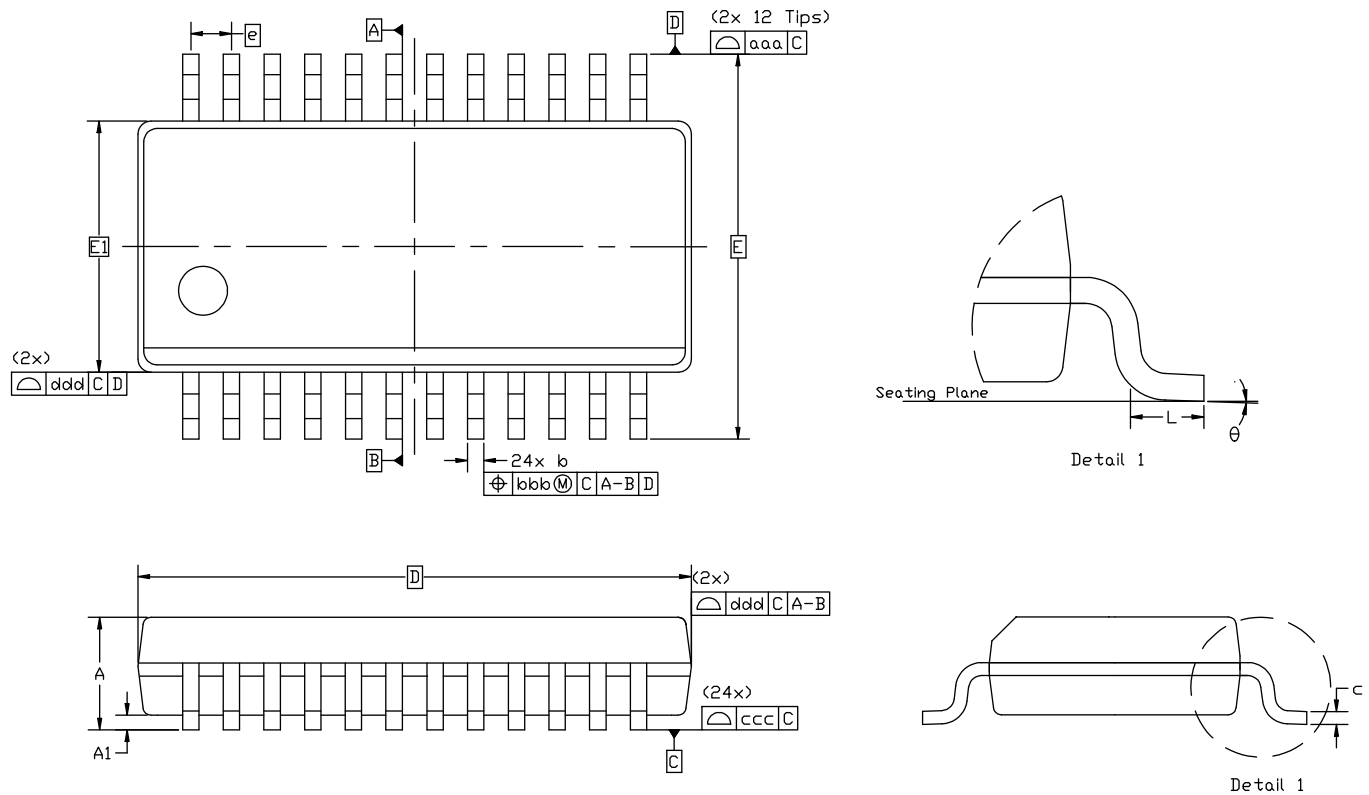


Figure 8.1. Package Drawing

Table 8.1. Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27

Dimension	Min	Typ	Max
theta	0°	—	8°
aaa	0.20		
bbb	0.18		
ccc	0.10		
ddd	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QSOP24 PCB Land Pattern

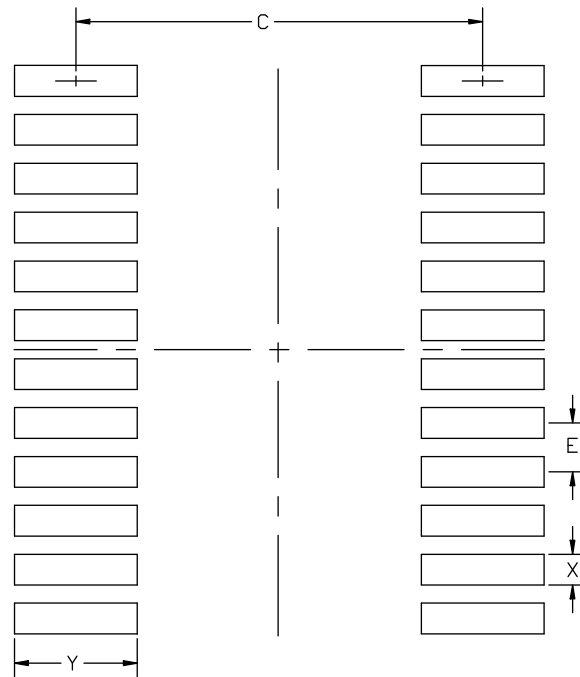


Figure 8.2. PCB Land Pattern Drawing

Table 8.2. PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3 QSOP24 Package Marking



Figure 8.3. Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

9. QFN20 Package Specifications

9.1 QFN20 Package Dimensions

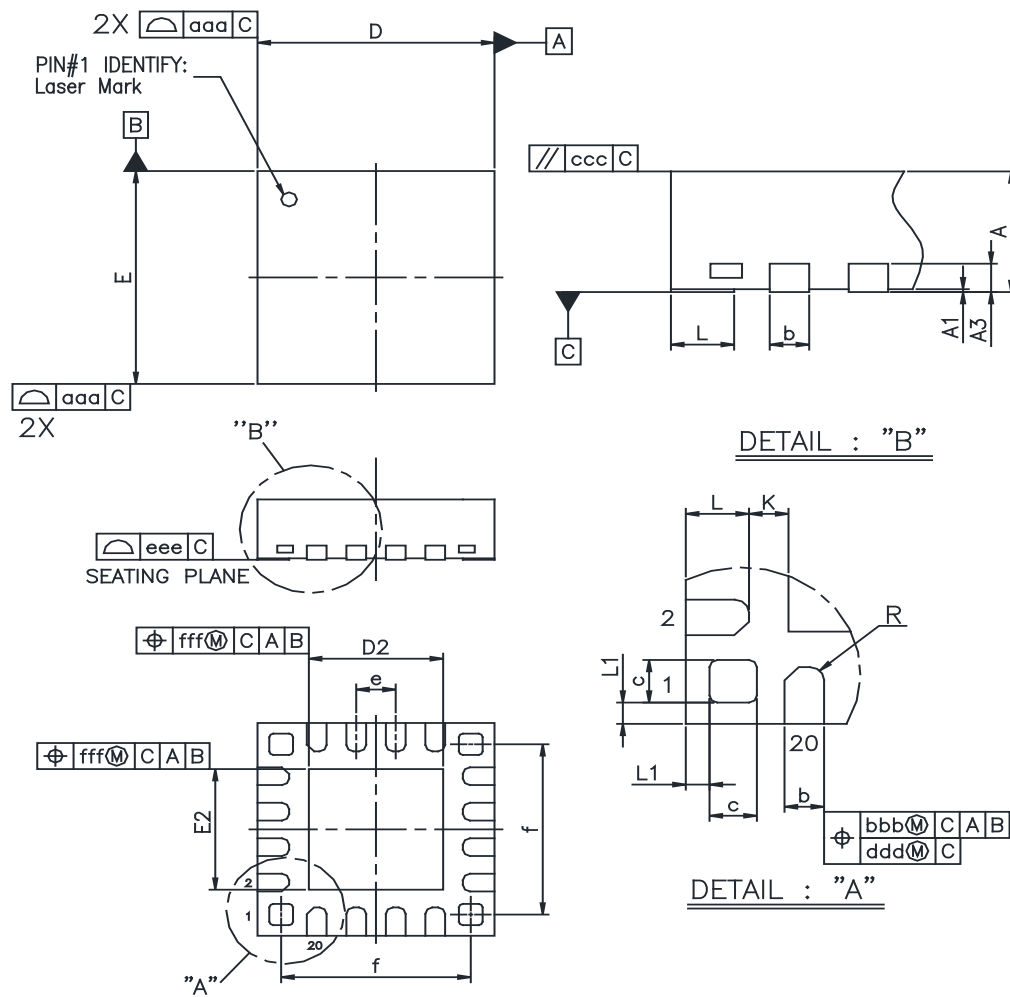


Figure 9.1. QFN20 Package Drawing

Table 9.1. QFN20 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
c	0.25	0.30	0.35
D	3.00 BSC		
D2	1.6	1.70	1.80
e	0.50 BSC		
E	3.00 BSC		

Dimension	Min	Typ	Max
E2	1.60	1.70	1.80
f	2.50 BSC		
L	0.30	0.40	0.50
K	0.25 REF		
R	0.09	0.125	0.15
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. The drawing complies with JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. A variation of the QFN20 Package has its exposed pad chamfered at one corner to indicate the pin 1 location.

9.2 QFN20 PCB Land Pattern

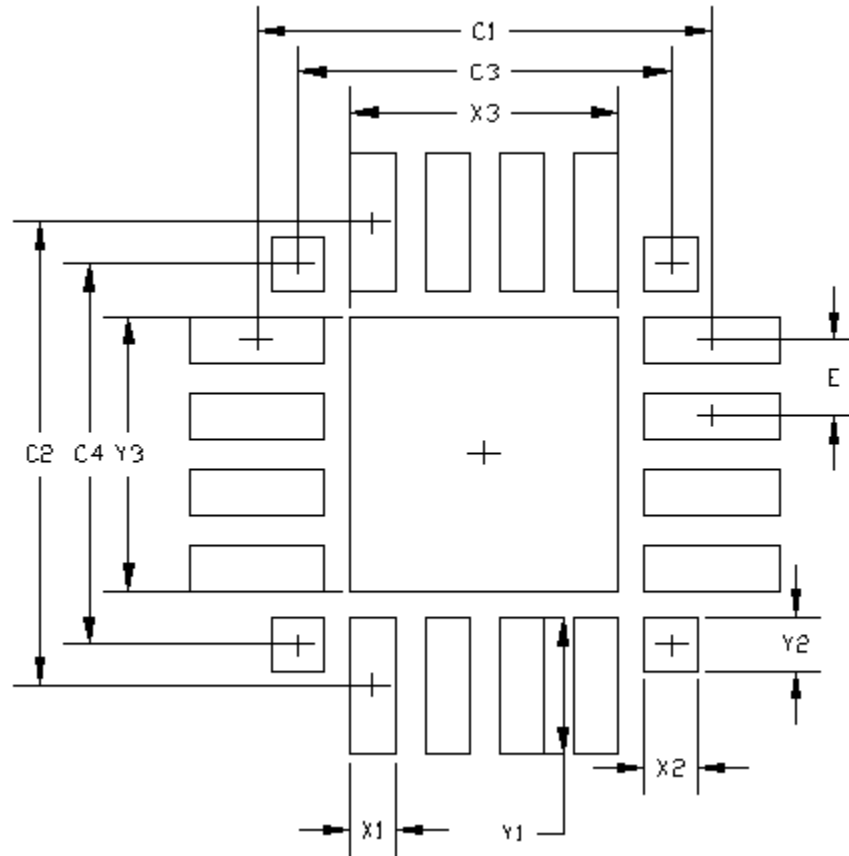


Figure 9.2. QFN20 PCB Land Pattern Drawing

Table 9.2. QFN20 PCB Land Pattern Dimensions

Dimension	Min	Max
C1		3.10
C2		3.10
C3		2.50
C4		2.50
E		0.50
X1		0.30
X2	0.25	0.35
X3		1.80
Y1		0.90
Y2	0.25	0.35
Y3		1.80

Dimension	Min	Max
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification. 3. This Land Pattern Design is based on the IPC-7351 guidelines. 4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. 5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 6. The stencil thickness should be 0.125 mm (5 mils). 7. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads. 8. A 2 x 2 array of 0.75 mm openings on a 0.95 mm pitch should be used for the center pad to assure proper paste volume. 9. A No-Clean, Type-3 solder paste is recommended. 10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.		

9.3 QFN20 Package Marking

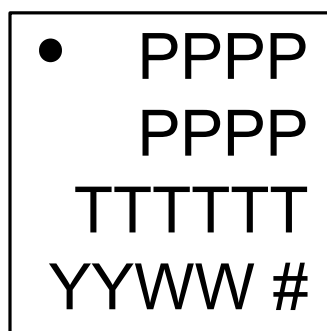


Figure 9.3. QFN20 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

Note: Firmware revision is not part of the package marking.

10. Revision History

Revision 1.6

October, 2025

- Moved select parts to NRND in [Table 2.1 Product Selection Guide on page 3](#).

Revision 1.5

March, 2024

- Noted that all QSOP Package OPNs are EOL.
- Added missing specifications for [4.1.15 SMBus](#).
- Added Z and Y dimensions and updated Note 3 in [Table 7.1 QFN28 Package Dimensions on page 47](#).
- Updated Silicon Labs recommendation for code security when using the Bootloader in the [3.10 Bootloader](#) section.
- Added more information to the [3.1 Introduction](#) section.
- Corrected 'E' dimension drawing in land pattern image in section [9.2 QFN20 PCB Land Pattern](#).
- Added Thermal Resistance (Junction to Case) for the QFN28 package and added Thermal Characterization Parameter (Junction to Top) for the QFN20 and QFN28 packages to [4.2 Thermal Conditions](#).
- Corrected the QFN20 C2D pin Crossbar information in [6.3 EFM8BB2x-QFN20 Pin Definitions](#).
- Changed revision history format, including listing revisions in bulleted lists and changing date format to <Month, Year>.

Revision 1.4

March, 2017

- Updated the language in [1. Feature List](#) to clarify the package offerings for each of the different temperature grades.
- Added bootloader pinout information to [3.10 Bootloader](#).
- Corrected the application note number for *AN124: Pin Sharing Techniques for the C2 Interface* in [5.2 Debug](#).
- Added CRC Calculation Time to [4.1.4 Flash Memory](#).
- Added specifications for [4.1.15 SMBus](#).

Revision 1.31

November, 2016

- Updated typical and maximum specifications in [4.1.2 Power Consumption](#).
- Added [4.1.11 1.8 V Internal LDO Voltage Regulator](#).

Revision 1.3

August, 2016

- Added A-grade parts.
- Added Thermal Resistance (Junction to Case) for QFN20 packages to [4.2 Thermal Conditions](#).
- Added a note to [Table 4.2 Power Consumption on page 17](#) providing more information about the Comparator Reference specification.
- Added a note linking to the Typical VOH and VOL Performance graphs in [4.1.14 Port I/O](#).
- Specified the sizes of the SMBus and I2CSLAVE transmit and receive FIFOs.
- Added a note to [3.1 Introduction](#) referencing the Reference Manual.

Revision 1.2

February, 2016

- Updated [Figure 5.3 Debug Connection Diagram on page 36](#) to move the pull-up resistor on C2D / RSTb to after the series resistor instead of before.
- Added a reference to *AN945: EFM8 Factory Bootloader User Guide* in [3.10 Bootloader](#).
- Added I-grade parts.
- Adjusted and added maximum specifications in [4.1.2 Power Consumption](#) for G-grade devices and added a note on which high frequency oscillator is used for the specification.
- Adjusted the Total Current Sunk into Supply Pin and Total Current Sourced out of Ground Pin specifications in [4.3 Absolute Maximum Ratings](#).

Revision 1.1

December, 2015

- Updated [3.2 Power](#) to properly reflect that a comparator falling edge wakes the device from Suspend and Snooze.
- Added Note 2 to [Table 4.1 Recommended Operating Conditions on page 16](#).
- Added [5.2 Debug](#).

Revision 1.0

- Updated any TBD numbers in and adjusted various specifications.
- Updated VOH and VOL graphs in [Figure 4.7 Typical VOH Curves on page 34](#) and [Figure 4.8 Typical VOL Curves on page 34](#) and updated the VOH and VOL specifications in [Table 4.14 Port I/O on page 27](#).
- Added more information to [3.10 Bootloader](#).
- Updated part numbers to Revision C.

Revision 0.3

- Updated QFN20 packaging and landing diagram dimensions.
- Updated QFN28 D and E minimum value.
- Updated some characterization TBD values.
- Updated the 5 V-to-3.3 V regulator Electrical Characteristics table.
- Added Stop mode to the Power Modes table in [3.2 Power](#).

Revision 0.2

- Initial release.

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