ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	RSD100N10TL
Manufacturer:	Rohm Semiconductor
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

https://antrexco.com/product/details/rohm-semiconductor/rsd100n10tl.html

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Contact Information

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Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

Secure sourcing support for OEM / EMS projects

Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

4V Drive Nch MOSFET

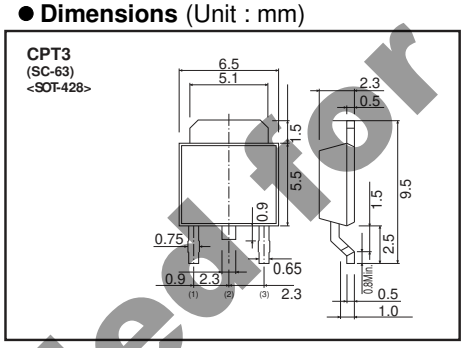
RSD100N10

● Structure
Silicon N-channel MOSFET

● Features
1) Low on-resistance.
2) 4V drive.
3) High power package.

● Application
Switching

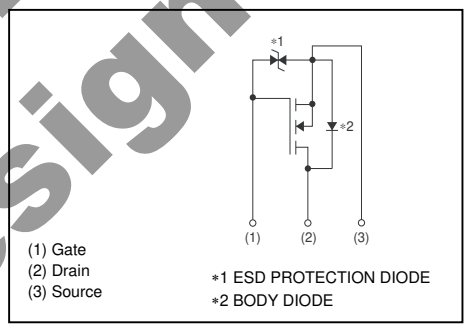
● Dimensions (Unit : mm)



● Packaging specifications

Type	Package	Taping
	Code	TL
	Basic ordering unit (pieces)	2500
RSD100N10		O

● Inner circuit



● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	100	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D *3	±10	A
	Pulsed	I_{DP} *1	±20	A
Source current (Body Diode)	Continuous	I_S *3	10	A
	Pulsed	I_{SP} *1	20	A
Power dissipation		P_D *2	20	W
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	−55 to +150	°C

*1 P_W≤10μs, Duty cycle≤1%

*2 T_C=25°C

*3 Please use within the range of SOA.

● Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to Case	Rth (ch-c)*	6.25	°C / W

* T_C=25°C

● **Electrical characteristics** (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	I_D=1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	V_{DS}=100V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	1	-	2.5	V	V_{DS}=10V, I_D=1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$ *	-	95	133	mΩ	I_D=5A, V_{GS}=10V
		-	100	140		I_D=5A, V_{GS}=4.5V
		-	105	147		I_D=5A, V_{GS}=4V
Forward transfer admittance	$\|Y_{fs}\|$ *	4.5	-	-	S	V_{DS}=10V, I_D=5A
Input capacitance	C_{iss}	-	700	-	pF	V_{DS}=25V
Output capacitance	C_{oss}	-	65	-	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	-	40	-	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$ *	-	10	-	ns	V_{DD}≒50V, I_D=5A
Rise time	t_r *	-	17	-	ns	V_{GS}=10V
Turn-off delay time	$t_{d(off)}$ *	-	50	-	ns	R_L=10Ω
Fall time	t_f *	-	20	-	ns	R_G=10Ω
Total gate charge	Q_g *	-	18	-	nC	V_{DD}≒50V, I_D=10A
Gate-source charge	Q_{gs} *	-	2	-	nC	V_{GS}=10V
Gate-drain charge	Q_{gd} *	-	4.5	-	nC	

*Pulsed

●**Body diode characteristics** (Source-Drain)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD} *	-	-	1.5	V	I_s=10A, V_{GS}=0V

*Pulsed

●Electrical characteristic curves (Ta=25°C)

Fig.1 Typical Output Characteristics (Ⅰ)

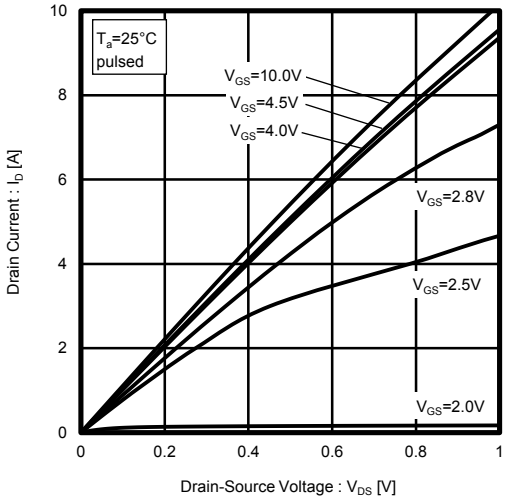


Fig.2 Typical Output Characteristics (Ⅱ)

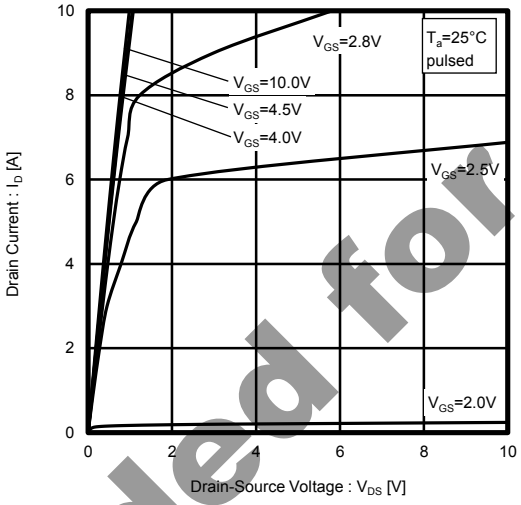


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

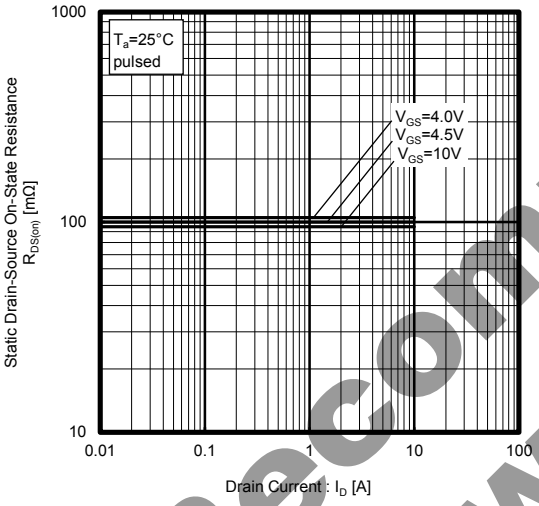


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

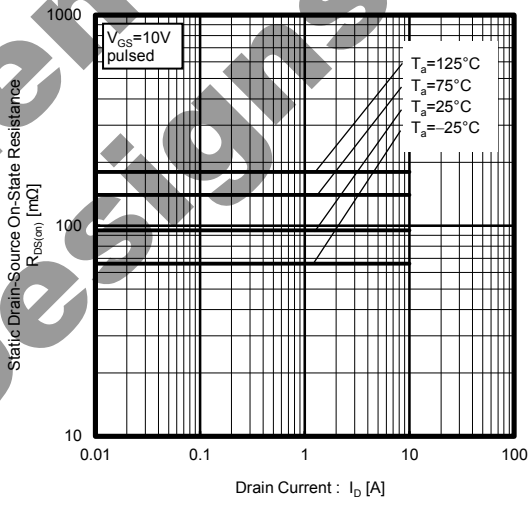


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

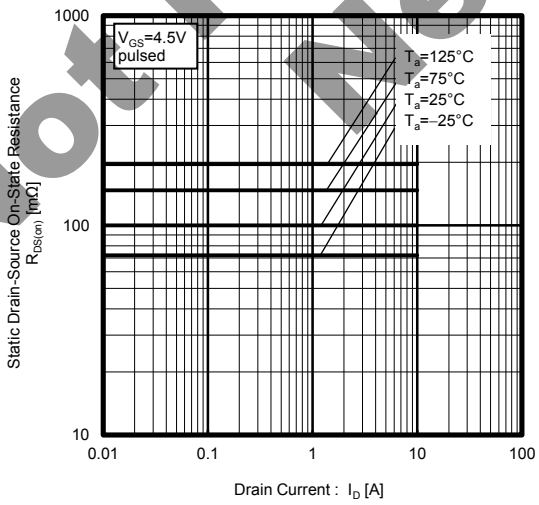


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

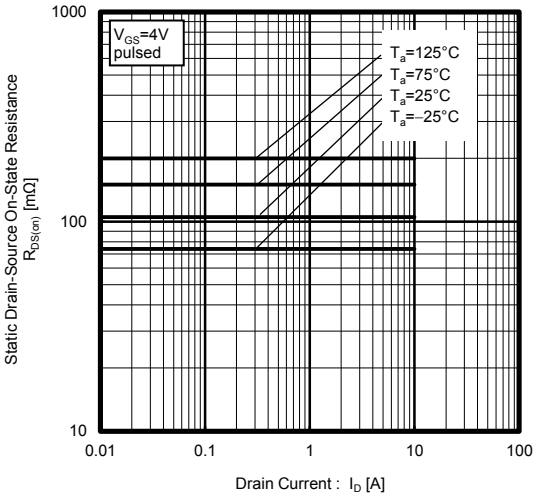


Fig.7 Forward Transfer Admittance vs. Drain Current

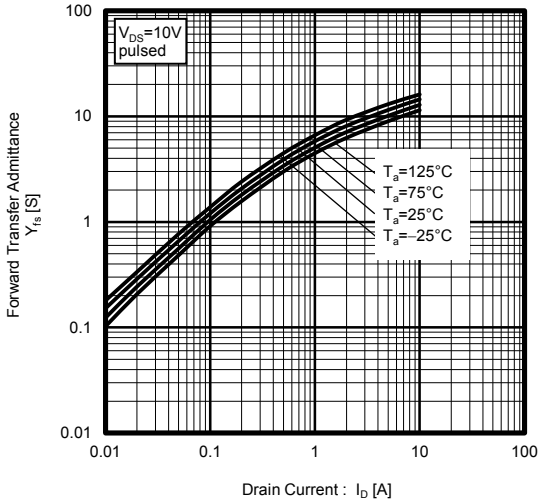


Fig.8 Typical Transfer Characteristics

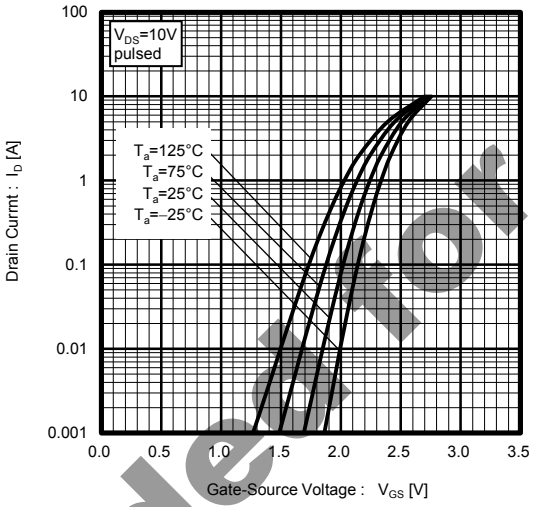


Fig.9 Source Current vs. Source-Drain Voltage

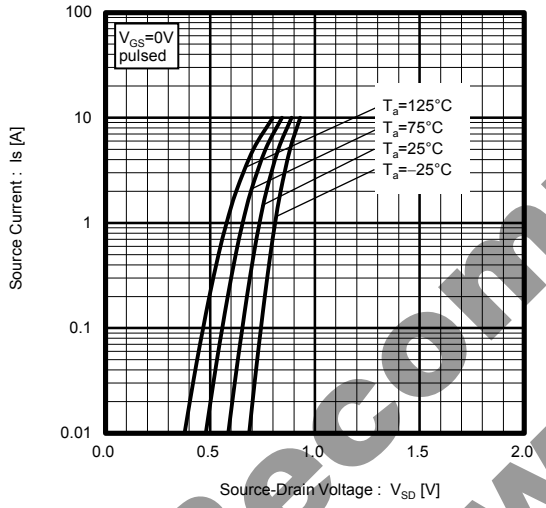


Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

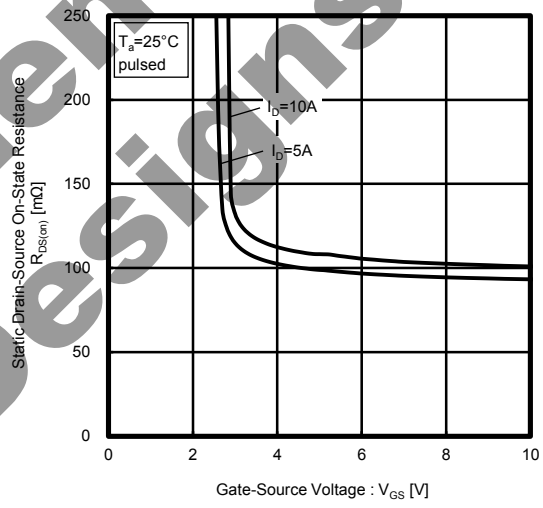


Fig.11 Switching Characteristics

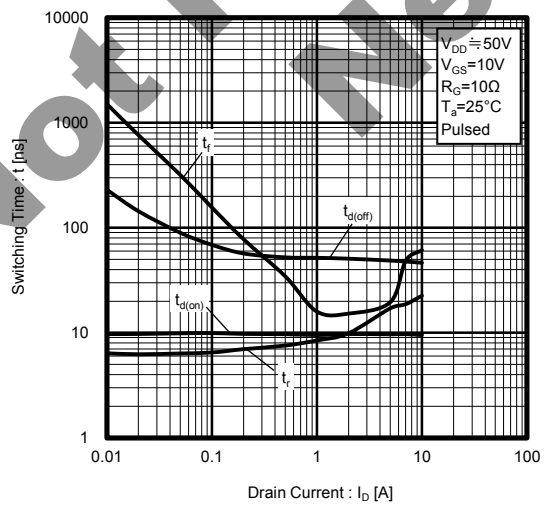


Fig.12 Dynamic Input Characteristics

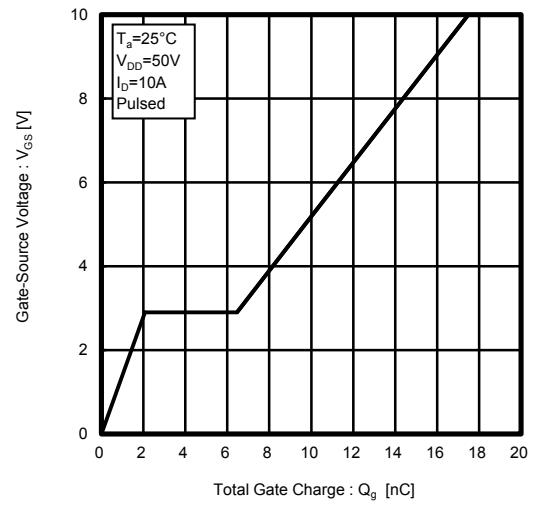


Fig.13 Typical Capacitance vs. Drain-Source Voltage

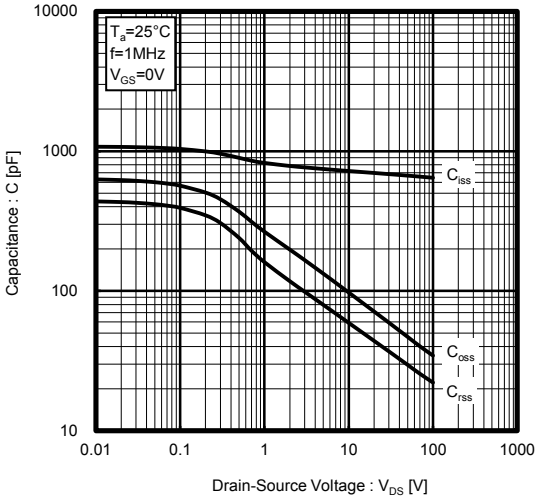


Fig.14 Normalized Transient Thermal Resistance v.s. Pulse Width

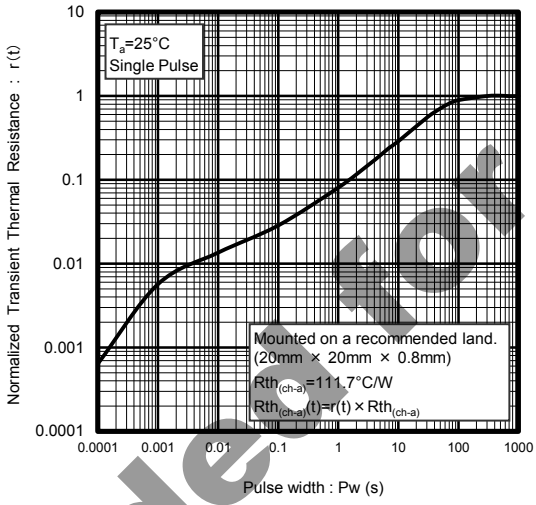
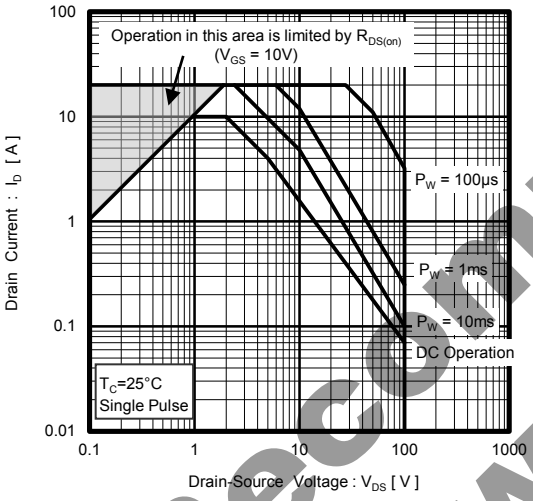


Fig.15 Maximum Safe Operating Area



● **Measurement circuits**

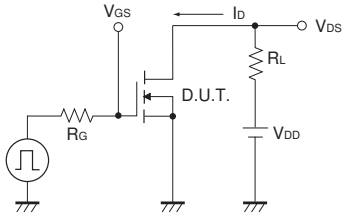


Fig.1-1 Switching Time Measurement Circuit

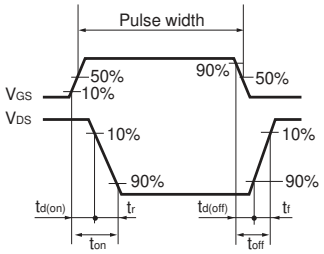


Fig.1-2 Switching Waveforms

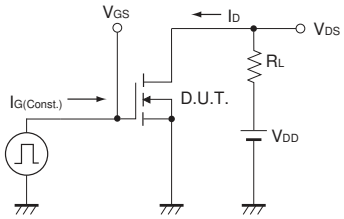


Fig.2-1 Gate Charge Measurement Circuit

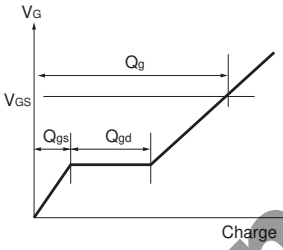


Fig.2-2 Gate Charge Waveform

Notes

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