

# ANTREX Electronics

## Electronic Components Sourcing Information

---

### Product Reference Information

**Part Number:** R7FA6T1AB3CFM#AA0

**Manufacturer:** Renesas Electronics Corporation

**Package:** 64-LQFP

**Availability:** Please confirm with sales

**Product Page:**

<https://antrexco.com/product/details/renesas-electronics-corporation/r7fa6t1ab3cfm-aa0.html>



Scan for product page

**Request a Quote:**

[Submit RFQ for this part](#)

### Contact Information

Email: [info@antrexco.com](mailto:info@antrexco.com)

WhatsApp: +86-186-8066-5326

Website: <https://antrexco.com>

### Quality & Trust

New & Original Components

Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

Secure sourcing support for OEM / EMS projects

**Note:**

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

---

Leading performance 120-MHz Arm® Cortex®-M4 core, up to 512-KB of code flash memory, 64-KB SRAM, security and safety features, and advanced analog.

## Features

### ■ Arm Cortex-M4 Core with Floating Point Unit (FPU)

- Armv7E-M architecture with DSP instruction set
- Maximum operating frequency: 120 MHz
- Support for 4-GB address space
- On-chip debugging system: JTAG, SWD, and ETM
- Boundary scan and Arm Memory Protection Unit (Arm MPU)

### ■ Memory

- Up to 512-KB code flash memory (40 MHz zero wait states)
- 8-KB data flash memory (125,000 erase/write cycles)
- 64-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Units (MPU)
- Memory Mirror Function (MMF)
- 128-bit unique ID

### ■ Connectivity

- Serial Communications Interface (SCI) with FIFO × 7
- Serial Peripheral Interface (SPI) × 2
- I<sup>2</sup>C bus interface (IIC) × 2
- CAN module (CAN) × 1
- IrDA interface

### ■ Analog

- 12-bit A/D Converter (ADC12) with 3 sample-and-hold circuits each × 2
- 12-bit D/A Converter (DAC12) × 2
- High-Speed Analog Comparator (ACMPHS) × 6
- Programmable Gain Amplifier (PGA) × 6
- Temperature Sensor (TSN)

### ■ Timers

- General PWM Timer 32-bit Enhanced High Resolution (GPT32EH) × 4
- General PWM Timer 32-bit Enhanced (GPT32E) × 4
- General PWM Timer 32-bit (GPT32) × 5
- Low Power Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

### ■ Safety

- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

### ■ System and Power Management

- Low power modes
- Event Link Controller (ELC)
- DMA Controller (DMAC) × 8
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

### ■ Security and Encryption

- AES128/192/256
- 3DES/ARC4
- SHA1/SHA224/SHA256/MD5
- GHASH
- RSA/DSA/ECC
- True Random Number Generator (TRNG)

### ■ Multiple Clock Sources

- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDG-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

### ■ General-Purpose I/O Ports

- Up to 76 input/output pins
  - Up to 9 CMOS input
  - Up to 67 CMOS input/output
  - Up to 14 input/output 5 V tolerant
  - Up to 13 high current (20 mA)

### ■ Operating Voltage

- VCC: 2.7 to 3.6 V

### ■ Operating Temperature and Packages

- Ta = -40°C to +105°C
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)

## 1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M4 core running up to 120 MHz with the following features:

- Up to 512-KB code flash memory
- 64-KB SRAM
- Security and safety features
- 12-bit A/D Converter (ADC12)
- 12-bit D/A Converter (DAC12)
- Analog peripherals.

### 1.1 Function Outline

**Table 1.1 Arm core**

| Feature            | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Arm Cortex-M4 core | <ul style="list-style-type: none"> <li>• Maximum operating frequency: up to 120 MHz</li> <li>• Arm Cortex-M4 core:               <ul style="list-style-type: none"> <li>- Revision: r0p1-01rel0</li> <li>- Armv7E-M architecture profile</li> <li>- Single precision floating-point unit compliant with the ANSI/IEEE Std 754-2008.</li> </ul> </li> <li>• Arm Memory Protection Unit (Arm MPU):               <ul style="list-style-type: none"> <li>- Armv7 Protected Memory System Architecture</li> <li>- 8 protect regions.</li> </ul> </li> <li>• SysTick timer:               <ul style="list-style-type: none"> <li>- Driven by SYSTICCLK (LOCO) or ICLK.</li> </ul> </li> </ul> |

**Table 1.2 Memory**

| Feature                      | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Code flash memory            | Up to 512-KB code flash memory. See section 41, Flash Memory in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| Data flash memory            | 8-KB data flash memory. See section 41, Flash Memory in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Memory Mirror Function (MMF) | The Memory Mirror Function (MMF) can be configured to mirror the target application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. Your application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual. |
| Option-setting memory        | The option-setting memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory in User's Manual.                                                                                                                                                                                                                                                                                                                                                                   |
| SRAM                         | On-chip high-speed SRAM. See section 40, SRAM in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                                   |

**Table 1.3 System (1 of 3)**

| Feature         | Functional description                                                                                                                                               |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Operating modes | Two operating modes: <ul style="list-style-type: none"> <li>• Single-chip mode</li> <li>• SCI boot mode.</li> </ul> See section 3, Operating Modes in User's Manual. |

**Table 1.3 System (2 of 3)**

| Feature                                            | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Resets                                             | <p>14 resets:</p> <ul style="list-style-type: none"> <li>• RES pin reset</li> <li>• Power-on reset</li> <li>• Voltage monitor 0 reset</li> <li>• Voltage monitor 1 reset</li> <li>• Voltage monitor 2 reset</li> <li>• Independent watchdog timer reset</li> <li>• Watchdog timer reset</li> <li>• Deep Software Standby reset</li> <li>• SRAM parity error reset</li> <li>• Bus master MPU error reset</li> <li>• Bus slave MPU error reset</li> <li>• Stack pointer error reset</li> <li>• Software reset.</li> </ul> <p>See section 6, Resets in User's Manual.</p>                                                                         |
| Low Voltage Detection (LVD)                        | <p>The Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD) in User's Manual.</p>                                                                                                                                                                                                                                                                                                                                                                                                                |
| Clocks                                             | <ul style="list-style-type: none"> <li>• Main clock oscillator (MOSC)</li> <li>• Sub-clock oscillator (SOSC)</li> <li>• High-speed on-chip oscillator (HOCO)</li> <li>• Middle-speed on-chip oscillator (MOCO)</li> <li>• Low-speed on-chip oscillator (LOCO)</li> <li>• PLL frequency synthesizer</li> <li>• IDWT-dedicated on-chip oscillator</li> <li>• Clock out support.</li> </ul> <p>See section 9, Clock Generation Circuit in User's Manual.</p>                                                                                                                                                                                      |
| Clock Frequency Accuracy Measurement Circuit (CAC) | <p>The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.</p> <p>When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.</p> <p>See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.</p> |
| Interrupt Controller Unit (ICU)                    | <p>The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 13, Interrupt Controller Unit (ICU) in User's Manual.</p>                                                                                                                                                                                                                                                                                                                                                                                                             |
| Key Interrupt Function (KINT)                      | <p>A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 20, Key Interrupt Function (KINT) in User's Manual.</p>                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Low power modes                                    | <p>Power consumption can be reduced in multiple ways, such as by setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 11, Low Power Modes in User's Manual.</p>                                                                                                                                                                                                                                                                                                                                                                                       |
| Register write protection                          | <p>The register write protection function protects important registers from being overwritten because of software errors. See section 12, Register Write Protection in User's Manual.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| Memory Protection Unit (MPU)                       | <p>Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 15, Memory Protection Unit (MPU) in User's Manual.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Watchdog Timer (WDT)                               | <p>The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and used as the condition for detecting when the system runs out of control. See section 25, Watchdog Timer (WDT) in User's Manual.</p>                                                                                                                                                       |

**Table 1.3 System (3 of 3)**

| Feature                           | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Independent Watchdog Timer (IWDT) | The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, or refresh error, or by a refresh of the count value in the registers. See section 26, Independent Watchdog Timer (IWDT) in User's Manual. |

**Table 1.4 Event link**

| Feature                     | Functional description                                                                                                                                                                                                                                                                             |
|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Event Link Controller (ELC) | The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 18, Event Link Controller (ELC) in User's Manual. |

**Table 1.5 Direct memory access**

| Feature                        | Functional description                                                                                                                                                                                                                                                                            |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Data Transfer Controller (DTC) | A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 17, Data Transfer Controller (DTC) in User's Manual.                                                                                                                |
| DMA Controller (DMAC)          | An 8-channel DMA Controller (DMAC) module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 16, DMA Controller (DMAC) in User's Manual. |

**Table 1.6 Timers**

| Feature                                            | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| General PWM Timer (GPT)                            | The General PWM Timer (GPT) is a 32-bit timer with 13 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 22, General PWM Timer (GPT) in User's Manual.                                                                                                        |
| Port Output Enable for GPT (POEG)                  | Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 21, Port Output Enable for GPT (POEG) in User's Manual.                                                                                                                                                                                                                                                                        |
| Low Power Asynchronous General-Purpose Timer (AGT) | The Low Power Asynchronous General-Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events.<br>This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and can be accessed with the AGT register. See section 24, Low Power Asynchronous General-Purpose Timer (AGT) in User's Manual. |

**Table 1.7 Communication interfaces**

| Feature                               | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Serial Communications Interface (SCI) | <p>The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces:</p> <ul style="list-style-type: none"> <li>• Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))</li> <li>• 8-bit clock synchronous interface</li> <li>• Simple IIC (master-only)</li> <li>• Simple SPI</li> <li>• Smart card interface.</li> </ul> <p>The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol.</p> <p>Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 27, Serial Communications Interface (SCI) in User's Manual.</p> |
| IrDA Interface (IrDA)                 | <p>The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0. See section 28, IrDA Interface in User's Manual.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| I <sup>2</sup> C bus interface (IIC)  | <p>The 2-channel I<sup>2</sup>C bus interface (IIC) conforms with and provides a subset of the NXP I<sup>2</sup>C (Inter-Integrated Circuit) bus interface functions. See section 29, I<sup>2</sup>C Bus Interface (IIC) in User's Manual.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Serial Peripheral Interface (SPI)     | <p>Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 31, Serial Peripheral Interface (SPI) in User's Manual.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Controller Area Network (CAN) module  | <p>The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically-noisy applications.</p> <p>The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 30, Controller Area Network (CAN) Module in User's Manual.</p>                                                                                                                                                                                                                        |

**Table 1.8 Analog**

| Feature                               | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12-bit A/D Converter (ADC12)          | <p>Two units of successive approximation 12-bit A/D Converter (ADC12) are provided. Analog input channels are selectable up to 11 in unit 0 and up to 8 in unit 1. Each 2 analog inputs of unit 0 and 1 are assigned to same port (AN005/AN105, AN006/AN106), up to 17 ports are available as analog input. The temperature sensor output and an internal reference voltage are selectable for conversion of each unit 0 and 1. The A/D conversion accuracy is selectable from 12-bit, 10-bit, and 8-bit conversion, making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 35, 12-Bit A/D Converter (ADC12) in User's Manual.</p> |
| 12-bit D/A Converter (DAC12)          | <p>A 12-bit D/A Converter (DAC12) converts data and includes an output amplifier. See section 36, 12-Bit D/A Converter (DAC12) in User's Manual.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Temperature Sensor (TSN)              | <p>The on-chip Temperature Sensor (TSN) can determine and monitor the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC12 for conversion and can also be used by the end application. See section 37, Temperature Sensor (TSN) in User's Manual.</p>                                                                                                                                                                                                                                |
| High-Speed Analog Comparator (ACMPHS) | <p>The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result.</p> <p>Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA.</p> <p>Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 38, High-Speed Analog Comparator (ACMPHS) in User's Manual.</p>                                                           |

**Table 1.9 Data processing**

| Feature                                  | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Cyclic Redundancy Check (CRC) calculator | The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generating polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 32, Cyclic Redundancy Check (CRC) Calculator in User's Manual. |
| Data Operation Circuit (DOC)             | The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 39, Data Operation Circuit (DOC) in User's Manual.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

**Table 1.10 Security**

| Feature                       | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Secure Crypto Engine 7 (SCE7) | <ul style="list-style-type: none"> <li>Security algorithms: <ul style="list-style-type: none"> <li>Symmetric algorithms: AES, 3DES, and ARC4</li> <li>Asymmetric algorithms: RSA, DSA, and ECC.</li> </ul> </li> <li>Other support features: <ul style="list-style-type: none"> <li>TRNG (True Random Number Generator)</li> <li>Hash-value generation: SHA1, SHA224, SHA256, GHASH, and MD5</li> <li>128-bit unique ID.</li> </ul> </li> </ul> |

**Table 1.11 I/O ports**

| Feature   | Functional description                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I/O ports | <ul style="list-style-type: none"> <li>I/O ports for the 100-pin LQFP <ul style="list-style-type: none"> <li>I/O pins: 67</li> <li>Input pins: 9</li> <li>Pull-Up resistors: 68</li> <li>N-ch open-drain outputs: 67</li> <li>5-V tolerance: 14</li> </ul> </li> <li>I/O ports for the 64-pin LQFP <ul style="list-style-type: none"> <li>I/O pins: 35</li> <li>Input pins: 5</li> <li>Pull-Up resistors: 36</li> <li>N-ch open-drain outputs: 35</li> <li>5-V tolerance: 9</li> </ul> </li> </ul> |

## 1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset, some individual devices within the group have a subset of the features.

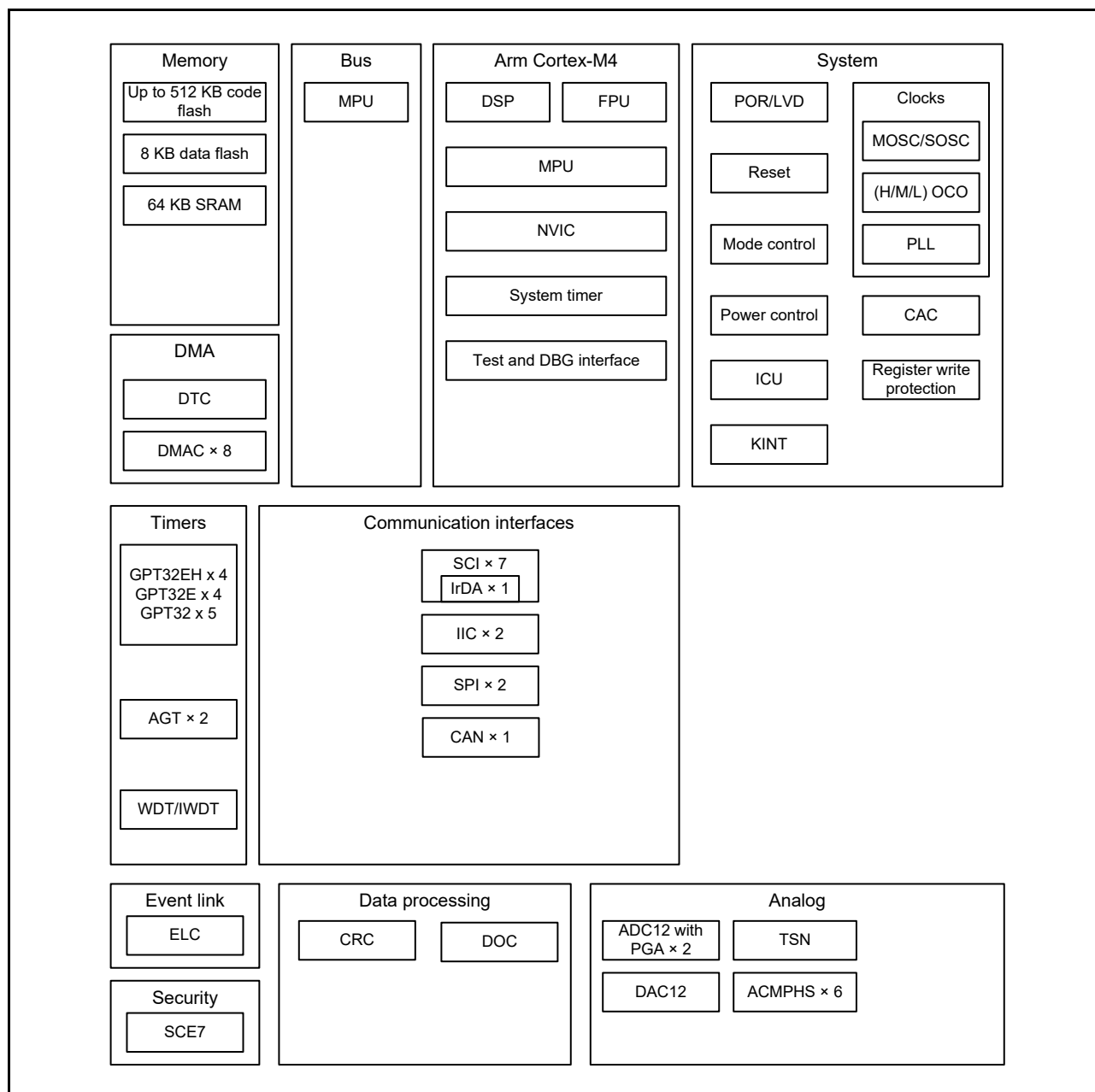


Figure 1.1 Block diagram

### 1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a list of products.

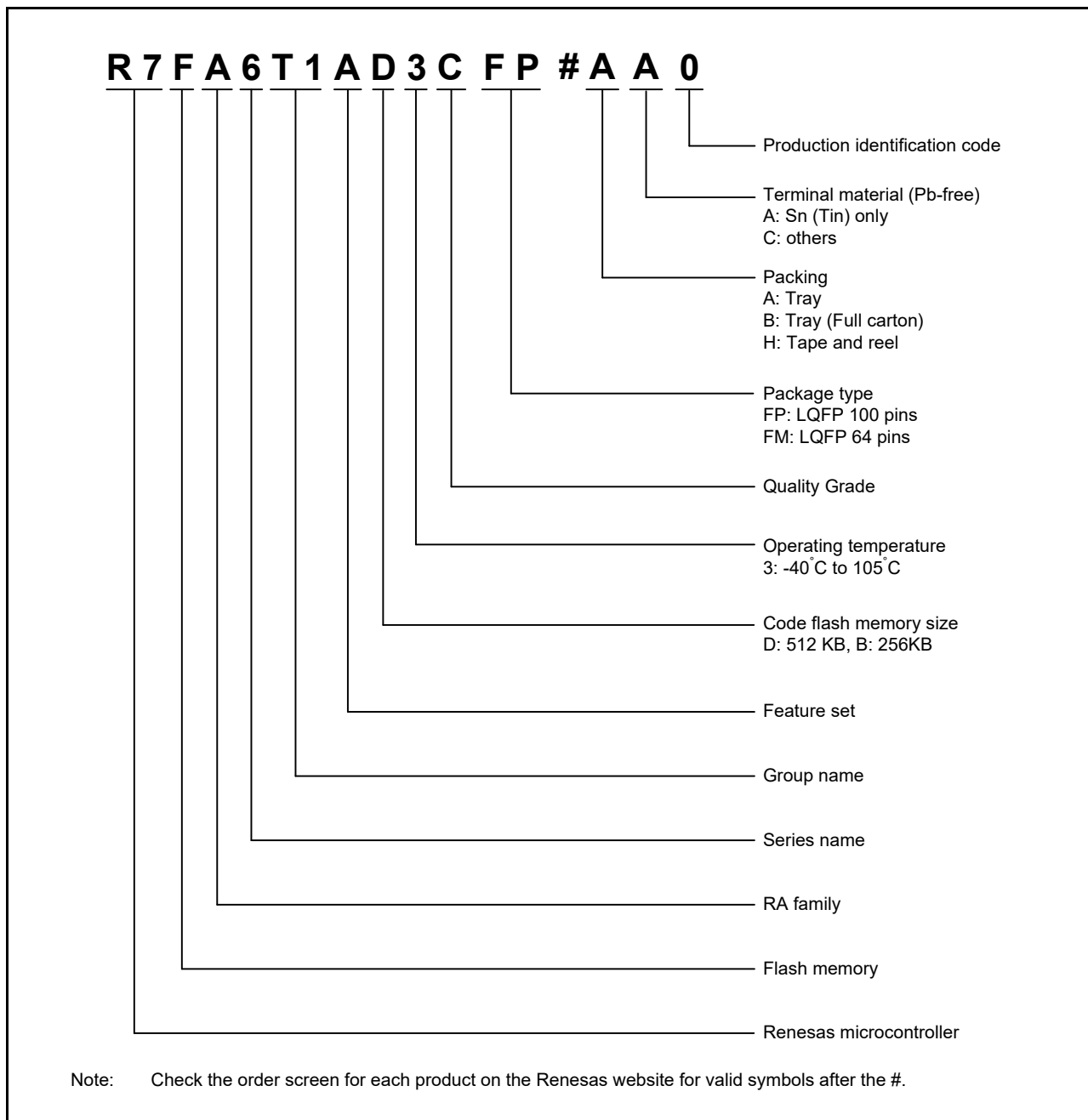


Figure 1.2 Part numbering scheme

Table 1.12 Product list

| Product part number | Package code | Code flash | Data flash | SRAM  | Operating temperature |
|---------------------|--------------|------------|------------|-------|-----------------------|
| R7FA6T1AD3CFP       | PLQP0100KB-B | 512 KB     | 8 KB       | 64 KB | -40 to +105°C         |
| R7FA6T1AB3CFP       | PLQP0100KB-B | 256 KB     |            |       | -40 to +105°C         |
| R7FA6T1AD3CFM       | PLQP0064KB-C | 512 KB     |            |       | -40 to +105°C         |
| R7FA6T1AB3CFM       | PLQP0064KB-C | 256 KB     |            |       | -40 to +105°C         |

## 1.4 Function Comparison

**Table 1.13 Functional comparison**

| Function          |                    | Part numbers                                     |  |               |  |                                                 |  |               |  |
|-------------------|--------------------|--------------------------------------------------|--|---------------|--|-------------------------------------------------|--|---------------|--|
|                   |                    | R7FA6T1AD3CFP                                    |  | R7FA6T1AB3CFP |  | R7FA6T1AD3CFM                                   |  | R7FA6T1AB3CFM |  |
| Pin count         |                    | 100                                              |  |               |  | 64                                              |  |               |  |
| Package           |                    | LQFP                                             |  |               |  |                                                 |  |               |  |
| Code flash memory |                    | 512 KB                                           |  | 256 KB        |  | 512 KB                                          |  | 256 KB        |  |
| Data flash memory |                    | 8 KB                                             |  |               |  |                                                 |  |               |  |
| SRAM              |                    | 64 KB                                            |  |               |  |                                                 |  |               |  |
|                   |                    | Parity                                           |  | 64 KB         |  |                                                 |  |               |  |
| System            | CPU clock          | 120 MHz                                          |  |               |  |                                                 |  |               |  |
|                   | Backup registers   | 512 Bytes                                        |  |               |  |                                                 |  |               |  |
|                   | ICU                | Yes                                              |  |               |  |                                                 |  |               |  |
|                   | KINT               | 8                                                |  |               |  |                                                 |  |               |  |
| Event link        | ELC                | Yes                                              |  |               |  |                                                 |  |               |  |
| DMA               | DTC                | Yes                                              |  |               |  |                                                 |  |               |  |
|                   | DMAC               | 8                                                |  |               |  |                                                 |  |               |  |
| Timers            | GPT32EH            | 4                                                |  |               |  |                                                 |  |               |  |
|                   | GPT32E             | 4                                                |  |               |  | 3                                               |  |               |  |
|                   | GPT32              | 5                                                |  |               |  | 4                                               |  |               |  |
|                   | AGT                | 2                                                |  |               |  |                                                 |  |               |  |
|                   | WDT/IWDT           | Yes                                              |  |               |  |                                                 |  |               |  |
| Communication     | SCI                | 7                                                |  |               |  |                                                 |  |               |  |
|                   | IIC                | 2                                                |  |               |  |                                                 |  |               |  |
|                   | SPI                | 2                                                |  |               |  |                                                 |  |               |  |
|                   | CAN                | 1                                                |  |               |  |                                                 |  |               |  |
| Analog            | ADC12              | Unit0: 11<br>Unit1: 8<br>Shared channel pin: 2*1 |  |               |  | Unit0: 7<br>Unit1: 3<br>Shared channel pin: 2*1 |  |               |  |
|                   | 3ch-S/H            | Unit0: 1 (3ch)<br>Unit1: 1 (3ch)                 |  |               |  | Unit0: 1 (3ch)                                  |  |               |  |
|                   | PGA                | Unit0: 3<br>Unit1: 3                             |  |               |  | Unit0: 3                                        |  |               |  |
|                   | DAC12              | 2                                                |  |               |  |                                                 |  |               |  |
|                   | ACMPHS             | 6                                                |  |               |  |                                                 |  |               |  |
|                   | TSN                | Yes                                              |  |               |  |                                                 |  |               |  |
| Data processing   | CRC                | Yes                                              |  |               |  |                                                 |  |               |  |
|                   | DOC                | Yes                                              |  |               |  |                                                 |  |               |  |
| Security          |                    | SCE7                                             |  |               |  |                                                 |  |               |  |
| I/O Ports         | I/O Pins           | 67                                               |  |               |  | 35                                              |  |               |  |
|                   | Input pins         | 9                                                |  |               |  | 5                                               |  |               |  |
|                   | Pull-up resistors  | 68                                               |  |               |  | 36                                              |  |               |  |
|                   | open-drain outputs | 67                                               |  |               |  | 35                                              |  |               |  |
|                   | 5-V tolerance      | 14                                               |  |               |  | 9                                               |  |               |  |

Note 1. Some input channels of the ADC units are sharing same port pin.

## 1.5 Pin Functions

**Table 1.14 Pin functions (1 of 3)**

| Function               | Signal                                   | I/O    | Description                                                                                                                                                                                                                                                                                       |
|------------------------|------------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Power supply           | VCC                                      | Input  | Power supply pin. This is used as the digital power supply for the respective modules and internal voltage regulator, and used to monitor the voltage of the POR/LVD. Connect this pin to the system power supply. Connect it to VSS by a 0.1-μF capacitor. Place the capacitor close to the pin. |
|                        | VCL0                                     | Input  | Connect this pin to VSS through a 0.1-μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.                                                                                                                                                   |
|                        | VCL                                      | Input  |                                                                                                                                                                                                                                                                                                   |
|                        | VSS                                      | Input  | Ground pin. Connect to the system power supply (0 V).                                                                                                                                                                                                                                             |
| Clock                  | XTAL                                     | Output | Pins for a crystal resonator. An external clock signal can be input through the XTAL pin.                                                                                                                                                                                                         |
|                        | EXTAL                                    | Input  |                                                                                                                                                                                                                                                                                                   |
|                        | XCIN                                     | Input  | Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOU and XCIN.                                                                                                                                                                                                |
|                        | XCOU                                     | Output |                                                                                                                                                                                                                                                                                                   |
|                        | CLKOUT                                   | Output | Clock output pin                                                                                                                                                                                                                                                                                  |
| Operating mode control | MD                                       | Input  | Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.                                                                                                                                            |
| System control         | RES                                      | Input  | Reset signal input pin. The MCU enters the reset state when this signal goes low.                                                                                                                                                                                                                 |
| CAC                    | CACREF                                   | Input  | Measurement reference clock input pin                                                                                                                                                                                                                                                             |
| Interrupt              | NMI                                      | Input  | Non-maskable interrupt request pin                                                                                                                                                                                                                                                                |
|                        | IRQ0 to IRQ13                            | Input  | Maskable interrupt request pins                                                                                                                                                                                                                                                                   |
| KINT                   | KR00 to KR07                             | Input  | A key interrupt can be generated by inputting a falling edge to the key interrupt input pins                                                                                                                                                                                                      |
| On-chip emulator       | TMS                                      | I/O    | On-chip emulator or boundary scan pins                                                                                                                                                                                                                                                            |
|                        | TDI                                      | Input  |                                                                                                                                                                                                                                                                                                   |
|                        | TCK                                      | Input  |                                                                                                                                                                                                                                                                                                   |
|                        | TDO                                      | Output |                                                                                                                                                                                                                                                                                                   |
|                        | TCLK                                     | Output | This pin outputs the clock for synchronization with the trace data                                                                                                                                                                                                                                |
|                        | TDATA0 to TDATA3                         | Output | Trace data output                                                                                                                                                                                                                                                                                 |
|                        | SWDIO                                    | I/O    | Serial wire debug data input/output pin                                                                                                                                                                                                                                                           |
|                        | SWCLK                                    | Input  | Serial wire clock pin                                                                                                                                                                                                                                                                             |
|                        | SWO                                      | Output | Serial wire trace output pin                                                                                                                                                                                                                                                                      |
| GPT                    | GTETRG, GTETRGB, GTETRGC, GTETRGD        | Input  | External trigger input pins                                                                                                                                                                                                                                                                       |
|                        | GTIOC0A to GTIOC12A, GTIOC0B to GTIOC12B | I/O    | Input capture, output compare, or PWM output pins                                                                                                                                                                                                                                                 |
|                        | GTIU                                     | Input  | Hall sensor input pin U                                                                                                                                                                                                                                                                           |
|                        | GTIV                                     | Input  | Hall sensor input pin V                                                                                                                                                                                                                                                                           |
|                        | GTIW                                     | Input  | Hall sensor input pin W                                                                                                                                                                                                                                                                           |
|                        | GTOUUP                                   | Output | 3-phase PWM output for BLDC motor control (positive U phase)                                                                                                                                                                                                                                      |
|                        | GTOULO                                   | Output | 3-phase PWM output for BLDC motor control (negative U phase)                                                                                                                                                                                                                                      |
|                        | GTOVUP                                   | Output | 3-phase PWM output for BLDC motor control (positive V phase)                                                                                                                                                                                                                                      |
|                        | GTOVLO                                   | Output | 3-phase PWM output for BLDC motor control (negative V phase)                                                                                                                                                                                                                                      |
|                        | GTOWUP                                   | Output | 3-phase PWM output for BLDC motor control (positive W phase)                                                                                                                                                                                                                                      |
|                        | GTOWLO                                   | Output | 3-phase PWM output for BLDC motor control (negative W phase)                                                                                                                                                                                                                                      |
| AGT                    | AGTEE0, AGTEE1                           | Input  | External event input enable signals                                                                                                                                                                                                                                                               |
|                        | AGTIO0, AGTIO1                           | I/O    | External event input and pulse output pins                                                                                                                                                                                                                                                        |
|                        | AGTO0, AGTO1                             | Output | Pulse output pins                                                                                                                                                                                                                                                                                 |
|                        | AGTOA0, AGTOA1                           | Output | Output compare match A output pins                                                                                                                                                                                                                                                                |
|                        | AGTOB0, AGTOB1                           | Output | Output compare match B output pins                                                                                                                                                                                                                                                                |

**Table 1.14 Pin functions (2 of 3)**

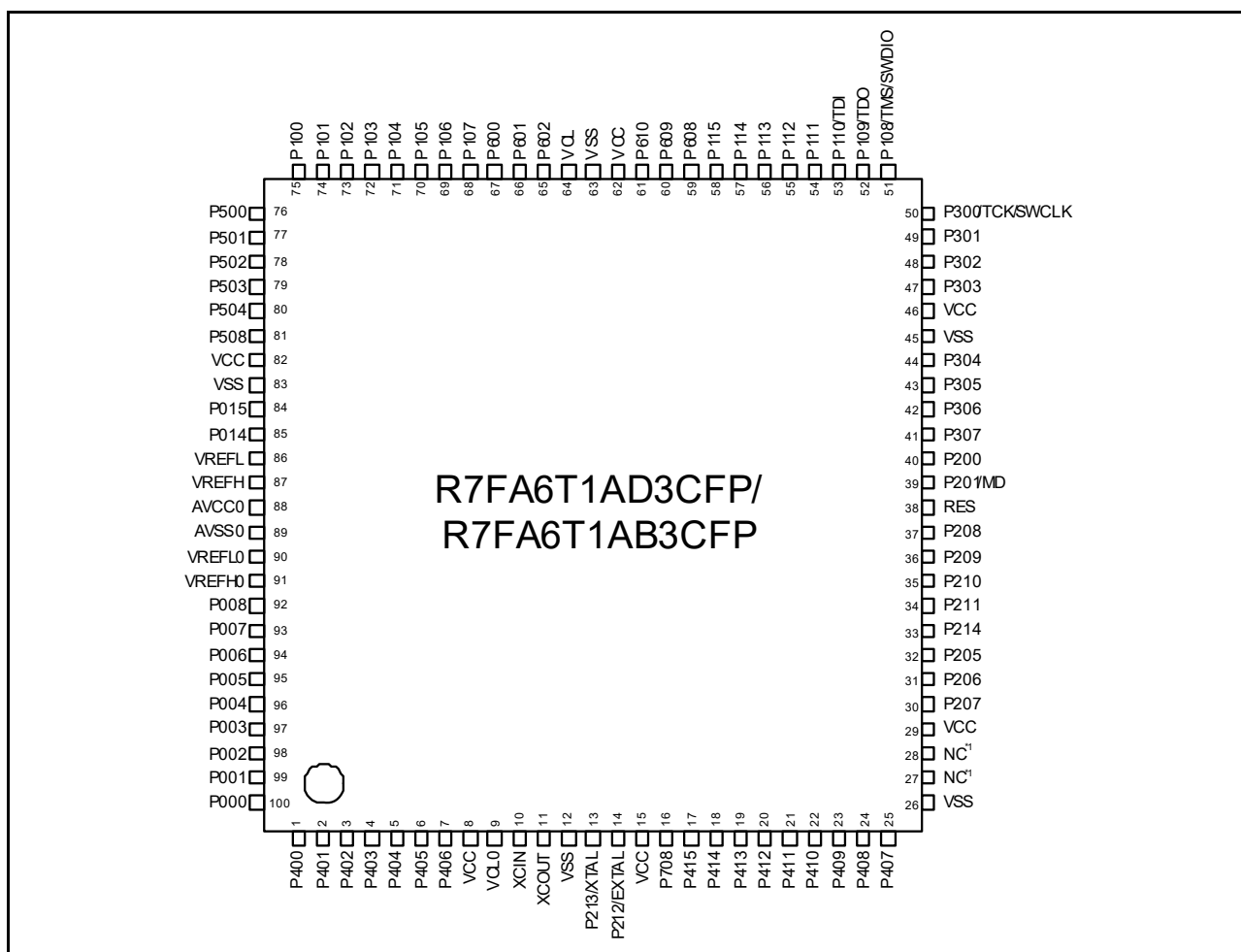
| Function            | Signal                                                | I/O    | Description                                                                                                                                                                                             |
|---------------------|-------------------------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SCI                 | SCK0 to SCK4, SCK8, SCK9                              | I/O    | Input/output pins for the clock (clock synchronous mode)                                                                                                                                                |
|                     | RXD0 to RXD4, RXD8, RXD9                              | Input  | Input pins for received data (asynchronous mode/clock synchronous mode)                                                                                                                                 |
|                     | TXD0 to TXD4, TXD8, TXD9                              | Output | Output pins for transmitted data (asynchronous mode/clock synchronous mode)                                                                                                                             |
|                     | CTS0_RTS0 to CTS4_RTS4, CTS8_RTS8, CTS9_RTS9          | I/O    | Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low                                                                        |
|                     | SCL0 to SCL4, SCL8, SCL9                              | I/O    | Input/output pins for the IIC clock (simple IIC mode)                                                                                                                                                   |
|                     | SDA0 to SDA4, SDA8, SDA9                              | I/O    | Input/output pins for the IIC data (simple IIC mode)                                                                                                                                                    |
|                     | SCK0 to SCK4, SCK8, SCK9                              | I/O    | Input/output pins for the clock (simple SPI mode)                                                                                                                                                       |
|                     | MISO0 to MISO4, MISO8, MISO9                          | I/O    | Input/output pins for slave transmission of data (simple SPI mode)                                                                                                                                      |
|                     | MOSI0 to MOSI4, MOSI8, MOSI9                          | I/O    | Input/output pins for master transmission of data (simple SPI mode)                                                                                                                                     |
|                     | SS0 to SS4, SS8, SS9                                  | Input  | Chip-select input pins (simple SPI mode), active-low                                                                                                                                                    |
| IIC                 | SCL0, SCL1                                            | I/O    | Input/output pins for the clock                                                                                                                                                                         |
|                     | SDA0, SDA1                                            | I/O    | Input/output pins for data                                                                                                                                                                              |
| SPI                 | RSPCKA, RSPCKB                                        | I/O    | Clock input/output pin                                                                                                                                                                                  |
|                     | MOSIA, MOSIB                                          | I/O    | Input or output pins for data output from the master                                                                                                                                                    |
|                     | MISOA, MISOB                                          | I/O    | Input or output pins for data output from the slave                                                                                                                                                     |
|                     | SSLA0, SSLB0                                          | I/O    | Input or output pin for slave selection                                                                                                                                                                 |
|                     | SSLA1 to SSLA3, SSLB1 to SSLB3                        | Output | Output pins for slave selection                                                                                                                                                                         |
| CAN                 | CRX0                                                  | Input  | Receive data                                                                                                                                                                                            |
|                     | CTX0                                                  | Output | Transmit data                                                                                                                                                                                           |
| Analog power supply | AVCC0                                                 | Input  | Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.                                                    |
|                     | AVSS0                                                 | Input  | Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.                                                                  |
|                     | VREFH0                                                | Input  | Analog reference voltage supply pin for the ADC12 (unit 0). Connect this pin to VCC when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002.                                   |
|                     | VREFL0                                                | Input  | Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002.                                                    |
|                     | VREFH                                                 | Input  | Analog reference voltage supply pin for the ADC12 (unit 1) and D/A Converter. Connect this pin to VCC when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter. |
|                     | VREFL                                                 | Input  | Analog reference ground pin for the ADC12 and D/A Converter. Connect this pin to VSS when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.                  |
| ADC12               | AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020 | Input  | Input pins for the analog signals to be processed by the ADC12. AN005 & AN105 and AN006 & AN106 are assigned to same port pin                                                                           |
|                     | AN100 to AN102, AN105 to AN107, AN116, AN117          | Input  |                                                                                                                                                                                                         |
|                     | ADTRG0                                                | Input  | Input pins for the external trigger signals that start the A/D conversion                                                                                                                               |
|                     | ADTRG1                                                | Input  |                                                                                                                                                                                                         |
|                     | PGAVSS000, PGAVSS100                                  | Input  | Pseudo-differential input pins                                                                                                                                                                          |

**Table 1.14 Pin functions (3 of 3)**

| Function  | Signal                        | I/O    | Description                                                       |
|-----------|-------------------------------|--------|-------------------------------------------------------------------|
| DAC12     | DA0, DA1                      | Output | Output pins for the analog signals processed by the D/A converter |
| ACMPHS    | VCOUT                         | Output | Comparator output pin                                             |
|           | IVREF0 to IVREF3              | Input  | Reference voltage input pins for comparator                       |
|           | IVCMP0 to IVCMP3              | Input  | Analog voltage input pins for comparator                          |
| I/O ports | P000 to P007                  | Input  | General-purpose input pins                                        |
|           | P008, P014, P015              | I/O    | General-purpose input/output pins                                 |
|           | P100 to P115                  | I/O    | General-purpose input/output pins                                 |
|           | P200                          | Input  | General-purpose input pin                                         |
|           | P201, P205 to P214            | I/O    | General-purpose input/output pins                                 |
|           | P300 to P307                  | I/O    | General-purpose input/output pins                                 |
|           | P400 to P415                  | I/O    | General-purpose input/output pins                                 |
|           | P500 to P504, P508            | I/O    | General-purpose input/output pins                                 |
|           | P600 to P602,<br>P608 to P610 | I/O    | General-purpose input/output pins                                 |
|           | P708                          | I/O    | General-purpose input/output pin                                  |

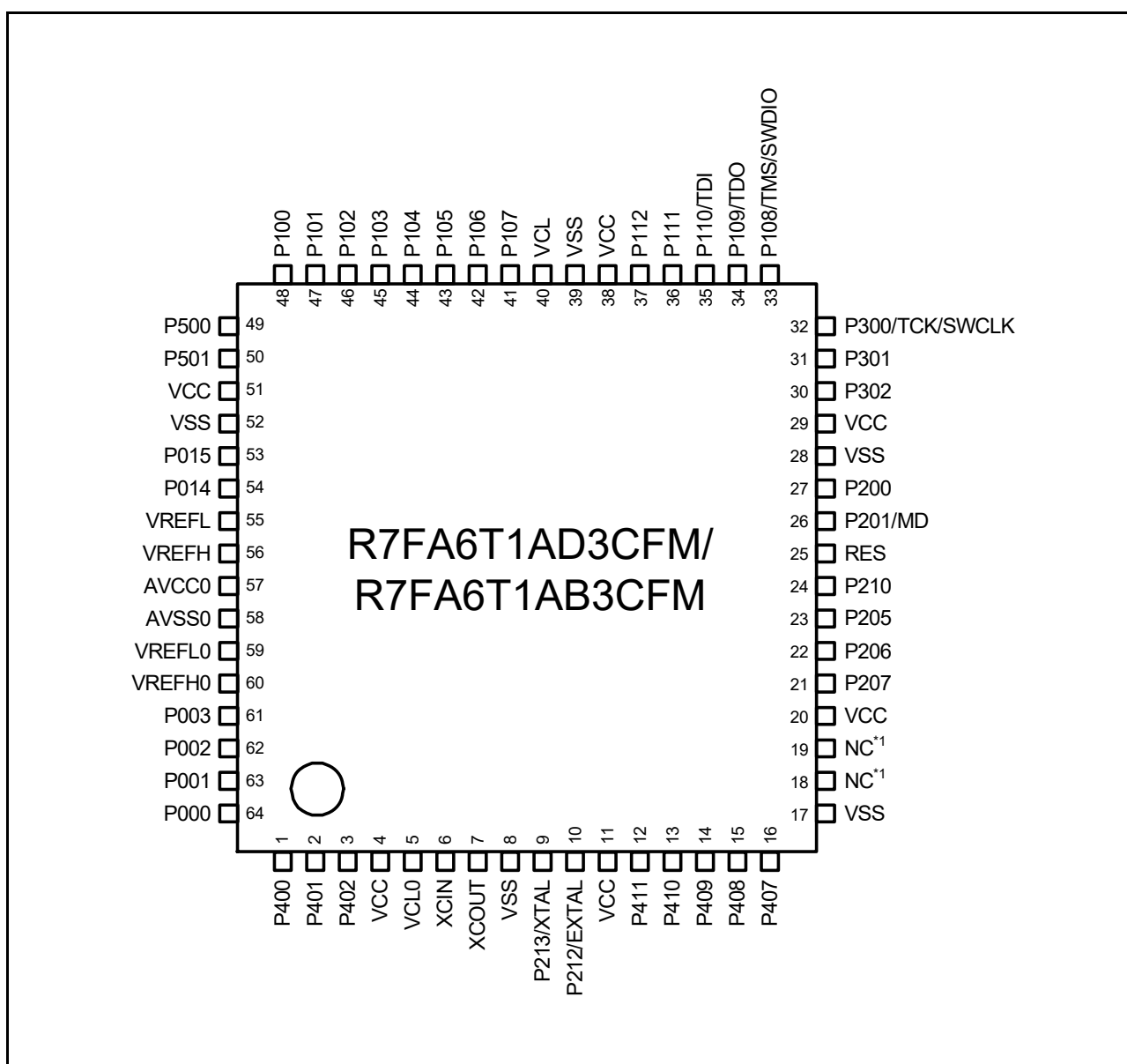
## 1.6 Pin Assignments

Figure 1.3 and Figure 1.4 show the pin assignments.



**Figure 1.3 Pin assignment for 100-pin LQFP (top view)**

Note 1. This pin should be left floating.



**Figure 1.4** Pin assignment for 64-pin LQFP (top view)

Note 1. This pin should be left floating.

## 1.7 Pin Lists

| Pin number |        |                |         |      |               | Timers  |           |      | Communication interfaces |                        |                      |        |          | Analog |               |
|------------|--------|----------------|---------|------|---------------|---------|-----------|------|--------------------------|------------------------|----------------------|--------|----------|--------|---------------|
| LQFP100    | LQFP64 |                |         |      |               | AGT     | GPT       | GPT  | CAN                      | SCI0,2,4,8<br>(30 MHz) | SCI1,3,9<br>(30 MHz) | IIC    | SPI      | ADC12  | DAC12, ACMPHS |
| 1          | 1      | -              | IRQ0    | P400 | AGTIO1        | -       | GTIOC6A   | -    | SCK4                     | -                      | SCL0_A               | -      | ADTRG1   | -      | -             |
| 2          | 2      | -              | IRQ5-DS | P401 | -             | GTETRGA | GTIOC6B   | CTX0 | CTS4_RTS4/S4             | -                      | SDA0_A               | -      | -        | -      | -             |
| 3          | 3      | CACREF         | IRQ4-DS | P402 | AGTIO0/AGTIO1 | -       | -         | CRX0 | -                        | -                      | -                    | -      | -        | -      | -             |
| 4          | -      | -              | -       | P403 | AGTIO0/AGTIO1 | -       | GTIOC3A   | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 5          | -      | -              | -       | P404 | -             | -       | GTIOC3B   | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 6          | -      | -              | -       | P405 | -             | -       | GTIOC1A   | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 7          | -      | -              | -       | P406 | -             | -       | GTIOC1B   | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 8          | 4      | VCC            | -       | -    | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 9          | 5      | VCL0           | -       | -    | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 10         | 6      | XCIN           | -       | -    | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 11         | 7      | XCOUT          | -       | -    | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 12         | 8      | VSS            | -       | -    | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 13         | 9      | XTAL           | IRQ2    | P213 | -             | GTETRGC | GTIOC0A   | -    | -                        | -                      | TXD1/MOSI1/S4        | -      | ADTRG1   | -      | -             |
| 14         | 10     | EXTAL          | IRQ3    | P212 | AGTEE1        | GTETRGD | GTIOC0B   | -    | -                        | -                      | RXD1/MISO1/SCL1      | -      | -        | -      | -             |
| 15         | 11     | VCC            | -       | -    | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 16         | -      | CACREF         | IRQ11   | P708 | -             | -       | -         | -    | -                        | -                      | RXD1/MISO1/SCL1      | -      | SSLA3_B  | -      | -             |
| 17         | -      | -              | IRQ8    | P415 | -             | -       | GTIOC0A   | -    | -                        | -                      | -                    | -      | SSLA2_B  | -      | -             |
| 18         | -      | -              | IRQ9    | P414 | -             | -       | GTIOC0B   | -    | -                        | -                      | -                    | -      | SSLA1_B  | -      | -             |
| 19         | -      | -              | -       | P413 | -             | GTOUUP  | -         | -    | CTS0_RTS0/S0             | -                      | -                    | -      | SSLA0_B  | -      | -             |
| 20         | -      | -              | -       | P412 | AGTEE1        | GTOULO  | -         | -    | SCK0                     | -                      | -                    | -      | RSPCKA_B | -      | -             |
| 21         | 12     | -              | IRQ4    | P411 | AGTOA1        | GTOVUP  | GTIOC9A   | -    | TXD0/MOSI0/S4            | CTS3_RTS3/S3           | -                    | -      | MOSIA_B  | -      | -             |
| 22         | 13     | -              | IRQ5    | P410 | AGTOB1        | GTOVLO  | GTIOC9B   | -    | RXD0/MISO0/SCL0          | SCK3                   | -                    | -      | MISOA_B  | -      | -             |
| 23         | 14     | -              | IRQ6    | P409 | -             | GTOUUP  | GTIOC10A  | -    | -                        | -                      | TXD3/MOSI3/S4        | -      | -        | -      | -             |
| 24         | 15     | -              | IRQ7    | P408 | -             | GTOVLO  | GTIOC10B  | -    | -                        | -                      | RXD3/MISO3/SCL3      | SCL0_B | -        | -      | -             |
| 25         | 16     | -              | -       | P407 | AGTIO0        | -       | -         | -    | CTS4_RTS4/S4             | -                      | SDA0_B               | -      | ADTRG0   | -      | -             |
| 26         | 17     | VSS            | -       | -    | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 27         | 18     | -              | -       | -    | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 28         | 19     | -              | -       | -    | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 29         | 20     | VCC            | -       | -    | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 30         | 21     | -              | -       | P207 | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 31         | 22     | -              | IRQ0-DS | P206 | -             | GTIU    | -         | -    | RXD4/MISO4/SCL4          | -                      | SDA1_A               | -      | -        | -      | -             |
| 32         | 23     | CLKOUT         | IRQ1-DS | P205 | AGTO1         | GTIV    | GTIOC4A   | -    | TXD4/MOSI4/S4            | CTS9_RTS9/S9           | SCL1_A               | -      | -        | -      | -             |
| 33         | -      | TCLK           | -       | P214 | -             | GTIU    | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 34         | -      | TDATA0         | -       | P211 | -             | GTIV    | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 35         | 24     | TDATA1         | -       | P210 | -             | GTIW    | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 36         | -      | TDATA2         | -       | P209 | -             | GTOVUP  | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 37         | -      | TDATA3         | -       | P208 | -             | GTOVLO  | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 38         | 25     | RES            | -       | -    | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 39         | 26     | MD             | -       | P201 | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 40         | 27     | -              | NMI     | P200 | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 41         | -      | -              | -       | P307 | -             | GTOUUP  | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 42         | -      | -              | -       | P306 | -             | GTOULO  | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 43         | -      | -              | IRQ8    | P305 | -             | GTOUUP  | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 44         | -      | -              | IRQ9    | P304 | -             | GTOVLO  | GTIOC7A   | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 45         | 28     | VSS            | -       | -    | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 46         | 29     | VCC            | -       | -    | -             | -       | -         | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 47         | -      | -              | -       | P303 | -             | -       | GTIOC7B   | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 48         | 30     | -              | IRQ5    | P302 | -             | GTOUUP  | GTIOC4A   | -    | TXD2/MOSI2/S4            | -                      | SSLB3_B              | -      | -        | -      | -             |
| 49         | 31     | -              | IRQ6    | P301 | AGTIO0        | GTOULO  | GTIOC4B   | -    | RXD2/MISO2/SCL2          | CTS9_RTS9/S9           | SSLB2_B              | -      | -        | -      | -             |
| 50         | 32     | TCK/SWCLK      | -       | P300 | -             | GTOUUP  | GTIOC0A_A | -    | -                        | -                      | -                    | -      | SSLB1_B  | -      | -             |
| 51         | 33     | TMS/SWDIO      | -       | P108 | -             | GTOULO  | GTIOC0B_A | -    | -                        | CTS9_RTS9/S9           | -                    | -      | SSLB0_B  | -      | -             |
| 52         | 34     | CLKOUT/TDO/SWO | -       | P109 | -             | GTOVUP  | GTIOC1A_A | -    | -                        | TXD9/MOSI9/S4          | -                    | -      | MOSIB_B  | -      | -             |
| 53         | 35     | TDI            | IRQ3    | P110 | -             | GTOVLO  | GTIOC1B_A | -    | CTS2_RTS2/S2             | RXD9/MISO9/SCL9        | -                    | -      | MISOB_B  | -      | VCOOUT        |
| 54         | 36     | -              | IRQ4    | P111 | -             | -       | GTIOC3A_A | -    | SCK2                     | SCK9                   | -                    | -      | RSPCKB_B | -      | -             |
| 55         | 37     | -              | -       | P112 | -             | -       | GTIOC3B_A | -    | TXD2/MOSI2/S4            | SCK1                   | -                    | -      | SSLB0_B  | -      | -             |
| 56         | -      | -              | -       | P113 | -             | -       | GTIOC2A   | -    | RXD2/MISO2/SCL2          | -                      | -                    | -      | -        | -      | -             |
| 57         | -      | -              | -       | P114 | -             | -       | GTIOC2B   | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 58         | -      | -              | -       | P115 | -             | -       | GTIOC4A   | -    | -                        | -                      | -                    | -      | -        | -      | -             |
| 59         | -      | -              | -       | P608 | -             | -       | GTIOC4B   | -    | -                        | -                      | -                    | -      | -        | -      | -             |

| Pin number |        |                   |           |      |        | Timers  |           |         | Communication interfaces |                        |                      |        |          | Analog              |                |
|------------|--------|-------------------|-----------|------|--------|---------|-----------|---------|--------------------------|------------------------|----------------------|--------|----------|---------------------|----------------|
| LQFP100    | LQFP64 |                   |           |      |        | AGT     | GPT       | GPT     | CAN                      | SCI0,2,4,8<br>(30 MHz) | SCI1,3,9<br>(30 MHz) | IIC    | SPI      | ADC12               | DAC12, ACMPHS  |
| 60         | -      | -                 | -         | P609 | -      | -       | -         | GTIOC5A | -                        | -                      | -                    | -      | -        | -                   | -              |
| 61         | -      | -                 | -         | P610 | -      | -       | -         | GTIOC5B | -                        | -                      | -                    | -      | -        | -                   | -              |
| 62         | 38     | VCC               | -         | -    | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | -                   | -              |
| 63         | 39     | VSS               | -         | -    | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | -                   | -              |
| 64         | 40     | VCL               | -         | -    | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | -                   | -              |
| 65         | -      | -                 | -         | P602 | -      | -       | -         | GTIOC7B | -                        | -                      | TXD9                 | -      | -        | -                   | -              |
| 66         | -      | -                 | -         | P601 | -      | -       | -         | GTIOC6A | -                        | -                      | RXD9                 | -      | -        | -                   | -              |
| 67         | -      | CLKOUT/CAC<br>REF | -         | P600 | -      | -       | -         | GTIOC6B | -                        | -                      | SCK9                 | -      | -        | -                   | -              |
| 68         | 41     | -                 | KR07      | P107 | AGTOA0 | -       | -         | GTIOC8A | -                        | CTS8_RTS8/S<br>S8      | -                    | -      | -        | -                   | -              |
| 69         | 42     | -                 | KR06      | P106 | AGTOB0 | -       | -         | GTIOC8B | -                        | SCK8                   | -                    | -      | SSLA3_A  | -                   | -              |
| 70         | 43     | -                 | IRQ0/KR05 | P105 | -      | GTETRGA | GTIOC1A   | -       | -                        | TXD8/MOSI8/S<br>DA8    | -                    | -      | SSLA2_A  | -                   | -              |
| 71         | 44     | -                 | IRQ1/KR04 | P104 | -      | GTETRGA | GTIOC1B   | -       | -                        | RXD8/MISO8/S<br>CL8    | -                    | -      | SSLA1_A  | -                   | -              |
| 72         | 45     | -                 | KR03      | P103 | -      | GTOWUP  | GTIOC2A_A | CTX0    | -                        | CTS0_RTS0/S<br>S0      | -                    | -      | SSLA0_A  | -                   | -              |
| 73         | 46     | -                 | KR02      | P102 | AGTO0  | GTOWLO  | GTIOC2B_A | CRX0    | -                        | SCK0                   | -                    | -      | RSPCKA_A | ADTRG0              | -              |
| 74         | 47     | -                 | IRQ1/KR01 | P101 | AGTEE0 | GTETRGA | GTIOC5A   | -       | -                        | TXD0/MOSI0/S<br>DA0    | CTS1_RTS1/S<br>S1    | SDA1_B | MOSIA_A  | -                   | -              |
| 75         | 48     | -                 | IRQ2/KR00 | P100 | AGTIO0 | GTETRGA | GTIOC5B   | -       | -                        | RXD0/MISO0/S<br>CL0    | SCK1                 | SCL1_B | MISOA_A  | -                   | -              |
| 76         | 49     | -                 | -         | P500 | AGTOA0 | GTIU    | GTIOC11A  | -       | -                        | -                      | -                    | -      | -        | AN016               | IVREF0         |
| 77         | 50     | -                 | IRQ11     | P501 | AGTOB0 | GTIV    | GTIOC11B  | -       | -                        | -                      | -                    | -      | -        | AN116               | IVREF1         |
| 78         | -      | -                 | IRQ12     | P502 | -      | GTIW    | GTIOC12A  | -       | -                        | -                      | -                    | -      | -        | AN017               | IVCMP0         |
| 79         | -      | -                 | -         | P503 | -      | GTETRGC | GTIOC12B  | -       | -                        | -                      | -                    | -      | -        | AN117               | -              |
| 80         | -      | -                 | -         | P504 | -      | GTETRGD | -         | -       | -                        | -                      | -                    | -      | -        | AN018               | -              |
| 81         | -      | -                 | -         | P508 | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | AN020               | -              |
| 82         | 51     | VCC               | -         | -    | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | -                   | -              |
| 83         | 52     | VSS               | -         | -    | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | -                   | -              |
| 84         | 53     | -                 | IRQ13     | P015 | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | AN006/AN106         | DA1/<br>IVCMP1 |
| 85         | 54     | -                 | -         | P014 | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | AN005/AN105         | DA0/<br>IVREF3 |
| 86         | 55     | VREFL             | -         | -    | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | -                   | -              |
| 87         | 56     | VREFH             | -         | -    | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | -                   | -              |
| 88         | 57     | AVCC0             | -         | -    | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | -                   | -              |
| 89         | 58     | AVSS0             | -         | -    | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | -                   | -              |
| 90         | 59     | VREFL0            | -         | -    | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | -                   | -              |
| 91         | 60     | VREFH0            | -         | -    | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | -                   | -              |
| 92         | -      | -                 | IRQ12-DS  | P008 | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | AN003               | -              |
| 93         | -      | -                 | -         | P007 | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | PGAVSS100/<br>AN107 | -              |
| 94         | -      | -                 | IRQ11-DS  | P006 | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | AN102               | IVCMP2         |
| 95         | -      | -                 | IRQ10-DS  | P005 | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | AN101               | IVCMP2         |
| 96         | -      | -                 | IRQ9-DS   | P004 | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | AN100               | IVCMP2         |
| 97         | 61     | -                 | -         | P003 | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | PGAVSS000/<br>AN007 | -              |
| 98         | 62     | -                 | IRQ8-DS   | P002 | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | AN002               | IVCMP2         |
| 99         | 63     | -                 | IRQ7-DS   | P001 | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | AN001               | IVCMP2         |
| 100        | 64     | -                 | IRQ6-DS   | P000 | -      | -       | -         | -       | -                        | -                      | -                    | -      | -        | AN000               | IVCMP2         |

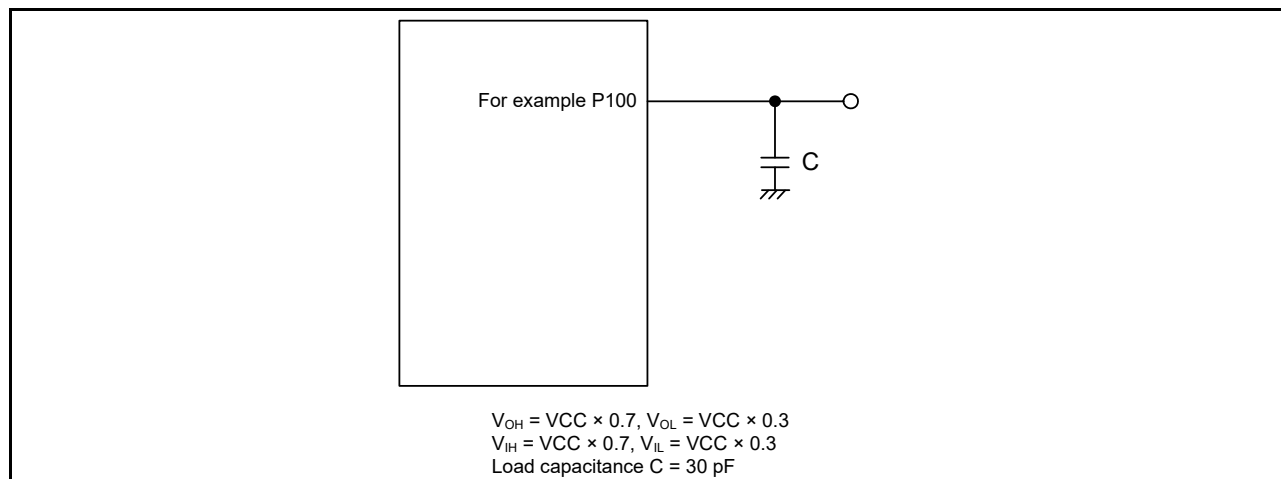
Note: Some pin names have the added suffix of \_A and \_B. When assigning the GPT, IIC, and SPI functionality, select the functional pins with the same suffix.

## 2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- $VCC = AVCC0 = 2.7$  to  $3.6$  V
- $2.7 \leq VREFH0/VREFH \leq AVCC0$
- $VSS = AVSS0 = VREFL0/VREFL = 0$  V
- $T_a = T_{opr}$

Figure 2.1 shows the timing conditions.



**Figure 2.1** Input or output timing measurement conditions

The measurement conditions for the timing specification of each peripheral are recommended for the best peripheral operation. However, make sure to adjust the driving abilities of each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the A/C specification of each function is not guaranteed.

### 2.1 Absolute Maximum Ratings

**Table 2.1** Absolute maximum ratings

| Parameter                                                                                       | Symbol       | Value                          | Unit |
|-------------------------------------------------------------------------------------------------|--------------|--------------------------------|------|
| Power supply voltage                                                                            | VCC          | -0.3 to +4.0                   | V    |
| Input voltage (except for 5 V-tolerant ports*1)                                                 | $V_{in}$     | -0.3 to VCC + 0.3              | V    |
| Input voltage (5 V-tolerant ports*1)                                                            | $V_{in}$     | -0.3 to + VCC + 4.0 (max. 5.8) | V    |
| Reference power supply voltage                                                                  | VREFH/VREFH0 | -0.3 to AVCC0 + 0.3            | V    |
| Analog power supply voltage                                                                     | AVCC0 *2     | -0.3 to +4.0                   | V    |
| Analog input voltage (except for P000 to P007)                                                  | $V_{AN}$     | -0.3 to AVCC0 + 0.3            | V    |
| Analog input voltage (P000 to P007) when PGA pseudo-differential input is disabled              | $V_{AN}$     | -0.3 to AVCC0 + 0.3            | V    |
| Analog input voltage (P000 to P002, P004 to P006) when PGA pseudo-differential input is enabled | $V_{AN}$     | -1.3 to AVCC0 + 0.3            | V    |
| Analog input voltage (P003, P007) when PGA pseudo-differential input is enabled                 | $V_{AN}$     | -0.8 to AVCC0 + 0.3            | V    |
| Operating temperature*3, *4                                                                     | $T_{opr}$    | -40 to +105                    | °C   |
| Storage temperature                                                                             | $T_{stg}$    | -55 to +125                    | °C   |

**Caution:** Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Note 1. Ports P205, P206, P400, P401, P407 to P415, and P708 are 5 V tolerant.

Note 2. Connect AVCC0 to VCC.

Note 3. See section 2.2.1,  $T_j/T_a$  Definition.

Note 4. Contact Renesas Electronics sales office for information on derating operation when  $T_a = +85^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ . Derating is the systematic reduction of load for improved reliability.

**Table 2.2 Recommended operating conditions**

| Parameter                    | Symbol  | Min | Typ | Max | Unit |
|------------------------------|---------|-----|-----|-----|------|
| Power supply voltages        | VCC     | 2.7 | -   | 3.6 | V    |
|                              | VSS     | -   | 0   | -   | V    |
| Analog power supply voltages | AVCC0*1 | -   | VCC | -   | V    |
|                              | AVSS0   | -   | 0   | -   | V    |

Note 1. Connect AVCC0 to VCC. When the A/D converter, the D/A converter, or the comparator are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

## 2.2 DC Characteristics

### 2.2.1 $T_j/T_a$ Definition

**Table 2.3 DC characteristics**

Conditions: Products with operating temperature ( $T_a$ )  $-40$  to  $+105^{\circ}\text{C}$ .

| Parameter                        |                             | Symbol | Typ | Max | Unit               | Test conditions                                         |
|----------------------------------|-----------------------------|--------|-----|-----|--------------------|---------------------------------------------------------|
| Permissible junction temperature | 100-pin LQFP<br>64-pin LQFP | $T_j$  | -   | 125 | $^{\circ}\text{C}$ | High-speed mode<br>Low-speed mode<br>Subosc-speed mode. |

Note: Make sure that  $T_j = T_a + \theta_{ja} \times \text{total power consumption (W)}$ ,  
where total power consumption =  $(V_{CC} - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CCmax} \times V_{CC}$ .

### 2.2.2 I/O $V_{IH}$ , $V_{IL}$

**Table 2.4 I/O  $V_{IH}$ ,  $V_{IL}$  (1 of 2)**

| Parameter                                                      |                               |                                                    | Symbol       | Min                  | Typ | Max                         | Unit |
|----------------------------------------------------------------|-------------------------------|----------------------------------------------------|--------------|----------------------|-----|-----------------------------|------|
| Input voltage<br>(except for<br>Schmitt trigger<br>input pins) | Peripheral<br>function<br>pin | EXTAL(external clock input), SPI (except<br>RSPCK) | $V_{IH}$     | $V_{CC} \times 0.8$  | -   | -                           | V    |
|                                                                |                               |                                                    | $V_{IL}$     | -                    | -   | $V_{CC} \times 0.2$         |      |
|                                                                |                               | IIC (SMBus)*1                                      | $V_{IH}$     | 2.1                  | -   | -                           |      |
|                                                                |                               |                                                    | $V_{IL}$     | -                    | -   | 0.8                         |      |
| Schmitt trigger<br>input voltage                               |                               | IIC (SMBus)*2                                      | $V_{IH}$     | 2.1                  | -   | $V_{CC} + 3.6$<br>(max 5.8) |      |
|                                                                |                               |                                                    | $V_{IL}$     | -                    | -   | 0.8                         |      |
|                                                                |                               | IIC (except for SMBus)*1                           | $V_{IH}$     | $V_{CC} \times 0.7$  | -   | -                           |      |
|                                                                |                               |                                                    | $V_{IL}$     | -                    | -   | $V_{CC} \times 0.3$         |      |
|                                                                |                               |                                                    | $\Delta V_T$ | $V_{CC} \times 0.05$ | -   | -                           |      |
|                                                                |                               | IIC (except for SMBus)*2                           | $V_{IH}$     | $V_{CC} \times 0.7$  | -   | $V_{CC} + 3.6$<br>(max 5.8) |      |
|                                                                |                               |                                                    | $V_{IL}$     | -                    | -   | $V_{CC} \times 0.3$         |      |
|                                                                |                               |                                                    | $\Delta V_T$ | $V_{CC} \times 0.05$ | -   | -                           |      |
|                                                                |                               | 5 V-tolerant ports*3, *7                           | $V_{IH}$     | $V_{CC} \times 0.8$  | -   | $V_{CC} + 3.6$<br>(max 5.8) |      |
|                                                                |                               |                                                    | $V_{IL}$     | -                    | -   | $V_{CC} \times 0.2$         |      |
|                                                                |                               |                                                    | $\Delta V_T$ | $V_{CC} \times 0.05$ | -   | -                           |      |

**Table 2.4** I/O  $V_{IH}$ ,  $V_{IL}$  (2 of 2)

| Parameter                     |                         |                                | Symbol       | Min               | Typ | Max                      | Unit |
|-------------------------------|-------------------------|--------------------------------|--------------|-------------------|-----|--------------------------|------|
| Schmitt trigger input voltage | Peripheral function pin | P402/AGTIO0,1<br>P403/AGTIO0,1 | $V_{IH}$     | $VCC \times 0.8$  | -   | $VCC + 0.3$              | V    |
|                               |                         |                                | $V_{IL}$     | -                 | -   | $VCC \times 0.2$         |      |
|                               |                         |                                | $\Delta V_T$ | $VCC \times 0.05$ | -   | -                        |      |
|                               |                         | Other input pins*4             | $V_{IH}$     | $VCC \times 0.8$  | -   | -                        |      |
|                               |                         |                                | $V_{IL}$     | -                 | -   | $VCC \times 0.2$         |      |
|                               |                         |                                | $\Delta V_T$ | $VCC \times 0.05$ | -   | -                        |      |
|                               | Ports                   | 5 V-tolerant ports*5, *7       | $V_{IH}$     | $VCC \times 0.8$  | -   | $VCC + 3.6$<br>(max 5.8) |      |
|                               |                         |                                | $V_{IL}$     | -                 | -   | $VCC \times 0.2$         |      |
|                               |                         | Other input pins*6             | $V_{IH}$     | $VCC \times 0.8$  | -   | -                        |      |
|                               |                         |                                | $V_{IL}$     | -                 | -   | $VCC \times 0.2$         |      |

Note 1. SCL1\_B, SDA1\_B (total 2 pins).

Note 2. SCL0\_A, SDA0\_A, SCL0\_B, SDA0\_B, SCL1\_A, SDA1\_A (total 6 pins).

Note 3. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P708 (total 15 pins).

Note 4. All input pins except for the peripheral function pins already described in the table.

Note 5. P205, P206, P400, P401, P407 to P415, P708 (total 14 pins).

Note 6. All input pins except for the ports already described in the table.

Note 7. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the breakdown voltage.

### 2.2.3 I/O $I_{OH}$ , $I_{OL}$

**Table 2.5** I/O  $I_{OH}$ ,  $I_{OL}$  (1 of 2)

| Parameter                                             |                                                               |                | Symbol   | Min | Typ | Max  | Unit |
|-------------------------------------------------------|---------------------------------------------------------------|----------------|----------|-----|-----|------|------|
| Permissible output current<br>(average value per pin) | Ports P008, P201                                              | -              | $I_{OH}$ | -   | -   | -2.0 | mA   |
|                                                       |                                                               |                | $I_{OL}$ | -   | -   | 2.0  | mA   |
|                                                       | Ports P014, P015                                              | -              | $I_{OH}$ | -   | -   | -4.0 | mA   |
|                                                       |                                                               |                | $I_{OL}$ | -   | -   | 4.0  | mA   |
|                                                       | Ports P205, P206, P407 to P415,<br>P602, P708 (total 13 pins) | Low drive*1    | $I_{OH}$ | -   | -   | -2.0 | mA   |
|                                                       |                                                               |                | $I_{OL}$ | -   | -   | 2.0  | mA   |
|                                                       |                                                               | Middle drive*2 | $I_{OH}$ | -   | -   | -4.0 | mA   |
|                                                       |                                                               |                | $I_{OL}$ | -   | -   | 4.0  | mA   |
|                                                       |                                                               | High drive*3   | $I_{OH}$ | -   | -   | -20  | mA   |
|                                                       |                                                               |                | $I_{OL}$ | -   | -   | 20   | mA   |
|                                                       | Other output pins*4                                           | Low drive*1    | $I_{OH}$ | -   | -   | -2.0 | mA   |
|                                                       |                                                               |                | $I_{OL}$ | -   | -   | 2.0  | mA   |
|                                                       |                                                               | Middle drive*2 | $I_{OH}$ | -   | -   | -4.0 | mA   |
|                                                       |                                                               |                | $I_{OL}$ | -   | -   | 4.0  | mA   |
|                                                       |                                                               | High drive*3   | $I_{OH}$ | -   | -   | -16  | mA   |
|                                                       |                                                               |                | $I_{OL}$ | -   | -   | 16   | mA   |

**Table 2.5 I/O  $I_{OH}$ ,  $I_{OL}$  (2 of 2)**

| Parameter                                                      |                                                               |                | Symbol                 | Min | Typ | Max  | Unit |
|----------------------------------------------------------------|---------------------------------------------------------------|----------------|------------------------|-----|-----|------|------|
| Permissible output current<br>(max value per pin)              | Ports P008, P201                                              | -              | I <sub>OH</sub>        | -   | -   | -4.0 | mA   |
|                                                                |                                                               |                | I <sub>OL</sub>        | -   | -   | 4.0  | mA   |
|                                                                | Ports P014, P015                                              | -              | I <sub>OH</sub>        | -   | -   | -8.0 | mA   |
|                                                                |                                                               |                | I <sub>OL</sub>        | -   | -   | 8.0  | mA   |
|                                                                | Ports P205, P206, P407 to P415,<br>P602, P708 (total 13 pins) | Low drive*1    | I <sub>OH</sub>        | -   | -   | -4.0 | mA   |
|                                                                |                                                               |                | I <sub>OL</sub>        | -   | -   | 4.0  | mA   |
|                                                                |                                                               | Middle drive*2 | I <sub>OH</sub>        | -   | -   | -8.0 | mA   |
|                                                                |                                                               |                | I <sub>OL</sub>        | -   | -   | 8.0  | mA   |
|                                                                |                                                               | High drive*3   | I <sub>OH</sub>        | -   | -   | -40  | mA   |
|                                                                |                                                               |                | I <sub>OL</sub>        | -   | -   | 40   | mA   |
|                                                                | Other output pins*4                                           | Low drive*1    | I <sub>OH</sub>        | -   | -   | -4.0 | mA   |
|                                                                |                                                               |                | I <sub>OL</sub>        | -   | -   | 4.0  | mA   |
|                                                                |                                                               | Middle drive*2 | I <sub>OH</sub>        | -   | -   | -8.0 | mA   |
|                                                                |                                                               |                | I <sub>OL</sub>        | -   | -   | 8.0  | mA   |
|                                                                |                                                               | High drive*3   | I <sub>OH</sub>        | -   | -   | -32  | mA   |
|                                                                |                                                               |                | I <sub>OL</sub>        | -   | -   | 32   | mA   |
| Permissible output current<br>(max value of total of all pins) | Maximum of all output pins                                    |                | ΣI <sub>OH</sub> (max) | -   | -   | -80  | mA   |
|                                                                |                                                               |                | ΣI <sub>OL</sub> (max) | -   | -   | 80   | mA   |

**Caution:** To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100  $\mu$ s.

- Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
- Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
- Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
- Note 4. Except for P000 to P007, P200, which are input ports.

## 2.2.4 I/O $V_{OH}$ , $V_{OL}$ , and Other Characteristics

**Table 2.6 I/O  $V_{OH}$ ,  $V_{OL}$ , and other characteristics (1 of 2)**

| Parameter             |                                                                    |                            | Symbol          | Min       | Typ | Max  | Unit | Test conditions                                  |
|-----------------------|--------------------------------------------------------------------|----------------------------|-----------------|-----------|-----|------|------|--------------------------------------------------|
| Output voltage        | IIC                                                                |                            | V <sub>OL</sub> | -         | -   | 0.4  | V    | I <sub>OL</sub> = 3.0 mA                         |
|                       |                                                                    |                            | V <sub>OL</sub> | -         | -   | 0.6  |      | I <sub>OL</sub> = 6.0 mA                         |
|                       | IIC*1                                                              |                            | V <sub>OL</sub> | -         | -   | 0.4  |      | I <sub>OL</sub> = 15.0 mA<br>(ICFER.FMPE = 1)    |
|                       |                                                                    |                            | V <sub>OL</sub> | -         | 0.4 | -    |      | I <sub>OL</sub> = 20.0 mA<br>(ICFER.FMPE = 1)    |
|                       | Ports P205, P206, P407 to P415,<br>P602, P708 (total of 13 pins)*2 |                            | V <sub>OH</sub> | VCC - 1.0 | -   | -    |      | I <sub>OH</sub> = -20 mA<br>VCC = 3.3 V          |
|                       |                                                                    |                            | V <sub>OL</sub> | -         | -   | 1.0  |      | I <sub>OL</sub> = 20 mA<br>VCC = 3.3 V           |
|                       | Other output pins                                                  |                            | V <sub>OH</sub> | VCC - 0.5 | -   | -    |      | I <sub>OH</sub> = -1.0 mA                        |
|                       |                                                                    |                            | V <sub>OL</sub> | -         | -   | 0.5  |      | I <sub>OL</sub> = 1.0 mA                         |
| Input leakage current | RES                                                                |                            | I <sub>in</sub> | -         | -   | 5.0  | μA   | V <sub>in</sub> = 0 V<br>V <sub>in</sub> = 5.5 V |
|                       | Ports P000 to P002, P004 to P006,<br>P200                          |                            |                 | -         | -   | 1.0  |      | V <sub>in</sub> = 0 V<br>V <sub>in</sub> = VCC   |
|                       | Ports P003, P007                                                   | Before<br>initialization*3 |                 | -         | -   | 45.0 |      | V <sub>in</sub> = 0 V<br>V <sub>in</sub> = VCC   |
|                       |                                                                    | After<br>initialization*4  |                 | -         | -   | 1.0  |      | V <sub>in</sub> = 0 V<br>V <sub>in</sub> = VCC   |

**Table 2.6 I/O  $V_{OH}$ ,  $V_{OL}$ , and other characteristics (2 of 2)**

| Parameter                               |                                                   | Symbol    | Min  | Typ | Max | Unit    | Test conditions                                                            |
|-----------------------------------------|---------------------------------------------------|-----------|------|-----|-----|---------|----------------------------------------------------------------------------|
| Three-state leakage current (off state) | 5 V-tolerant ports                                | $I_{TSI}$ | -    | -   | 5.0 | $\mu A$ | $V_{in} = 0 V$<br>$V_{in} = 5.5 V$                                         |
|                                         | Other ports (except for ports P000 to P007, P200) |           | -    | -   | 1.0 |         | $V_{in} = 0 V$<br>$V_{in} = V_{CC}$                                        |
| Input pull-up MOS current               | Ports P0 to P7 (except for ports P000 to P007)    | $I_p$     | -300 | -   | -10 | $\mu A$ | $V_{CC} = 2.7$ to $3.6 V$<br>$V_{in} = 0 V$                                |
| Input capacitance                       | Ports P003, P007, P014, P015, P400, P401          | $C_{in}$  | -    | -   | 16  | pF      | $V_{bias} = 0 V$<br>$V_{amp} = 20 mV$<br>$f = 1 MHz$<br>$T_a = 25^\circ C$ |
|                                         | Other input pins                                  |           | -    | -   | 8   |         |                                                                            |

Note 1. SCL0\_A, SDA0\_A (total 2 pins).

Note 2. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 3. P0nPFS.ASEL(n = 3 or 7) = 1

Note 4. P0nPFS.ASEL(n = 3 or 7) = 0

## 2.2.5 Operating and Standby Current

**Table 2.7 Operating and standby current (1 of 2)**

| Parameter                   |                                             |                                    |                                                                           | Symbol             | Min | Typ        | Max        | Unit | Test conditions                                                                                           |                   |
|-----------------------------|---------------------------------------------|------------------------------------|---------------------------------------------------------------------------|--------------------|-----|------------|------------|------|-----------------------------------------------------------------------------------------------------------|-------------------|
| Supply current*1            | High-speed mode                             | Maximum*2                          |                                                                           | I <sub>CC</sub> *3 | -   | -          | 87         | mA   | ICLK = 120 MHz<br>PCLKA = 120 MHz<br>PCLKB = 60 MHz<br>PCLKC = 60 MHz<br>PCLKD = 120 MHz<br>FCLK = 60 MHz |                   |
|                             |                                             | CoreMark®*5                        |                                                                           |                    | -   | 17         | -          |      |                                                                                                           |                   |
|                             |                                             | Normal mode                        | All peripheral clocks enabled, while (1) code executing from flash*4      |                    | -   | 24         | -          |      |                                                                                                           |                   |
|                             |                                             |                                    | All peripheral clocks disabled, while (1) code executing from flash*5, *6 |                    | -   | 12         | -          |      |                                                                                                           |                   |
|                             |                                             | Sleep mode*5, *6                   |                                                                           |                    | -   | 9          | 33.5       |      |                                                                                                           |                   |
|                             |                                             | Increase during BGO operation      | Data flash P/E                                                            |                    | -   | 6          | -          |      |                                                                                                           |                   |
|                             |                                             |                                    | Code flash P/E                                                            |                    | -   | 8          | -          |      |                                                                                                           |                   |
|                             |                                             | Low-speed mode*5                   |                                                                           |                    | -   | 1.2        | -          |      |                                                                                                           | ICLK = 1 MHz      |
|                             |                                             | Subosc-speed mode*5                |                                                                           |                    | -   | 1.0        | -          |      |                                                                                                           | ICLK = 32.768 kHz |
|                             |                                             | Software Standby mode              |                                                                           |                    | -   | 1.3        | 13         |      |                                                                                                           | Ta ≤ 85°C         |
|                             |                                             |                                    | -                                                                         | 1.3                | 21  | Ta ≤ 105°C |            |      |                                                                                                           |                   |
|                             | Deep Software Standby mode                  | DPSBYCR.DEEPCUT[1:0] = 00b*8       | -                                                                         | 28                 | 65  | μA         | Ta ≤ 85°C  |      |                                                                                                           |                   |
|                             |                                             |                                    | -                                                                         | 28                 | 93  |            | Ta ≤ 105°C |      |                                                                                                           |                   |
|                             |                                             | DPSBYCR.DEEPCUT[1:0] = 01b*8       | -                                                                         | 11.6               | 28  |            | Ta ≤ 85°C  |      |                                                                                                           |                   |
|                             |                                             |                                    | -                                                                         | 11.6               | 32  |            | Ta ≤ 105°C |      |                                                                                                           |                   |
|                             |                                             | DPSBYCR.DEEPCUT[1:0] = 11b*8       | -                                                                         | 4.9                | 21  |            | Ta ≤ 85°C  |      |                                                                                                           |                   |
|                             |                                             |                                    | -                                                                         | 4.9                | 26  |            | Ta ≤ 105°C |      |                                                                                                           |                   |
|                             |                                             | Increase when the AGT is operating | When the low-speed on-chip oscillator (LOCO) is in use                    | -                  | 4.4 |            | -          | -    |                                                                                                           |                   |
|                             |                                             |                                    | When a crystal oscillator for low clock loads is in use                   | -                  | 1.0 |            | -          | -    |                                                                                                           |                   |
|                             |                                             |                                    | When a crystal oscillator for standard clock loads is in use              | -                  | 1.4 |            | -          | -    |                                                                                                           |                   |
| Analog power supply current | During 12-bit A/D conversion                |                                    | Al <sub>CC</sub>                                                          | -                  | 0.8 | 1.1        | mA         | -    |                                                                                                           |                   |
|                             | During 12-bit A/D conversion with S/H amp   |                                    |                                                                           | -                  | 2.3 | 3.3        |            | -    |                                                                                                           |                   |
|                             | PGA (1ch)                                   |                                    |                                                                           | -                  | 1   | 3          |            | -    |                                                                                                           |                   |
|                             | ACMPHS (1 unit)                             |                                    |                                                                           | -                  | 100 | 150        |            | μA   | -                                                                                                         |                   |
|                             | Temperature sensor                          |                                    |                                                                           | -                  | 0.1 | 0.2        |            | mA   | -                                                                                                         |                   |
|                             | During D/A conversion (per unit)            | Without AMP output                 |                                                                           | -                  | 0.1 | 0.2        |            | mA   | -                                                                                                         |                   |
|                             |                                             | With AMP output                    |                                                                           | -                  | 0.6 | 1.1        |            | mA   | -                                                                                                         |                   |
|                             | Waiting for A/D, D/A conversion (all units) |                                    |                                                                           | -                  | 0.9 | 1.6        |            | mA   | -                                                                                                         |                   |
|                             | ADC12, DAC12 in standby modes (all units)*7 |                                    |                                                                           | -                  | 2   | 8          |            | μA   | -                                                                                                         |                   |

**Table 2.7 Operating and standby current (2 of 2)**

| Parameter                               |                                                             |                    | Symbol              | Min | Typ  | Max | Unit | Test conditions |
|-----------------------------------------|-------------------------------------------------------------|--------------------|---------------------|-----|------|-----|------|-----------------|
| Reference power supply current (VREFH0) | During 12-bit A/D conversion (unit 0)                       |                    | AI <sub>REFH0</sub> | -   | 70   | 120 | μA   | -               |
|                                         | Waiting for 12-bit A/D conversion (unit 0)                  |                    |                     | -   | 0.07 | 0.5 | μA   | -               |
|                                         | ADC12 in standby modes (unit 0)                             |                    |                     | -   | 0.07 | 0.5 | μA   | -               |
| Reference power supply current (VREFH)  | During 12-bit A/D conversion (unit 1)                       |                    | AI <sub>REFH</sub>  | -   | 70   | 120 | μA   | -               |
|                                         | During D/A conversion (per unit)                            | Without AMP output |                     | -   | 0.1  | 0.4 | mA   | -               |
|                                         |                                                             | With AMP ouput     |                     | -   | 0.1  | 0.4 | mA   | -               |
|                                         | Waiting for 12-bit A/D (unit 1), D/A (all units) conversion |                    |                     | -   | 0.07 | 0.8 | μA   | -               |
|                                         | ADC12 unit 1 in standby modes                               |                    |                     | -   | 0.07 | 0.8 | μA   | -               |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOS transistors in the off state.

Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 3. I<sub>CC</sub> depends on f (ICLK) as follows. (ICLK:PCLKA:PCLKB:PCLKC:PCLKD = 2:2:1:1:2)

I<sub>CC</sub> Max. = 0.53 × f + 23 (maximum operation in High-speed mode)

I<sub>CC</sub> Typ. = 0.08 × f + 2.4 (normal operation in High-speed mode)

I<sub>CC</sub> Typ. = 0.1 × f + 1.1 (Low-speed mode)

I<sub>CC</sub> Max. = 0.09 × f + 23 (Sleep mode).

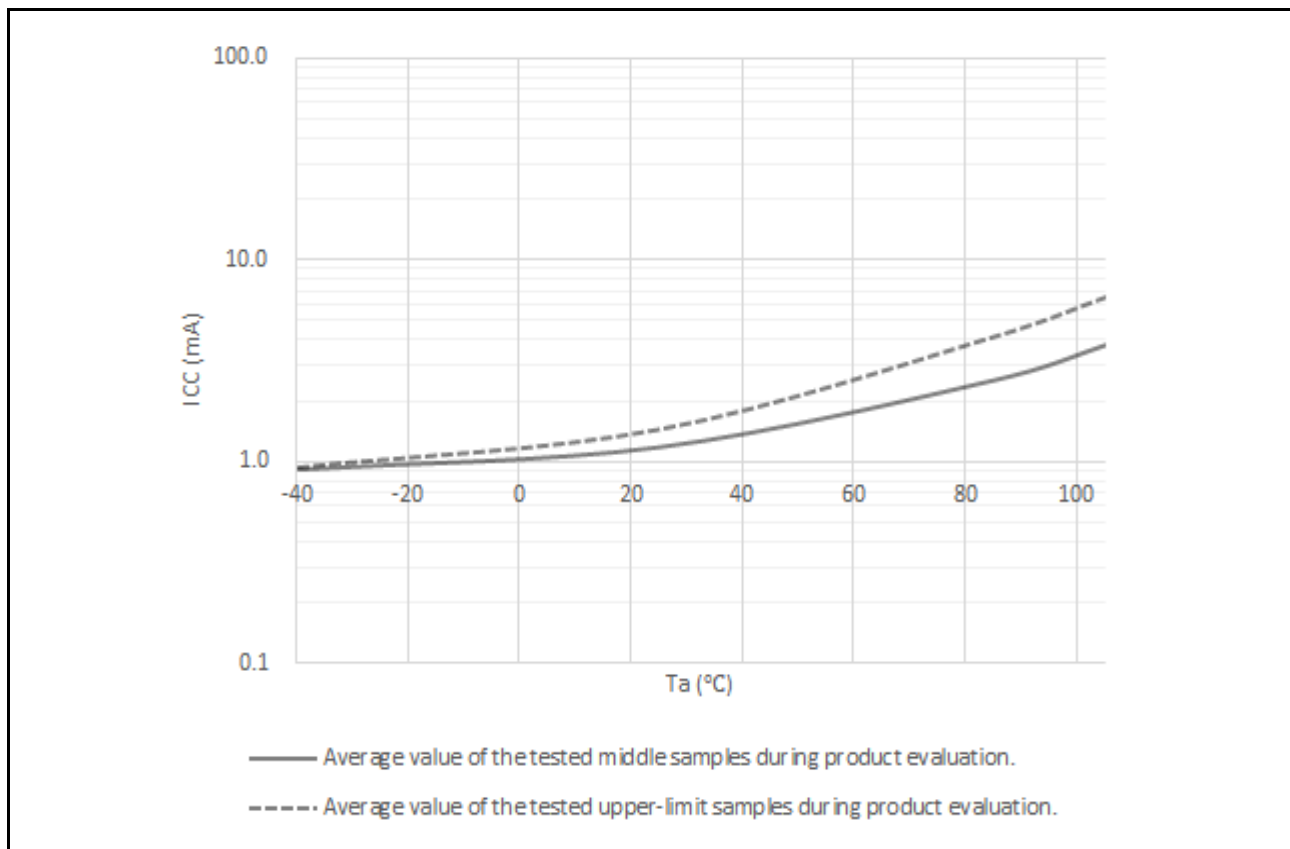
Note 4. This does not include the BGO operation.

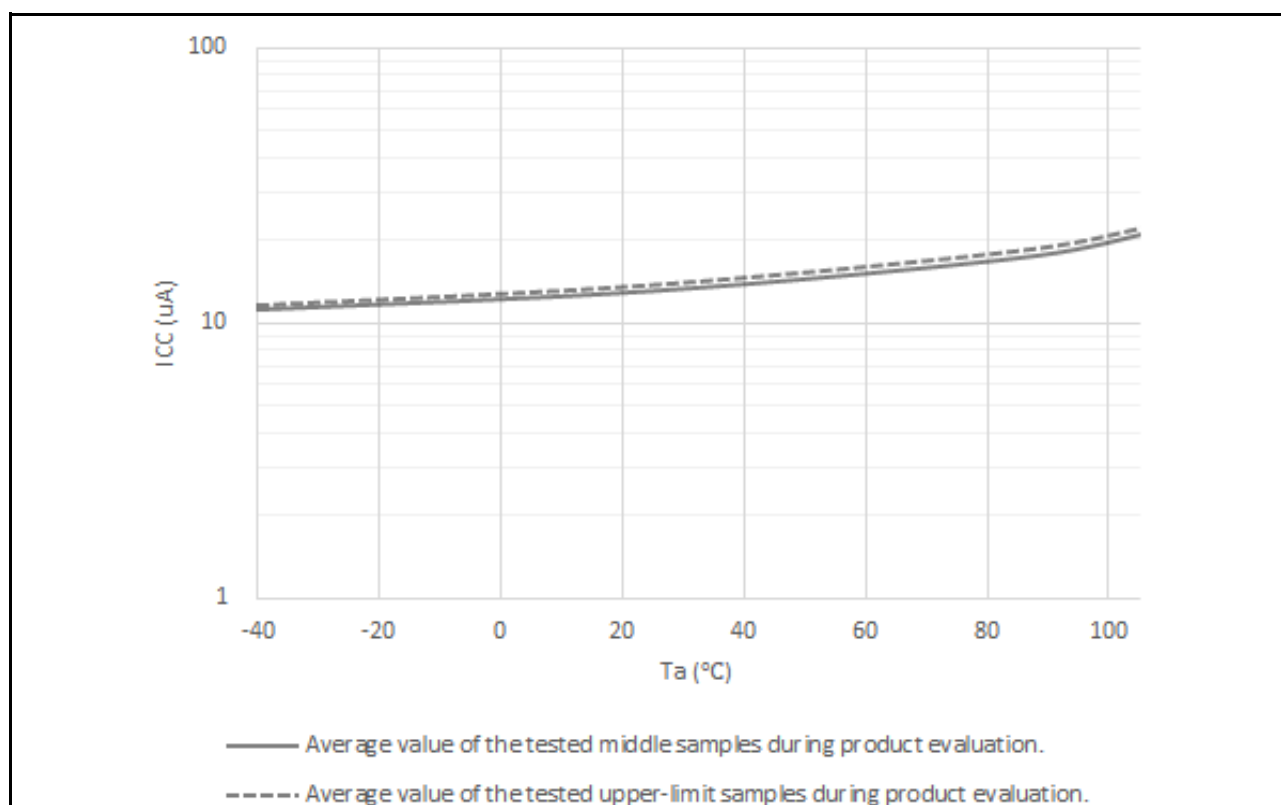
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Note 6. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.75 MHz).

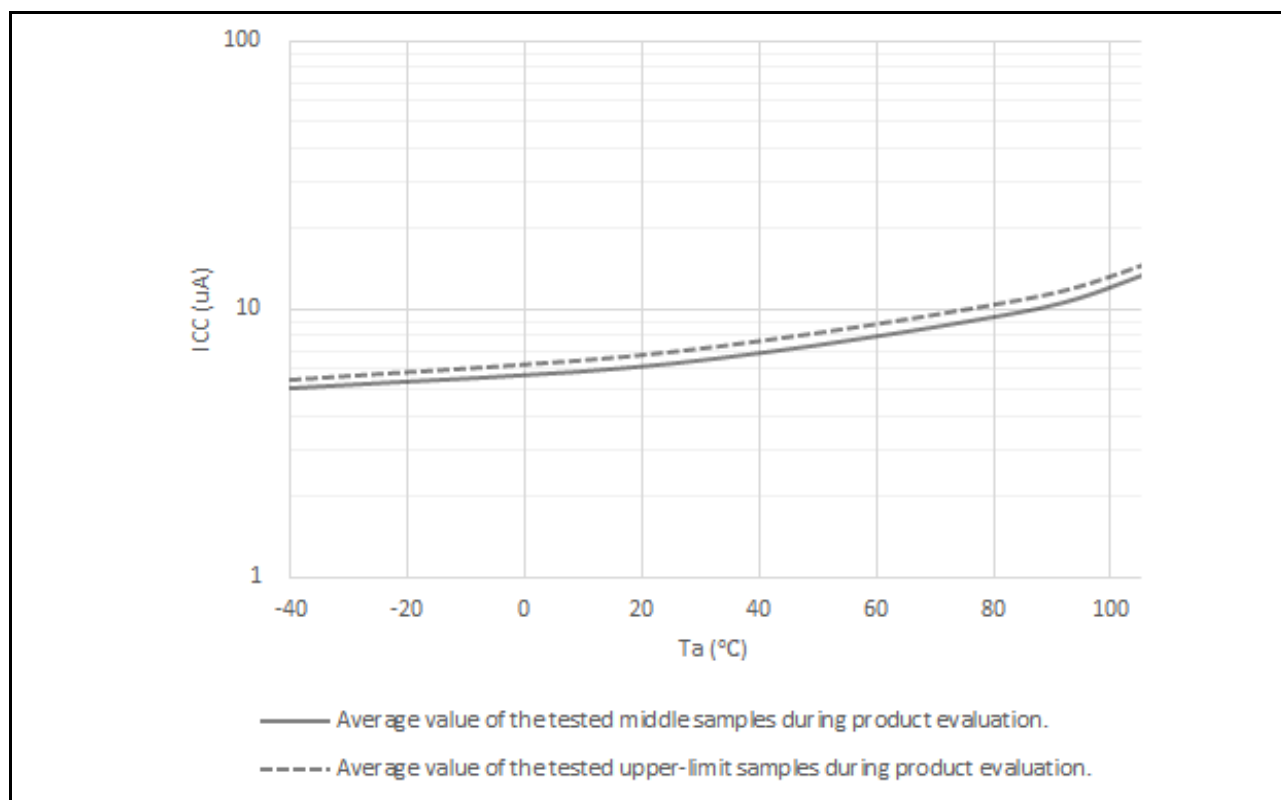
Note 7. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-bit A/D Converter 0 Module Stop bit) and MSTPCRD.MSTPD15 (12-bit A/D Converter 1 Module Stop bit) are in the module-stop state. See section 35.6.8, Available functions and register settings of AN000 to AN002, AN007, AN100 to AN102, and AN107 in User's Manual.

Note 8. For more information on the DBSBYCR register, see section 11.2.11, Deep Software Standby Control Register (DPSBYCR) in User's Manual.

**Figure 2.2 Temperature dependency in Software Standby mode (reference data)**



**Figure 2.3** Temperature dependency in Deep Software Standby mode, power-on reset circuit low power function disabled (reference data)



**Figure 2.4** Temperature dependency in Deep Software Standby mode, power-on reset circuit low power function enabled (reference data)

## 2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

**Table 2.8 Rising gradient characteristics**

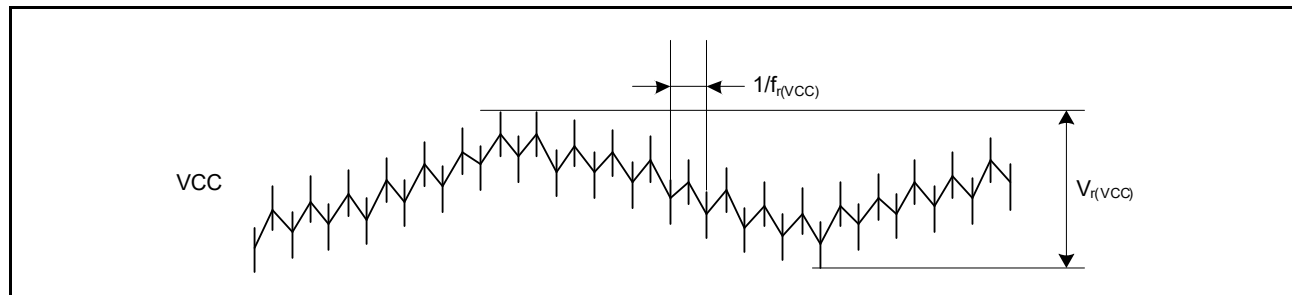
| Parameter           |                                             | Symbol | Min    | Typ | Max | Unit | Test conditions |
|---------------------|---------------------------------------------|--------|--------|-----|-----|------|-----------------|
| VCC rising gradient | Voltage monitor 0 reset disabled at startup | SrVCC  | 0.0084 | -   | 20  | ms/V | -               |
|                     | Voltage monitor 0 reset enabled at startup  |        | 0.0084 | -   | -   |      | -               |
|                     | SCI boot mode*1                             |        | 0.0084 | -   | 20  |      | -               |

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

**Table 2.9 Rise and fall gradient and ripple frequency characteristics**

The ripple voltage must meet the allowable ripple frequency  $f_r(VCC)$  within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds  $VCC \pm 10\%$ , the allowable voltage change rising and falling gradient  $dt/dVCC$  must be met.

| Parameter                                            | Symbol     | Min | Typ | Max | Unit | Test conditions                               |
|------------------------------------------------------|------------|-----|-----|-----|------|-----------------------------------------------|
| Allowable ripple frequency                           | $f_r(VCC)$ | -   | -   | 10  | kHz  | Figure 2.5<br>$V_r(VCC) \leq VCC \times 0.2$  |
|                                                      |            | -   | -   | 1   | MHz  | Figure 2.5<br>$V_r(VCC) \leq VCC \times 0.08$ |
|                                                      |            | -   | -   | 10  | MHz  | Figure 2.5<br>$V_r(VCC) \leq VCC \times 0.06$ |
| Allowable voltage change rising and falling gradient | $dt/dVCC$  | 1.0 | -   | -   | ms/V | When VCC change exceeds $VCC \pm 10\%$        |



**Figure 2.5 Ripple waveform**

## 2.3 AC Characteristics

### 2.3.1 Frequency

**Table 2.10 Operation frequency value in high-speed mode**

| Parameter           |                                   | Symbol | Min | Typ | Max | Unit |
|---------------------|-----------------------------------|--------|-----|-----|-----|------|
| Operation frequency | System clock (ICLK)*2             | f      | -   | -   | 120 | MHz  |
|                     | Peripheral module clock (PCLKA)*2 |        | -   | -   | 120 |      |
|                     | Peripheral module clock (PCLKB)*2 |        | -   | -   | 60  |      |
|                     | Peripheral module clock (PCLKC)*2 |        | -*3 | -   | 60  |      |
|                     | Peripheral module clock (PCLKD)*2 |        | -   | -   | 120 |      |
|                     | Flash interface clock (FCLK)*2    |        | -*1 | -   | 60  |      |

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.

Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK frequencies.

Note 3. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

**Table 2.11 Operation frequency value in low-speed mode**

| Parameter           |                                       | Symbol | Min | Typ | Max | Unit |
|---------------------|---------------------------------------|--------|-----|-----|-----|------|
| Operation frequency | System clock (ICLK)*2                 | f      | -   | -   | 1   | MHz  |
|                     | Peripheral module clock (PCLKA)*2     |        | -   | -   | 1   |      |
|                     | Peripheral module clock (PCLKB)*2     |        | -   | -   | 1   |      |
|                     | Peripheral module clock (PCLKC)*2, *3 |        | ~*3 | -   | 1   |      |
|                     | Peripheral module clock (PCLKD)*2     |        | -   | -   | 1   |      |
|                     | Flash interface clock (FCLK)*1, *2    |        | -   | -   | 1   |      |

Note 1. Programming or erasing the flash memory is disabled in Low-speed mode.

Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK frequencies.

Note 3. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

**Table 2.12 Operation frequency value in Subosc-speed mode**

| Parameter           |                                       | Symbol | Min  | Typ | Max  | Unit |
|---------------------|---------------------------------------|--------|------|-----|------|------|
| Operation frequency | System clock (ICLK)*2                 | f      | 29.4 | -   | 36.1 | kHz  |
|                     | Peripheral module clock (PCLKA)*2     |        | -    | -   | 36.1 |      |
|                     | Peripheral module clock (PCLKB)*2     |        | -    | -   | 36.1 |      |
|                     | Peripheral module clock (PCLKC)*2, *3 |        | -    | -   | 36.1 |      |
|                     | Peripheral module clock (PCLKD)*2     |        | -    | -   | 36.1 |      |
|                     | Flash interface clock (FCLK)*1, *2    |        | 29.4 | -   | 36.1 |      |

Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.

Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, and FCLK frequencies.

Note 3. The ADC12 cannot be used.

## 2.3.2 Clock Timing

**Table 2.13 Clock timing except for sub-clock oscillator (1 of 2)**

| Parameter                                                   | Symbol          | Min     | Typ    | Max     | Unit | Test conditions |
|-------------------------------------------------------------|-----------------|---------|--------|---------|------|-----------------|
| EXTAL external clock input cycle time                       | $t_{EXCyc}$     | 41.66   | -      | -       | ns   | Figure 2.6      |
| EXTAL external clock input high pulse width                 | $t_{EXH}$       | 15.83   | -      | -       | ns   |                 |
| EXTAL external clock input low pulse width                  | $t_{EXL}$       | 15.83   | -      | -       | ns   |                 |
| EXTAL external clock rise time                              | $t_{EXr}$       | -       | -      | 5.0     | ns   |                 |
| EXTAL external clock fall time                              | $t_{EXf}$       | -       | -      | 5.0     | ns   |                 |
| Main clock oscillator frequency                             | $f_{MAIN}$      | 8       | -      | 24      | MHz  | -               |
| Main clock oscillation stabilization wait time (crystal) *1 | $t_{MAINOSCWT}$ | -       | -      | ~*1     | ms   | Figure 2.7      |
| LOCO clock oscillation frequency                            | $f_{LOCO}$      | 29.4912 | 32.768 | 36.0448 | kHz  | -               |
| LOCO clock oscillation stabilization wait time              | $t_{LOCOWT}$    | -       | -      | 60.4    | μs   | Figure 2.8      |
| ILOCO clock oscillation frequency                           | $f_{ILOCO}$     | 13.5    | 15     | 16.5    | kHz  | -               |
| MOCO clock oscillation frequency                            | $F_{MOCO}$      | 6.8     | 8      | 9.2     | MHz  | -               |
| MOCO clock oscillation stabilization wait time              | $t_{MOCOWT}$    | -       | -      | 15.0    | μs   | -               |

**Table 2.13 Clock timing except for sub-clock oscillator (2 of 2)**

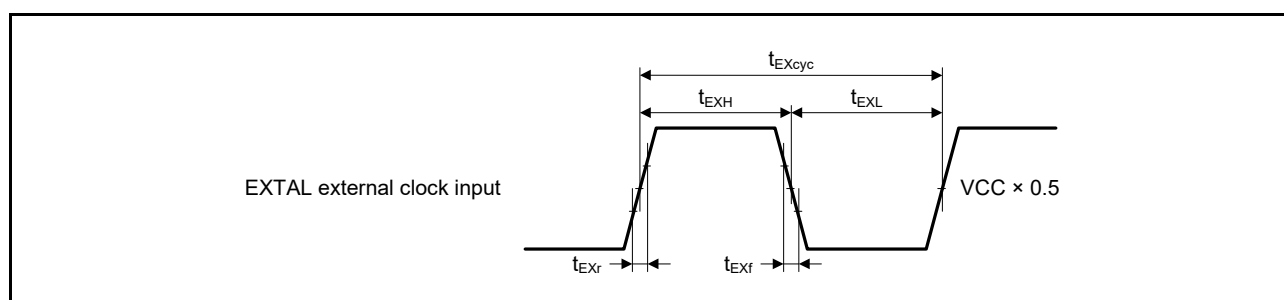
| Parameter                                        |             | Symbol       | Min    | Typ | Max    | Unit          | Test conditions                                                                        |
|--------------------------------------------------|-------------|--------------|--------|-----|--------|---------------|----------------------------------------------------------------------------------------|
| HOCO clock oscillator oscillation frequency      | Without FLL | $f_{HOCO16}$ | 15.78  | 16  | 16.22  | MHz           | $-20 \leq T_a \leq 105^\circ\text{C}$                                                  |
|                                                  |             | $f_{HOCO18}$ | 17.75  | 18  | 18.25  |               |                                                                                        |
|                                                  |             | $f_{HOCO20}$ | 19.72  | 20  | 20.28  |               |                                                                                        |
|                                                  |             | $f_{HOCO16}$ | 15.71  | 16  | 16.29  |               | $-40 \leq T_a \leq -20^\circ\text{C}$                                                  |
|                                                  |             | $f_{HOCO18}$ | 17.68  | 18  | 18.32  |               |                                                                                        |
|                                                  |             | $f_{HOCO20}$ | 19.64  | 20  | 20.36  |               |                                                                                        |
|                                                  | With FLL    | $f_{HOCO16}$ | 15.960 | 16  | 16.040 |               | $-40 \leq T_a \leq 105^\circ\text{C}$<br>Sub-clock frequency accuracy is $\pm 50$ ppm. |
|                                                  |             | $f_{HOCO18}$ | 17.955 | 18  | 18.045 |               |                                                                                        |
|                                                  |             | $f_{HOCO20}$ | 19.950 | 20  | 20.050 |               |                                                                                        |
| HOCO clock oscillation stabilization wait time*2 |             | $t_{HOCOWT}$ | -      | -   | 64.7   | $\mu\text{s}$ | -                                                                                      |
| FLL stabilization wait time                      |             | $t_{FLLWT}$  | -      | -   | 1.8    | ms            | -                                                                                      |
| PLL clock frequency                              |             | $f_{PLL}$    | 120    | -   | 240    | MHz           | -                                                                                      |
| PLL clock oscillation stabilization wait time    |             | $t_{PLLWT}$  | -      | -   | 174.9  | $\mu\text{s}$ | Figure 2.9                                                                             |

- Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.  
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.
- Note 2. This is the time from release from reset state until the HOCO oscillation frequency ( $f_{HOCO}$ ) reaches the range for guaranteed operation.

**Table 2.14 Clock timing for the sub-clock oscillator**

| Parameter                                     | Symbol         | Min | Typ    | Max | Unit | Test conditions |
|-----------------------------------------------|----------------|-----|--------|-----|------|-----------------|
| Sub-clock frequency                           | $f_{SUB}$      | -   | 32.768 | -   | kHz  | -               |
| Sub-clock oscillation stabilization wait time | $t_{SUBOSCWT}$ | -   | -      | *1  | s    | Figure 2.10     |

- Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.  
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

**Figure 2.6 EXTAL external clock input timing**

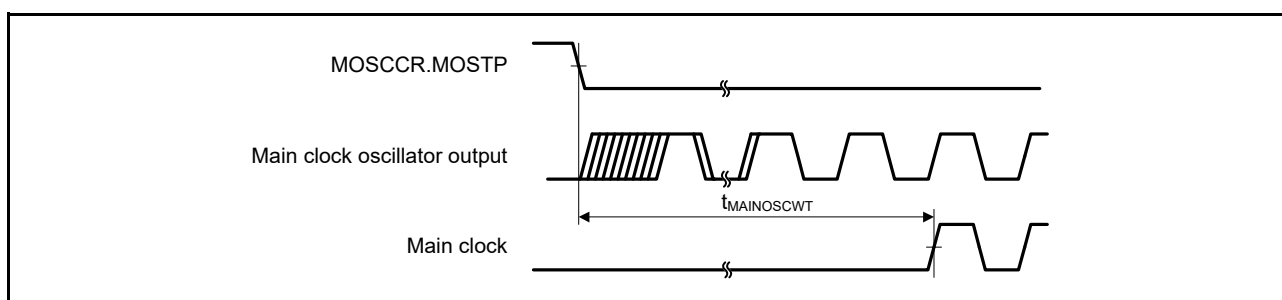


Figure 2.7 Main clock oscillation start timing

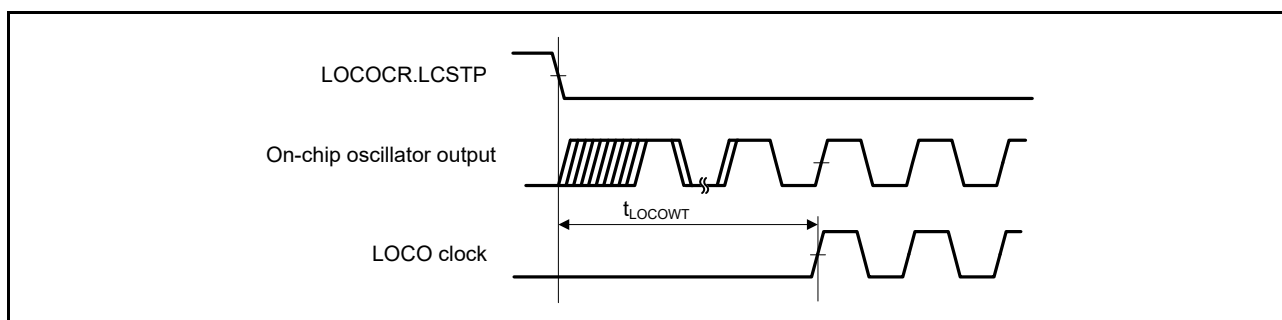


Figure 2.8 LOCO clock oscillation start timing

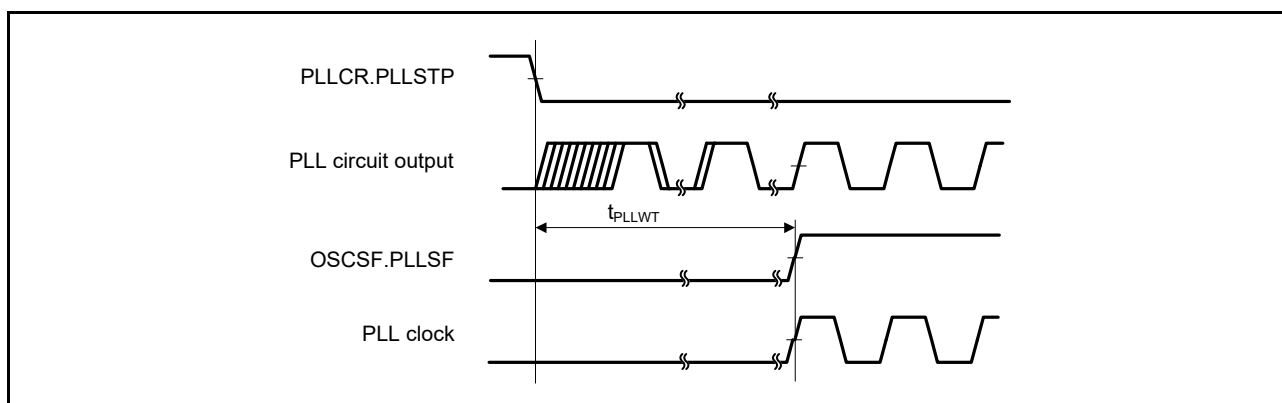


Figure 2.9 PLL clock oscillation start timing

Note: Only operate the PLL after the main clock oscillation has stabilized.

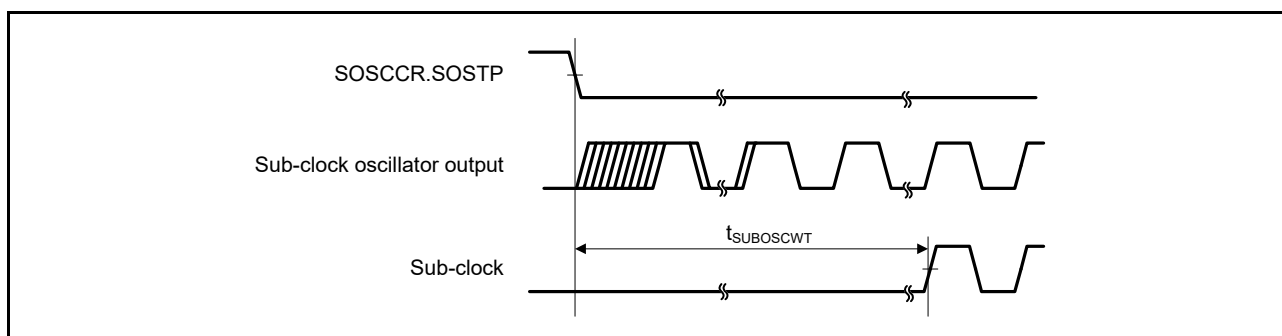
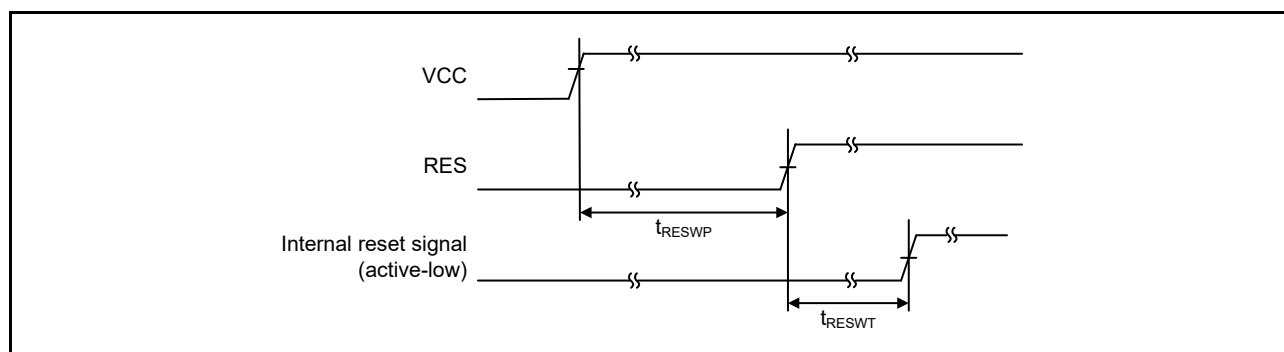
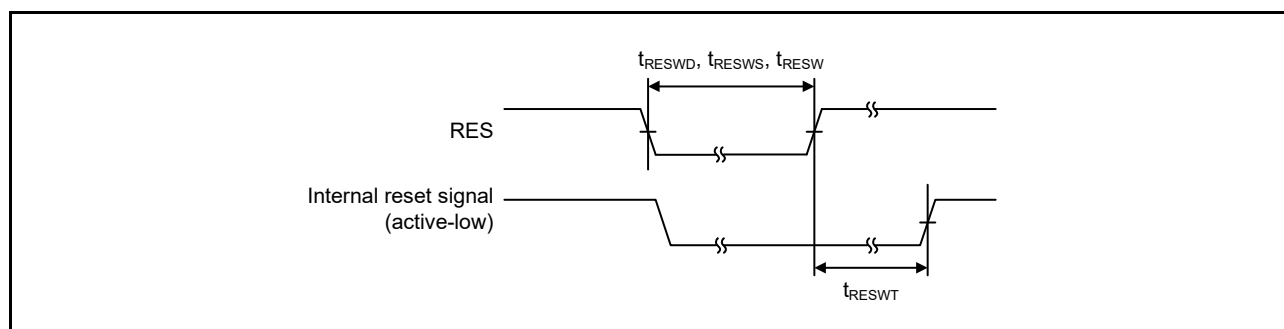


Figure 2.10 Sub-clock oscillation start timing

## 2.3.3 Reset Timing

**Table 2.15** Reset timing

| Parameter                                                                                                                                                                                      |                                          | Symbol      | Min | Typ | Max | Unit    | Test conditions |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|-------------|-----|-----|-----|---------|-----------------|
| RES pulse width                                                                                                                                                                                | Power-on                                 | $t_{RESWP}$ | 1   | -   | -   | ms      | Figure 2.11     |
|                                                                                                                                                                                                | Deep Software Standby mode               | $t_{RESWD}$ | 0.6 | -   | -   | ms      | Figure 2.12     |
|                                                                                                                                                                                                | Software Standby mode, Subosc-speed mode | $t_{RESWS}$ | 0.3 | -   | -   | ms      |                 |
|                                                                                                                                                                                                | All other                                | $t_{RESW}$  | 200 | -   | -   | $\mu$ s |                 |
| Wait time after RES cancellation                                                                                                                                                               |                                          | $t_{RESWT}$ | -   | 29  | 32  | $\mu$ s | Figure 2.11     |
| Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset) |                                          | $t_{RESW2}$ | -   | 320 | 390 | $\mu$ s | -               |

**Figure 2.11** Power-on reset timing**Figure 2.12** Reset input timing

## 2.3.4 Wakeup Timing

Table 2.16 Timing of recovery from low power modes

| Parameter                                                  |                                                           |                                                         | Symbol              | Min | Typ        | Max        | Unit             | Test conditions                                            |
|------------------------------------------------------------|-----------------------------------------------------------|---------------------------------------------------------|---------------------|-----|------------|------------|------------------|------------------------------------------------------------|
| Recovery time from Software Standby mode*1                 | Crystal resonator connected to main clock oscillator      | System clock source is main clock oscillator*2          | t <sub>SBYMC</sub>  | -   | 2.4*9      | 2.8*9      | ms               | Figure 2.13<br>The division ratio of all oscillators is 1. |
|                                                            |                                                           | System clock source is PLL with main clock oscillator*3 | t <sub>SBYPC</sub>  | -   | 2.7*9      | 3.2*9      | ms               |                                                            |
|                                                            | External clock input to main clock oscillator             | System clock source is main clock oscillator*4          | t <sub>SBYEX</sub>  | -   | 230*9      | 280*9      | μs               |                                                            |
|                                                            |                                                           | System clock source is PLL with main clock oscillator*5 | t <sub>SBYPE</sub>  | -   | 570*9      | 700*9      | μs               |                                                            |
|                                                            | System clock source is sub-clock oscillator*8             |                                                         | t <sub>SBYSC</sub>  | -   | 1.2*9      | 1.3*9      | ms               |                                                            |
|                                                            | System clock source is LOCO*8                             |                                                         | t <sub>SBYLO</sub>  | -   | 1.2*9      | 1.4*9      | ms               |                                                            |
|                                                            | System clock source is HOCO*6                             |                                                         | t <sub>SBYHO</sub>  | -   | 240*9, *10 | 300*9, *10 | μs               |                                                            |
|                                                            | System clock source is MOCO*7                             |                                                         | t <sub>SBYMO</sub>  | -   | 220*9      | 300*9      | μs               |                                                            |
| Recovery time from Deep Software Standby mode              |                                                           |                                                         | t <sub>DSBY</sub>   | -   | 0.65       | 1.0        | ms               | Figure 2.14                                                |
| Wait time after cancellation of Deep Software Standby mode |                                                           |                                                         | t <sub>DSBYWT</sub> | 34  | -          | 35         | t <sub>cyc</sub> |                                                            |
| Recovery time from Software Standby mode to Snooze mode    | High-speed mode when system clock source is HOCO (20 MHz) |                                                         | t <sub>SNZ</sub>    | -   | 35*9, *10  | 70*9, *10  | μs               | Figure 2.15                                                |
|                                                            | High-speed mode when system clock source is MOCO (8 MHz)  |                                                         | t <sub>SNZ</sub>    | -   | 11*9       | 14*9       | μs               |                                                            |

- Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:  
Total recovery time = recovery time for an oscillator as the system clock source + the longest oscillation stabilization time of any oscillators requiring longer stabilization times than the system clock source + 2 LOCO cycles (when LOCO is operating) + 3 SOSC cycles (when Subosc is oscillating and MSTPC0 = 0 (CAC module stop)).
- Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:  
 $t_{SBYMC}(\text{MOSCWTCR} = Xh) = t_{SBYMC}(\text{MOSCWTCR} = 05h) + (t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = Xh) - t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = 05h))$
- Note 3. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:  
 $t_{SBYMC}(\text{MOSCWTCR} = Xh) = t_{SBYMC}(\text{MOSCWTCR} = 05h) + (t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = Xh) - t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = 05h))$
- Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 01h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:  
 $t_{SBYMC}(\text{MOSCWTCR} = Xh) = t_{SBYMC}(\text{MOSCWTCR} = 01h) + (t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = Xh) - t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = 01h))$
- Note 5. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 01h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:  
 $t_{SBYMC}(\text{MOSCWTCR} = Xh) = t_{SBYMC}(\text{MOSCWTCR} = 01h) + (t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = Xh) - t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = 01h))$
- Note 6. The HOCO frequency is 20 MHz.
- Note 7. The MOCO frequency is 8 MHz.
- Note 8. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.
- Note 9. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time:  
STCONR.STCON[1:0] = 00b:16 μs (typical), 34 μs (maximum)  
STCONR.STCON[1:0] = 11b:16 μs (typical), 104 μs (maximum).
- Note 10. When the SNZCR.RXDREQEN bit is set to 0, 16 μs (typical) or 18 μs (maximum) is added as the HOCO wait time.

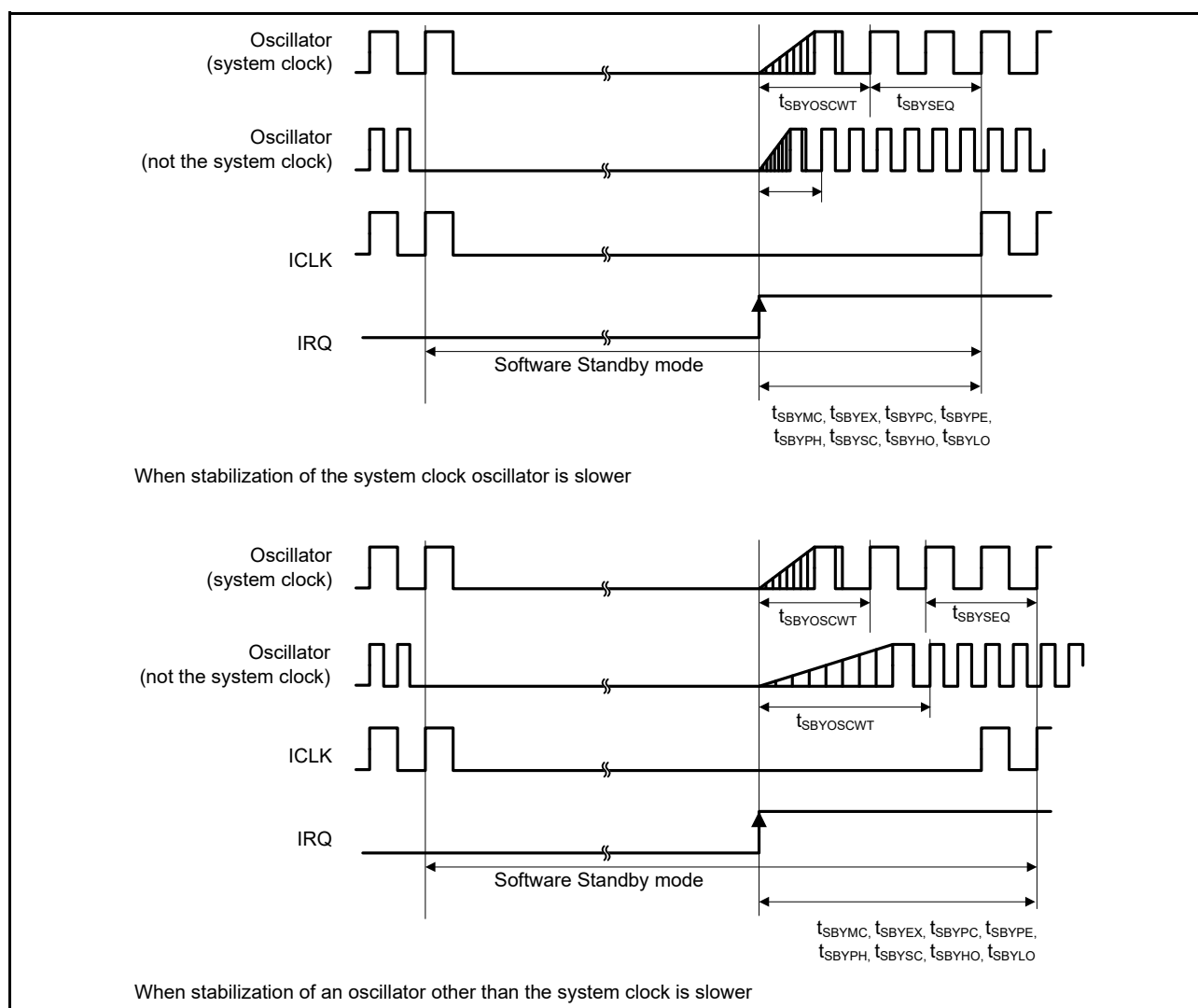


Figure 2.13 Software Standby mode cancellation timing

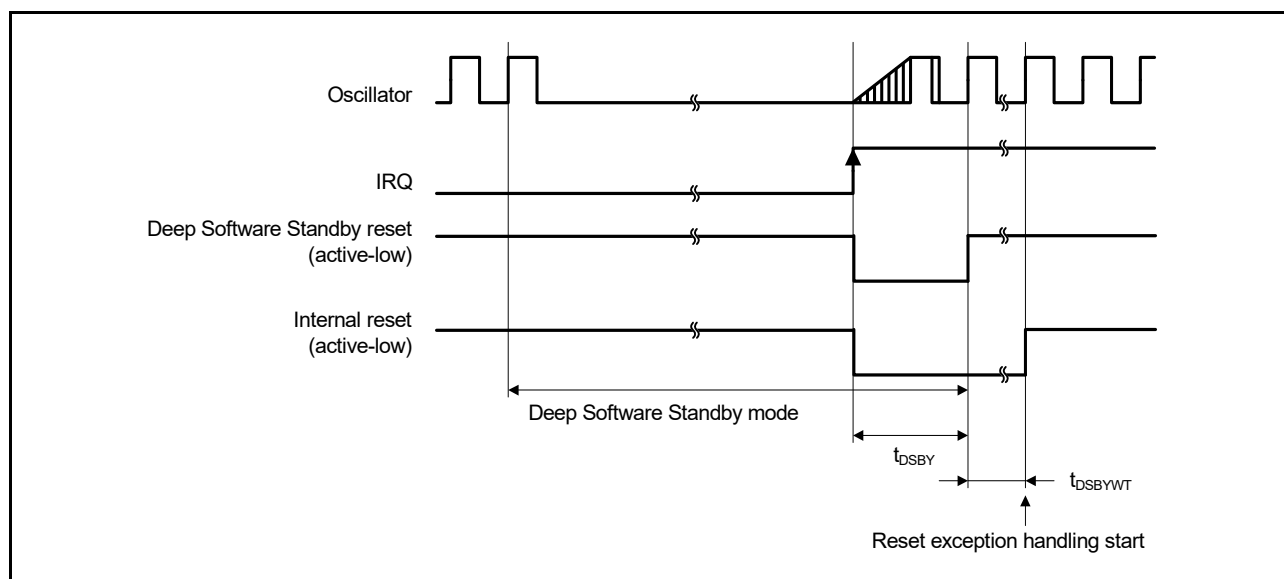


Figure 2.14 Deep Software Standby mode cancellation timing

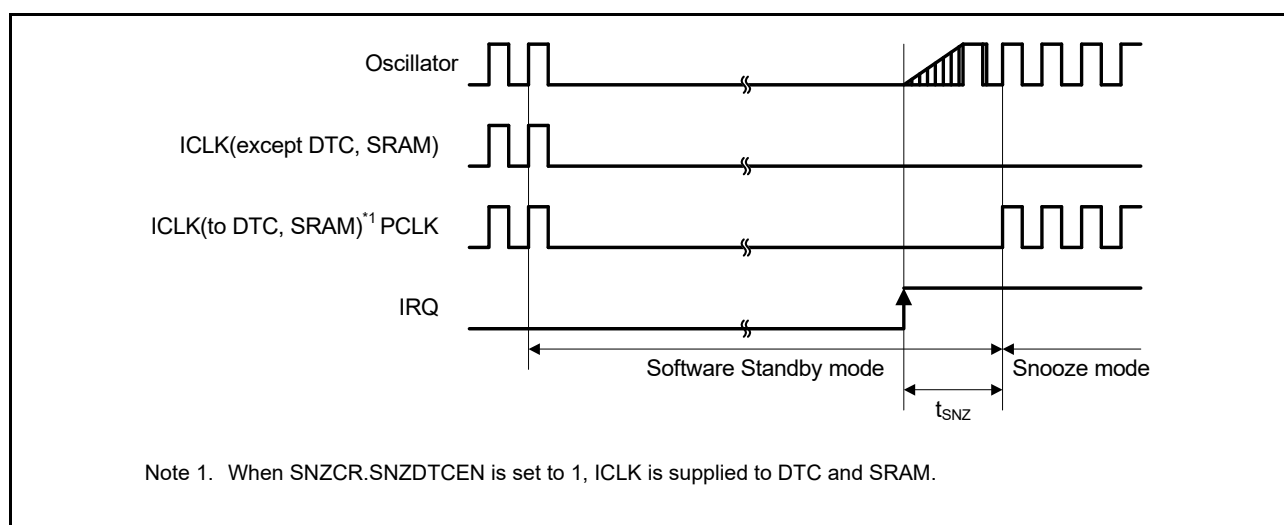


Figure 2.15 Recovery timing from Software Standby mode to Snooze mode

### 2.3.5 NMI and IRQ Noise Filter

Table 2.17 NMI and IRQ noise filter

| Parameter       | Symbol     | Min                         | Typ | Max | Unit | Test conditions             |                                  |
|-----------------|------------|-----------------------------|-----|-----|------|-----------------------------|----------------------------------|
| NMI pulse width | $t_{NMIW}$ | 200                         | -   | -   | ns   | NMI digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns  |
|                 |            | $t_{Pcyc} \times 2^{*1}$    | -   | -   |      |                             | $t_{Pcyc} \times 2 > 200$ ns     |
|                 |            | 200                         | -   | -   |      | NMI digital filter enabled  | $t_{NMICK} \times 3 \leq 200$ ns |
|                 |            | $t_{NMICK} \times 3.5^{*2}$ | -   | -   |      |                             | $t_{NMICK} \times 3 > 200$ ns    |
| IRQ pulse width | $t_{IRQW}$ | 200                         | -   | -   | ns   | IRQ digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns  |
|                 |            | $t_{Pcyc} \times 2^{*1}$    | -   | -   |      |                             | $t_{Pcyc} \times 2 > 200$ ns     |
|                 |            | 200                         | -   | -   |      | IRQ digital filter enabled  | $t_{IRQCK} \times 3 \leq 200$ ns |
|                 |            | $t_{IRQCK} \times 3.5^{*3}$ | -   | -   |      |                             | $t_{IRQCK} \times 3 > 200$ ns    |

Note: 200 ns minimum in Software Standby mode.

Note: If the clock source is switched, add 4 clock cycles of the switched source.

Note 1.  $t_{Pcyc}$  indicates the PCLKB cycle.

Note 2.  $t_{NMICK}$  indicates the cycle of the NMI digital filter sampling clock.

Note 3.  $t_{IRQCK}$  indicates the cycle of the IRQi digital filter sampling clock.

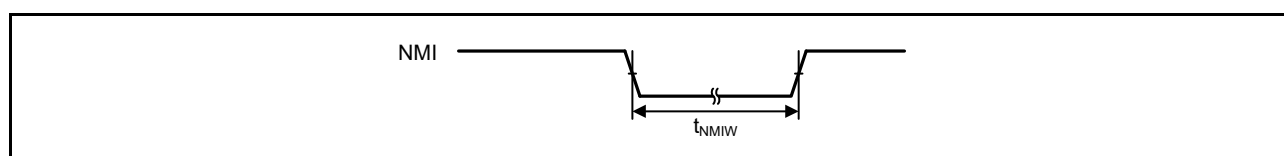


Figure 2.16 NMI interrupt input timing

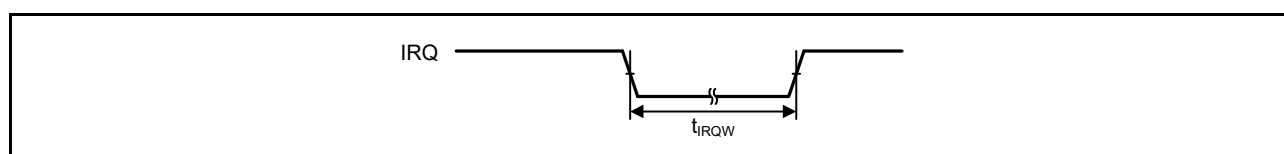


Figure 2.17 IRQ interrupt input timing

## 2.3.6 I/O Ports, POEG, GPT32, AGT, KINT, and ADC12 Trigger Timing

**Table 2.18 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing**

GPT32 conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

AGT conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

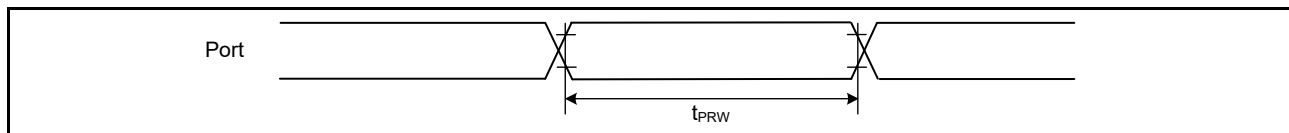
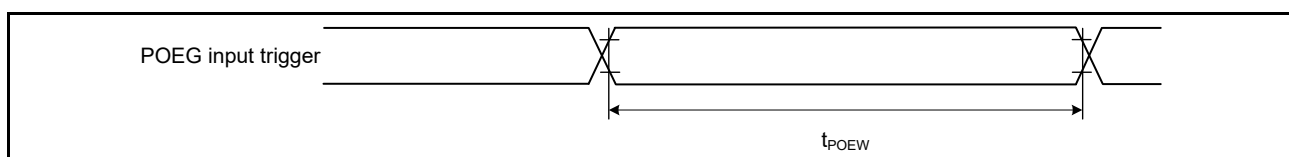
| Parameter                                   |                                                                      |                     | Symbol                      | Min  | Max | Unit        | Test conditions |
|---------------------------------------------|----------------------------------------------------------------------|---------------------|-----------------------------|------|-----|-------------|-----------------|
| I/O ports                                   | Input data pulse width                                               |                     | $t_{PRW}$                   | 1.5  | -   | $t_{Pcyc}$  | Figure 2.18     |
| POEG                                        | POEG input trigger pulse width                                       |                     | $t_{POEW}$                  | 3    | -   | $t_{Pcyc}$  | Figure 2.19     |
| GPT32                                       | Input capture pulse width                                            | Single edge         | $t_{GTICW}$                 | 1.5  | -   | $t_{PDcyc}$ | Figure 2.20     |
|                                             |                                                                      | Dual edge           |                             | 2.5  | -   |             |                 |
|                                             | GTIOCxY output skew<br>(x = 0 to 7, Y = A or B)                      | Middle drive buffer | $t_{GTISK}^{*1}$            | -    | 4   | ns          | Figure 2.21     |
|                                             |                                                                      | High drive buffer   |                             | -    | 4   |             |                 |
|                                             | GTIOCxY output skew<br>(x = 8 to 12, Y = A or B)                     | Middle drive buffer |                             | -    | 4   |             |                 |
|                                             |                                                                      | High drive buffer   |                             | -    | 4   |             |                 |
|                                             | GTIOCxY output skew<br>(x = 0 to 12, Y = A or B)                     | Middle drive buffer |                             | -    | 6   |             |                 |
|                                             |                                                                      | High drive buffer   |                             | -    | 6   |             |                 |
|                                             | OPS output skew<br>GTOUUP, GTOULO, GTOVUP,<br>GTOVLO, GTOWUP, GTOWLO |                     | $t_{GTOSK}$                 | -    | 5   | ns          | Figure 2.22     |
| GPT<br>(PWM Delay<br>Generation<br>Circuit) | GTIOCxY_Z output skew<br>(x = 0 to 3, Y = A or B, Z = A)             |                     | $t_{HRSK}^{*2}$             | -    | 2.0 | ns          | Figure 2.23     |
| AGT                                         | AGTIO, AGTEE input cycle                                             |                     | $t_{ACYC}^{*3}$             | 100  | -   | ns          | Figure 2.24     |
|                                             | AGTIO, AGTEE input high width, low width                             |                     | $t_{ACKWH},$<br>$t_{ACKWL}$ | 40   | -   | ns          |                 |
|                                             | AGTIO, AGTO, AGTOA, AGTOB output cycle                               |                     | $t_{ACYC2}$                 | 62.5 | -   | ns          |                 |
| ADC12                                       | ADC12 trigger input pulse width                                      |                     | $t_{TRGW}$                  | 1.5  | -   | $t_{Pcyc}$  | Figure 2.25     |
| KINT                                        | KRn(n = 00 to 07) pulse width                                        |                     | $t_{KR}$                    | 250  | -   | ns          | Figure 2.26     |

Note:  $t_{Pcyc}$ : PCLKB cycle,  $t_{PDcyc}$ : PCLKD cycle.

Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.

Note 2. The load is 30 pF.

Note 3. Constraints on input cycle:

When not switching the source clock:  $t_{Pcyc} \times 2 < t_{ACYC}$  should be satisfied.When switching the source clock:  $t_{Pcyc} \times 6 < t_{ACYC}$  should be satisfied.**Figure 2.18 I/O ports input timing****Figure 2.19 POEG input trigger timing**

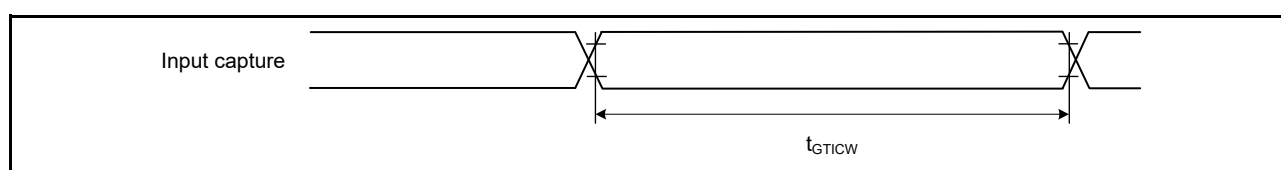


Figure 2.20 GPT32 input capture timing

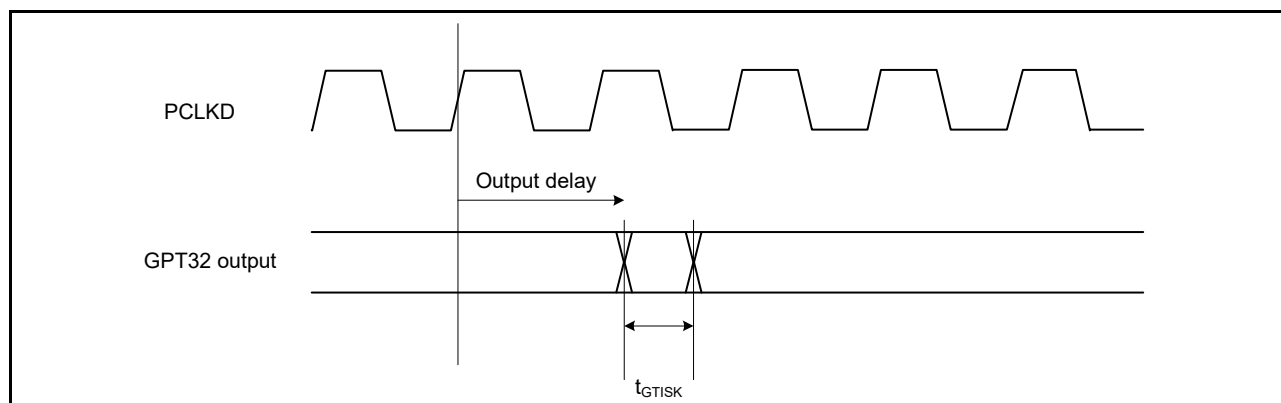


Figure 2.21 GPT32 output delay skew

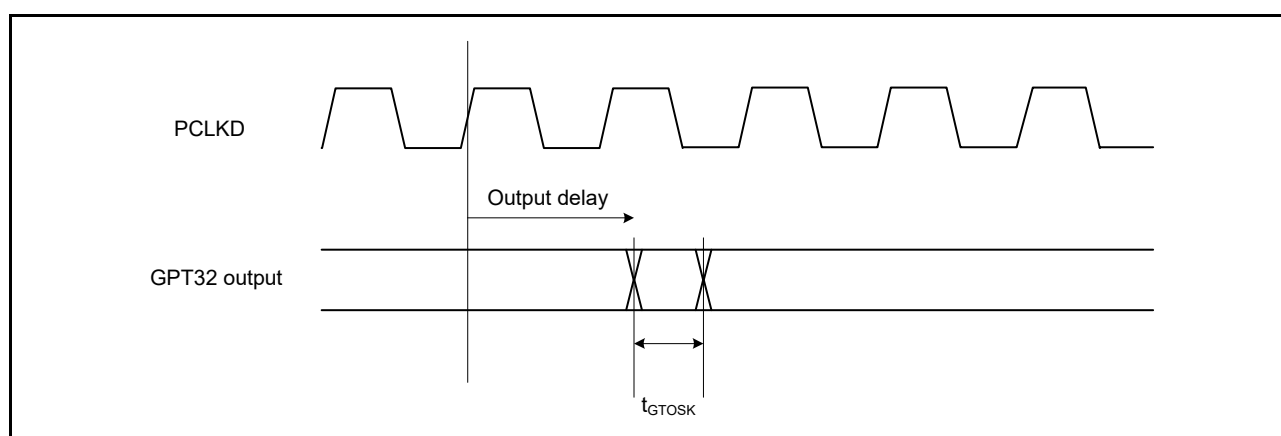


Figure 2.22 GPT32 output delay skew for OPS

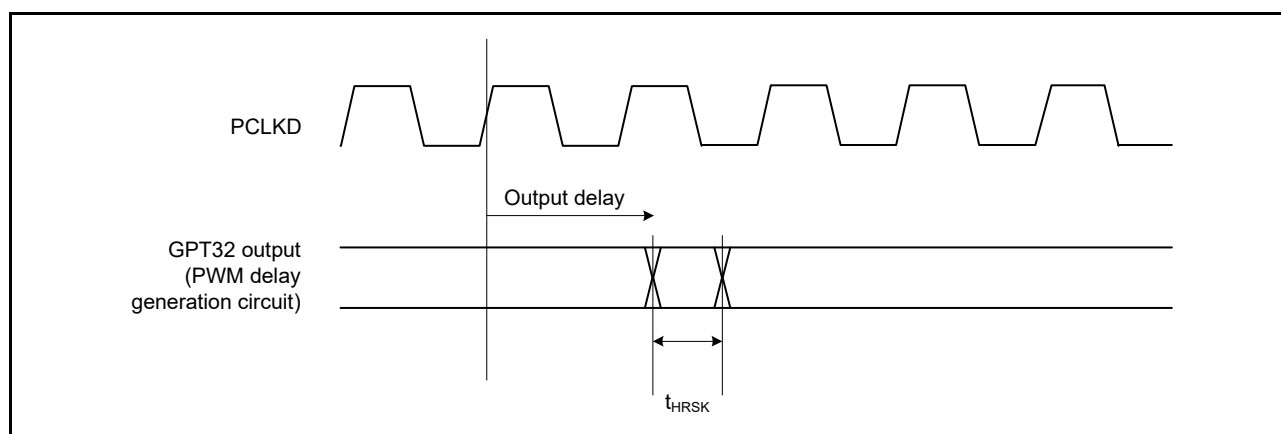


Figure 2.23 GPT32 (PWM delay generation circuit) output delay skew

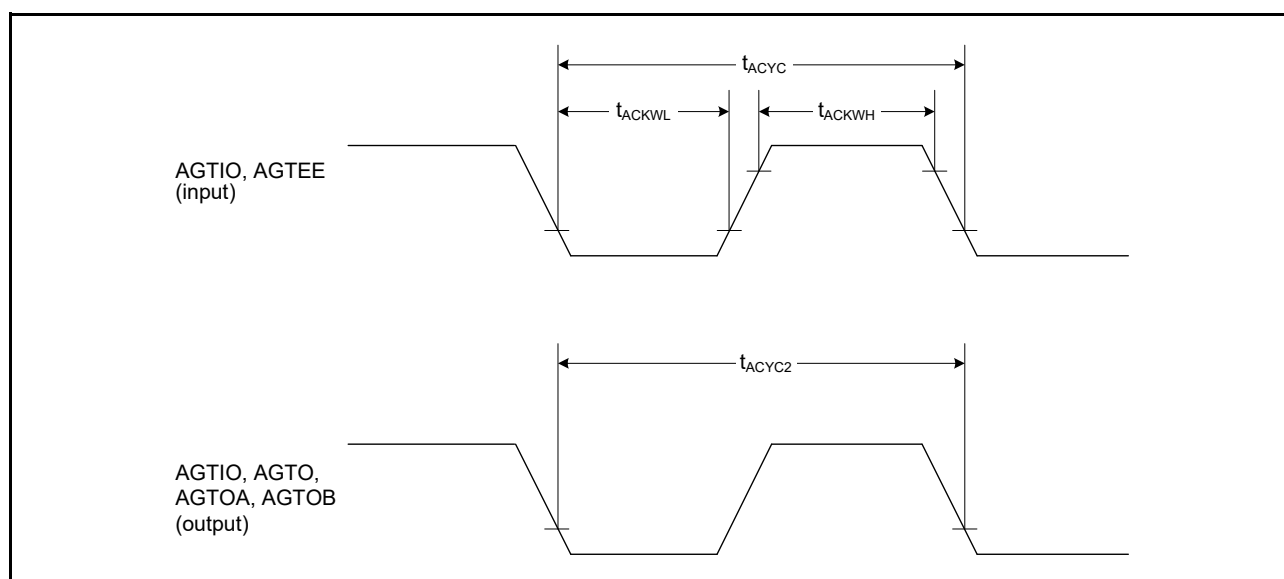


Figure 2.24 AGT input/output timing

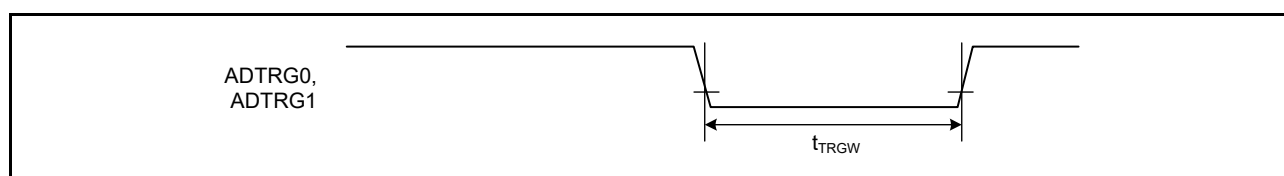


Figure 2.25 ADC12 trigger input timing

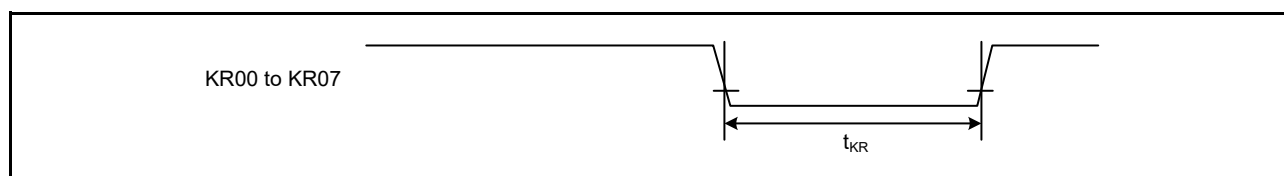


Figure 2.26 Key interrupt input timing

### 2.3.7 PWM Delay Generation Circuit Timing

Table 2.19 PWM Delay Generation Circuit timing

| Parameter           | Min | Typ  | Max | Unit | Test conditions |
|---------------------|-----|------|-----|------|-----------------|
| Operation frequency | 80  | -    | 120 | MHz  | -               |
| Resolution          | -   | 260  | -   | ps   | PCLKD = 120 MHz |
| DNL*1               | -   | ±2.0 | -   | LSB  | -               |

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

### 2.3.8 CAC Timing

Table 2.20 CAC timing

| Parameter |                          |                             | Symbol       | Min                                       | Typ | Max | Unit | Test conditions |
|-----------|--------------------------|-----------------------------|--------------|-------------------------------------------|-----|-----|------|-----------------|
| CAC       | CACREF input pulse width | $t_{PBcyc} \leq t_{cac}^*2$ | $t_{CACREF}$ | $4.5 \times t_{cac} + 3 \times t_{PBcyc}$ | -   | -   | ns   | -               |
|           |                          | $t_{PBcyc} > t_{cac}^*2$    |              | $5 \times t_{cac} + 6.5 \times t_{PBcyc}$ | -   | -   | ns   |                 |

Note 1.  $t_{pBcyc}$ : PCLKB cycle.

Note 2.  $t_{cac}$ : CAC count clock source cycle.

### 2.3.9 SCI Timing

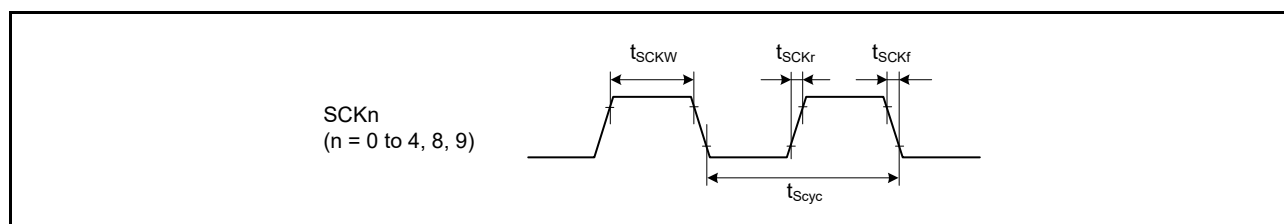
**Table 2.21 SCI timing (1)**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SCK0 to SCK4, SCK8, SCK9.

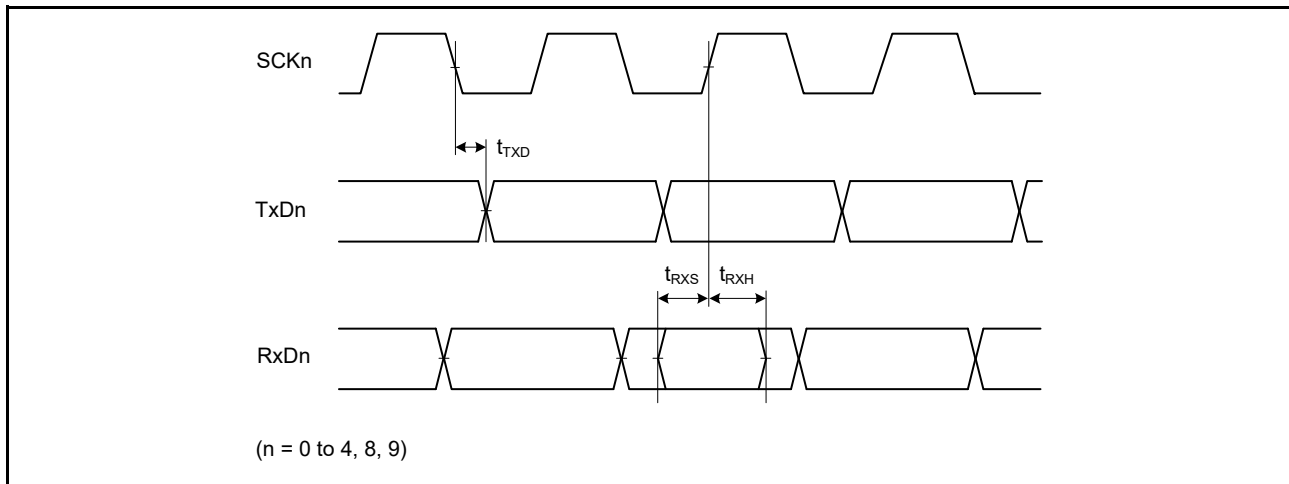
For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter |                          |                   | Symbol     | Min | Max | Unit*1     | Test conditions |             |
|-----------|--------------------------|-------------------|------------|-----|-----|------------|-----------------|-------------|
| SCI       | Input clock cycle        | Asynchronous      | $t_{Scyc}$ | 4   | -   | $t_{Pcyc}$ | Figure 2.27     |             |
|           |                          | Clock synchronous |            | 6   | -   |            |                 |             |
|           | Input clock pulse width  |                   | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ |                 |             |
|           | Input clock rise time    |                   | $t_{SCKr}$ | -   | 5   | ns         |                 |             |
|           | Input clock fall time    |                   | $t_{SCKf}$ | -   | 5   | ns         |                 |             |
|           | Output clock cycle       | Asynchronous      | $t_{Scyc}$ | 6   | -   | $t_{Pcyc}$ |                 |             |
|           |                          | Clock synchronous |            | 4   | -   |            |                 |             |
|           | Output clock pulse width |                   | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ |                 |             |
|           | Output clock rise time   |                   | $t_{SCKr}$ | -   | 5   | ns         |                 |             |
|           | Output clock fall time   |                   | $t_{SCKf}$ | -   | 5   | ns         |                 |             |
|           | Transmit data delay      | Clock synchronous | $t_{TXD}$  | -   | 25  | ns         |                 | Figure 2.28 |
|           | Receive data setup time  | Clock synchronous | $t_{RXS}$  | 15  | -   | ns         |                 |             |
|           | Receive data hold time   | Clock synchronous | $t_{RXH}$  | 5   | -   | ns         |                 |             |

Note 1.  $t_{Pcyc}$ : PCLKA cycle.



**Figure 2.27 SCK clock input/output timing**



**Figure 2.28** SCI input/output timing in clock synchronous mode

**Table 2.22** SCI timing (2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SCK0 to SCK4, SCK8, SCK9.

For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter  |                                 | Symbol                    | Min                                       | Max                                       | Unit        | Test conditions               |
|------------|---------------------------------|---------------------------|-------------------------------------------|-------------------------------------------|-------------|-------------------------------|
| Simple SPI | SCK clock cycle output (master) | $t_{SPCyc}$               | 4 (PCLKA ≤ 60 MHz)<br>8 (PCLKA > 60 MHz)  | 65536                                     | $t_{PCyc}$  | Figure 2.29                   |
|            | SCK clock cycle input (slave)   | -                         | 6 (PCLKA ≤ 60 MHz)<br>12 (PCLKA > 60 MHz) | 65536                                     |             |                               |
|            | SCK clock high pulse width      | $t_{SPCKWH}$              | 0.4                                       | 0.6                                       | $t_{SPCyc}$ |                               |
|            | SCK clock low pulse width       | $t_{SPCKWL}$              | 0.4                                       | 0.6                                       | $t_{SPCyc}$ |                               |
|            | SCK clock rise and fall time    | $t_{SPCKr}$ , $t_{SPCKf}$ | -                                         | 20                                        | ns          |                               |
|            | Data input setup time           | $t_{SU}$                  | 33.3                                      | -                                         | ns          | Figure 2.30 to<br>Figure 2.33 |
|            | Data input hold time            | $t_H$                     | 33.3                                      | -                                         | ns          |                               |
|            | SS input setup time             | $t_{LEAD}$                | 1                                         | -                                         | $t_{SPCyc}$ |                               |
|            | SS input hold time              | $t_{LAG}$                 | 1                                         | -                                         | $t_{SPCyc}$ |                               |
|            | Data output delay               | $t_{OD}$                  | -                                         | 33.3                                      | ns          |                               |
|            | Data output hold time           | $t_{OH}$                  | -10                                       | -                                         | ns          |                               |
|            | Data rise and fall time         | $t_{Dr}$ , $t_{Df}$       | -                                         | 16.6                                      | ns          |                               |
|            | SS input rise and fall time     | $t_{SSLr}$ , $t_{SSLf}$   | -                                         | 16.6                                      | ns          |                               |
|            | Slave access time               | $t_{SA}$                  | -                                         | 4 (PCLKA ≤ 60 MHz)<br>8 (PCLKA > 60 MHz)  | $t_{PCyc}$  | Figure 2.33                   |
|            | Slave output release time       | $t_{REL}$                 | -                                         | 5 (PCLKA ≤ 60 MHz)<br>10 (PCLKA > 60 MHz) | $t_{PCyc}$  |                               |

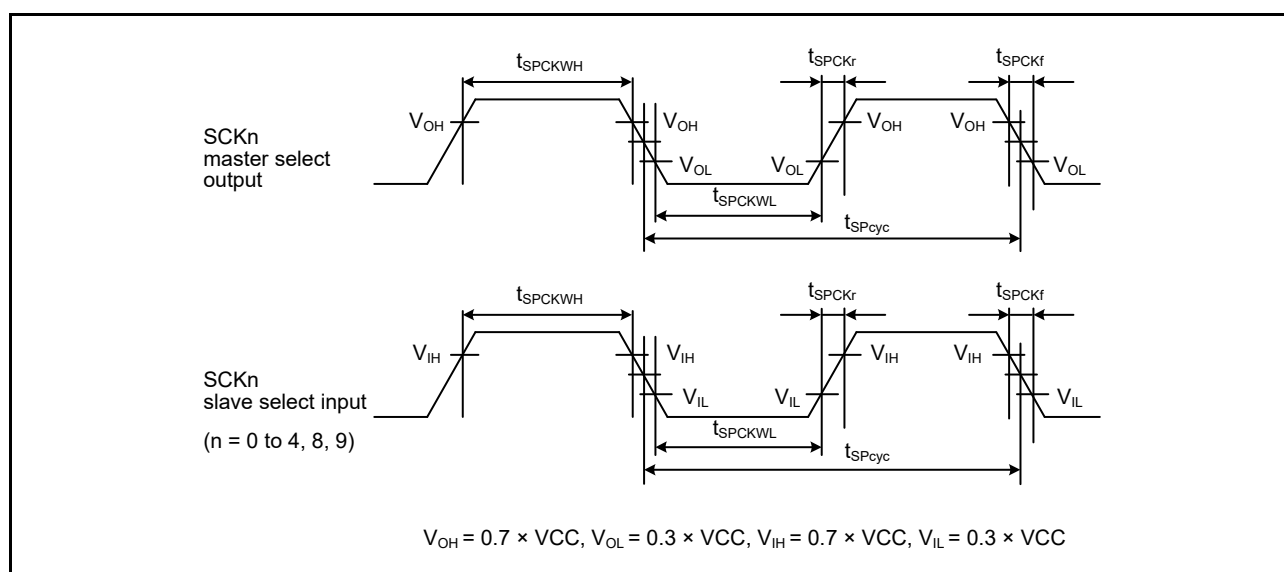


Figure 2.29 SCI simple SPI mode clock timing

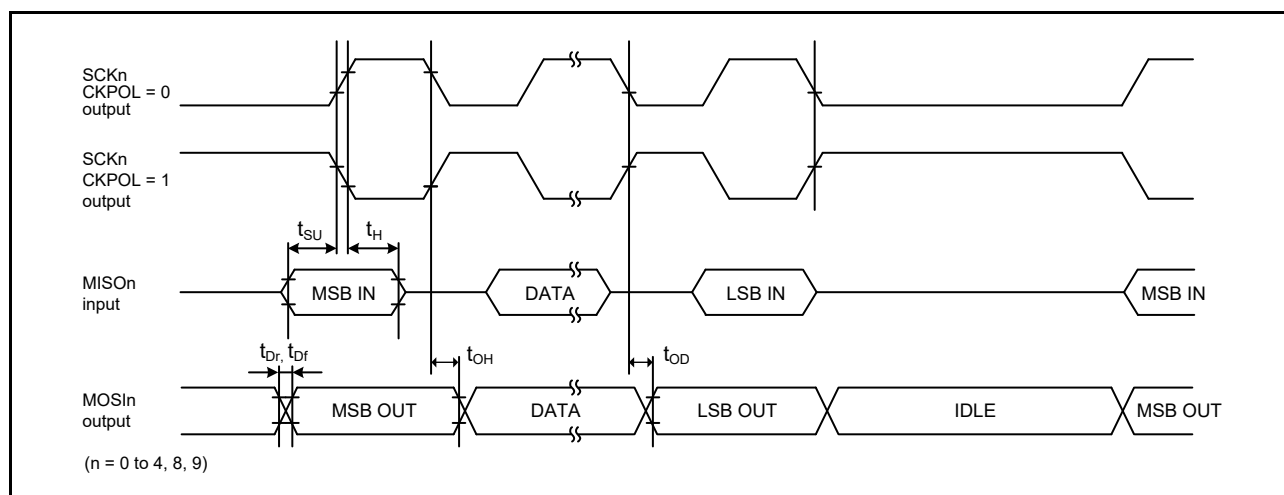


Figure 2.30 SCI simple SPI mode timing for master when CKPH = 1

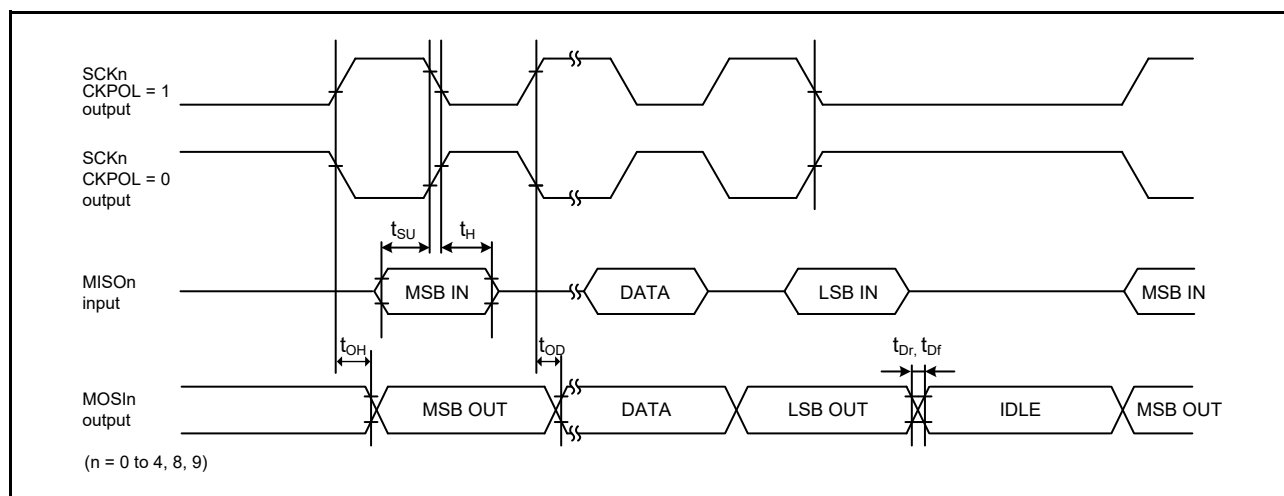


Figure 2.31 SCI simple SPI mode timing for master when CKPH = 0

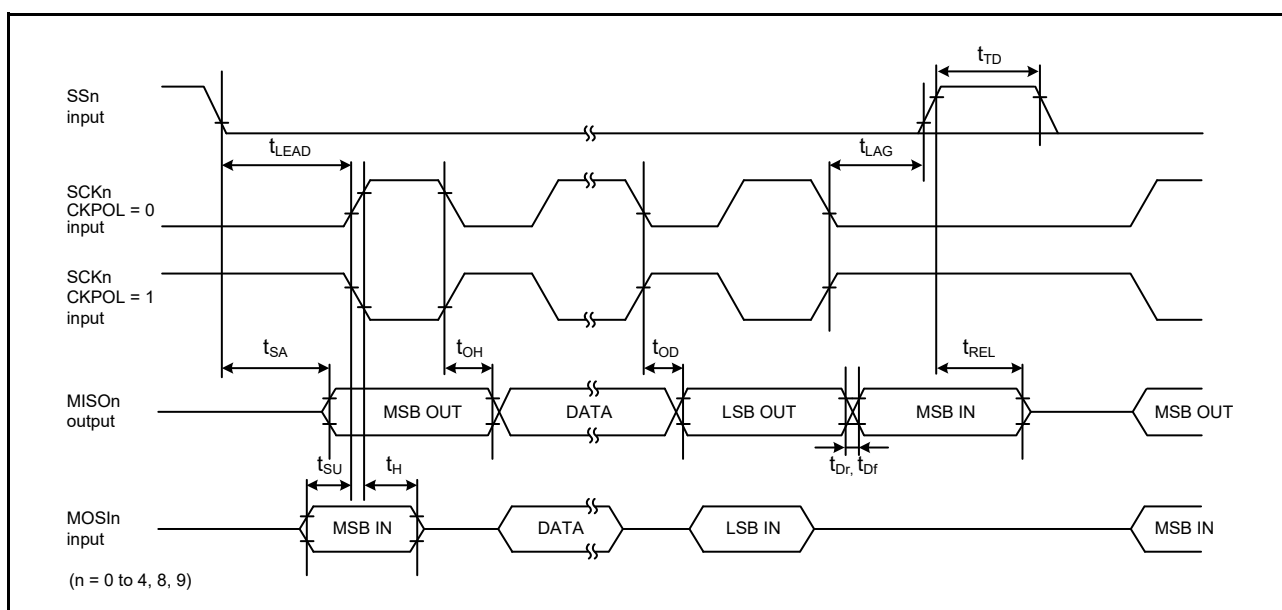


Figure 2.32 SCI simple SPI mode timing for slave when CKPH = 1

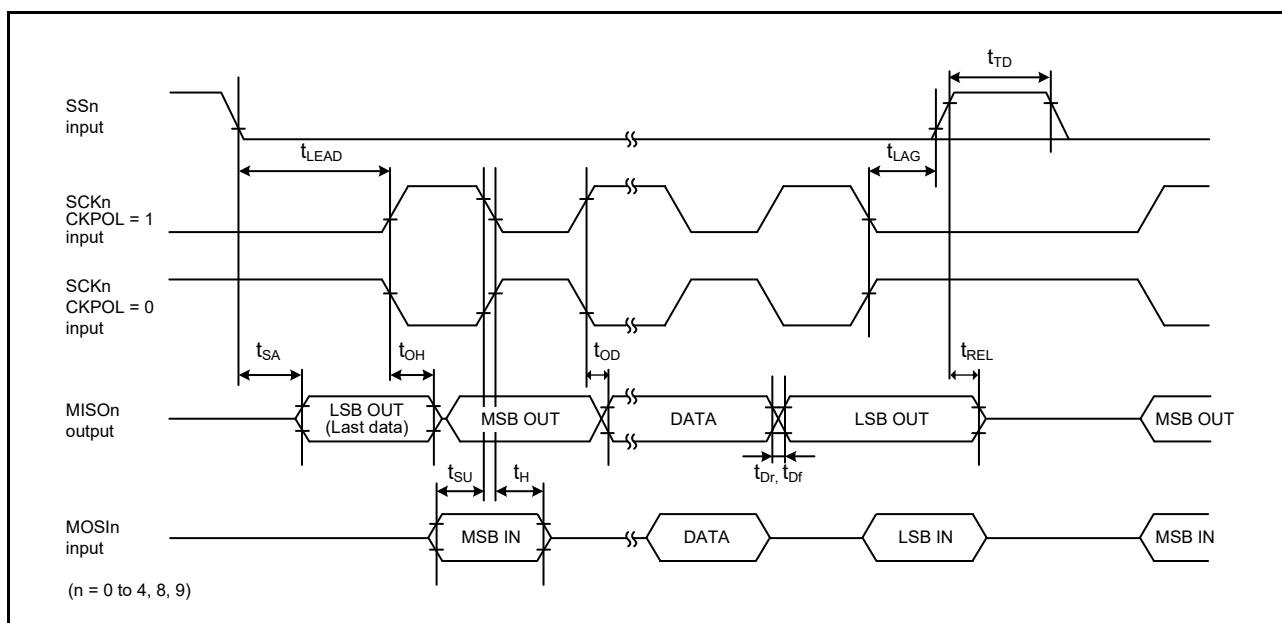


Figure 2.33 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.23 SCI timing (3) (1 of 2)

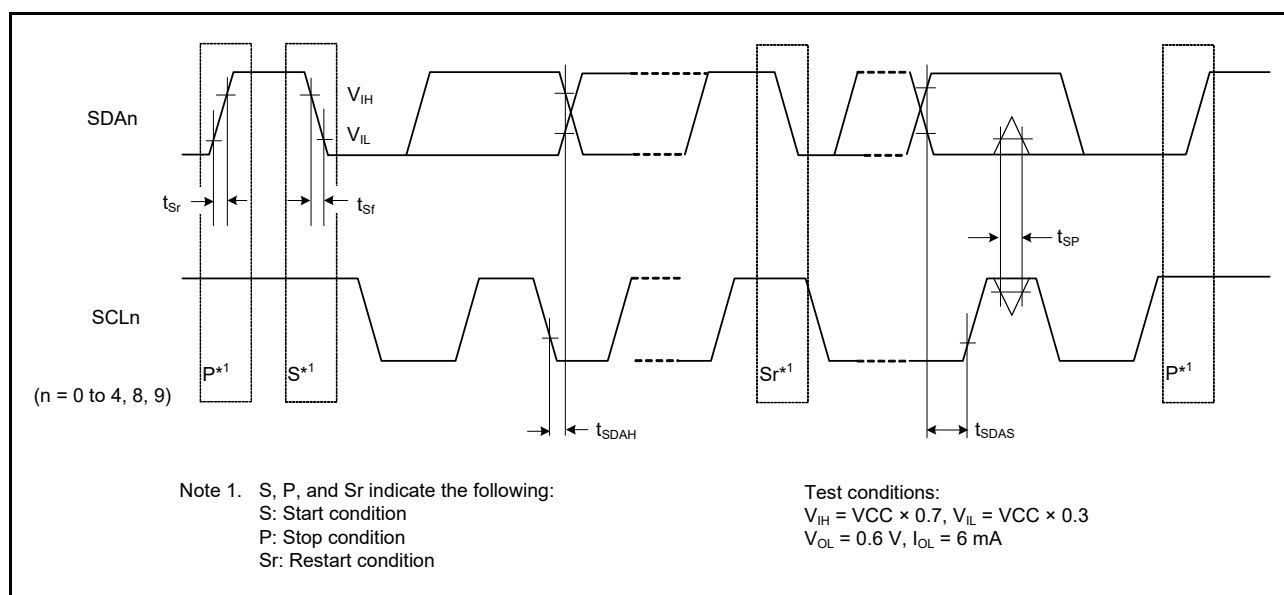
Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter                     | Symbol                             | Min        | Max | Unit                  | Test conditions |
|-------------------------------|------------------------------------|------------|-----|-----------------------|-----------------|
| Simple IIC<br>(Standard mode) | SDA input rise time                | $t_{Sr}$   | -   | 1000                  | ns              |
|                               | SDA input fall time                | $t_{Sf}$   | -   | 300                   | ns              |
|                               | SDA input spike pulse removal time | $t_{SP}$   | 0   | $4 \times t_{IICcyc}$ | ns              |
|                               | Data input setup time              | $t_{SDAS}$ | 250 | -                     | ns              |
|                               | Data input hold time               | $t_{SDAH}$ | 0   | -                     | ns              |
|                               | SCL, SDA capacitive load           | $C_b^{*1}$ | -   | 400                   | pF              |

**Table 2.23 SCI timing (3) (2 of 2)**

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter              | Symbol                             | Min        | Max | Unit                  | Test conditions |
|------------------------|------------------------------------|------------|-----|-----------------------|-----------------|
| Simple IIC (Fast mode) | SDA input rise time                | $t_{Sr}$   | -   | 300                   | ns              |
|                        | SDA input fall time                | $t_{Sf}$   | -   | 300                   | ns              |
|                        | SDA input spike pulse removal time | $t_{SP}$   | 0   | $4 \times t_{IICcyc}$ | ns              |
|                        | Data input setup time              | $t_{SDAS}$ | 100 | -                     | ns              |
|                        | Data input hold time               | $t_{SDAH}$ | 0   | -                     | ns              |
|                        | SCL, SDA capacitive load           | $C_b^{*1}$ | -   | 400                   | pF              |

Note:  $t_{IICcyc}$ : IIC internal reference clock (IIC $\phi$ ) cycle.Note 1.  $C_b$  indicates the total capacity of the bus line.**Figure 2.34 SCI simple IIC mode timing**

## 2.3.10 SPI Timing

**Table 2.24 SPI timing**

Conditions:

For RSPCKA and RSPCKB pins, high drive output is selected with the Port Drive Capability bit in the PmnPFS register.

For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter |                                  |                                                             | Symbol           | Min                                             | Max                                      | Unit*1     | Test conditions*2                          |
|-----------|----------------------------------|-------------------------------------------------------------|------------------|-------------------------------------------------|------------------------------------------|------------|--------------------------------------------|
| SPI       | RSPCK clock cycle                | Master                                                      | $t_{SPCyc}$      | 2 (PCLKA $\leq$ 60 MHz)<br>4 (PCLKA $>$ 60 MHz) | 4096                                     | $t_{Pcyc}$ | Figure 2.35<br>C = 30 pF                   |
|           |                                  | Slave                                                       |                  | 4                                               | 4096                                     |            |                                            |
|           | RSPCK clock high pulse width     | Master                                                      | $t_{SPCKWH}$     | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$   | -                                        | ns         |                                            |
|           |                                  | Slave                                                       |                  | $2 \times t_{Pcyc}$                             | -                                        |            |                                            |
|           | RSPCK clock low pulse width      | Master                                                      | $t_{SPCKWL}$     | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$   | -                                        | ns         | Figure 2.36 to<br>Figure 2.41<br>C = 30 pF |
|           |                                  | Slave                                                       |                  | $2 \times t_{Pcyc}$                             | -                                        |            |                                            |
|           | RSPCK clock rise and fall time   | Master                                                      | $t_{SPCKr}$      | -                                               | 5                                        | ns         |                                            |
|           |                                  | Slave                                                       | $t_{SPCKf}$      | -                                               | 1                                        | $\mu$ s    |                                            |
|           | Data input setup time            | Master                                                      | $t_{SU}$         | 4                                               | -                                        | ns         |                                            |
|           |                                  | Slave                                                       |                  | 5                                               | -                                        |            |                                            |
|           | Data input hold time             | Master (PCLKA division ratio set to 1/2)                    | $t_{HF}$         | 0                                               | -                                        | ns         |                                            |
|           |                                  | Master (PCLKA division ratio set to a value other than 1/2) | $t_H$            | $t_{Pcyc}$                                      | -                                        |            |                                            |
|           |                                  | Slave                                                       | $t_H$            | 20                                              | -                                        |            |                                            |
|           | SSL setup time                   | Master                                                      | $t_{LEAD}$       | $N \times t_{SPCyc} - 10^3$                     | $N \times t_{SPCyc} + 100^3$             | ns         |                                            |
|           |                                  | Slave                                                       |                  | $6 \times t_{Pcyc}$                             | -                                        | ns         |                                            |
|           | SSL hold time                    | Master                                                      | $t_{LAG}$        | $N \times t_{SPCyc} - 10^4$                     | $N \times t_{SPCyc} + 100^4$             | ns         |                                            |
|           |                                  | Slave                                                       |                  | $6 \times t_{Pcyc}$                             | -                                        | ns         |                                            |
|           | Data output delay                | Master                                                      | $t_{OD}$         | -                                               | 6.3                                      | ns         |                                            |
|           |                                  | Slave                                                       |                  | -                                               | 20                                       |            |                                            |
|           | Data output hold time            | Master                                                      | $t_{OH}$         | 0                                               | -                                        | ns         |                                            |
|           |                                  | Slave                                                       |                  | 0                                               | -                                        |            |                                            |
|           | Successive transmission delay    | Master                                                      | $t_{TD}$         | $t_{SPCyc} + 2 \times t_{Pcyc}$                 | $8 \times t_{SPCyc} + 2 \times t_{Pcyc}$ | ns         | Figure 2.40 and<br>Figure 2.41<br>C = 30pF |
|           |                                  | Slave                                                       |                  | $6 \times t_{Pcyc}$                             |                                          |            |                                            |
|           | MOSI and MISO rise and fall time | Output                                                      | $t_{Dr}, t_{Df}$ | -                                               | 5                                        | ns         |                                            |
|           |                                  | Input                                                       |                  | -                                               | 1                                        | $\mu$ s    |                                            |
|           | SSL rise and fall time           | Output                                                      | $t_{SSLr}$       | -                                               | 5                                        | ns         |                                            |
|           |                                  | Input                                                       | $t_{SSLf}$       | -                                               | 1                                        | $\mu$ s    |                                            |
|           | Slave access time                |                                                             | $t_{SA}$         | -                                               | $2 \times t_{Pcyc} + 28$                 | ns         |                                            |
|           | Slave output release time        |                                                             | $t_{REL}$        | -                                               | $2 \times t_{Pcyc} + 28$                 |            |                                            |

Note 1.  $t_{Pcyc}$ : PCLKA cycle.

- Note 2. Must use pins that have a letter appended to their name, for instance “\_A”, “\_B”, to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
- Note 3. N is set to an integer from 1 to 8 by the SPCKD register.
- Note 4. N is set to an integer from 1 to 8 by the SSLND register.

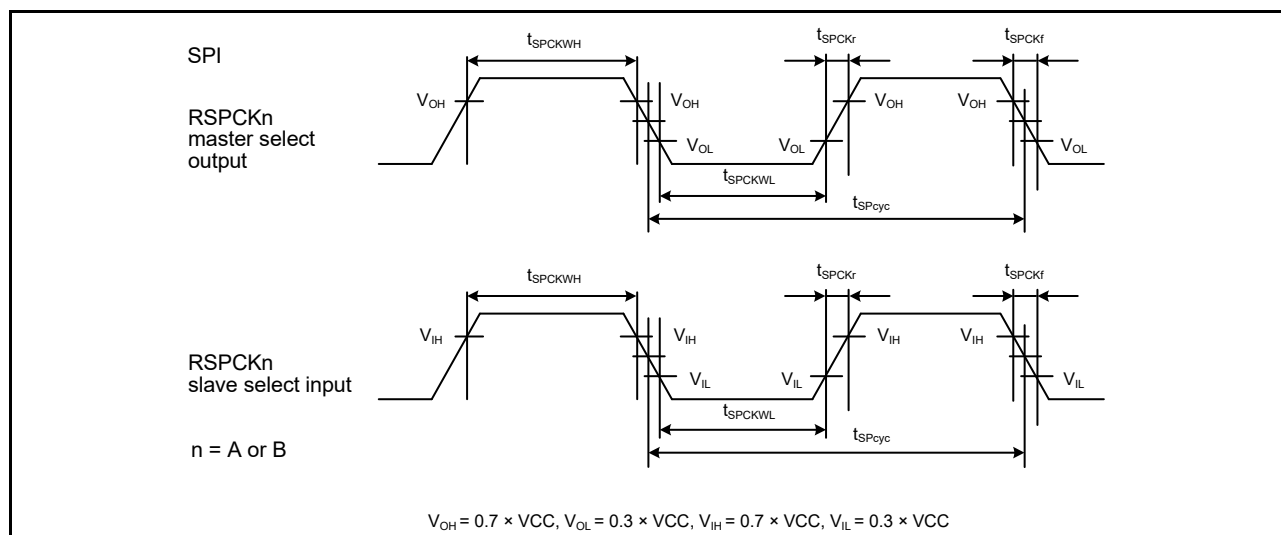


Figure 2.35 SPI clock timing

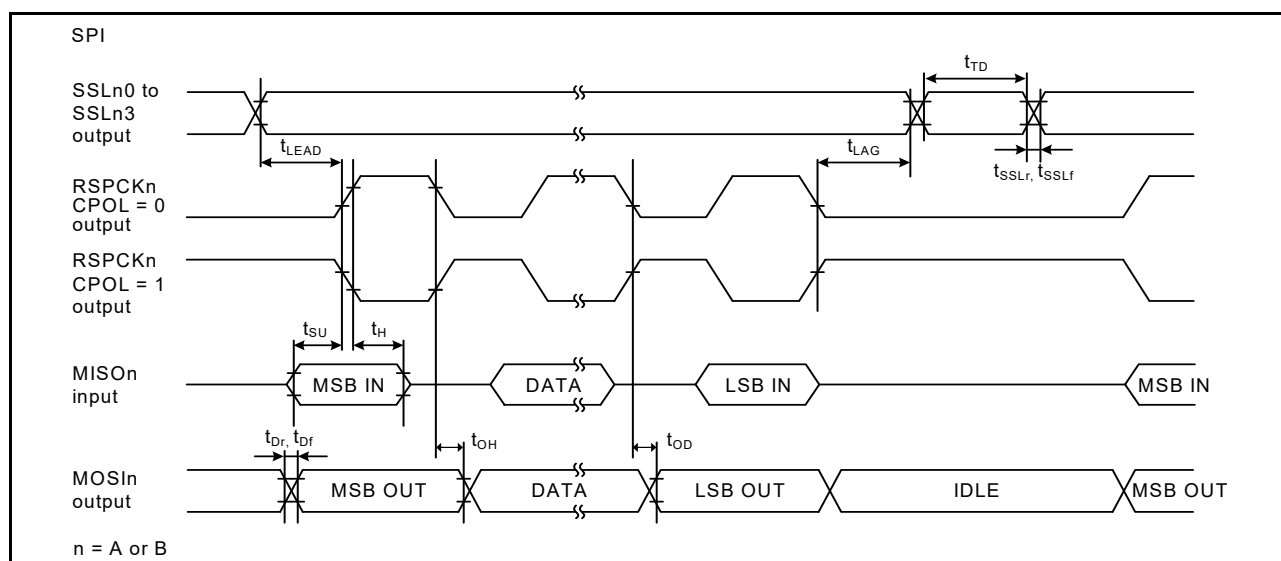
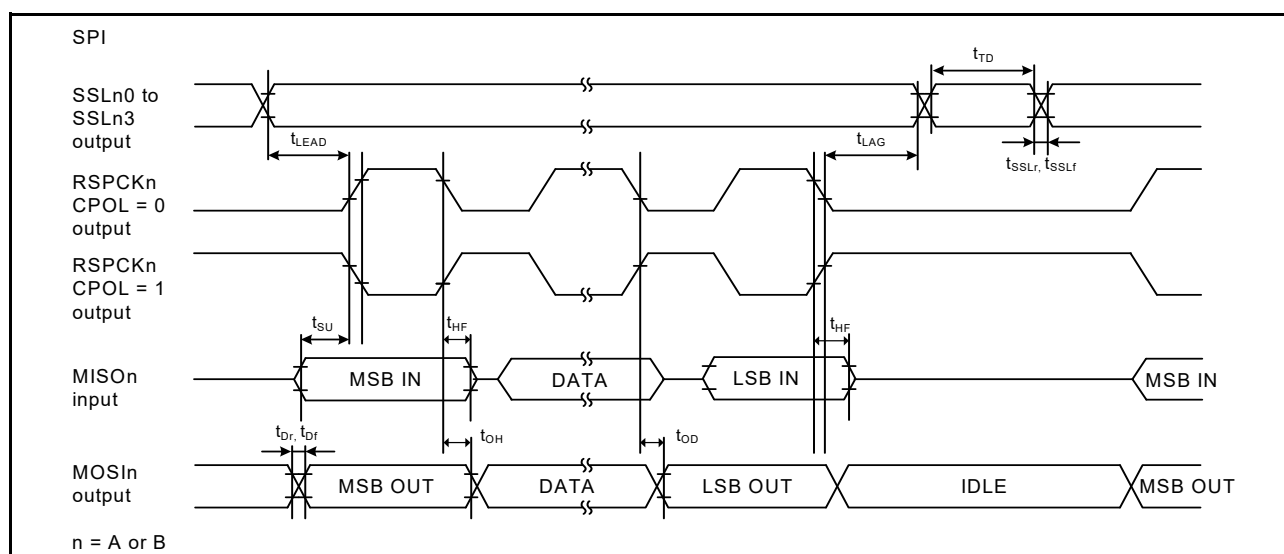
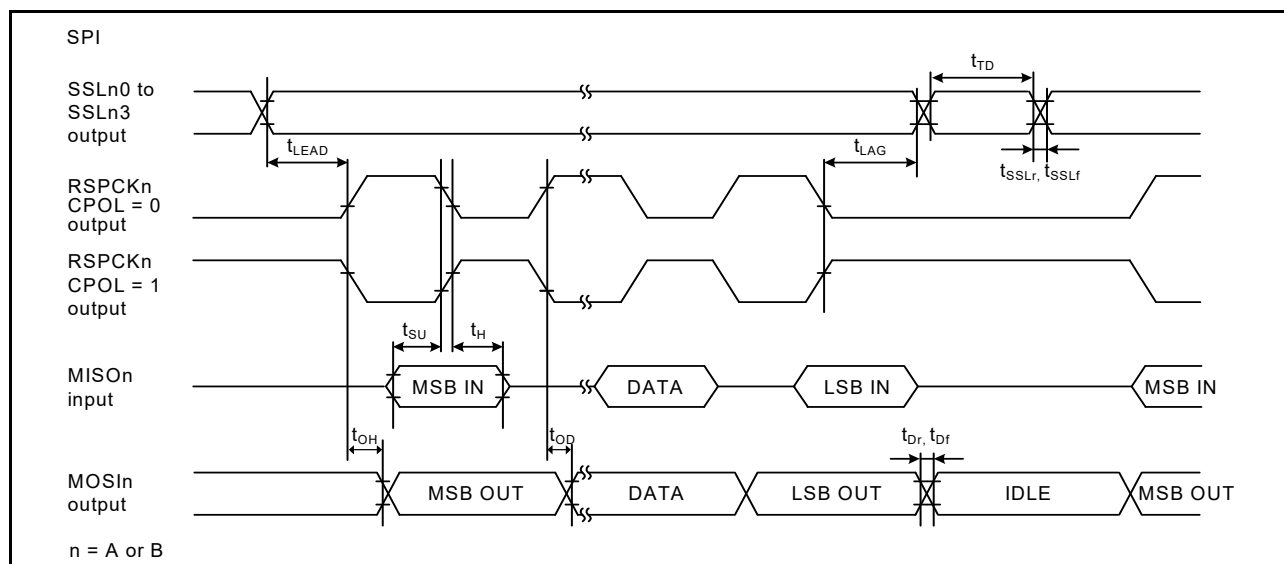


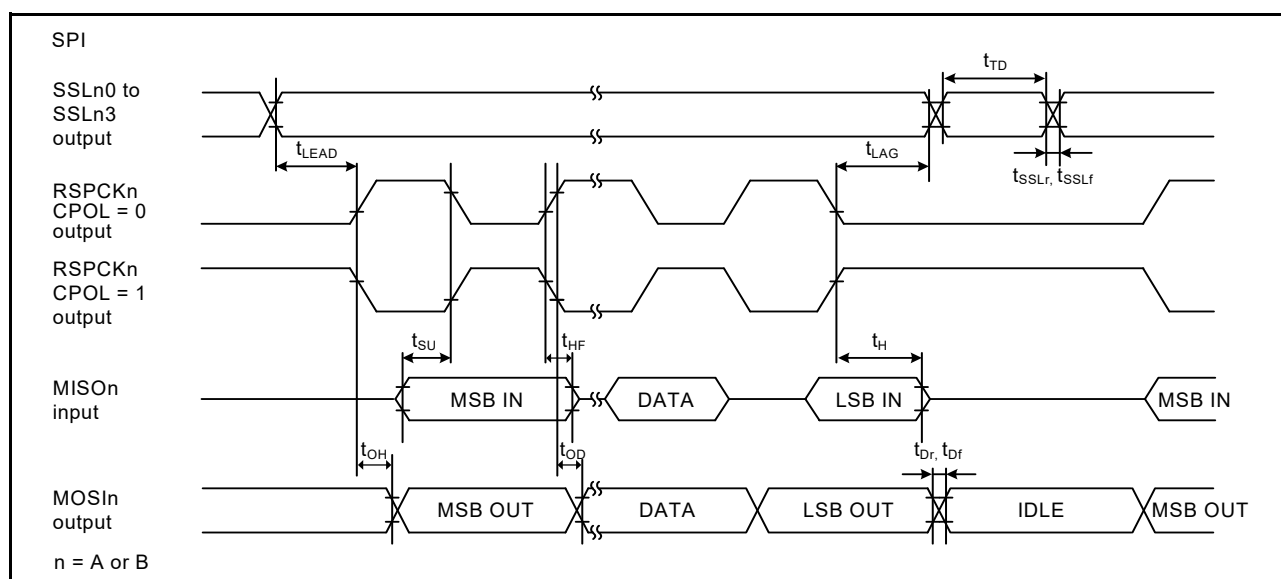
Figure 2.36 SPI timing for master when CPHA = 0



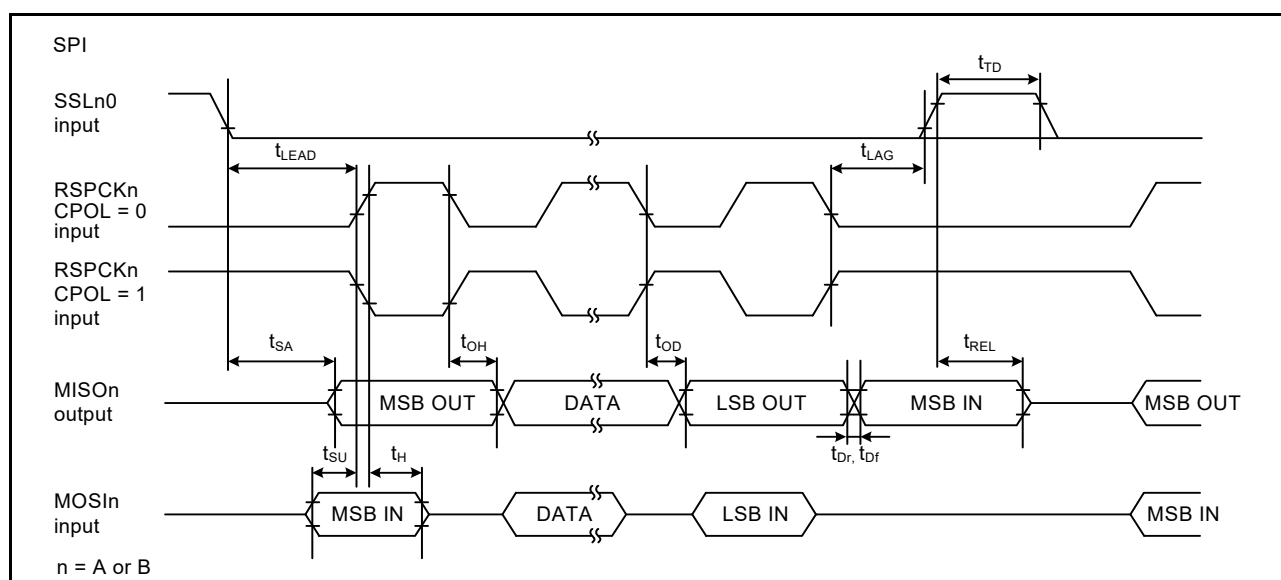
**Figure 2.37** SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2



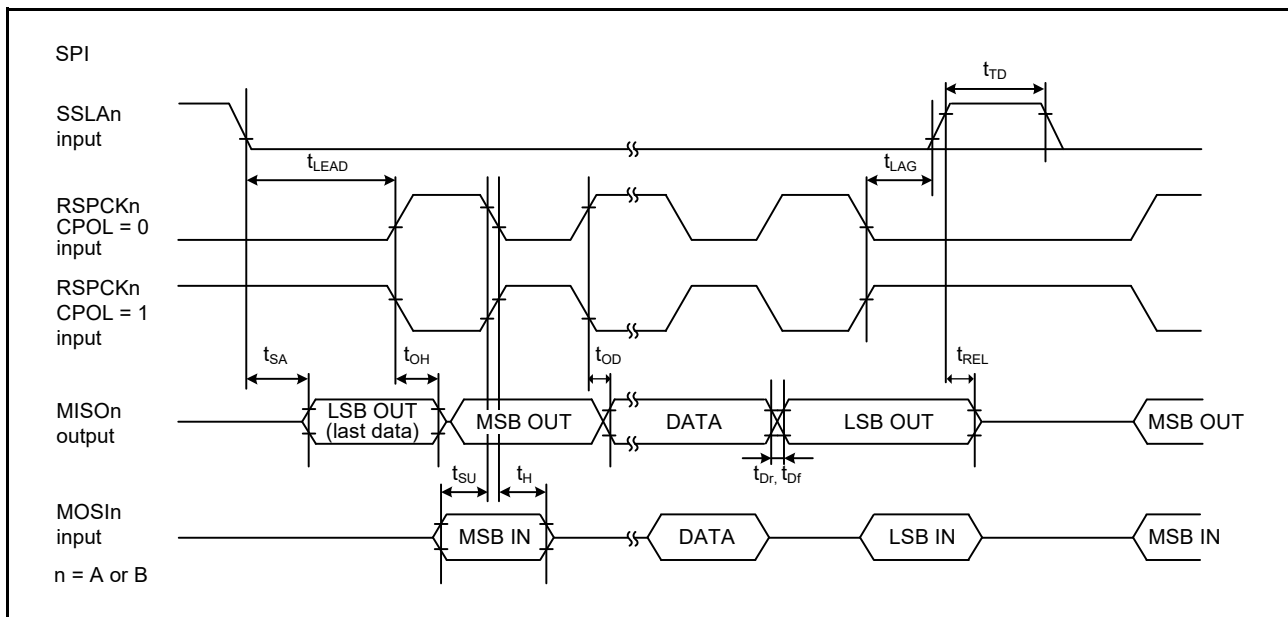
**Figure 2.38** SPI timing for master when CPHA = 1



**Figure 2.39** RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2



**Figure 2.40** SPI timing for slave when CPHA = 0



**Figure 2.41** SPI timing for slave when CPHA = 1

### 2.3.11 IIC Timing

**Table 2.25** IIC timing (1) (1 of 2)

- (1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0\_B, SCL0\_B, SDA1\_A, SCL1\_A, SDA1\_B, SCL1\_B.  
 (2) The following pins do not require setting: SCL0\_A, SDA0\_A.  
 (3) Use pins that have a letter appended to their names, for instance “\_A” or “\_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

| Parameter                                          | Symbol                                                           | Min*1      | Max                                                 | Unit                      | Test conditions*3 |
|----------------------------------------------------|------------------------------------------------------------------|------------|-----------------------------------------------------|---------------------------|-------------------|
| IIC<br>(Standard mode,<br>SMBus)<br>ICFER.FMPE = 0 | SCL input cycle time                                             | $t_{SCL}$  | $6 (12) \times t_{IICcyc} + 1300$                   | -                         | ns                |
|                                                    | SCL input high pulse width                                       | $t_{SCLH}$ | $3 (6) \times t_{IICcyc} + 300$                     | -                         | ns                |
|                                                    | SCL input low pulse width                                        | $t_{SCLL}$ | $3 (6) \times t_{IICcyc} + 300$                     | -                         | ns                |
|                                                    | SCL, SDA input rise time                                         | $t_{Sr}$   | -                                                   | 1000                      | ns                |
|                                                    | SCL, SDA input fall time                                         | $t_{Sf}$   | -                                                   | 300                       | ns                |
|                                                    | SCL, SDA input spike pulse removal time                          | $t_{SP}$   | 0                                                   | $1 (4) \times t_{IICcyc}$ | ns                |
|                                                    | SDA input bus free time when wakeup function is disabled         | $t_{BUF}$  | $3 (6) \times t_{IICcyc} + 300$                     | -                         | ns                |
|                                                    | SDA input bus free time when wakeup function is enabled          | $t_{BUF}$  | $3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$ | -                         | ns                |
|                                                    | START condition input hold time when wakeup function is disabled | $t_{STAH}$ | $t_{IICcyc} + 300$                                  | -                         | ns                |
|                                                    | START condition input hold time when wakeup function is enabled  | $t_{STAH}$ | $1 (5) \times t_{IICcyc} + t_{Pcyc} + 300$          | -                         | ns                |
|                                                    | Repeated START condition input setup time                        | $t_{STAS}$ | 1000                                                | -                         | ns                |
|                                                    | STOP condition input setup time                                  | $t_{STOS}$ | 1000                                                | -                         | ns                |
|                                                    | Data input setup time                                            | $t_{SDAS}$ | $t_{IICcyc} + 50$                                   | -                         | ns                |
|                                                    | Data input hold time                                             | $t_{SDAH}$ | 0                                                   | -                         | ns                |
|                                                    | SCL, SDA capacitive load                                         | $C_b$      | -                                                   | 400                       | pF                |

**Table 2.25 IIC timing (1) (2 of 2)**

- (1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0\_B, SCL0\_B, SDA1\_A, SCL1\_A, SDA1\_B, SCL1\_B.
- (2) The following pins do not require setting: SCL0\_A, SDA0\_A.
- (3) Use pins that have a letter appended to their names, for instance “\_A” or “\_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

| Parameter                |                                                                  | Symbol     | Min*1                                               | Max                       | Unit | Test conditions*3 |
|--------------------------|------------------------------------------------------------------|------------|-----------------------------------------------------|---------------------------|------|-------------------|
| IIC<br>(Fast mode)       | SCL input cycle time                                             | $t_{SCL}$  | $6 (12) \times t_{IICcyc} + 600$                    | -                         | ns   | Figure 2.42       |
|                          | SCL input high pulse width                                       | $t_{SCLH}$ | $3 (6) \times t_{IICcyc} + 300$                     | -                         | ns   |                   |
|                          | SCL input low pulse width                                        | $t_{SCLL}$ | $3 (6) \times t_{IICcyc} + 300$                     | -                         | ns   |                   |
|                          | SCL, SDA input rise time                                         | $t_{Sr}$   | $20 \times (\text{external pullup voltage}/5.5V)^2$ | 300                       | ns   |                   |
|                          | SCL, SDA input fall time                                         | $t_{Sf}$   | $20 \times (\text{external pullup voltage}/5.5V)^2$ | 300                       | ns   |                   |
|                          | SCL, SDA input spike pulse removal time                          | $t_{SP}$   | 0                                                   | $1 (4) \times t_{IICcyc}$ | ns   |                   |
|                          | SDA input bus free time when wakeup function is disabled         | $t_{BUF}$  | $3 (6) \times t_{IICcyc} + 300$                     | -                         | ns   |                   |
|                          | SDA input bus free time when wakeup function is enabled          | $t_{BUF}$  | $3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$ | -                         | ns   |                   |
|                          | START condition input hold time when wakeup function is disabled | $t_{STAH}$ | $t_{IICcyc} + 300$                                  | -                         | ns   |                   |
|                          | START condition input hold time when wakeup function is enabled  | $t_{STAH}$ | $1 (5) \times t_{IICcyc} + t_{Pcyc} + 300$          | -                         | ns   |                   |
|                          | Repeated START condition input setup time                        | $t_{STAS}$ | 300                                                 | -                         | ns   |                   |
|                          | STOP condition input setup time                                  | $t_{STOS}$ | 300                                                 | -                         | ns   |                   |
|                          | Data input setup time                                            | $t_{SDAS}$ | $t_{IICcyc} + 50$                                   | -                         | ns   |                   |
|                          | Data input hold time                                             | $t_{SDAH}$ | 0                                                   | -                         | ns   |                   |
| SCL, SDA capacitive load |                                                                  | $C_b$      | -                                                   | 400                       | pF   |                   |

Note:  $t_{IICcyc}$ : IIC internal reference clock (IIC $\phi$ ) cycle,  $t_{Pcyc}$ : PCLKB cycle.

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 2. Only supported for SCL0\_A, SDA0\_A.

Note 3. Must use pins that have a letter appended to their name, for instance “\_A”, “\_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

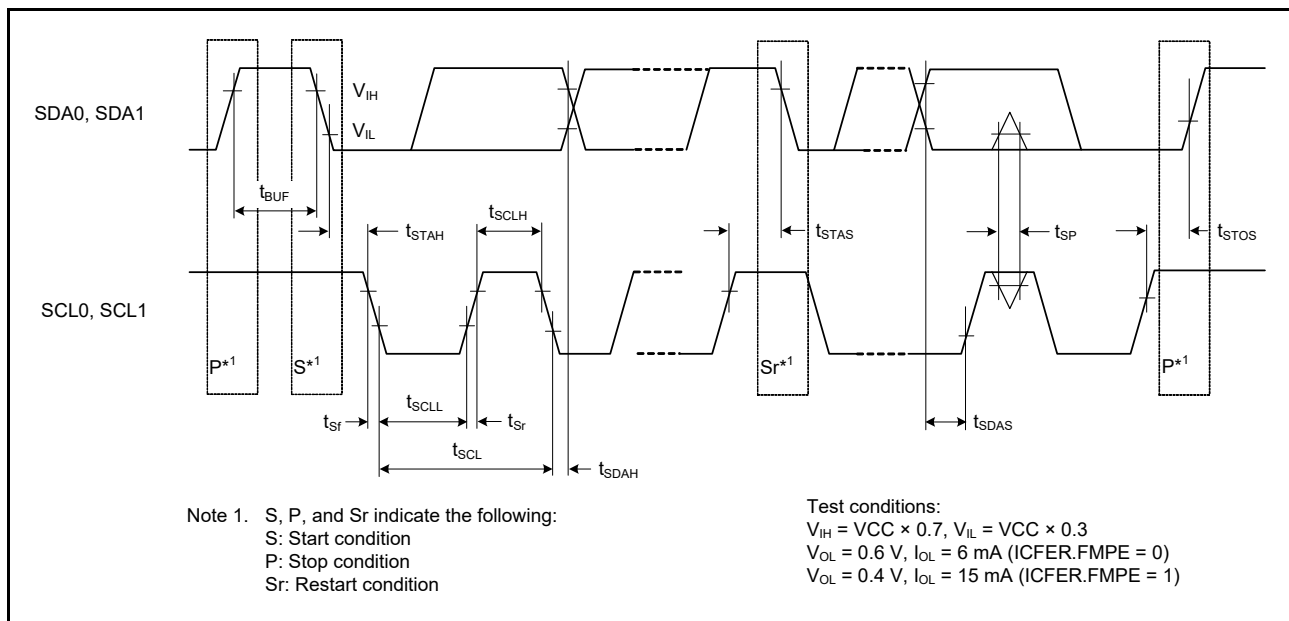
**Table 2.26 IIC timing (2)**

Setting of the SCL0\_A, SDA0\_A pins is not required with the Port Drive Capability bit in the PmnPFS register.

| Parameter                             |                                                                  | Symbol            | Min*1,*2                                                  | Max                         | Unit | Test conditions |
|---------------------------------------|------------------------------------------------------------------|-------------------|-----------------------------------------------------------|-----------------------------|------|-----------------|
| IIC<br>(Fast mode+)<br>ICFER.FMPE = 1 | SCL input cycle time                                             | t <sub>SCL</sub>  | 6 (12) × t <sub>IICcyc</sub> + 240                        | -                           | ns   | Figure 2.42     |
|                                       | SCL input high pulse width                                       | t <sub>SCLH</sub> | 3 (6) × t <sub>IICcyc</sub> + 120                         | -                           | ns   |                 |
|                                       | SCL input low pulse width                                        | t <sub>SCLL</sub> | 3 (6) × t <sub>IICcyc</sub> + 120                         | -                           | ns   |                 |
|                                       | SCL, SDA input rise time                                         | t <sub>Sr</sub>   | -                                                         | 120                         | ns   |                 |
|                                       | SCL, SDA input fall time                                         | t <sub>Sf</sub>   | -                                                         | 120                         | ns   |                 |
|                                       | SCL, SDA input spike pulse removal time                          | t <sub>SP</sub>   | 0                                                         | 1 (4) × t <sub>IICcyc</sub> | ns   |                 |
|                                       | SDA input bus free time when wakeup function is disabled         | t <sub>BUF</sub>  | 3 (6) × t <sub>IICcyc</sub> + 120                         | -                           | ns   |                 |
|                                       | SDA input bus free time when wakeup function is enabled          | t <sub>BUF</sub>  | 3 (6) × t <sub>IICcyc</sub> + 4 × t <sub>Pcyc</sub> + 120 | -                           | ns   |                 |
|                                       | Start condition input hold time when wakeup function is disabled | t <sub>STAH</sub> | t <sub>IICcyc</sub> + 120                                 | -                           | ns   |                 |
|                                       | START condition input hold time when wakeup function is enabled  | t <sub>STAH</sub> | 1 (5) × t <sub>IICcyc</sub> + t <sub>Pcyc</sub> + 120     | -                           | ns   |                 |
|                                       | Restart condition input setup time                               | t <sub>STAS</sub> | 120                                                       | -                           | ns   |                 |
|                                       | Stop condition input setup time                                  | t <sub>STOS</sub> | 120                                                       | -                           | ns   |                 |
|                                       | Data input setup time                                            | t <sub>SDAS</sub> | t <sub>IICcyc</sub> + 30                                  | -                           | ns   |                 |
|                                       | Data input hold time                                             | t <sub>SDAH</sub> | 0                                                         | -                           | ns   |                 |
|                                       | SCL, SDA capacitive load                                         | C <sub>b</sub>    | -                                                         | 550                         | pF   |                 |

Note:  $t_{IICcyc}$ : IIC internal reference clock (IIC $\phi$ ) cycle,  $t_{Pcyc}$ : PCLKB cycle.

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 2.  $C_b$  indicates the total capacity of the bus line.**Figure 2.42 I<sup>2</sup>C bus interface input/output timing**

## 2.4 ADC12 Characteristics

**Table 2.27 A/D conversion characteristics for unit 0 (1 of 2)**

Conditions: PCLKC = 1 to 60 MHz

| Parameter                                                                        |                                                             |                                                 | Min                             | Typ  | Max           | Unit | Test conditions                                                                                  |
|----------------------------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------|---------------------------------|------|---------------|------|--------------------------------------------------------------------------------------------------|
| Frequency                                                                        |                                                             |                                                 | 1                               | -    | 60            | MHz  | -                                                                                                |
| Analog input capacitance                                                         |                                                             |                                                 | -                               | -    | 30            | pF   | -                                                                                                |
| Quantization error                                                               |                                                             |                                                 | -                               | ±0.5 | -             | LSB  | -                                                                                                |
| Resolution                                                                       |                                                             |                                                 | -                               | -    | 12            | Bits | -                                                                                                |
| Channel-dedicated sample-and-hold circuits in use* <sup>3</sup> (AN000 to AN002) | Conversion time* <sup>1</sup> (operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 1.06 (0.4 + 0.25)* <sup>2</sup> | -    | -             | μs   | • Sampling of channel-dedicated sample-and-hold circuits in 24 states<br>• Sampling in 15 states |
|                                                                                  | Offset error                                                |                                                 | -                               | ±1.5 | ±3.5          | LSB  | AN000 to AN002 = 0.25 V                                                                          |
|                                                                                  | Full-scale error                                            |                                                 | -                               | ±1.5 | ±3.5          | LSB  | AN000 to AN002 = VREFH0- 0.25 V                                                                  |
|                                                                                  | Absolute accuracy                                           |                                                 | -                               | ±2.5 | ±5.5          | LSB  | -                                                                                                |
|                                                                                  | DNL pseudo-differential nonlinearity error                  |                                                 | -                               | ±1.0 | ±2.0          | LSB  | -                                                                                                |
|                                                                                  | INL integral nonlinearity error                             |                                                 | -                               | ±1.5 | ±3.0          | LSB  | -                                                                                                |
|                                                                                  | Holding characteristics of sample-and hold circuits         |                                                 | -                               | -    | 20            | μs   | -                                                                                                |
|                                                                                  | Dynamic range                                               |                                                 | 0.25                            | -    | VREFH0 - 0.25 | V    | -                                                                                                |
| Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002)           | Conversion time* <sup>1</sup> (operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.48 (0.267)* <sup>2</sup>      | -    | -             | μs   | Sampling in 16 states                                                                            |
|                                                                                  | Offset error                                                |                                                 | -                               | ±1.0 | ±2.5          | LSB  | -                                                                                                |
|                                                                                  | Full-scale error                                            |                                                 | -                               | ±1.0 | ±2.5          | LSB  | -                                                                                                |
|                                                                                  | Absolute accuracy                                           |                                                 | -                               | ±2.0 | ±4.5          | LSB  | -                                                                                                |
|                                                                                  | DNL pseudo-differential nonlinearity error                  |                                                 | -                               | ±0.5 | ±1.5          | LSB  | -                                                                                                |
|                                                                                  | INL integral nonlinearity error                             |                                                 | -                               | ±1.0 | ±2.5          | LSB  | -                                                                                                |
| High-precision channels (AN003, AN005, AN006)                                    | Conversion time* <sup>1</sup> (operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.48 (0.267)* <sup>2</sup>      | -    | -             | μs   | Sampling in 16 states                                                                            |
|                                                                                  |                                                             | Max. = 400 Ω                                    | 0.40 (0.183)* <sup>2</sup>      | -    | -             | μs   | Sampling in 11 states<br>VCC = AVCC0 = 3.0 to 3.6 V<br>3.0 V ≤ VREFH0 ≤ AVCC0                    |
|                                                                                  | Offset error                                                |                                                 | -                               | ±1.0 | ±2.5          | LSB  | -                                                                                                |
|                                                                                  | Full-scale error                                            |                                                 | -                               | ±1.0 | ±2.5          | LSB  | -                                                                                                |
|                                                                                  | Absolute accuracy                                           |                                                 | -                               | ±2.0 | ±4.5          | LSB  | -                                                                                                |
|                                                                                  | DNL pseudo-differential nonlinearity error                  |                                                 | -                               | ±0.5 | ±1.5          | LSB  | -                                                                                                |
|                                                                                  | INL integral nonlinearity error                             |                                                 | -                               | ±1.0 | ±2.5          | LSB  | -                                                                                                |
| High-precision channels (AN007)                                                  | Conversion time* <sup>1</sup> (operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.75 (0.533)* <sup>2</sup>      | -    | -             | μs   | Sampling in 32 states                                                                            |
|                                                                                  | Offset error                                                |                                                 | -                               | ±1.0 | ±2.5          | LSB  | -                                                                                                |
|                                                                                  | Full-scale error                                            |                                                 | -                               | ±1.0 | ±2.5          | LSB  | -                                                                                                |
|                                                                                  | Absolute accuracy                                           |                                                 | -                               | ±2.0 | ±4.5          | LSB  | -                                                                                                |
|                                                                                  | DNL pseudo-differential nonlinearity error                  |                                                 | -                               | ±0.5 | ±1.5          | LSB  | -                                                                                                |
|                                                                                  | INL integral nonlinearity error                             |                                                 | -                               | ±1.0 | ±2.5          | LSB  | -                                                                                                |

**Table 2.27 A/D conversion characteristics for unit 0 (2 of 2)**

Conditions: PCLKC = 1 to 60 MHz

| Parameter                                            |                                                    |                                                    | Min            | Typ  | Max  | Unit | Test conditions       |
|------------------------------------------------------|----------------------------------------------------|----------------------------------------------------|----------------|------|------|------|-----------------------|
| Normal-precision channels<br>(AN016 to AN018, AN020) | Conversion time*1<br>(Operation at PCLKC = 60 MHz) | Permissible signal source impedance<br>Max. = 1 kΩ | 0.88 (0.667)*2 | -    | -    | μs   | Sampling in 40 states |
|                                                      | Offset error                                       |                                                    | -              | ±1.0 | ±5.5 | LSB  | -                     |
|                                                      | Full-scale error                                   |                                                    | -              | ±1.0 | ±5.5 | LSB  | -                     |
|                                                      | Absolute accuracy                                  |                                                    | -              | ±2.0 | ±7.5 | LSB  | -                     |
|                                                      | DNL pseudo-differential nonlinearity error         |                                                    | -              | ±0.5 | ±4.5 | LSB  | -                     |
|                                                      | INL integral nonlinearity error                    |                                                    | -              | ±1.0 | ±5.5 | LSB  | -                     |

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, the values might not fall within the indicated ranges.

The use of ports 0 as digital outputs is not allowed when the 12-bit A/D converter is used.

The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Note 3. When simultaneously using channel-dedicated sample-and-hold circuits in unit 0 and unit 1, see [Table 2.29](#).

**Table 2.28 A/D conversion characteristics for unit 1 (1 of 2)**

Conditions: PCLKC = 1 to 60 MHz

| Parameter                                                                 |                                                     |                                                    | Min                    | Typ  | Max          | Unit | Test conditions                                                                                                                                      |
|---------------------------------------------------------------------------|-----------------------------------------------------|----------------------------------------------------|------------------------|------|--------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| Frequency                                                                 |                                                     |                                                    | 1                      | -    | 60           | MHz  | -                                                                                                                                                    |
| Analog input capacitance                                                  |                                                     |                                                    | -                      | -    | 30           | pF   | -                                                                                                                                                    |
| Quantization error                                                        |                                                     |                                                    | -                      | ±0.5 | -            | LSB  | -                                                                                                                                                    |
| Resolution                                                                |                                                     |                                                    | -                      | -    | 12           | Bits | -                                                                                                                                                    |
| Channel-dedicated sample-and-hold circuits in use*3<br>(AN100 to AN102)   | Conversion time*1<br>(operation at PCLKC = 60 MHz)  | Permissible signal source impedance<br>Max. = 1 kΩ | 1.06<br>(0.4 + 0.25)*2 | -    | -            | μs   | <ul style="list-style-type: none"> <li>Sampling of channel-dedicated sample-and-hold circuits in 24 states</li> <li>Sampling in 15 states</li> </ul> |
|                                                                           | Offset error                                        |                                                    | -                      | ±1.5 | ±3.5         | LSB  | AN100 to AN102 = 0.25 V                                                                                                                              |
|                                                                           | Full-scale error                                    |                                                    | -                      | ±1.5 | ±3.5         | LSB  | AN100 to AN102 = VREFH - 0.25 V                                                                                                                      |
|                                                                           | Absolute accuracy                                   |                                                    | -                      | ±2.5 | ±5.5         | LSB  | -                                                                                                                                                    |
|                                                                           | DNL pseudo-differential nonlinearity error          |                                                    | -                      | ±1.0 | ±2.0         | LSB  | -                                                                                                                                                    |
|                                                                           | INL integral nonlinearity error                     |                                                    | -                      | ±1.5 | ±3.0         | LSB  | -                                                                                                                                                    |
|                                                                           | Holding characteristics of sample-and-hold circuits |                                                    | -                      | -    | 20           | μs   | -                                                                                                                                                    |
|                                                                           | Dynamic range                                       |                                                    | 0.25                   | -    | VREFH - 0.25 | V    | -                                                                                                                                                    |
| Channel-dedicated sample-and-hold circuits not in use<br>(AN100 to AN102) | Conversion time*1<br>(Operation at PCLKC = 60 MHz)  | Permissible signal source impedance<br>Max. = 1 kΩ | 0.48<br>(0.267)*2      | -    | -            | μs   | Sampling in 16 states                                                                                                                                |
|                                                                           | Offset error                                        |                                                    | -                      | ±1.0 | ±2.5         | LSB  | -                                                                                                                                                    |
|                                                                           | Full-scale error                                    |                                                    | -                      | ±1.0 | ±2.5         | LSB  | -                                                                                                                                                    |
|                                                                           | Absolute accuracy                                   |                                                    | -                      | ±2.0 | ±4.5         | LSB  | -                                                                                                                                                    |
|                                                                           | DNL pseudo-differential nonlinearity error          |                                                    | -                      | ±0.5 | ±1.5         | LSB  | -                                                                                                                                                    |
|                                                                           | INL integral nonlinearity error                     |                                                    | -                      | ±1.0 | ±2.5         | LSB  | -                                                                                                                                                    |

**Table 2.28 A/D conversion characteristics for unit 1 (2 of 2)**

Conditions: PCLKC = 1 to 60 MHz

| Parameter                                   |                                                    |                                                    | Min               | Typ  | Max  | Unit | Test conditions                                                              |
|---------------------------------------------|----------------------------------------------------|----------------------------------------------------|-------------------|------|------|------|------------------------------------------------------------------------------|
| High-precision channels<br>(AN105, AN106)   | Conversion time*1<br>(Operation at PCLKC = 60 MHz) | Permissible signal source impedance<br>Max. = 1 kΩ | 0.48<br>(0.267)*2 | -    | -    | μs   | Sampling in 16 states                                                        |
|                                             |                                                    | Max. = 400 Ω                                       | 0.40<br>(0.183)*2 | -    | -    | μs   | Sampling in 11 states<br>VCC = AVCC0 = 3.0 to 3.6 V<br>3.0 V ≤ VREFH ≤ AVCC0 |
|                                             | Offset error                                       |                                                    | -                 | ±1.0 | ±2.5 | LSB  | -                                                                            |
|                                             | Full-scale error                                   |                                                    | -                 | ±1.0 | ±2.5 | LSB  | -                                                                            |
|                                             | Absolute accuracy                                  |                                                    | -                 | ±2.0 | ±4.5 | LSB  | -                                                                            |
|                                             | DNL pseudo-differential nonlinearity error         |                                                    | -                 | ±0.5 | ±1.5 | LSB  | -                                                                            |
|                                             | INL integral nonlinearity error                    |                                                    | -                 | ±1.0 | ±2.5 | LSB  | -                                                                            |
| High-precision channels<br>(AN107)          | Conversion time*1<br>(Operation at PCLKC = 60 MHz) | Permissible signal source impedance<br>Max. = 1 kΩ | 0.75<br>(0.533)*2 | -    | -    | μs   | Sampling in 32 states                                                        |
|                                             |                                                    |                                                    |                   |      |      |      |                                                                              |
|                                             | Offset error                                       |                                                    | -                 | ±1.0 | ±2.5 | LSB  | -                                                                            |
|                                             | Full-scale error                                   |                                                    | -                 | ±1.0 | ±2.5 | LSB  | -                                                                            |
|                                             | Absolute accuracy                                  |                                                    | -                 | ±2.0 | ±4.5 | LSB  | -                                                                            |
|                                             | DNL pseudo-differential nonlinearity error         |                                                    | -                 | ±0.5 | ±1.5 | LSB  | -                                                                            |
| Normal-precision channels<br>(AN116, AN117) | Conversion time*1<br>(Operation at PCLKC = 60 MHz) | Permissible signal source impedance<br>Max. = 1 kΩ | 0.88<br>(0.667)*2 | -    | -    | μs   | Sampling in 40 states                                                        |
|                                             |                                                    |                                                    |                   |      |      |      |                                                                              |
|                                             | Offset error                                       |                                                    | -                 | ±1.0 | ±5.5 | LSB  | -                                                                            |
|                                             | Full-scale error                                   |                                                    | -                 | ±1.0 | ±5.5 | LSB  | -                                                                            |
|                                             | Absolute accuracy                                  |                                                    | -                 | ±2.0 | ±7.5 | LSB  | -                                                                            |
|                                             | DNL pseudo-differential nonlinearity error         |                                                    | -                 | ±0.5 | ±4.5 | LSB  | -                                                                            |
|                                             | INL integral nonlinearity error                    |                                                    | -                 | ±1.0 | ±5.5 | LSB  | -                                                                            |

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, the values might not fall within the indicated ranges.

The use of ports 0 as digital outputs is not allowed when the 12-bit A/D converter is used.

The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Note 3. When simultaneously using channel-dedicated sample-and-hold circuits in unit 0 and unit 1, see [Table 2.29](#).

**Table 2.29 A/D conversion characteristics for simultaneous use of channel-dedicated sample-and-hold circuits in unit 0 and unit 1**

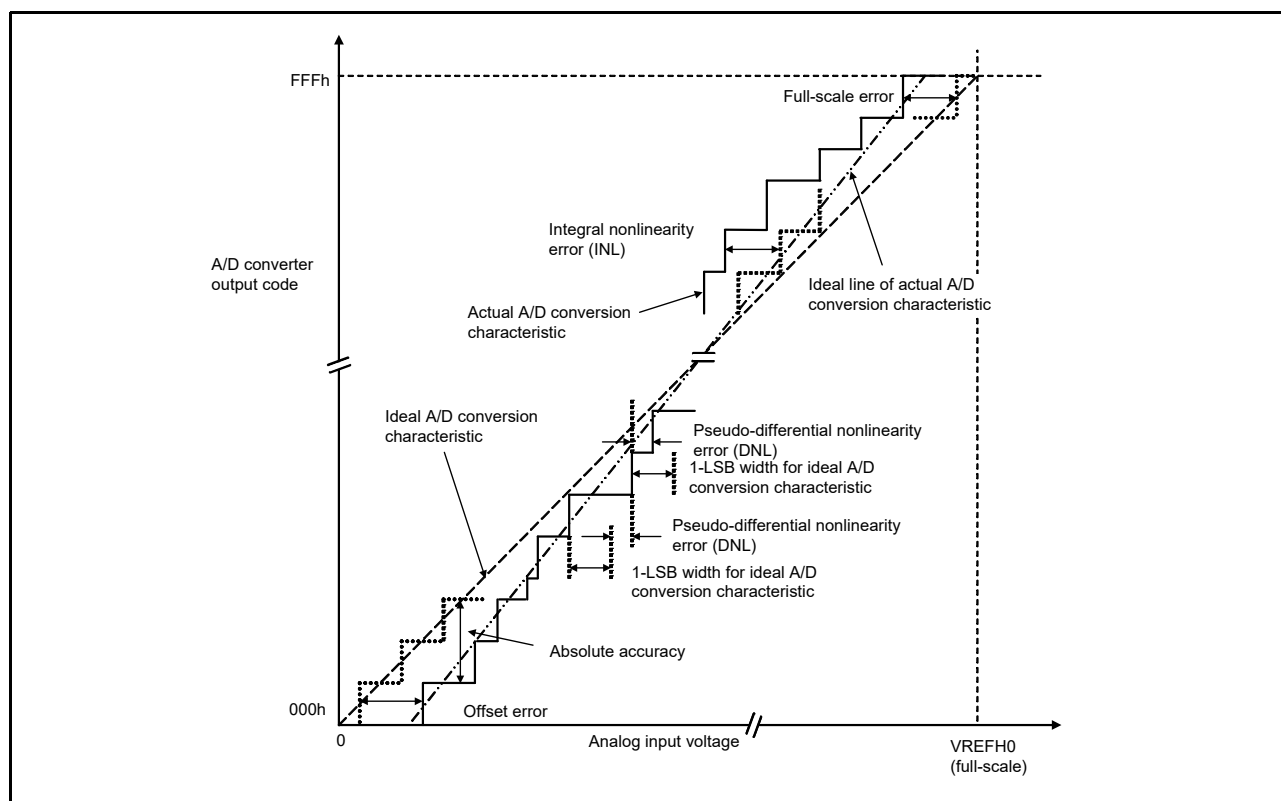
Conditions: PCLKC = 30/60 MHz

| Parameter                                                                                                    |                   | Min | Typ  | Max       | Test conditions                                                                                 |
|--------------------------------------------------------------------------------------------------------------|-------------------|-----|------|-----------|-------------------------------------------------------------------------------------------------|
| Channel-dedicated sample-and-hold circuits in use with continuous sampling function enabled (AN000 to AN002) | Offset error      | -   | ±1.5 | ±5.0      | <ul style="list-style-type: none"> <li>PCLKC = 60 MHz</li> <li>Sampling in 15 states</li> </ul> |
|                                                                                                              | Full-scale error  | -   | ±2.5 | ±5.0      |                                                                                                 |
|                                                                                                              | Absolute accuracy | -   | ±4.0 | ±8.0      |                                                                                                 |
| Channel-dedicated sample-and-hold circuits in use with continuous sampling function enabled (AN100 to AN102) | Offset error      | -   | ±1.5 | ±5.0      |                                                                                                 |
|                                                                                                              | Full-scale error  | -   | ±2.5 | ±5.0      |                                                                                                 |
|                                                                                                              | Absolute accuracy | -   | ±4.0 | ±8.0      |                                                                                                 |
| Channel-dedicated sample-and-hold circuits in use with continuous sampling function enabled (AN000 to AN002) | Offset error      | -   | ±1.5 | ±3.5      | <ul style="list-style-type: none"> <li>PCLKC = 30 MHz</li> <li>Sampling in 7 states</li> </ul>  |
|                                                                                                              | Full-scale error  | -   | ±1.5 | ±3.5      |                                                                                                 |
|                                                                                                              | Absolute accuracy | -   | ±3.0 | +4.5/-6.5 |                                                                                                 |
| Channel-dedicated sample-and-hold circuits in use with continuous sampling function enabled (AN100 to AN102) | Offset error      | -   | ±1.5 | ±3.5      |                                                                                                 |
|                                                                                                              | Full-scale error  | -   | ±1.5 | ±3.5      |                                                                                                 |
|                                                                                                              | Absolute accuracy | -   | ±3.0 | +4.5/-6.5 |                                                                                                 |

Note: When simultaneously using channel-dedicated sample-and-hold circuits in unit 0 and unit 1, setting the ADSHMSR.SHMD bit to 1 is recommended.

**Table 2.30 A/D internal reference voltage characteristics**

| Parameter                      | Min  | Typ  | Max  | Unit | Test conditions |
|--------------------------------|------|------|------|------|-----------------|
| A/D internal reference voltage | 1.13 | 1.18 | 1.23 | V    | -               |
| Sampling time                  | 4.15 | -    | -    | μs   | -               |



**Figure 2.43 Illustration of ADC12 characteristic terms**

### Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 is 3.072 V, then the 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of  $\pm 5$  LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

### Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

### Pseudo-differential nonlinearity error (DNL)

Pseudo-differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

### Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

**Full-scale error**

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

**2.5 DAC12 Characteristics****Table 2.31 D/A conversion characteristics**

| Parameter                | Min | Typ  | Max         | Unit | Test conditions                               |
|--------------------------|-----|------|-------------|------|-----------------------------------------------|
| Resolution               | -   | -    | 12          | Bits | -                                             |
| Without output amplifier |     |      |             |      |                                               |
| Absolute accuracy        | -   | -    | ±24         | LSB  | Resistive load 2 MΩ                           |
| INL                      | -   | ±2.0 | ±8.0        | LSB  | Resistive load 2 MΩ                           |
| DNL                      | -   | ±1.0 | ±2.0        | LSB  | -                                             |
| Output impedance         | -   | 8.5  | -           | kΩ   | -                                             |
| Conversion time          | -   | -    | 3.0         | μs   | Resistive load 2 MΩ,<br>Capacitive load 20 pF |
| Output voltage range     | 0   | -    | VREFH       | V    | -                                             |
| With output amplifier    |     |      |             |      |                                               |
| INL                      | -   | ±2.0 | ±4.0        | LSB  | -                                             |
| DNL                      | -   | ±1.0 | ±2.0        | LSB  | -                                             |
| Conversion time          | -   | -    | 4.0         | μs   | -                                             |
| Resistive load           | 5   | -    | -           | kΩ   | -                                             |
| Capacitive load          | -   | -    | 50          | pF   | -                                             |
| Output voltage range     | 0.2 | -    | VREFH - 0.2 | V    | -                                             |

**2.6 TSN Characteristics****Table 2.32 TSN characteristics**

| Parameter                     | Symbol             | Min  | Typ  | Max | Unit  | Test conditions |
|-------------------------------|--------------------|------|------|-----|-------|-----------------|
| Relative accuracy             | -                  | -    | ±1.0 | -   | °C    | -               |
| Temperature slope             | -                  | -    | 4.0  | -   | mV/°C | -               |
| Output voltage (at 25°C)      | -                  | -    | 1.24 | -   | V     | -               |
| Temperature sensor start time | t <sub>START</sub> | -    | -    | 30  | μs    | -               |
| Sampling time                 | -                  | 4.15 | -    | -   | μs    | -               |

**2.7 OSC Stop Detect Characteristics****Table 2.33 Oscillation stop detection circuit characteristics**

| Parameter      | Symbol          | Min | Typ | Max | Unit | Test conditions |
|----------------|-----------------|-----|-----|-----|------|-----------------|
| Detection time | t <sub>dr</sub> | -   | -   | 1   | ms   | Figure 2.44     |

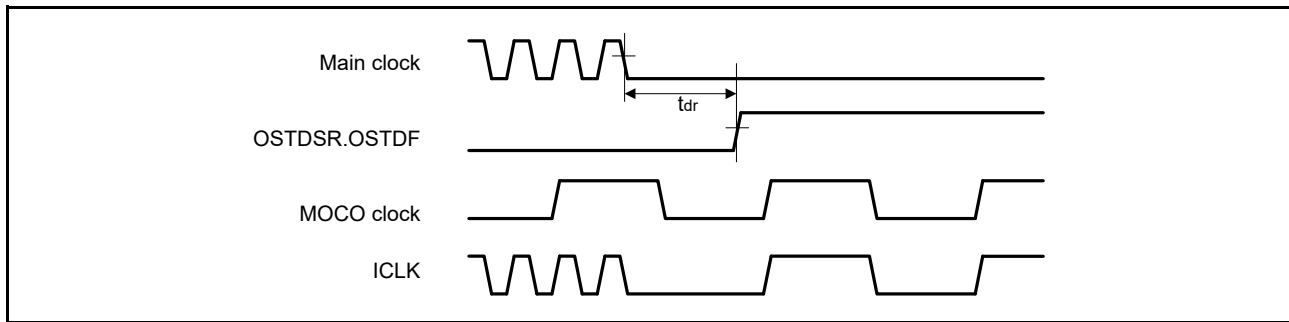


Figure 2.44 Oscillation stop detection timing

## 2.8 POR and LVD Characteristics

Table 2.34 Power-on reset circuit and voltage detection circuit characteristics

| Parameter                                               |                                  |                                   | Symbol              | Min  | Typ  | Max  | Unit | Test conditions            |
|---------------------------------------------------------|----------------------------------|-----------------------------------|---------------------|------|------|------|------|----------------------------|
| Voltage detection level                                 | Power-on reset (POR)             | DPSBYCR.DEEPCUT[1:0] = 00b or 01b | V <sub>POR</sub>    | 2.5  | 2.6  | 2.7  | V    | Figure 2.45                |
|                                                         |                                  | DPSBYCR.DEEPCUT[1:0] = 11b        |                     | 1.8  | 2.25 | 2.7  |      |                            |
|                                                         | Voltage detection circuit (LVD0) |                                   | V <sub>det0_1</sub> | 2.84 | 2.94 | 3.04 |      | Figure 2.46                |
|                                                         |                                  |                                   | V <sub>det0_2</sub> | 2.77 | 2.87 | 2.97 |      |                            |
|                                                         |                                  |                                   | V <sub>det0_3</sub> | 2.70 | 2.80 | 2.90 |      |                            |
|                                                         | Voltage detection circuit (LVD1) |                                   | V <sub>det1_1</sub> | 2.89 | 2.99 | 3.09 |      | Figure 2.47                |
|                                                         |                                  |                                   | V <sub>det1_2</sub> | 2.82 | 2.92 | 3.02 |      |                            |
|                                                         |                                  |                                   | V <sub>det1_3</sub> | 2.75 | 2.85 | 2.95 |      |                            |
|                                                         | Voltage detection circuit (LVD2) |                                   | V <sub>det2_1</sub> | 2.89 | 2.99 | 3.09 |      | Figure 2.48                |
|                                                         |                                  |                                   | V <sub>det2_2</sub> | 2.82 | 2.92 | 3.02 |      |                            |
|                                                         |                                  |                                   | V <sub>det2_3</sub> | 2.75 | 2.85 | 2.95 |      |                            |
| Internal reset time                                     | Power-on reset time              |                                   | t <sub>POR</sub>    | -    | 4.5  | -    | ms   | Figure 2.45                |
|                                                         | LVD0 reset time                  |                                   | t <sub>LVD0</sub>   | -    | 0.51 | -    |      | Figure 2.46                |
|                                                         | LVD1 reset time                  |                                   | t <sub>LVD1</sub>   | -    | 0.38 | -    |      | Figure 2.47                |
|                                                         | LVD2 reset time                  |                                   | t <sub>LVD2</sub>   | -    | 0.38 | -    |      | Figure 2.48                |
| Minimum VCC down time*1                                 |                                  |                                   | t <sub>VOFF</sub>   | 200  | -    | -    | μs   | Figure 2.45, Figure 2.46   |
| Response delay                                          |                                  |                                   | t <sub>det</sub>    | -    | -    | 200  | μs   | Figure 2.45 to Figure 2.48 |
| LVD operation stabilization time (after LVD is enabled) |                                  |                                   | t <sub>d(E-A)</sub> | -    | -    | 10   | μs   | Figure 2.47, Figure 2.48   |
| Hysteresis width (LVD1 and LVD2)                        |                                  |                                   | V <sub>LVH</sub>    | -    | 70   | -    | mV   |                            |

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels  $V_{POR}$ ,  $V_{det1}$ , and  $V_{det2}$  for POR and LVD.

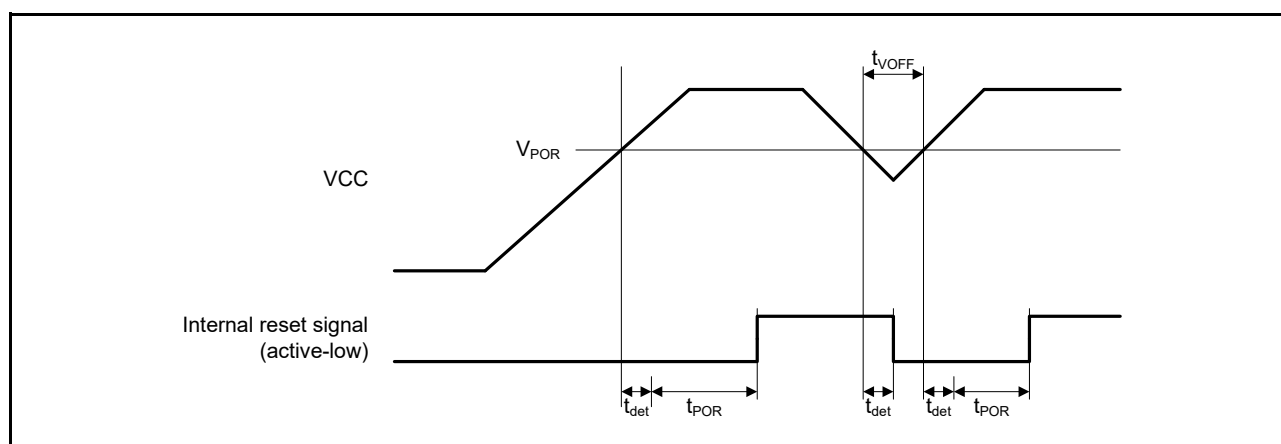
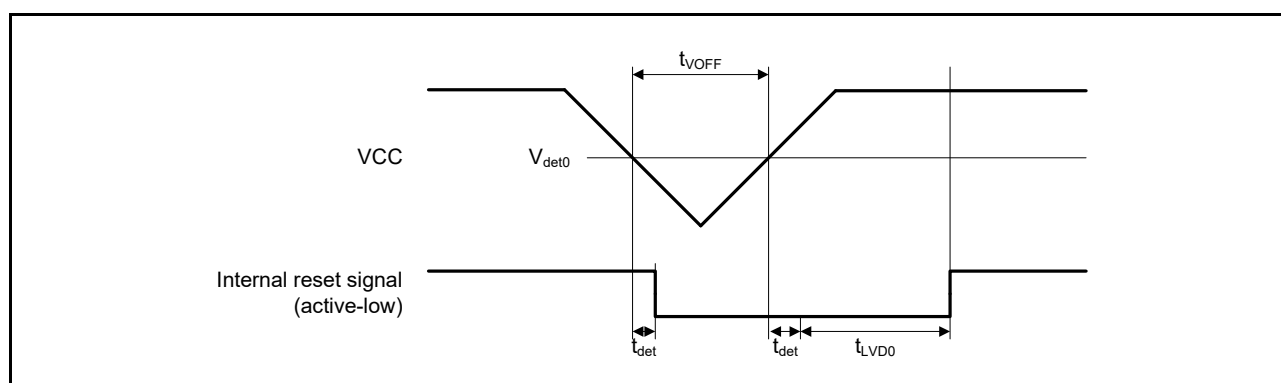


Figure 2.45 Power-on reset timing

Figure 2.46 Voltage detection circuit timing ( $V_{det0}$ )

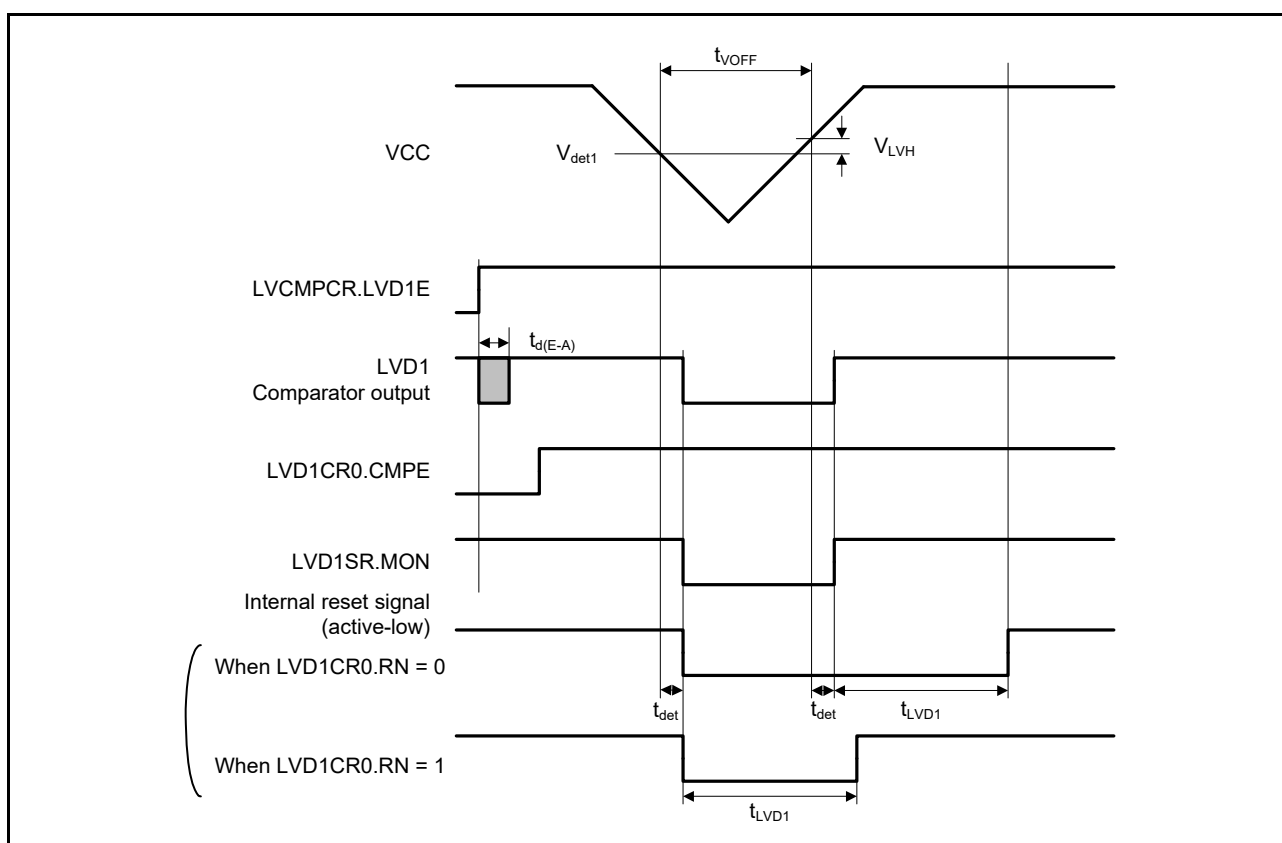


Figure 2.47 Voltage detection circuit timing (V<sub>det1</sub>)

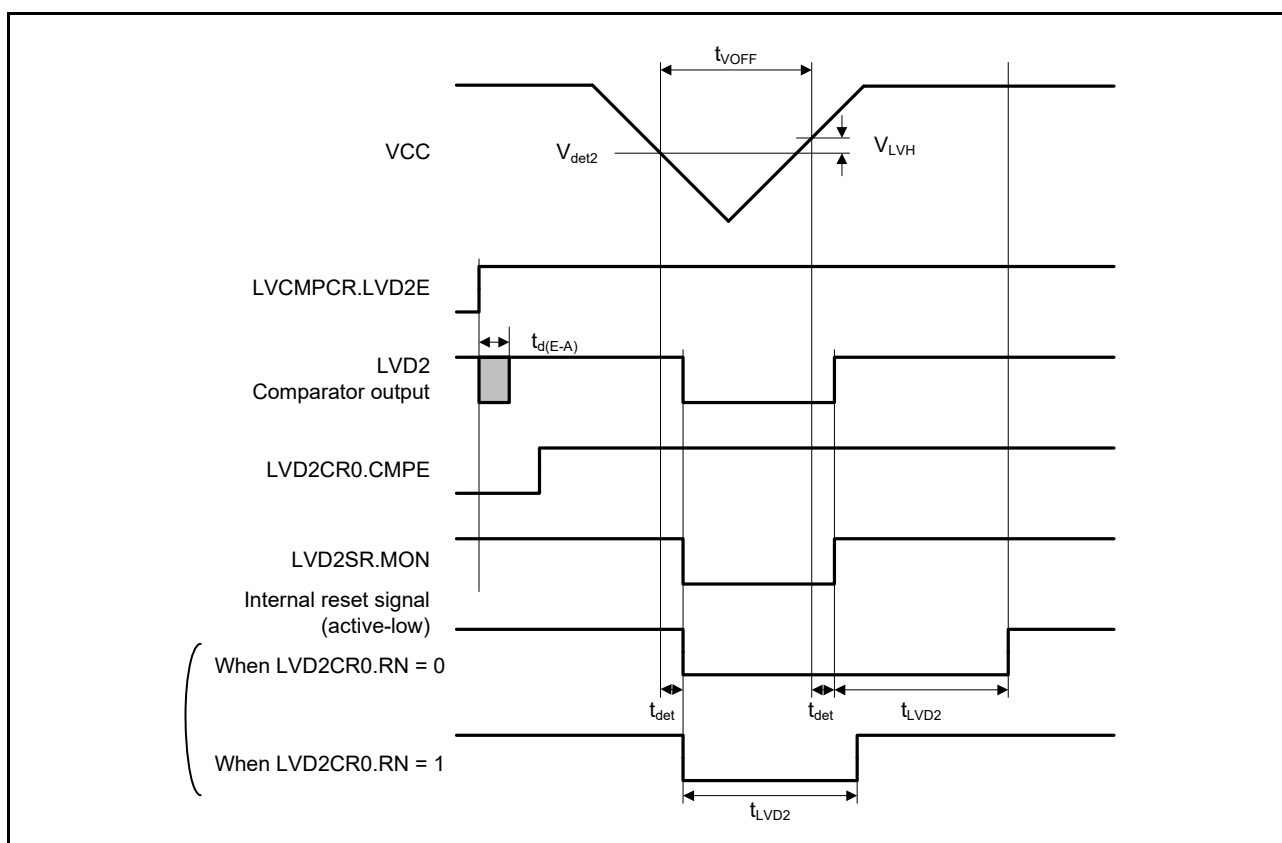


Figure 2.48 Voltage detection circuit timing (V<sub>det2</sub>)

## 2.9 ACMPHS Characteristics

**Table 2.35 ACMPHS characteristics**

| Parameter                  | Symbol | Min  | Typ  | Max   | Unit | Test conditions    |
|----------------------------|--------|------|------|-------|------|--------------------|
| Reference voltage range    | VREF   | 0    | -    | AVCC0 | V    | -                  |
| Input voltage range        | VI     | 0    | -    | AVCC0 | V    | -                  |
| Output delay*1             | Td     | -    | 50   | 100   | ns   | VI = VREF ± 100 mV |
| Internal reference voltage | Vref   | 1.13 | 1.18 | 1.23  | V    | -                  |

Note 1. This value is the internal propagation delay.

## 2.10 PGA Characteristics

**Table 2.36 PGA characteristics in single mode**

| Parameter                  | Symbol              | Min                         | Typ | Max                         | Unit |
|----------------------------|---------------------|-----------------------------|-----|-----------------------------|------|
| PGAVSS input voltage range | PGAVSS              | 0                           | -   | 0                           | V    |
|                            | AIN0 (G = 2.000)    | $0.050 \times \text{AVCC0}$ | -   | $0.45 \times \text{AVCC0}$  | V    |
|                            | AIN1 (G = 2.500)    | $0.047 \times \text{AVCC0}$ | -   | $0.360 \times \text{AVCC0}$ | V    |
|                            | AIN2 (G = 2.667)    | $0.046 \times \text{AVCC0}$ | -   | $0.337 \times \text{AVCC0}$ | V    |
|                            | AIN3 (G = 2.857)    | $0.046 \times \text{AVCC0}$ | -   | $0.32 \times \text{AVCC0}$  | V    |
|                            | AIN4 (G = 3.077)    | $0.045 \times \text{AVCC0}$ | -   | $0.292 \times \text{AVCC0}$ | V    |
|                            | AIN5 (G = 3.333)    | $0.044 \times \text{AVCC0}$ | -   | $0.265 \times \text{AVCC0}$ | V    |
|                            | AIN6 (G = 3.636)    | $0.042 \times \text{AVCC0}$ | -   | $0.247 \times \text{AVCC0}$ | V    |
|                            | AIN7 (G = 4.000)    | $0.040 \times \text{AVCC0}$ | -   | $0.212 \times \text{AVCC0}$ | V    |
|                            | AIN8 (G = 4.444)    | $0.036 \times \text{AVCC0}$ | -   | $0.191 \times \text{AVCC0}$ | V    |
|                            | AIN9 (G = 5.000)    | $0.033 \times \text{AVCC0}$ | -   | $0.17 \times \text{AVCC0}$  | V    |
|                            | AIN10 (G = 5.714)   | $0.031 \times \text{AVCC0}$ | -   | $0.148 \times \text{AVCC0}$ | V    |
|                            | AIN11 (G = 6.667)   | $0.029 \times \text{AVCC0}$ | -   | $0.127 \times \text{AVCC0}$ | V    |
|                            | AIN12 (G = 8.000)   | $0.027 \times \text{AVCC0}$ | -   | $0.09 \times \text{AVCC0}$  | V    |
|                            | AIN13 (G = 10.000)  | $0.025 \times \text{AVCC0}$ | -   | $0.08 \times \text{AVCC0}$  | V    |
|                            | AIN14 (G = 13.333)  | $0.023 \times \text{AVCC0}$ | -   | $0.06 \times \text{AVCC0}$  | V    |
| Gain error                 | Gerr0 (G = 2.000)   | -1.0                        | -   | 1.0                         | %    |
|                            | Gerr1 (G = 2.500)   | -1.0                        | -   | 1.0                         | %    |
|                            | Gerr2 (G = 2.667)   | -1.0                        | -   | 1.0                         | %    |
|                            | Gerr3 (G = 2.857)   | -1.0                        | -   | 1.0                         | %    |
|                            | Gerr4 (G = 3.077)   | -1.0                        | -   | 1.0                         | %    |
|                            | Gerr5 (G = 3.333)   | -1.5                        | -   | 1.5                         | %    |
|                            | Gerr6 (G = 3.636)   | -1.5                        | -   | 1.5                         | %    |
|                            | Gerr7 (G = 4.000)   | -1.5                        | -   | 1.5                         | %    |
|                            | Gerr8 (G = 4.444)   | -2.0                        | -   | 2.0                         | %    |
|                            | Gerr9 (G = 5.000)   | -2.0                        | -   | 2.0                         | %    |
|                            | Gerr10 (G = 5.714)  | -2.0                        | -   | 2.0                         | %    |
|                            | Gerr11 (G = 6.667)  | -2.0                        | -   | 2.0                         | %    |
|                            | Gerr12 (G = 8.000)  | -2.0                        | -   | 2.0                         | %    |
|                            | Gerr13 (G = 10.000) | -2.0                        | -   | 2.0                         | %    |
|                            | Gerr14 (G = 13.333) | -2.0                        | -   | 2.0                         | %    |
| Offset error               | Voff                | -8                          | -   | 8                           | mV   |

**Table 2.37 PGA characteristics in pseudo-differential mode**

| Parameter                               |           | Symbol     | Min   | Typ | Max  | Unit |
|-----------------------------------------|-----------|------------|-------|-----|------|------|
| PGAVSS input voltage range              |           | PGAVSS     | -0.5  | -   | 0.3  | V    |
| Pseudo-differential input voltage range | G = 1.500 | AIN-PGAVSS | -0.5  | -   | 0.5  | V    |
|                                         | G = 2.333 |            | -0.4  | -   | 0.4  | V    |
|                                         | G = 4.000 |            | -0.2  | -   | 0.2  | V    |
|                                         | G = 5.667 |            | -0.15 | -   | 0.15 | V    |
| Gain error                              | G = 1.500 | Gerr       | -1.0  | -   | 1.0  | %    |
|                                         | G = 2.333 |            | -1.0  | -   | 1.0  |      |
|                                         | G = 4.000 |            | -1.0  | -   | 1.0  |      |
|                                         | G = 5.667 |            | -1.0  | -   | 1.0  |      |

## 2.11 Flash Memory Characteristics

### 2.11.1 Code Flash Memory Characteristics

**Table 2.38 Code flash memory characteristics**

Conditions: Program or erase: FCLK = 4 to 60 MHz

Read: FCLK ≤ 60 MHz

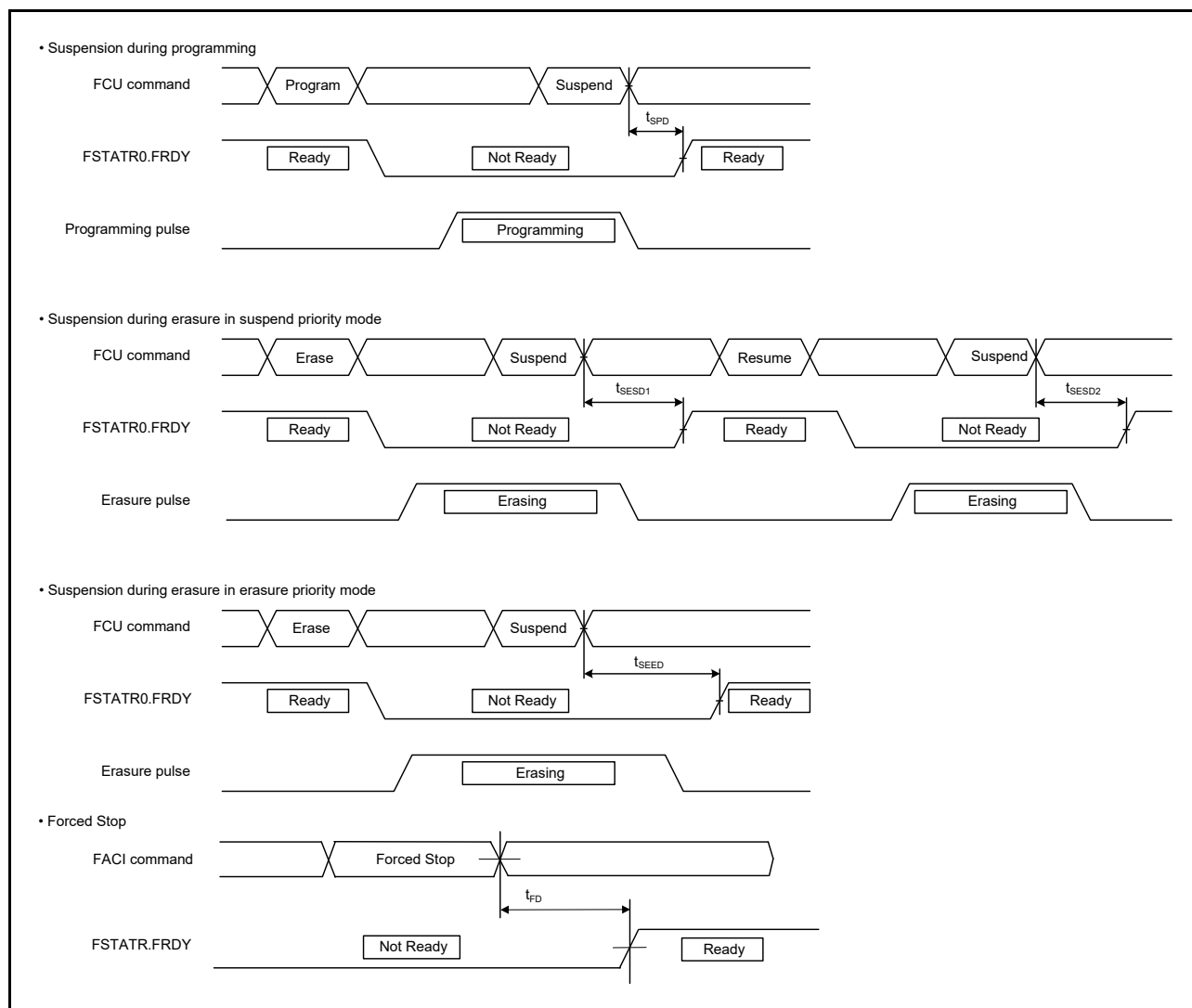
| Parameter                                                  |          | Symbol      | FCLK = 4 MHz |      |      | 20 MHz ≤ FCLK ≤ 60 MHz |      |     | Unit  | Test conditions |
|------------------------------------------------------------|----------|-------------|--------------|------|------|------------------------|------|-----|-------|-----------------|
|                                                            |          |             | Min          | Typ  | Max  | Min                    | Typ  | Max |       |                 |
| Programming time<br>$N_{PEC} \leq 100$ times               | 128-byte | $t_{P128}$  | -            | 0.75 | 13.2 | -                      | 0.34 | 6.0 | ms    |                 |
|                                                            | 8-KB     | $t_{P8K}$   | -            | 49   | 176  | -                      | 22   | 80  | ms    |                 |
|                                                            | 32-KB    | $t_{P32K}$  | -            | 194  | 704  | -                      | 88   | 320 | ms    |                 |
| Programming time<br>$N_{PEC} > 100$ times                  | 128-byte | $t_{P128}$  | -            | 0.91 | 15.8 | -                      | 0.41 | 7.2 | ms    |                 |
|                                                            | 8-KB     | $t_{P8K}$   | -            | 60   | 212  | -                      | 27   | 96  | ms    |                 |
|                                                            | 32-KB    | $t_{P32K}$  | -            | 234  | 848  | -                      | 106  | 384 | ms    |                 |
| Erase time<br>$N_{PEC} \leq 100$ times                     | 8-KB     | $t_{E8K}$   | -            | 78   | 216  | -                      | 43   | 120 | ms    |                 |
|                                                            | 32-KB    | $t_{E32K}$  | -            | 283  | 864  | -                      | 157  | 480 | ms    |                 |
| Erase time<br>$N_{PEC} > 100$ times                        | 8-KB     | $t_{E8K}$   | -            | 94   | 260  | -                      | 52   | 144 | ms    |                 |
|                                                            | 32-KB    | $t_{E32K}$  | -            | 341  | 1040 | -                      | 189  | 576 | ms    |                 |
| Reprogramming/erase cycle*4                                |          | $N_{PEC}$   | 10000*1      | -    | -    | 10000*1                | -    | -   | Times |                 |
| Suspend delay during programming                           |          | $t_{SPD}$   | -            | -    | 264  | -                      | -    | 120 | μs    |                 |
| First suspend delay during erase in suspend priority mode  |          | $t_{SESD1}$ | -            | -    | 216  | -                      | -    | 120 | μs    |                 |
| Second suspend delay during erase in suspend priority mode |          | $t_{SESD2}$ | -            | -    | 1.7  | -                      | -    | 1.7 | ms    |                 |
| Suspend delay during erase in erase priority mode          |          | $t_{SEED}$  | -            | -    | 1.7  | -                      | -    | 1.7 | ms    |                 |
| Forced stop command                                        |          | $t_{FD}$    | -            | -    | 32   | -                      | -    | 20  | μs    |                 |
| Data hold time*2                                           |          | $t_{DRP}$   | 10*2, *3     | -    | -    | 10*2, *3               | -    | -   | Years | Ta = +85°C      |
|                                                            |          |             | 30*2, *3     | -    | -    | 30*2, *3               | -    | -   |       |                 |

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 3. This result is obtained from reliability testing.

Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times ( $n = 10000$ ), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.



**Figure 2.49** Suspension and forced stop timing for flash memory programming and erasure

## 2.11.2 Data Flash Memory Characteristics

**Table 2.39 Data flash memory characteristics**

Conditions: Program or erase: FCLK = 4 to 60 MHz

Read: FCLK ≤ 60 MHz

| Parameter                                                    |          | Symbol              | FCLK = 4 MHz |      |     | 20 MHz ≤ FCLK ≤ 60 MHz |      |     | Unit | Test conditions |
|--------------------------------------------------------------|----------|---------------------|--------------|------|-----|------------------------|------|-----|------|-----------------|
|                                                              |          |                     | Min          | Typ  | Max | Min                    | Typ  | Max |      |                 |
| Programming time                                             | 4-byte   | t <sub>DP4</sub>    | -            | 0.36 | 3.8 | -                      | 0.16 | 1.7 | ms   |                 |
|                                                              | 8-byte   | t <sub>DP8</sub>    | -            | 0.38 | 4.0 | -                      | 0.17 | 1.8 |      |                 |
|                                                              | 16-byte  | t <sub>DP16</sub>   | -            | 0.42 | 4.5 | -                      | 0.19 | 2.0 |      |                 |
| Erasure time                                                 | 64-byte  | t <sub>DE64</sub>   | -            | 3.1  | 18  | -                      | 1.7  | 10  | ms   |                 |
|                                                              | 128-byte | t <sub>DE128</sub>  | -            | 4.7  | 27  | -                      | 2.6  | 15  |      |                 |
|                                                              | 256-byte | t <sub>DE256</sub>  | -            | 8.9  | 50  | -                      | 4.9  | 28  |      |                 |
| Blank check time                                             | 4-byte   | t <sub>DBC4</sub>   | -            | -    | 84  | -                      | -    | 30  | μs   |                 |
| Reprogramming/erase cycle*1                                  |          | N <sub>DPEC</sub>   | 125000*2     | -    | -   | 125000*2               | -    | -   | -    |                 |
| Suspend delay during programming                             | 4-byte   | t <sub>DSPD</sub>   | -            | -    | 264 | -                      | -    | 120 | μs   |                 |
|                                                              | 8-byte   |                     | -            | -    | 264 | -                      | -    | 120 |      |                 |
|                                                              | 16-byte  |                     | -            | -    | 264 | -                      | -    | 120 |      |                 |
| First suspend delay during erasure in suspend priority mode  | 64-byte  | t <sub>DSESD1</sub> | -            | -    | 216 | -                      | -    | 120 | μs   |                 |
|                                                              | 128-byte |                     | -            | -    | 216 | -                      | -    | 120 |      |                 |
|                                                              | 256-byte |                     | -            | -    | 216 | -                      | -    | 120 |      |                 |
| Second suspend delay during erasure in suspend priority mode | 64-byte  | t <sub>DSESD2</sub> | -            | -    | 300 | -                      | -    | 300 | μs   |                 |
|                                                              | 128-byte |                     | -            | -    | 390 | -                      | -    | 390 |      |                 |
|                                                              | 256-byte |                     | -            | -    | 570 | -                      | -    | 570 |      |                 |
| Suspend delay during erasing in erasure priority mode        | 64-byte  | t <sub>DSEED</sub>  | -            | -    | 300 | -                      | -    | 300 | μs   |                 |
|                                                              | 128-byte |                     | -            | -    | 390 | -                      | -    | 390 |      |                 |
|                                                              | 256-byte |                     | -            | -    | 570 | -                      | -    | 570 |      |                 |
| Forced stop command                                          |          | t <sub>FD</sub>     | -            | -    | 32  | -                      | -    | 20  | μs   |                 |
| Data hold time*3                                             |          | t <sub>DRP</sub>    | 10*3,*4      | -    | -   | 10*3,*4                | -    | -   | Year |                 |
|                                                              |          |                     | 30*3,*4      | -    | -   | 30*3,*4                | -    | -   |      | Ta = +85°C      |

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 4. This result is obtained from reliability testing.

## 2.12 Boundary Scan

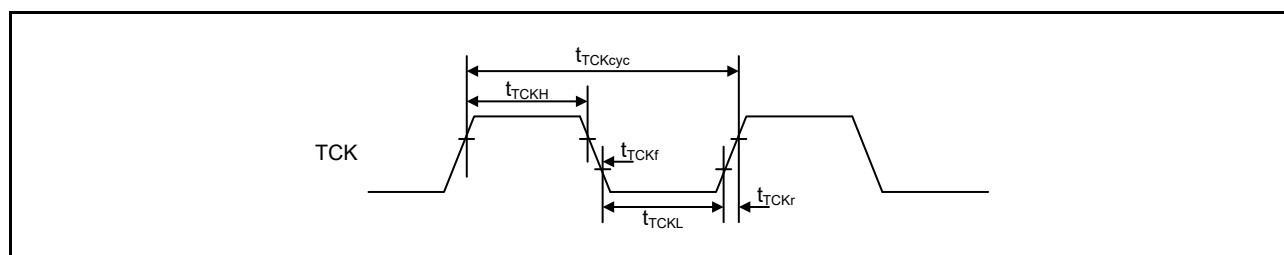
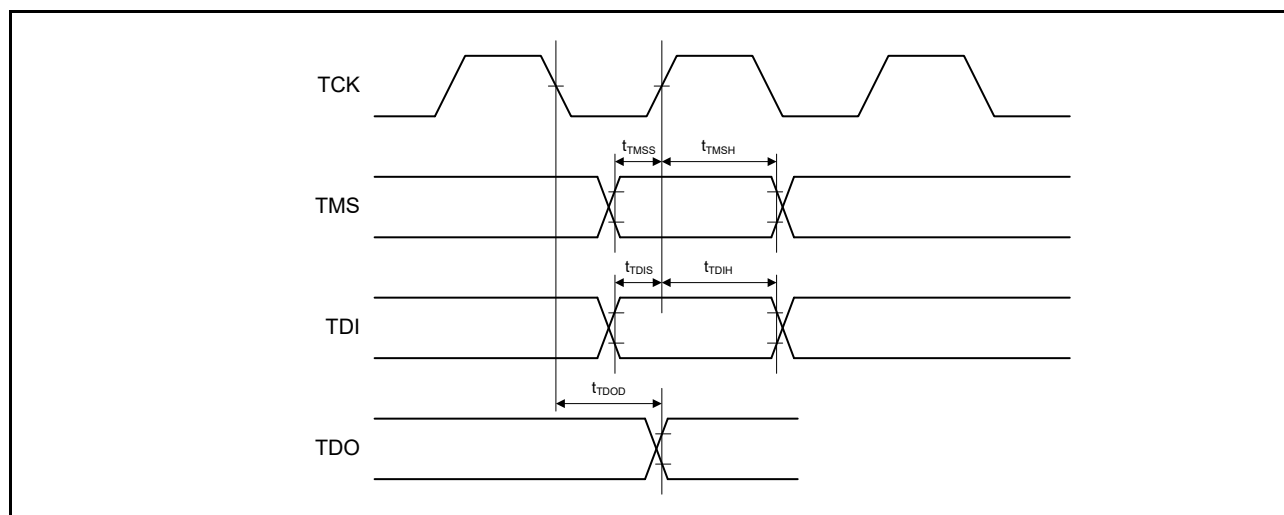
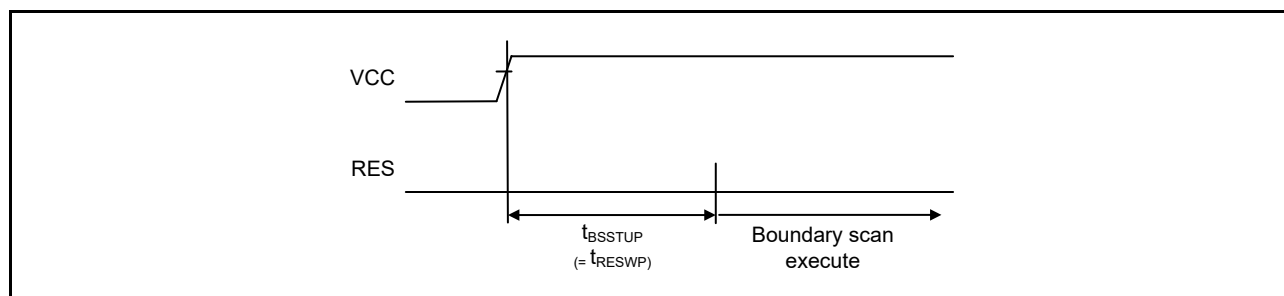
**Table 2.40 Boundary scan characteristics (1 of 2)**

| Parameter                  | Symbol              | Min | Typ | Max | Unit | Test conditions |
|----------------------------|---------------------|-----|-----|-----|------|-----------------|
| TCK clock cycle time       | t <sub>TCKcyc</sub> | 100 | -   | -   | ns   | Figure 2.50     |
| TCK clock high pulse width | t <sub>TCKH</sub>   | 45  | -   | -   | ns   |                 |
| TCK clock low pulse width  | t <sub>TCKL</sub>   | 45  | -   | -   | ns   |                 |
| TCK clock rise time        | t <sub>TCKr</sub>   | -   | -   | 5   | ns   |                 |
| TCK clock fall time        | t <sub>TCKf</sub>   | -   | -   | 5   | ns   |                 |

**Table 2.40 Boundary scan characteristics (2 of 2)**

| Parameter                            | Symbol       | Min         | Typ | Max | Unit | Test conditions |
|--------------------------------------|--------------|-------------|-----|-----|------|-----------------|
| TMS setup time                       | $t_{TMSS}$   | 20          | -   | -   | ns   | Figure 2.51     |
| TMS hold time                        | $t_{TMSH}$   | 20          | -   | -   | ns   |                 |
| TDI setup time                       | $t_{TDIS}$   | 20          | -   | -   | ns   |                 |
| TDI hold time                        | $t_{TDIH}$   | 20          | -   | -   | ns   |                 |
| TDO data delay                       | $t_{TDOD}$   | -           | -   | 40  | ns   |                 |
| Boundary scan circuit startup time*1 | $T_{BSSTUP}$ | $t_{RESWP}$ | -   | -   | -    | Figure 2.52     |

Note 1. Boundary scan does not function until the power-on reset becomes negative.

**Figure 2.50 Boundary scan TCK timing****Figure 2.51 Boundary scan input/output timing****Figure 2.52 Boundary scan circuit startup timing**

## 2.13 Joint Test Action Group (JTAG)

Table 2.41 JTAG

| Parameter                  | Symbol       | Min | Typ | Max | Unit | Test conditions |
|----------------------------|--------------|-----|-----|-----|------|-----------------|
| TCK clock cycle time       | $t_{TCKcyc}$ | 40  | -   | -   | ns   | Figure 2.50     |
| TCK clock high pulse width | $t_{TCKH}$   | 15  | -   | -   | ns   |                 |
| TCK clock low pulse width  | $t_{TCKL}$   | 15  | -   | -   | ns   |                 |
| TCK clock rise time        | $t_{TCKr}$   | -   | -   | 5   | ns   |                 |
| TCK clock fall time        | $t_{TCKf}$   | -   | -   | 5   | ns   |                 |
| TMS setup time             | $t_{TMSS}$   | 8   | -   | -   | ns   | Figure 2.51     |
| TMS hold time              | $t_{TMSh}$   | 8   | -   | -   | ns   |                 |
| TDI setup time             | $t_{TDis}$   | 8   | -   | -   | ns   |                 |
| TDI hold time              | $t_{TDIH}$   | 8   | -   | -   | ns   |                 |
| TDO data delay time        | $t_{TDOD}$   | -   | -   | 20  | ns   |                 |

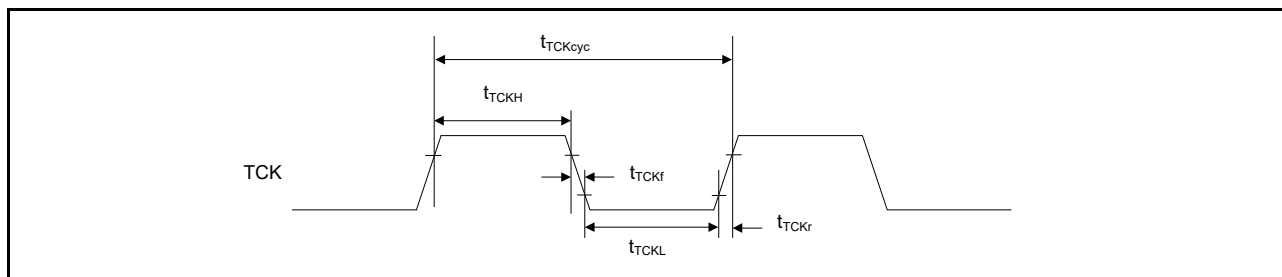


Figure 2.53 JTAG TCK timing

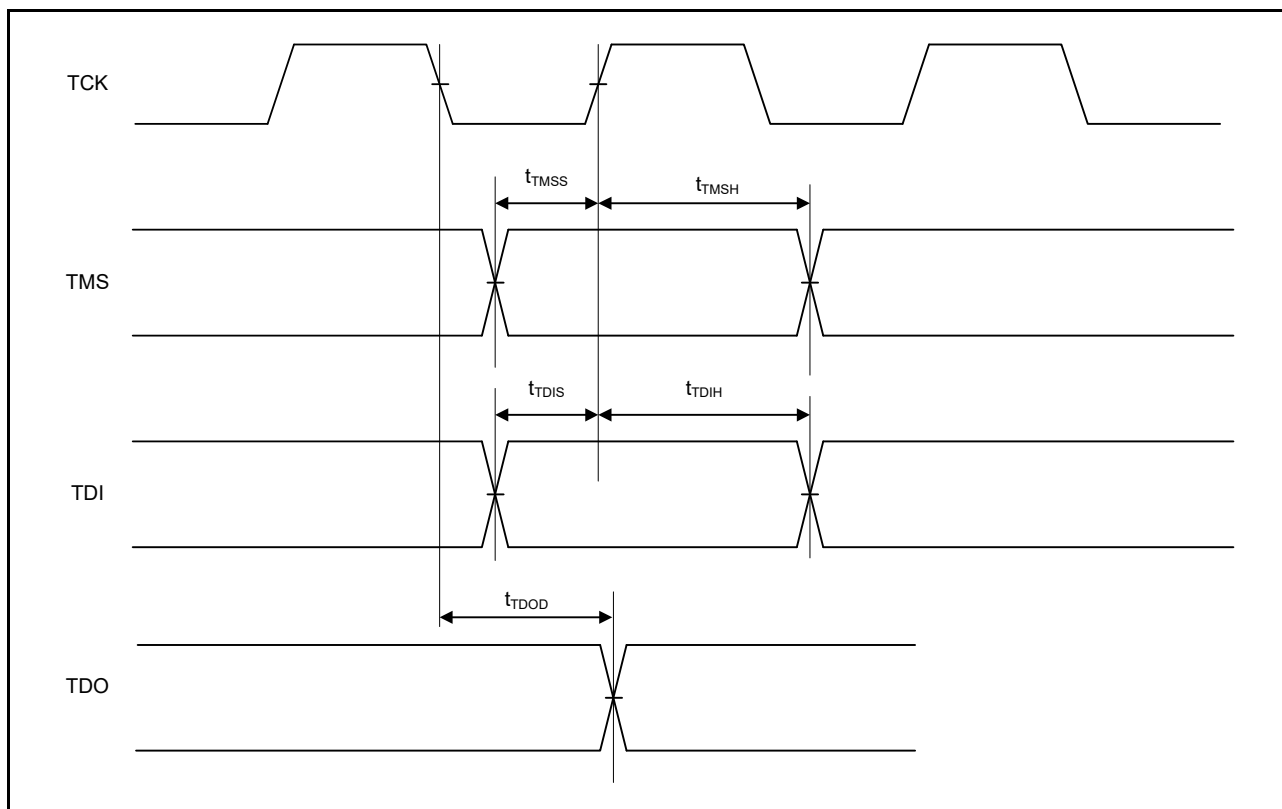


Figure 2.54 JTAG input/output timing

## 2.14 Serial Wire Debug (SWD)

Table 2.42 SWD

| Parameter                    | Symbol                | Min | Typ | Max | Unit | Test conditions |
|------------------------------|-----------------------|-----|-----|-----|------|-----------------|
| SWCLK clock cycle time       | $t_{\text{SWCLKcyc}}$ | 40  | -   | -   | ns   | Figure 2.55     |
| SWCLK clock high pulse width | $t_{\text{SWCKH}}$    | 15  | -   | -   | ns   |                 |
| SWCLK clock low pulse width  | $t_{\text{SWCKL}}$    | 15  | -   | -   | ns   |                 |
| SWCLK clock rise time        | $t_{\text{SWCKr}}$    | -   | -   | 5   | ns   |                 |
| SWCLK clock fall time        | $t_{\text{SWCKf}}$    | -   | -   | 5   | ns   |                 |
| SWDIO setup time             | $t_{\text{SWDS}}$     | 8   | -   | -   | ns   | Figure 2.56     |
| SWDIO hold time              | $t_{\text{SWDH}}$     | 8   | -   | -   | ns   |                 |
| SWDIO data delay time        | $t_{\text{SWDD}}$     | 2   | -   | 28  | ns   |                 |

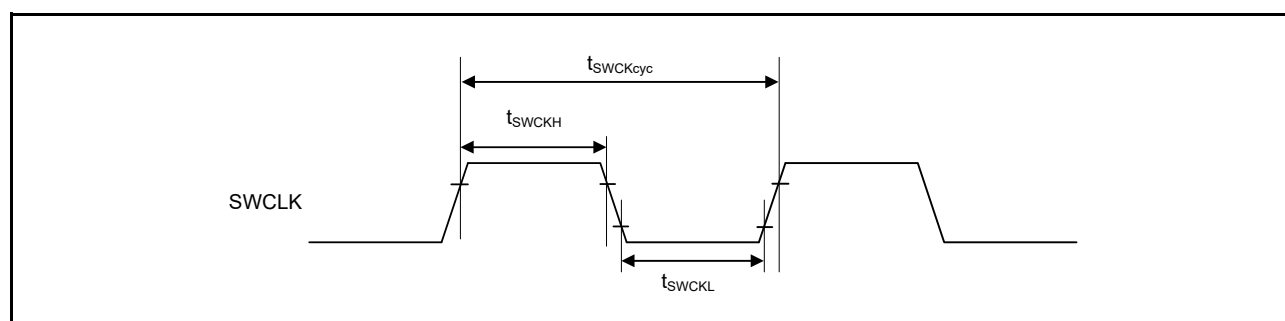


Figure 2.55 SWD SWCLK timing

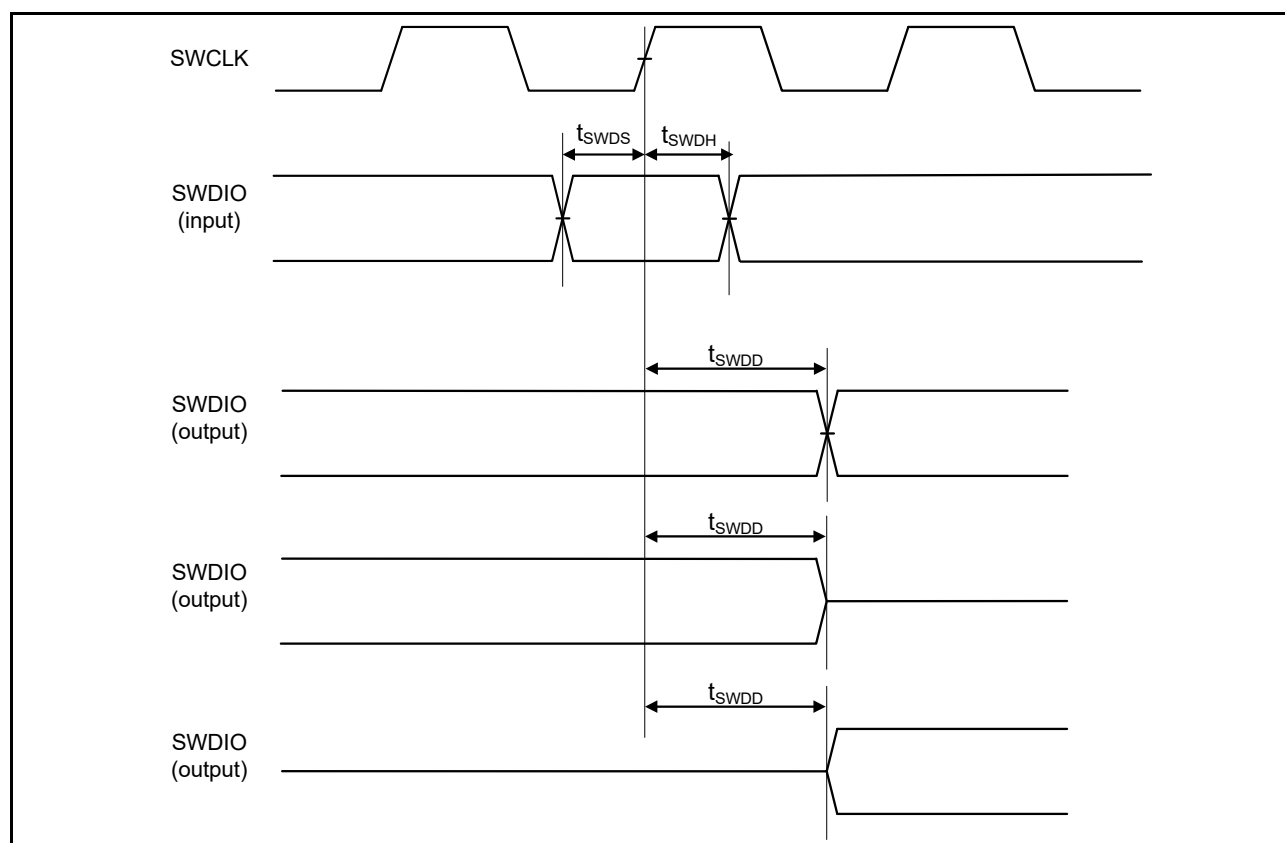


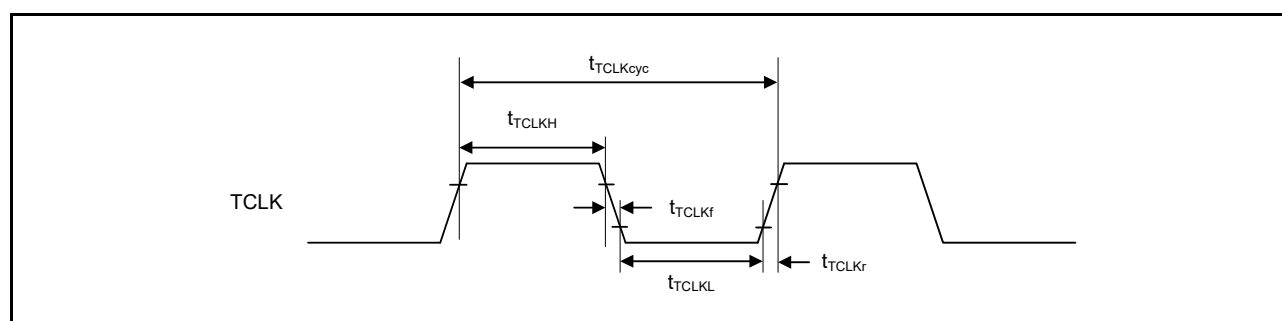
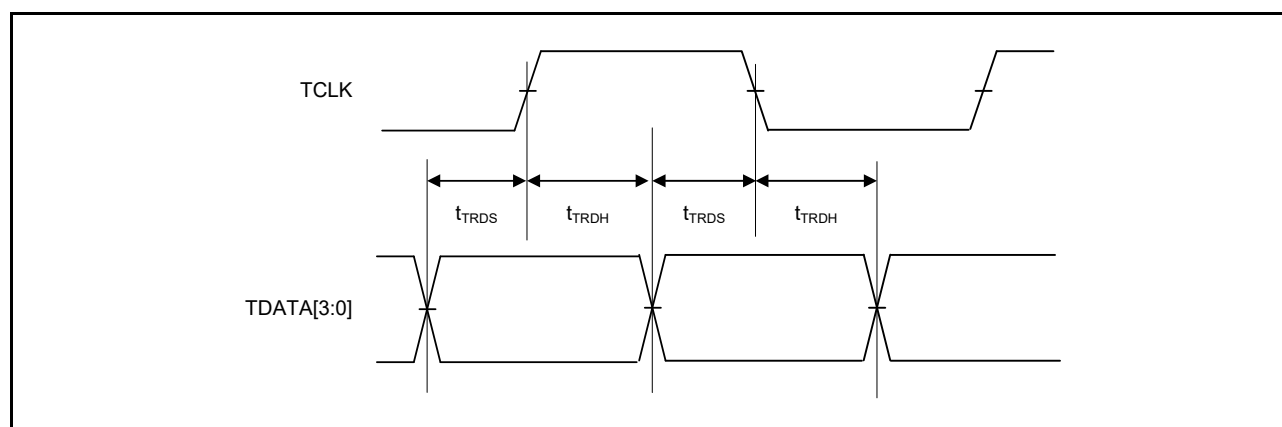
Figure 2.56 SWD input/output timing

## 2.15 Embedded Trace Macro Interface (ETM)

**Table 2.43 ETM**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter                    | Symbol           | Min  | Typ | Max | Unit | Test conditions |
|------------------------------|------------------|------|-----|-----|------|-----------------|
| TCLK clock cycle time        | $t_{TCLK_{cyc}}$ | 33.3 | -   | -   | ns   | Figure 2.57     |
| TCLK clock high pulse width  | $t_{TCLKH}$      | 13.6 | -   | -   | ns   |                 |
| TCLK clock low pulse width   | $t_{TCLKL}$      | 13.6 | -   | -   | ns   |                 |
| TCLK clock rise time         | $t_{TCLKr}$      | -    | -   | 3   | ns   |                 |
| TCLK clock fall time         | $t_{TCLKf}$      | -    | -   | 3   | ns   |                 |
| TDATA[3:0] output setup time | $t_{TRDS}$       | 3.5  | -   | -   | ns   | Figure 2.58     |
| TDATA[3:0] output hold time  | $t_{TRDH}$       | 2.5  | -   | -   | ns   |                 |

**Figure 2.57 ETM TCLK timing****Figure 2.58 ETM output timing**

## Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings is shown in “Packages” on the Renesas Electronics Corporation website.

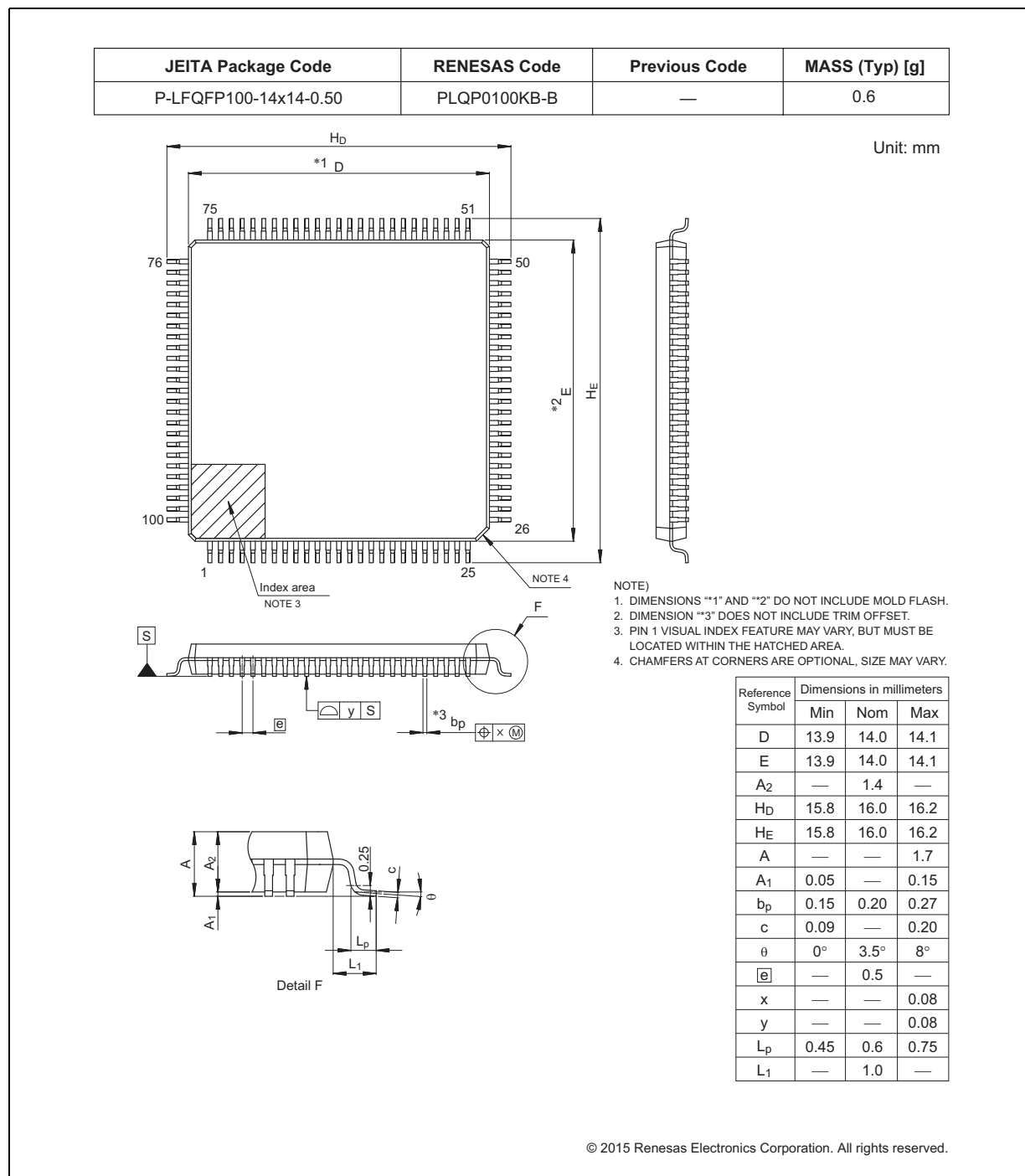
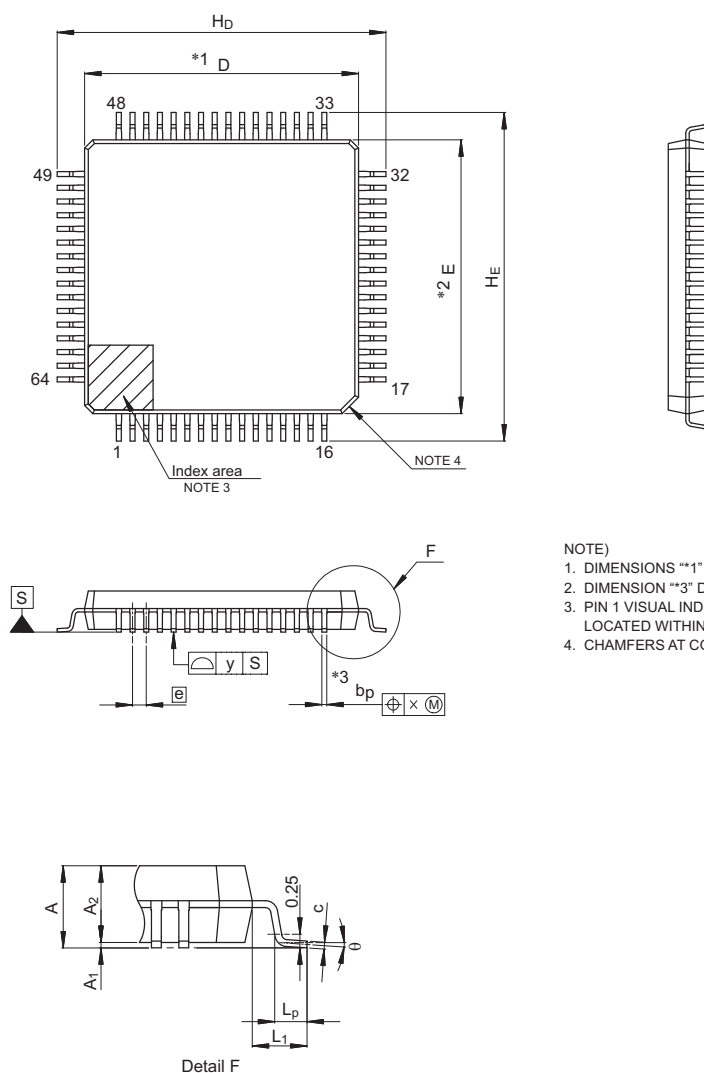


Figure 1.1 100-pin LQFP

| JEITA Package Code   | RENESAS Code | Previous Code | MASS (Typ) [g] |
|----------------------|--------------|---------------|----------------|
| P-LFQFP64-10x10-0.50 | PLQP0064KB-C | —             | 0.3            |

Unit: mm



| Reference Symbol | Dimensions in millimeters |      |      |
|------------------|---------------------------|------|------|
|                  | Min                       | Nom  | Max  |
| D                | 9.9                       | 10.0 | 10.1 |
| E                | 9.9                       | 10.0 | 10.1 |
| A <sub>2</sub>   | —                         | 1.4  | —    |
| H <sub>D</sub>   | 11.8                      | 12.0 | 12.2 |
| H <sub>E</sub>   | 11.8                      | 12.0 | 12.2 |
| A                | —                         | —    | 1.7  |
| A <sub>1</sub>   | 0.05                      | —    | 0.15 |
| b <sub>p</sub>   | 0.15                      | 0.20 | 0.27 |
| c                | 0.09                      | —    | 0.20 |
| θ                | 0°                        | 3.5° | 8°   |
| e                | —                         | 0.5  | —    |
| x                | —                         | —    | 0.08 |
| y                | —                         | —    | 0.08 |
| L <sub>p</sub>   | 0.45                      | 0.6  | 0.75 |
| L <sub>1</sub>   | —                         | 1.0  | —    |

© 2015 Renesas Electronics Corporation. All rights reserved.

Figure 1.2 64-pin LQFP

|                  |                       |
|------------------|-----------------------|
| Revision History | RA6T1 Group Datasheet |
|------------------|-----------------------|

| Rev. | Date         | Chapter | Summary               |
|------|--------------|---------|-----------------------|
| 1.00 | May 29, 2020 | -       | First Edition issued  |
| 1.10 | Feb 24, 2022 | -       | Second Edition issued |
| 1.20 | Mar 3, 2023  | -       | Third Edition issued  |

### Proprietary Notice

All text, graphics, photographs, trademarks, logos, artwork and computer code, collectively known as content, contained in this document is owned, controlled or licensed by or to Renesas, and is protected by trade dress, copyright, patent and trademark laws, and other intellectual property rights and unfair competition laws. Except as expressly provided herein, no part of this document or content may be copied, reproduced, republished, posted, publicly displayed, encoded, translated, transmitted or distributed in any other medium for publication or distribution or for any commercial enterprise, without prior written consent from Renesas.

Arm® and Cortex® are registered trademarks of Arm Limited. CoreSight™ is a trademark of Arm Limited.

CoreMark® is a registered trademark of the Embedded Microprocessor Benchmark Consortium.

Magic Packet™ is a trademark of Advanced Micro Devices, Inc.

SuperFlash® is a registered trademark of Silicon Storage Technology, Inc. in several countries including the United States and Japan.

Other brands and names mentioned in this document may be the trademarks or registered trademarks of their respective holders.

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

## 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

## 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

## 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

## 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

## 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

## 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

## 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

## 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

## Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

## Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)