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Product Reference Information

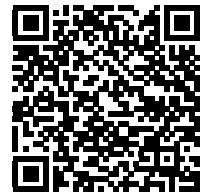
Part Number:	IDT5V993A-7QGI
Manufacturer:	Renesas Electronics Corporation
Package:	28-SSOP (0.154", 3.90mm Width)
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/renesas-electronics-corporation/idt5v993a-7qgi.html>

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Supplier verification and packaging condition review

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



3.3V PROGRAMMABLE SKEW PLL CLOCK DRIVER TURBOCLOCK™

IDT5V993A

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES OCTOBER 28, 2014

FEATURES:

- Ref input is 5V tolerant
- 3 pairs of programmable skew outputs
- Low skew: 200ps same pair, 250ps all outputs
- Selectable positive or negative edge synchronization:
Excellent for DSP applications
- Synchronous output enable
- Output frequency: 3.75MHz to 85MHz
- 2x, 4x, 1/2, and 1/4 outputs
- 3 skew grades:
IDT5V993A-2: tsKEW0<250ps
IDT5V993A-5: tsKEW0<500ps
IDT5V993A-7: tsKEW0<750ps
- 3-level inputs for skew and PLL range control
- PLL bypass for DC testing
- External feedback, internal loop filter
- 12mA balanced drive outputs
- Low Jitter: <200ps peak-to-peak
- Available in QSOP package
- Use replacement part: 87952AYI-147LF

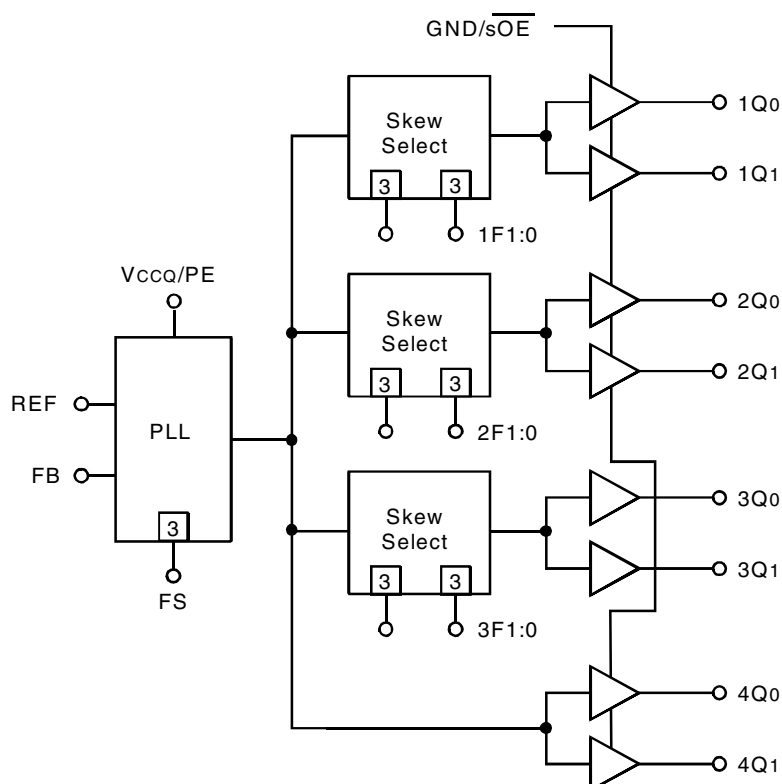
DESCRIPTION:

The IDT5V993A is a high fanout 3.3V PLL based clock driver intended for high performance computing and data-communications applications. A key feature of the programmable skew is the ability of outputs to lead or lag the REF input signal. The IDT5V993A has six programmable skew outputs and two zero skew outputs. Skew is controlled by 3-level input signals that may be hard-wired to appropriate HIGH-MID-LOW levels.

When the GND/sOE pin is held low, all the outputs are synchronously enabled. However, if GND/sOE is held high, all the outputs except 3Q0 and 3Q1 are synchronously disabled.

Furthermore, when the VccQ/PE is held high, all the outputs are synchronized with the positive edge of the REF clock input. When VccQ/PE is held low, all the outputs are synchronized with the negative edge of REF. Both devices have LVTTTL outputs with 12mA balanced drive outputs.

FUNCTIONAL BLOCK DIAGRAM

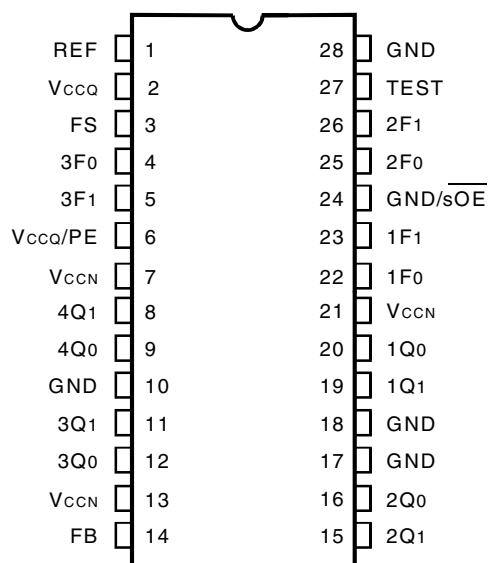


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

COMMERCIAL AND INDUSTRIAL TEMPERATURE RANGES

JULY 2012

PIN CONFIGURATION



QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
	Supply Voltage to Ground	-0.5 to +7	V
V _I	DC Input Voltage	-0.5 to V _{CC} +0.5	V
	REF Input Voltage	-0.5 to +5.5	V
	Maximum Power Dissipation (T _A = 85°C)	0.66	W
T _{STG}	Storage Temperature	-65 to +150	°C

NOTE:

- Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{IN} = 0V)

Parameter	Description	Typ.	Max.	Unit
C _{IN}	Input Capacitance	4	6	pF

NOTE:

- Capacitance applies to all inputs except TEST and FS. It is characterized but not production tested.

PIN DESCRIPTION

Pin Name	Type	Description
REF	IN	Reference Clock Input
FB	IN	Feedback Input
TEST ⁽¹⁾	IN	When MID or HIGH, disables PLL (except for conditions of Note 1). REF goes to all outputs. Skew Selections (See Control Summary Table) remain in effect. Set LOW for normal operation.
GND/ $\overline{\text{sOE}}$ ⁽¹⁾	IN	Synchronous Output Enable. When HIGH, it stops clock outputs (except 3Q0 and 3Q1) in a LOW state - 3Q0 and 3Q1 may be used as the feedback signal to maintain phase lock. When TEST is held at MID level and GND/ $\overline{\text{sOE}}$ is HIGH, the nF[1:0] pins act as output disable controls for individual banks when nF[1:0] = LL. Set GND/ $\overline{\text{sOE}}$ LOW for normal operation.
VCCQ/PE	IN	Selectable positive or negative edge control. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock.
nF[1:0]	IN	3-level inputs for selecting 1 of 9 skew taps or frequency functions
FS	IN	Selects appropriate oscillator circuit based on anticipated frequency range. (See PLL Programmable Skew Range.)
nQ[1:0]	OUT	Three output banks of two outputs with programmable skew (1Q:3Q), and 4Q output has fixed zero skew outputs.
VCCN	PWR	Power supply for output buffers
VCCQ	PWR	Power supply for phase locked loop and other internal circuitry
GND	PWR	Ground

NOTE:

- When TEST = MID and GND/ $\overline{\text{sOE}}$ = HIGH, PLL remains active.

PROGRAMMABLE SKEW

Output skew with respect to the REF input is adjustable to compensate for PCB trace delays, backplane propagation delays or to accommodate requirements for special timing relationships between clocked components. Skew is selectable as a multiple of a time unit t_u which is of the order of a nanosecond (see PLL Programmable Skew Range and Resolution Table). There are nine skew configurations available for each output pair. These configurations are chosen

by the nF_{1:0} control pins. In order to minimize the number of control pins, 3-level inputs (HIGH-MID-LOW) are used, they are intended for but not restricted to hard-wiring. Undriven 3-level inputs default to the MID level. Where programmable skew is not a requirement, the control pins can be left open for the zero skew default setting. The Control Summary Table shows how to select specific skew taps by using the nF_{1:0} control pins.

EXTERNAL FEEDBACK

By providing external feedback, the IDT5V993A gives users flexibility with regard to skew adjustment. The FB signal is compared with the input REF signal at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly.

An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

PLL PROGRAMMABLE SKEW RANGE AND RESOLUTION TABLE

	FS = LOW	FS = MID	FS = HIGH	Comments
Timing Unit Calculation (tu)	$1/(44 \times F_{NOM})$	$1/(26 \times F_{NOM})$	$1/(16 \times F_{NOM})$	
VCO Frequency Range (F_{NOM}) ^(1,2)	15 to 35MHz	25 to 60MHz	40 to 85 MHz	
Skew Adjustment Range ⁽³⁾				
Max Adjustment:	$\pm 9.09ns$	$\pm 9.23ns$	$\pm 9.38ns$	ns
	$\pm 49^\circ$	$\pm 83^\circ$	$\pm 135^\circ$	Phase Degrees
	$\pm 14\%$	$\pm 23\%$	$\pm 37\%$	% of Cycle Time
Example 1, $F_{NOM} = 15MHz$	tu = 1.52ns	—	—	
Example 2, $F_{NOM} = 25MHz$	tu = 0.91ns	tu = 1.54ns	—	
Example 3, $F_{NOM} = 30MHz$	tu = 0.76ns	tu = 1.28ns	—	
Example 4, $F_{NOM} = 40MHz$	—	tu = 0.96ns	tu = 1.56ns	
Example 5, $F_{NOM} = 50MHz$	—	tu = 0.77ns	tu = 1.25ns	
Example 6, $F_{NOM} = 80MHz$	—	—	tu = 0.78ns	

NOTES:

- The device may be operated outside recommended frequency ranges without damage, but functional operation is not guaranteed. Selecting the appropriate FS value based on input frequency range allows the PLL to operate in its 'sweet spot' where jitter is lowest.
- The level to be set on FS is determined by the nominal operating frequency of the VCO and Time Unit Generator. The VCO frequency always appears at 1Q1:0, 2Q1:0, and the higher outputs when they are operated in their undivided modes. The frequency appearing at the REF and FB inputs will be the same as the VCO when the output connected to FB is undivided. The frequency of the REF and FB inputs will be 1/2 or 1/4 the VCO frequency when the part is configured for a frequency multiplication by using a divided output as the FB input.
- Skew adjustment range assumes that a zero skew output is used for feedback. If a skewed Q output is used for feedback, then adjustment range will be greater. For example if a 4tu skewed output is used for feedback, all other outputs will be skewed -4tu in addition to whatever skew value is programmed for those outputs. 'Max adjustment' range applies to output pairs 3 and 4 where $\pm 6tu$ skew adjustment is possible and at the lowest F_{NOM} value.

CONTROL SUMMARY TABLE FOR FEEDBACK SIGNALS

nF1:0	Skew (Pair #1, #2)	Skew (Pair #3)
LL ⁽¹⁾	-4tu	Divide by 2
LM	-3tu	-6tu
LH	-2tu	-4tu
ML	-1tu	-2tu
MM	Zero Skew	Zero Skew
MH	1tu	2tu
HL	2tu	4tu
HM	3tu	6tu
HH	4tu	Divide by 4

NOTE:

- LL disables outputs if TEST = MID and $GND/\overline{sOE} = HIGH$.

RECOMMENDED OPERATING RANGE

Symbol	Description	IDT5V993A-5, -7 (Industrial)		IDT5V993A-2 (Commercial)		Unit
		Min.	Max.	Min.	Max.	
V _{CC}	Power Supply Voltage	3	3.6	3	3.6	V
T _A	Ambient Operating Temperature	-40	+85	0	+70	°C

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH (REF, FB Inputs Only)	2	—	V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW (REF, FB Inputs Only)	—	0.8	V
V _{IHH}	Input HIGH Voltage ⁽¹⁾	3-Level Inputs Only	V _{CC} −0.6	—	V
V _{IMM}	Input MID Voltage ⁽¹⁾	3-Level Inputs Only	V _{CC} /2−0.3	V _{CC} /2+0.3	V
V _{ILL}	Input LOW Voltage ⁽¹⁾	3-Level Inputs Only	—	0.6	V
I _{IN}	Input Leakage Current (REF, FB Inputs Only)	V _{IN} = V _{CC} or GND V _{CC} = Max.	—	±5	μA
I ₃	3-Level Input DC Current (TEST, FS)	V _{IN} = V _{CC} HIGH Level	—	±200	μA
		V _{IN} = V _{CC} /2 MID Level	—	±50	
		V _{IN} = GND LOW Level	—	±200	
I _{PU}	Input Pull-Up Current (V _{CCQ} /PE)	V _{CC} = Max., V _{IN} = GND	—	±100	μA
I _{PD}	Input Pull-Down Current (GND/sOE)	V _{CC} = Max., V _{IN} = V _{CC}	—	±100	μA
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = −12mA	2.4	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12mA	—	0.55	V

NOTE:

- These inputs are normally wired to V_{CC}, GND, or unconnected. Internal termination resistors bias unconnected inputs to V_{CC}/2. If these inputs are switched, the function and timing of the outputs may be glitched, and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Typ. ⁽²⁾	Max.	Unit
I _{CCQ}	Quiescent Power Supply Current	V _{CC} = Max., TEST = MID, REF = LOW, V _{CCQ} /PE = LOW, GND/sOE = LOW, All outputs unloaded	8	25	mA
ΔI _{CC}	Power Supply Current per Input HIGH	V _{CC} = Max., V _{IN} = 3V	1	30	μA
I _{CCD}	Dynamic Power Supply Current per Output	V _{CC} = Max., CL = 0pF	55	90	μA/MHz
I _{TOT}	Total Power Supply Current	V _{CC} = 3.3V, F _{REF} = 20MHz, CL = 160pF ⁽¹⁾	29	—	mA
		V _{CC} = 3.3V, F _{REF} = 33MHz, CL = 160pF ⁽¹⁾	42	—	
		V _{CC} = 3.3V, F _{REF} = 66MHz, CL = 160pF ⁽¹⁾	76	—	

NOTE:

- For eight outputs, each loaded with 20pF.

INPUT TIMING REQUIREMENTS

Symbol	Description ⁽¹⁾	Min.	Max.	Unit
t _r , t _f	Maximum input rise and fall times, 0.8V to 2V	—	10	ns/V
t _{PWC}	Input clock pulse, HIGH or LOW	3	—	ns
D _H	Input duty cycle	10	90	%
REF	Reference Clock Input	3.75	85	MHz

NOTE:

1. Where pulse width implied by D_H is less than t_{PWC} limit, t_{PWC} limit applies.

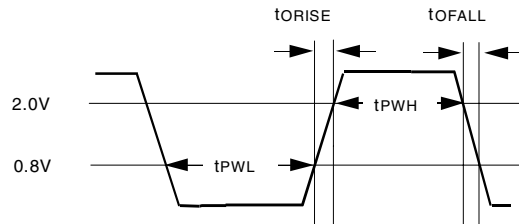
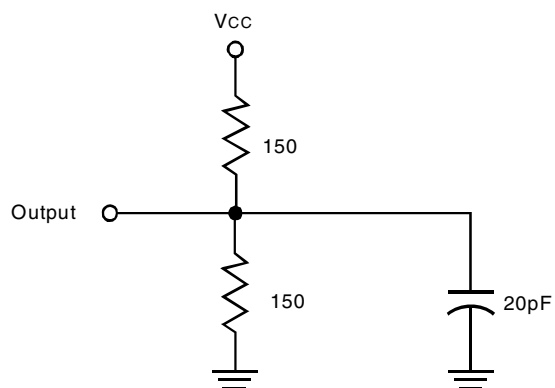
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter		IDT5V993A-2			IDT5V993A-5			IDT5V993A-7			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
F _{NOM}	VCO Frequency Range		See PLL Programmable Skew Range and Resolution Table									
t _{RPWH}	REF Pulse Width HIGH ^(1,1)		3	—	—	3	—	—	3	—	—	ns
t _{RPWL}	REF Pulse Width LOW ^(1,1)		3	—	—	3	—	—	3	—	—	ns
t _u	Programmable Skew Time Unit		See Control Summary Table									
t _{SKEWPR}	Zero Output Matched-Pair Skew (xQ ₀ , xQ ₁) ^(1,2,3)		—	0.05	0.2	—	0.1	0.25	—	0.1	0.25	ns
t _{SKEW0}	Zero Output Skew (All Outputs) ^(1,4)		—	0.1	0.25	—	0.25	0.5	—	0.3	0.75	ns
t _{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs) ^(1,6)		—	0.25	0.5	—	0.6	0.7	—	0.6	1	ns
t _{SKEW2}	Output Skew (Rise-Fall, Divided-Divided) ^(1,6)		—	0.3	1.2	—	0.5	1.2	—	1	1.5	ns
t _{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs) ^(1,6)		—	0.25	0.5	—	0.5	0.7	—	0.7	1.2	ns
t _{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided) ^(1,2)		—	0.5	0.9	—	0.5	1	—	1.2	1.7	ns
t _{DEV}	Device-to-Device Skew ^(1,2,7)		—	—	0.75	—	—	1.25	—	—	1.65	ns
t _{PD}	REF Input to FB Propagation Delay ^(1,9)		−0.25	0	0.25	−0.5	0	0.5	−0.7	0	0.7	ns
t _{ODCV}	Output Duty Cycle Variation from 50% ⁽¹⁾		−1.2	0	1.2	−1.2	0	1.2	−1.2	0	1.2	ns
t _{PWH}	Output HIGH Time Deviation from 50% ^(1,10)		—	—	2	—	—	2.5	—	—	3	ns
t _{PWL}	Output LOW Time Deviation from 50% ^(1,11)		—	—	1.5	—	—	3	—	—	3.5	ns
t _{ORISE}	Output Rise Time ⁽¹⁾		0.15	1	1.2	0.15	1	1.8	0.15	1.5	2.5	ns
t _{OFALL}	Output Fall Time ⁽¹⁾		0.15	1	1.2	0.15	1	1.8	0.15	1.5	2.5	ns
t _{LOCK}	PLL Lock Time ^(1,8)		—	—	0.5	—	—	0.5	—	—	0.5	ms
t _{JR}	Cycle-to-Cycle Output Jitter ⁽¹⁾	RMS	—	—	25	—	—	25	—	—	25	ps
		Peak-to-Peak	—	—	200	—	—	200	—	—	200	

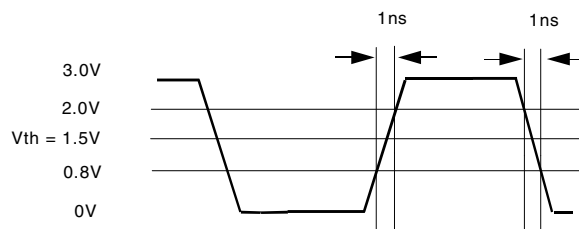
NOTES:

- All timing and jitter tolerances apply for F_{NOM} > 25MHz.
- Skew is the time between the earliest and the latest output transition among all outputs for which the same t_u delay has been selected when all are loaded with the specified load.
- t_{SKEWPR} is the skew between a pair of outputs (xQ₀ and xQ₁) when all eight outputs are selected for 0t_u.
- t_{SKEW0} is the skew between outputs when they are selected for 0t_u.
- For IDT5V993A-2 t_{SKEW0} is measured with C_L = 0pF; for C_L = 20pF, t_{SKEW0} = 0.35ns Max.
- There are 2 classes of outputs: Nominal (multiple of t_u delay), and Divided (3Qx only in Divide-by-2 or Divide-by-4 mode).
- t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{cc}, ambient temperature, air flow, etc.)
- t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{cc} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.
- t_{PD} is measured with REF input rise and fall times (from 0.8V to 2V) of 1ns.
- Measured at 2V.
- Measured at 0.8V.

AC TEST LOADS AND WAVEFORMS

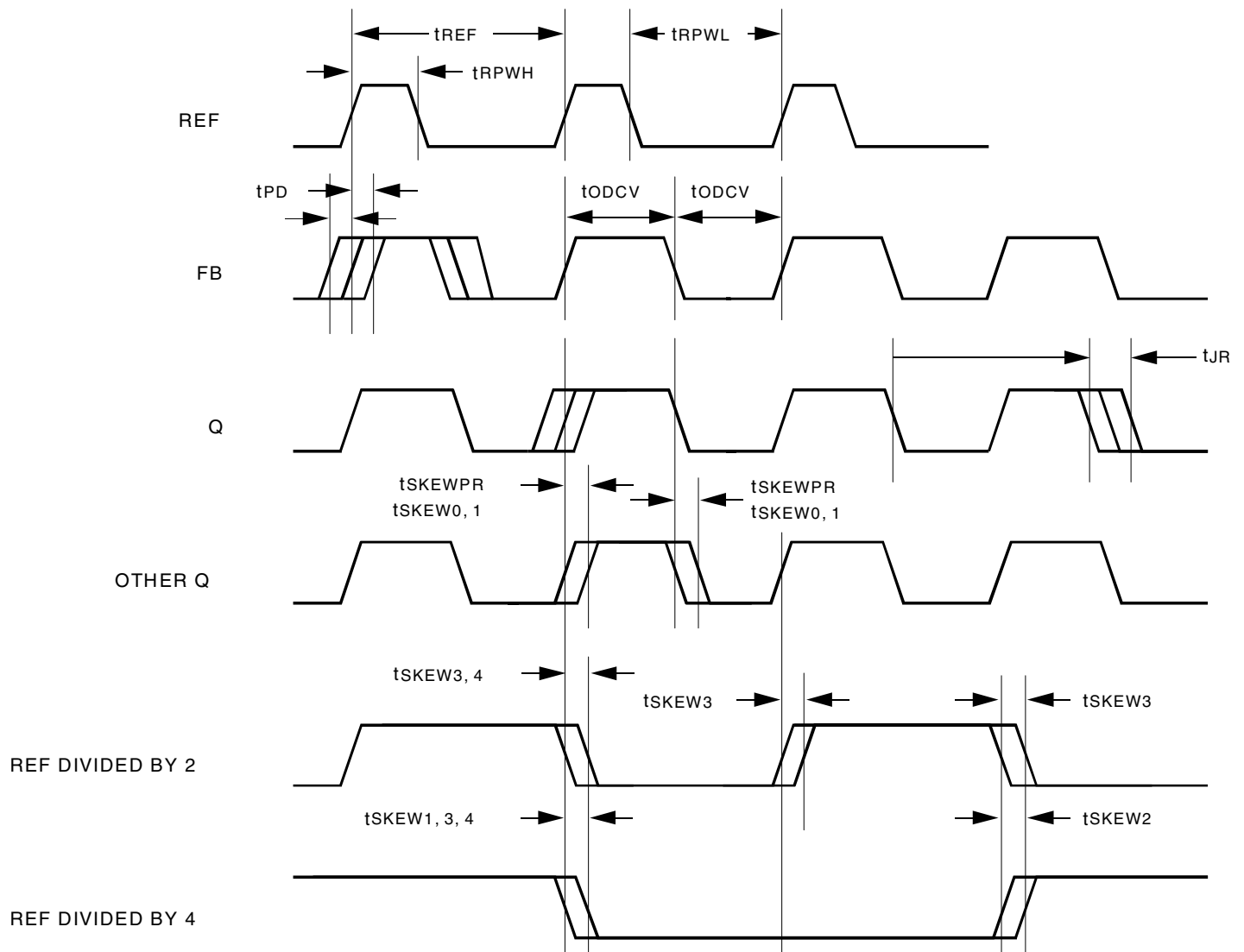


LVTTTL Output Waveform



LVTTTL Input Test Waveform

AC TIMING DIAGRAM



NOTES:

V_{CCQ}/PE: The AC Timing Diagram applies to $V_{CCQ}/PE=V_{CC}$. For $V_{CCQ}/PE=GND$, the negative edge of FB aligns with the negative edge of REF, divided outputs change on the negative edge of REF, and the positive edges of the divide-by-2 and the divide-by-4 signals align.

Skew: The time between the earliest and the latest output transition among all outputs for which the same t_u delay has been selected when all are loaded with 20pF and terminated with 75Ω to $V_{CC}/2$.

t_{SKEWPR}: The skew between a pair of outputs (xQ_0 and xQ_1) when all eight outputs are selected for $0t_u$.

t_{SKEW0}: The skew between outputs when they are selected for $0t_u$.

t_{DEV}: The output-to-output skew between any two devices operating under the same conditions (V_{CC} , ambient temperature, air flow, etc.)

t_{ODCV}: The deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.

t_{PWH} is measured at 2V.

t_{PWL} is measured at 0.8V.

t_{ORISE} and **t_{OFALL}** are measured between 0.8V and 2V.

t_{LOCK}: The time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

ORDERING INFORMATION

IDT	XXXXX	XX	X		
	Device Type	Package	Process		
				Blank	0°C to +70°C (Commercial)
				I	-40°C to +85°C (Industrial)
				QG	QSOP - Green
				5V993A-2	3.3V Programmable Skew PLL Clock Driver
				5V993A-5	TurboClock
				5V993A-7	

REVISION HISTORY

12/19/13 PDN - Product Discontinuation Notice - Last Time Buy Expires October 28, 2014
PDN# CQ-13-02



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