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Electronic Components Sourcing Information

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

SSN1N45B

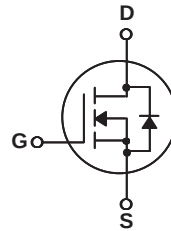
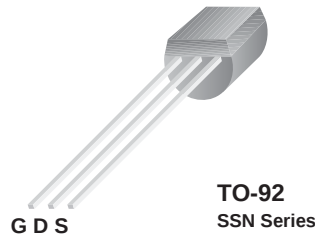
450V N-Channel MOSFET

General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for electronic ballasts based on half bridge configuration.

Features

- 0.5A, 450V, $R_{DS(on)} = 4.25\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 6.5 nC)
- Low C_{rss} (typical 6.5 pF)
- 100% avalanche tested
- Improved dv/dt capability
- Gate-Source Voltage $\pm 50V$ guaranteed



Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	SSN1N45B	Units
V_{DSS}	Drain-Source Voltage	450	V
I_D	Drain Current - Continuous ($T_C = 25^\circ C$)	0.5	A
	- Continuous ($T_C = 100^\circ C$)	0.32	A
I_{DM}	Drain Current - Pulsed (Note 1)	4.0	A
V_{GSS}	Gate-Source Voltage	± 50	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	108	mJ
I_{AR}	Avalanche Current (Note 1)	0.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.25	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ C$)	0.9	W
	Power Dissipation ($T_L = 25^\circ C$)	2.5	W
	- Derate above $25^\circ C$	0.02	W/ $^\circ C$
T_J, T_{stg}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ C$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead (Note 6a)	--	50	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 6b)	--	140	$^\circ C/W$

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	450	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.5	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 450\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 360\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 50\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -50\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.3	3.0	3.7	V
		$V_{DS} = V_{GS}, I_D = 250\text{ mA}$	3.5	4.2	4.9	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 0.25\text{ A}$	--	3.4	4.25	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 0.25\text{ A}$	--	0.7	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	185	240	pF
C_{oss}	Output Capacitance		--	29	40	pF
C_{rss}	Reverse Transfer Capacitance		--	6.5	8.5	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 225\text{ V}, I_D = 0.5\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4,5)	--	7.5	25	ns
t_r	Turn-On Rise Time		--	21	50	ns
$t_{d(off)}$	Turn-Off Delay Time		--	23	55	ns
t_f	Turn-Off Fall Time		--	36	80	ns
Q_g	Total Gate Charge	$V_{DS} = 360\text{ V}, I_D = 0.5\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4,5)	--	6.5	8.5	nC
Q_{gs}	Gate-Source Charge		--	0.9	--	nC
Q_{gd}	Gate-Drain Charge		--	3.2	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	0.5	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	4.0	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.5 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 0.5 A,	--	102	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs (Note 4)	--	0.26	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 75\text{ mH}, I_{AS} \approx 1.6\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 0.5\text{ A}, dI/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature
6. a) Reference point of the $R_{\theta JL}$ is the drain lead
b) When mounted on 3"x4.5" FR-4 PCB without any pad copper in a still air environment
($R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance. $R_{\theta CA}$ is determined by the user's board design)

Typical Characteristics

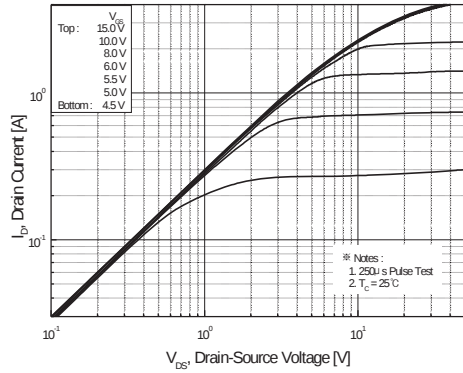


Figure 1. On-Region Characteristics

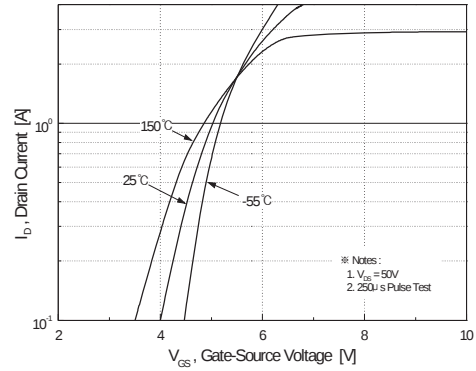


Figure 2. Transfer Characteristics

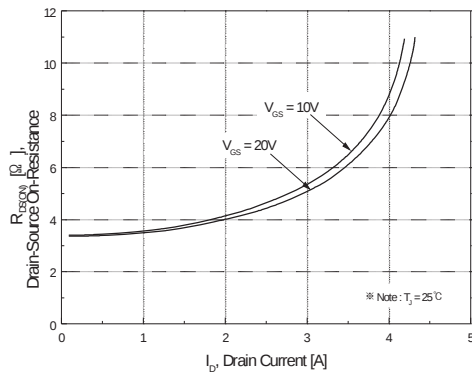


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

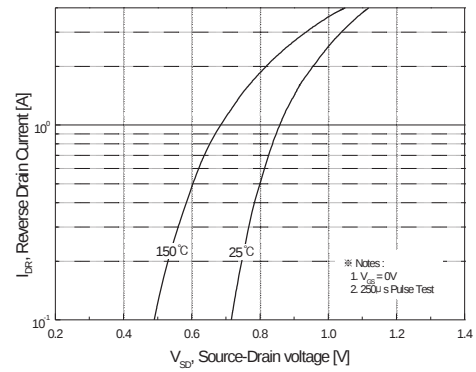


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

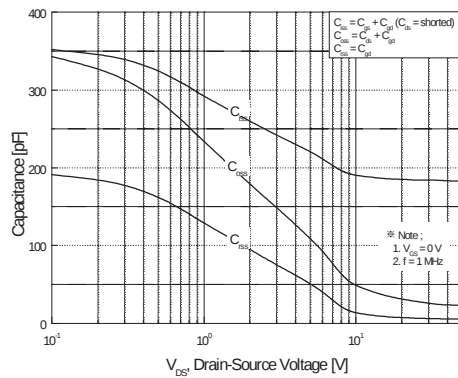


Figure 5. Capacitance Characteristics

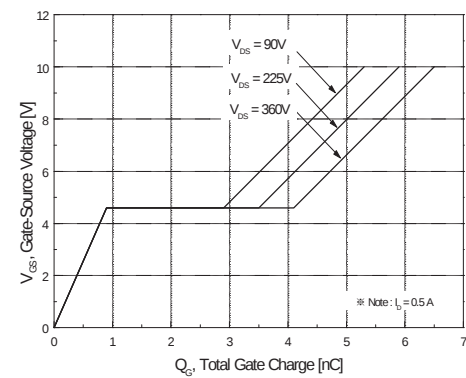


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

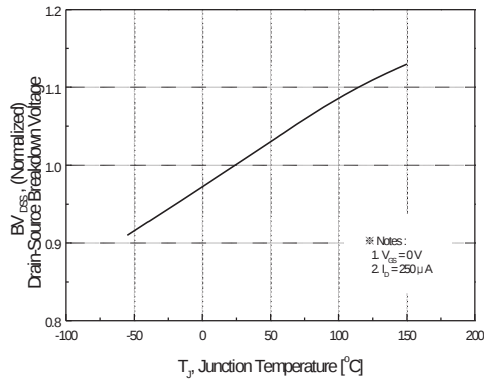


Figure 7. Breakdown Voltage Variation vs. Temperature

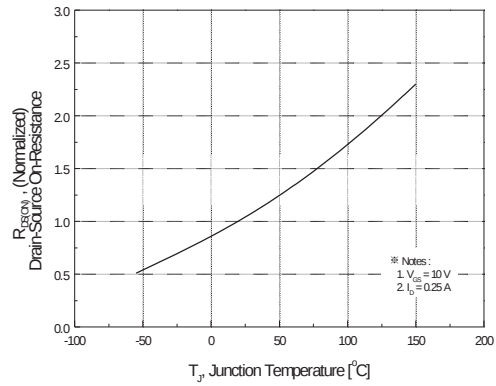


Figure 8. On-Resistance Variation vs. Temperature

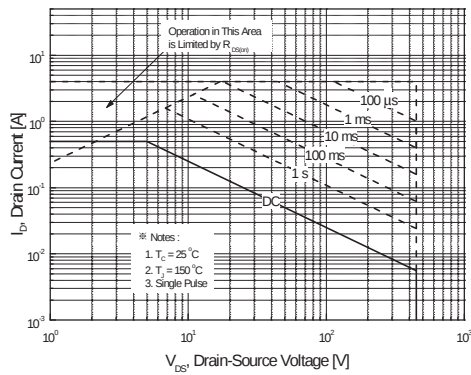


Figure 9. Maximum Safe Operating Area

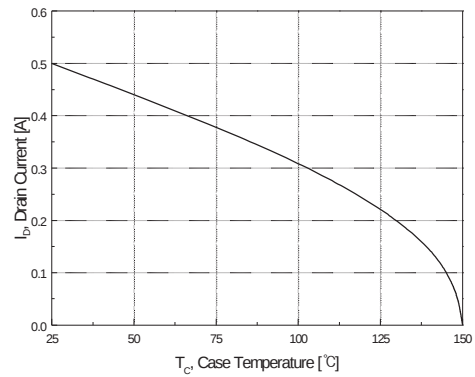


Figure 10. Maximum Drain Current vs. Case Temperature

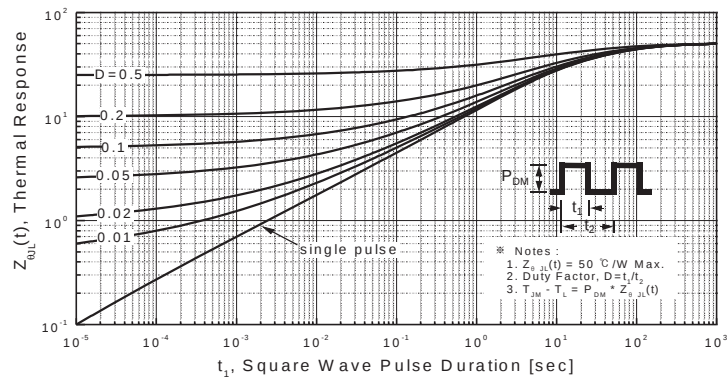
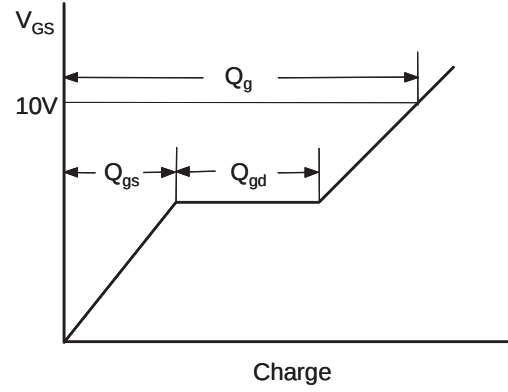
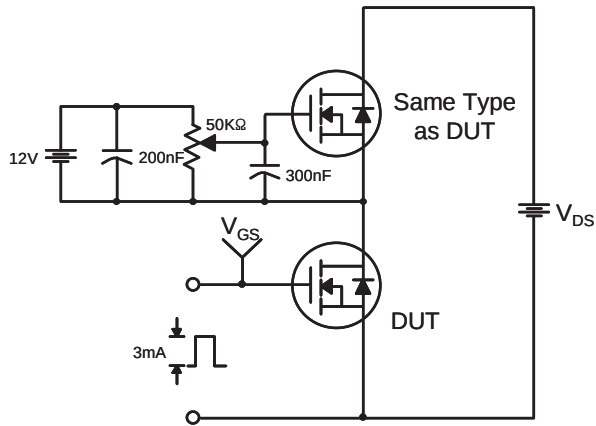
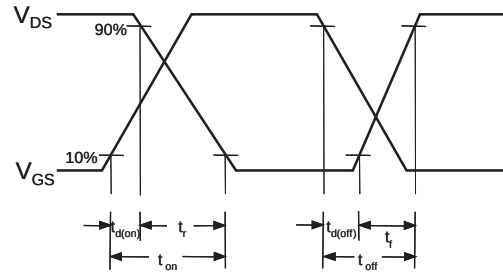
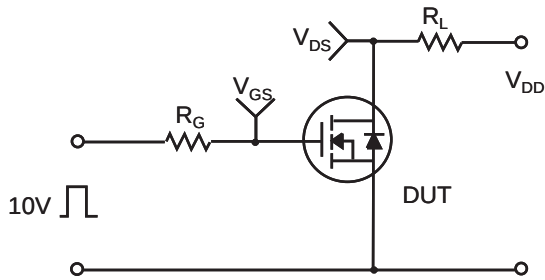


Figure 11. Transient Thermal Response Curve

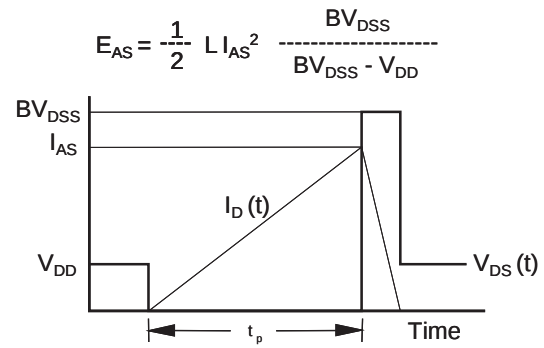
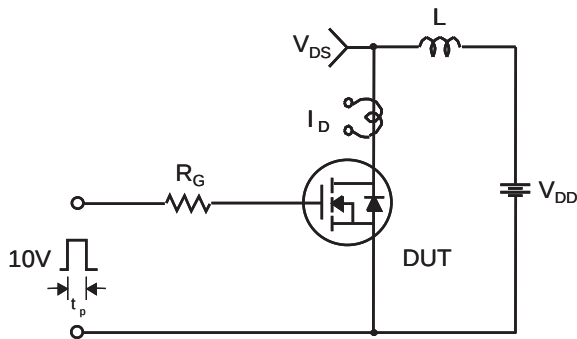
Gate Charge Test Circuit & Waveform



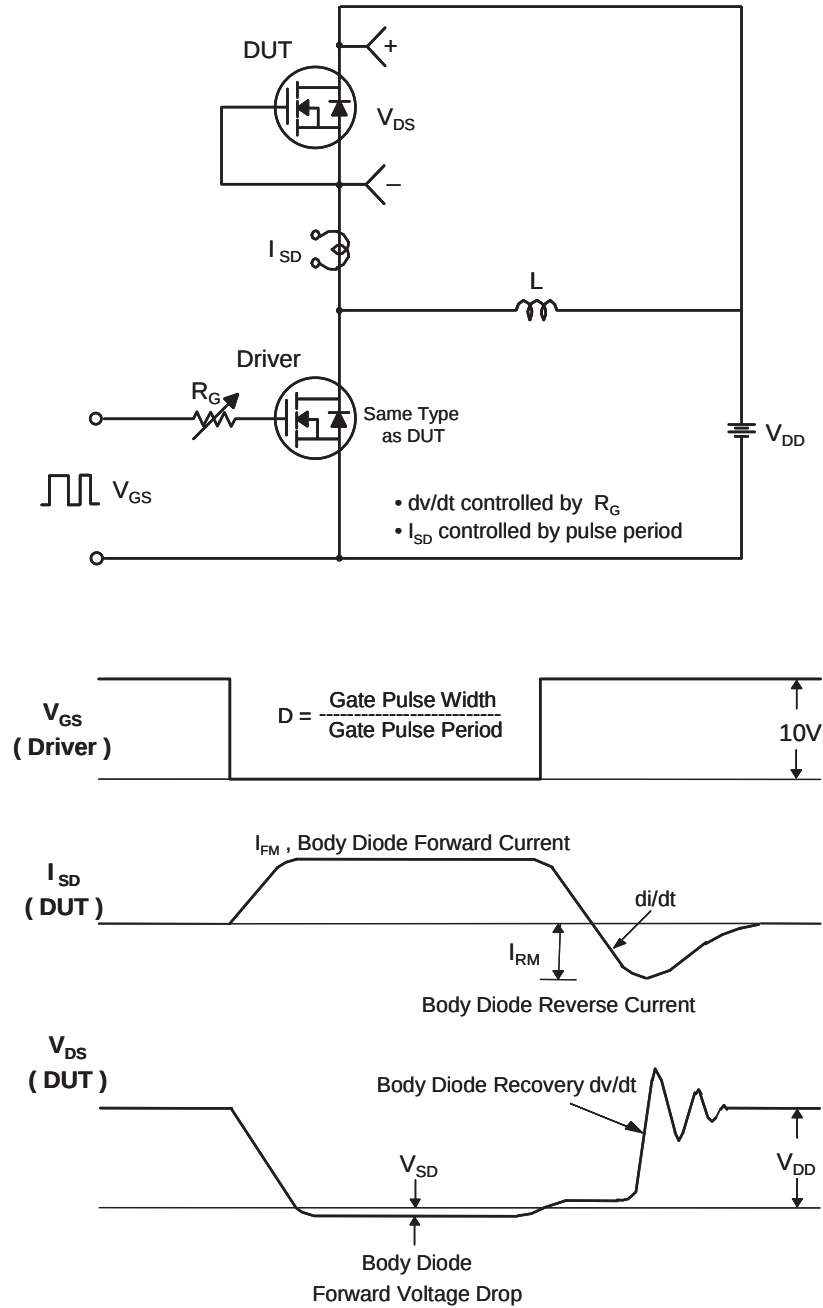
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

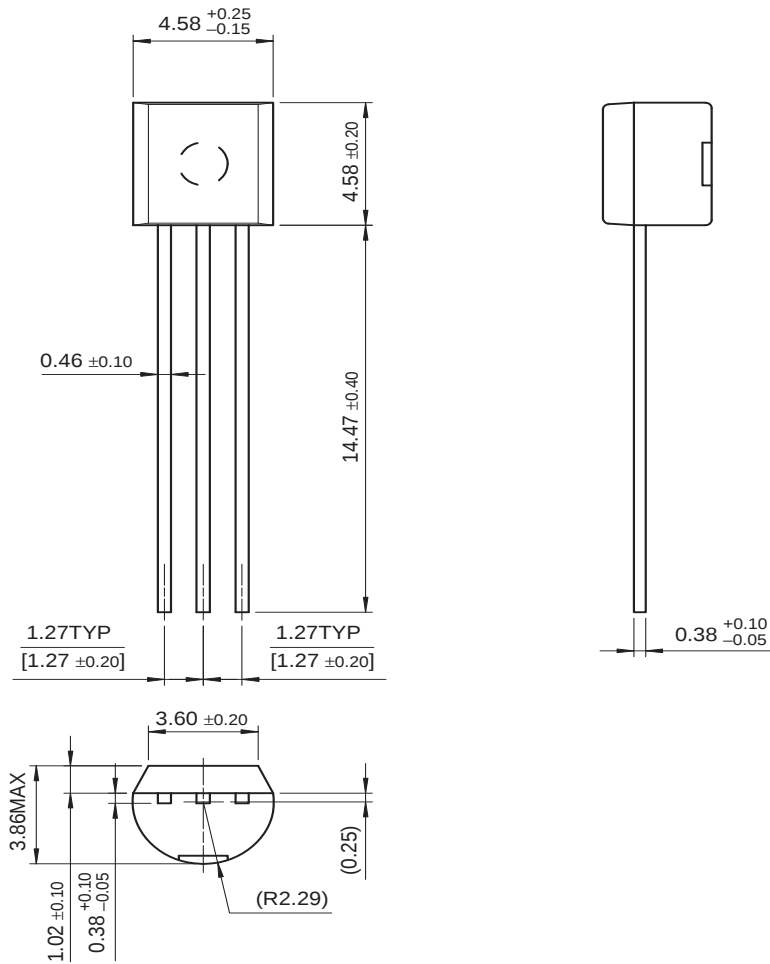


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

TO-92



Dimensions in Millimeters

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

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SSN1N45B

450V N-Channel B-FET

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General description

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Product status/pricing/packaging

BUY

Product	Product status	Pb-free Status	Pricing*	Package type	Leads	Packing method	Package Marking Convention**

SSN1N45BBU	Full Production	 Full Production	\$0.466	TO-92	3	BULK	Line 1: 1N45B Line 2: 3
SSN1N45BTA	Full Production	 Full Production	\$0.394	TO-92	3	AMMO	Line 1: 1N45B Line 2: 3

* Fairchild 1,000 piece Budgetary Pricing

** A sample button will appear if the part is available through Fairchild's on-line samples program. If there is no sample button, please contact a [Fairchild distributor](#) to obtain samples



Indicates product with Pb-free second-level interconnect. For more information [click here](#).

Package marking information for product SSN1N45B is available. [Click here for more information](#).

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Qualification Support

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