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### Product Reference Information

**Part Number:** UDA1351H/N1,551  
**Manufacturer:** NXP USA Inc.  
**Package:** 44-QFP  
**Availability:** Please confirm with sales

**Product Page:**

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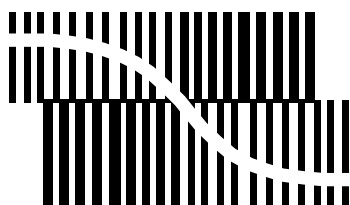
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**Note:**

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

# DATA SHEET



BITSTREAM CONVERSION

## UDA1351H

### 96 kHz IEC 958 audio DAC

Product specification  
Supersedes data of 2000 Feb 18  
File under Integrated Circuits, IC01

2000 Jul 27

**96 kHz IEC 958 audio DAC****UDA1351H****CONTENTS**

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## 96 kHz IEC 958 audio DAC

## UDA1351H

**1 FEATURES****1.1 General**

- 2.7 to 3.6 V power supply
- Integrated digital filter and Digital-to-Analog Converter (DAC)
- Master-mode data output interface for off-chip sound processing
- $256f_s$  system clock output
- 20-bit data-path in interpolator
- High performance
- No analog post filtering required for DAC
- Supports sampling frequencies from 28 up to 100 kHz
- The UDA1351H is fully pin and function compatible with the UDA1350AH.

**1.2 Control**

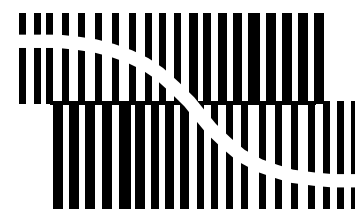
- Controlled either by means of static pins or via the L3 microcontroller interface.

**1.3 IEC 958 input**

- On-chip amplifier for converting IEC 958 input to CMOS levels
- Selectable IEC 958 input channel, one out of two
- Lock indication signal available on pin LOCK
- Lock indication signal combined on-chip with the Pulse Code Modulation (PCM) status bit; in case non-PCM has been detected pin LOCK indicates out-of-lock
- Key channel-status bits available via L3 interface (lock, pre-emphasis, audio sample frequency, 2 channel PCM indication and clock accuracy).

**1.4 Digital output and input interfaces**

- When the UDA1351H is clock master of the data output interfaces:
  - BCKO and WSO signals are output
  - I<sup>2</sup>S-bus or LSB-justified 16, 20 and 24 bits formats are supported.
- When the UDA1351H is clock slave of the data input interface:
  - BCK and WS signals are input
  - I<sup>2</sup>S-bus or LSB-justified 16, 20 and 24 bits formats are supported.



BITSTREAM CONVERSION

**1.5 Digital sound processing and DAC**

- Pre-emphasis information of IEC 958 input bitstream available in L3 interface register and on pins
- Automatic de-emphasis when using IEC 958 input with 32.0, 44.1 and 48.0 kHz audio sample frequencies
- Soft mute by means of a cosine roll-off circuit selectable via pin MUTE or the L3 interface
- Interpolating filter ( $f_s$  to  $128f_s$ ) by means of a cascade of a recursive filter and a FIR filter
- Third-order noise shaper operating at  $128f_s$  generates bitstream for the DAC
- Filter stream digital-to-analog converter.

**2 APPLICATIONS**

- Digital audio systems.

**3 GENERAL DESCRIPTION**

The UDA1351H is a single chip IEC 958 audio decoder with an integrated stereo digital-to-analog converter employing bitstream conversion techniques.

Besides the UDA1351H, which is the full featured version in QFP44 package, there also exists the UDA1351TS. The UDA1351TS has IEC 958 input to the DAC only and is in SSOP28 package.

The UDA1351H can operate in various operating modes:

- IEC 958 input to the DAC including on-chip signal processing
- IEC 958 input via the digital data output interface to the external Digital Signal Processor (DSP)
- IEC 958 input to the DAC and a DSP
- IEC 958 input via a DSP to the DAC including on-chip signal processing
- External source data input to the DAC including on-chip signal processing.

## 96 kHz IEC 958 audio DAC

## UDA1351H

The IEC 958 input audio data including the accompanying pre-emphasis information is available on the output data interface.

By default the DAC output and the data output interface are muted when the decoder is out-of-lock. However, this setting can be overruled in the L3 control mode.

A lock indication signal is available on pin LOCK indicating that the IEC 958 decoder is locked.

## 4 QUICK REFERENCE DATA

| SYMBOL                      | PARAMETER                                            | CONDITIONS                                          | MIN. | TYP. | MAX. | UNIT |
|-----------------------------|------------------------------------------------------|-----------------------------------------------------|------|------|------|------|
| Supplies                    |                                                      |                                                     |      |      |      |      |
| V <sub>DDD</sub>            | digital supply voltage                               |                                                     | 2.7  | 3.0  | 3.6  | V    |
| V <sub>DDA</sub>            | analog supply voltage                                |                                                     | 2.7  | 3.0  | 3.6  | V    |
| I <sub>DDA(DAC)</sub>       | analog supply current of DAC                         | power-on                                            | –    | 8.0  | –    | mA   |
|                             |                                                      | power-down                                          | –    | 750  | –    | μA   |
| I <sub>DDA(PLL)</sub>       | analog supply current of PLL                         | at 48 kHz                                           | –    | 0.7  | –    | mA   |
|                             |                                                      | at 96 kHz                                           | –    | 1.0  | –    | mA   |
| I <sub>DDD(C)</sub>         | digital supply current of core                       | at 48 kHz                                           | –    | 16.0 | –    | mA   |
|                             |                                                      | at 96 kHz                                           | –    | 24.5 | –    | mA   |
| I <sub>DDD</sub>            | digital supply current                               | at 48 kHz                                           | –    | 2.0  | –    | mA   |
|                             |                                                      | at 96 kHz                                           | –    | 3.0  | –    | mA   |
| P                           | power consumption at 48 kHz                          | DAC in playback mode                                | –    | 80   | –    | mW   |
|                             |                                                      | DAC in Power-down mode                              | –    | 58   | –    | mW   |
|                             | power consumption at 96 kHz                          | DAC in playback mode                                | –    | 109  | –    | mW   |
|                             |                                                      | DAC in Power-down mode                              | –    | 87   | –    | mW   |
| General                     |                                                      |                                                     |      |      |      |      |
| t <sub>rst</sub>            | reset active time                                    |                                                     | –    | 250  | –    | μs   |
| T <sub>amb</sub>            | ambient temperature                                  |                                                     | –40  | –    | +85  | °C   |
| Digital-to-analog converter |                                                      |                                                     |      |      |      |      |
| V <sub>o(rms)</sub>         | output voltage (RMS value)                           | note 1                                              | –    | 900  | –    | mV   |
| (THD + N)/S                 | total harmonic distortion-plus-noise to signal ratio | f <sub>i</sub> = 1.0 kHz tone at 48 kHz             |      |      |      |      |
|                             |                                                      | at 0 dB                                             | –    | –90  | –85  | dB   |
|                             |                                                      | at –40 dB; A-weighted                               | –    | –60  | –55  | dB   |
|                             |                                                      | f <sub>i</sub> = 1.0 kHz tone at 96 kHz             |      |      |      |      |
| S/N                         | signal-to-noise ratio at 48 kHz                      | at 0 dB                                             | –    | –85  | –80  | dB   |
|                             |                                                      | at –40 dB; A-weighted                               | –    | –58  | –53  | dB   |
|                             | signal-to-noise ratio at 96 kHz                      | f <sub>i</sub> = 1.0 kHz tone; code = 0; A-weighted | 95   | 100  | –    | dB   |
|                             |                                                      | f <sub>i</sub> = 1.0 kHz tone; code = 0; A-weighted | 95   | 100  | –    | dB   |
| α <sub>cs</sub>             | channel separation                                   | f <sub>i</sub> = 1.0 kHz tone                       | –    | 96   | –    | dB   |
| ΔV <sub>o</sub>             | unbalance of output voltages                         | f <sub>i</sub> = 1.0 kHz tone                       | 0.4  | 0.1  | –    | dB   |

**Note**

1. The DAC output voltage is proportionally to the DAC power supply voltage.

96 kHz IEC 958 audio DAC

UDA1351H

5 ORDERING INFORMATION

| TYPE<br>NUMBER | PACKAGE |                                                                                     |          |
|----------------|---------|-------------------------------------------------------------------------------------|----------|
|                | NAME    | DESCRIPTION                                                                         | VERSION  |
| UDA1351H       | QFP44   | plastic quad flat package; 44 leads (lead length 1.3 mm);<br>body 10 × 10 × 1.75 mm | SOT307-2 |

6 BLOCK DIAGRAM

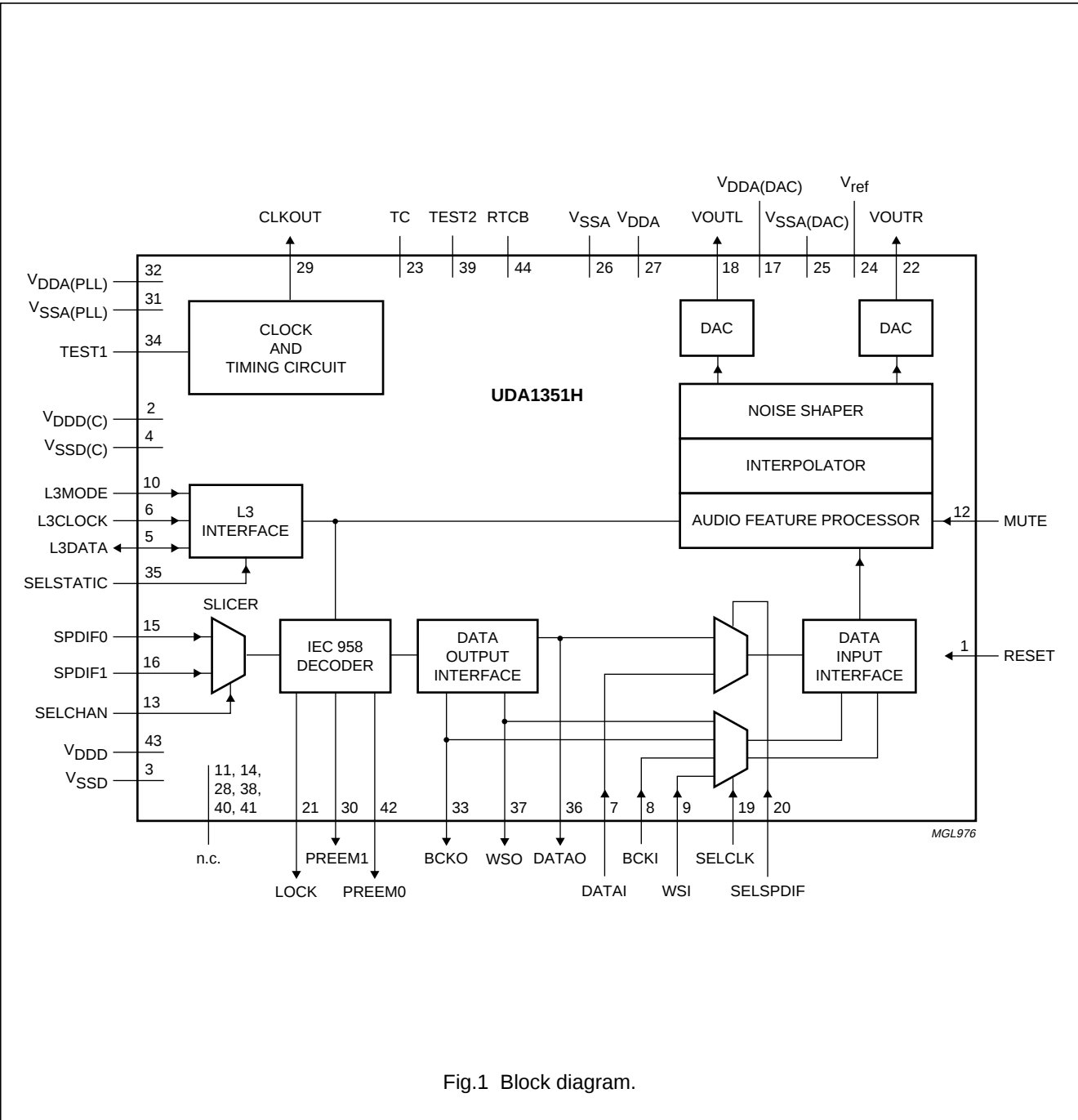


Fig.1 Block diagram.

## 96 kHz IEC 958 audio DAC

## UDA1351H

## 7 PINNING

| SYMBOL                | PIN | TYPE <sup>(1)</sup> | DESCRIPTION                                                                 |
|-----------------------|-----|---------------------|-----------------------------------------------------------------------------|
| RESET                 | 1   | DISD                | reset input                                                                 |
| V <sub>DDD(C)</sub>   | 2   | DS                  | digital supply voltage for core                                             |
| V <sub>SSD</sub>      | 3   | DGND                | digital ground                                                              |
| V <sub>SSD(C)</sub>   | 4   | DGND                | digital ground for core                                                     |
| L3DATA                | 5   | DIOS                | L3 interface data input and output                                          |
| L3CLOCK               | 6   | DIS                 | L3 interface clock input                                                    |
| DATAI                 | 7   | DISD                | I <sup>2</sup> S-bus data input                                             |
| BCKI                  | 8   | DISD                | I <sup>2</sup> S-bus bit clock input                                        |
| WSI                   | 9   | DISD                | I <sup>2</sup> S-bus word select input                                      |
| L3MODE                | 10  | DIS                 | L3 interface mode input                                                     |
| n.c.                  | 11  | –                   | not connected                                                               |
| MUTE                  | 12  | DID                 | mute control input                                                          |
| SELCHAN               | 13  | DID                 | IEC 958 channel selection input                                             |
| n.c.                  | 14  | –                   | not connected                                                               |
| SPDIF0                | 15  | AI                  | IEC 958 channel 0 input                                                     |
| SPDIF1                | 16  | AI                  | IEC 958 channel 1 input                                                     |
| V <sub>DDA(DAC)</sub> | 17  | AS                  | analog supply voltage for DAC                                               |
| VOU <sub>TL</sub>     | 18  | AO                  | DAC left channel analog output                                              |
| SELCLK                | 19  | DID                 | clock source for PLL selection input                                        |
| SELSPDIF              | 20  | DIU                 | IEC 958 data selection input                                                |
| LOCK                  | 21  | DO                  | SPDIF and PLL lock indicator output                                         |
| VOU <sub>TR</sub>     | 22  | AO                  | DAC right channel analog output                                             |
| TC                    | 23  | DID                 | test pin; must be connected to digital ground (V <sub>SSD</sub> )           |
| V <sub>ref</sub>      | 24  | A                   | DAC reference voltage                                                       |
| V <sub>SSA(DAC)</sub> | 25  | AGND                | analog ground for DAC                                                       |
| V <sub>SSA</sub>      | 26  | AGND                | analog ground                                                               |
| V <sub>DDA</sub>      | 27  | AS                  | analog supply voltage                                                       |
| n.c.                  | 28  | –                   | not connected                                                               |
| CLKOUT                | 29  | DO                  | clock output (256f <sub>s</sub> )                                           |
| PREEM1                | 30  | DO                  | IEC 958 input pre-emphasis output 1                                         |
| V <sub>SSA(PLL)</sub> | 31  | AGND                | analog ground for PLL                                                       |
| V <sub>DDA(PLL)</sub> | 32  | AS                  | analog supply voltage for PLL                                               |
| BCKO                  | 33  | DO                  | I <sup>2</sup> S-bus bit clock output                                       |
| TEST1                 | 34  | DIU                 | test pin 1: must be connected to digital supply voltage (V <sub>DDD</sub> ) |
| SELSTATIC             | 35  | DIU                 | static pin control selection input                                          |
| DATAO                 | 36  | DO                  | I <sup>2</sup> S-bus data output                                            |
| WSO                   | 37  | DO                  | I <sup>2</sup> S-bus word select output                                     |
| n.c.                  | 38  | –                   | not connected                                                               |
| TEST2                 | 39  | DISD                | test pin 2; must be connected to digital ground (V <sub>SSD</sub> )         |
| n.c.                  | 40  | –                   | not connected                                                               |

## 96 kHz IEC 958 audio DAC

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| SYMBOL           | PIN | TYPE <sup>(1)</sup> | DESCRIPTION                                                       |
|------------------|-----|---------------------|-------------------------------------------------------------------|
| n.c.             | 41  | –                   | not connected                                                     |
| PREEM0           | 42  | DO                  | IEC 958 input pre-emphasis output 0                               |
| V <sub>DDD</sub> | 43  | DS                  | digital supply voltage                                            |
| RTCB             | 44  | DID                 | test pin; must be connected to digital ground (V <sub>SSD</sub> ) |

**Note**

1. See Table 1.

**Table 1** Pin type references

| PIN TYPE | DESCRIPTION                                                      |
|----------|------------------------------------------------------------------|
| DS       | digital supply                                                   |
| DGND     | digital ground                                                   |
| AS       | analog supply                                                    |
| AGND     | analog ground                                                    |
| DI       | digital input                                                    |
| DIS      | digital Schmitt-triggered input                                  |
| DID      | digital input with internal pull-down resistor                   |
| DISD     | digital Schmitt-triggered input with internal pull-down resistor |
| DIU      | digital input with internal pull-up resistor                     |
| DO       | digital output                                                   |
| DIO      | digital input and output                                         |
| DIOS     | digital Schmitt-triggered input and output                       |
| A        | analog reference voltage                                         |
| AI       | analog input                                                     |
| AO       | analog output                                                    |

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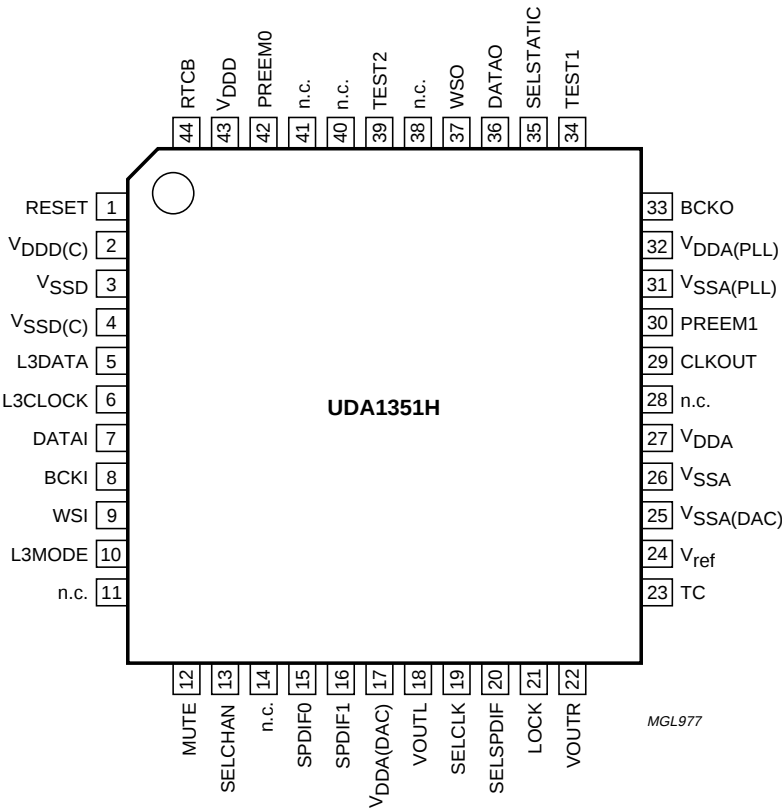


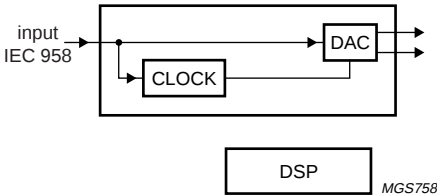
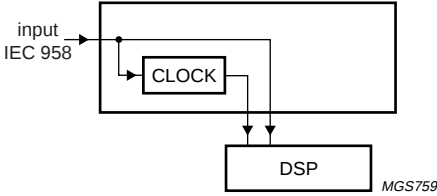
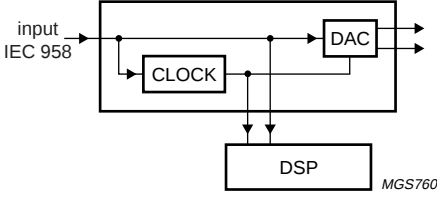
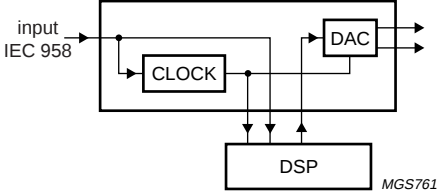
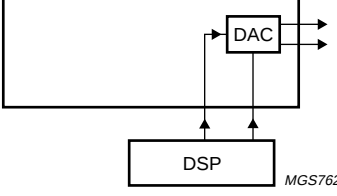
Fig.2 Pin configuration.

96 kHz IEC 958 audio DAC

UDA1351H

8 FUNCTIONAL DESCRIPTION

8.1 Operating modes

| MODE | DESCRIPTION                                                                                                 | SCHEMATIC                                                                            |
|------|-------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| 1    | IEC 958 input to the DAC                                                                                    |    |
| 2    | IEC 958 input via the data output interface to the DSP                                                      |    |
| 3    | IEC 958 input to the DAC and via the data output interface to the DSP                                       |  |
| 4    | IEC 958 input via the data output interface to the external DSP and via the data input interface to the DAC |  |
| 5    | Data input interface signal to the DAC                                                                      |  |

The UDA1351H is a low cost multi-purpose IEC 958 decoder DAC with a variety of operating modes.

In modes 1, 2, 3 and 4 the UDA1351H is clock master; it generates the clock for both the outgoing and incoming digital data streams. Consequently, any device providing data for the UDA1351H via the data input interface in mode 4 will be slave to the clock generated by the UDA1351H.

In mode 5 the UDA1351H locks to signal WSI from the digital data input interface. Conforming to IEC 958, the audio sample frequency of the data input interface must be between 28.0 and 100.0 kHz.

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## 8.2 Clock regeneration and lock detection

The UDA1351H contains an on-board PLL for regenerating a system clock from the IEC 958 input bitstream or the incoming digital data stream via the data input interface. In addition to the system clock for the on-board digital sound processing the PLL also generates a  $256f_s$  clock output for use in the application. In the absence of an input signal the clock will generate a minimum frequency to warrant system functionality.

**Remark:** in case of no input signal, the PLL generates a minimum frequency and the output spectrum shifts accordingly. Since the analog output does not have a analog mute, this means noise which is out of band noise under normal operation conditions, can move into the audio band.

When the on-board clock has locked to the incoming frequency the lock indicator bit will be set and can be read via the L3 interface. Internally the PLL lock indication is combined with the PCM status bit of the input data stream. When both the IEC 958 decoder and the on-board clock have locked to the incoming signal and the input data stream is PCM data, then pin LOCK will be asserted. However, when the IC is locked but the PCM status bit reports non-PCM data then pin LOCK is returned to LOW level.

The lock indication output can be used, for example, for muting purposes. The lock signal can be used to drive an external analog mute circuit to prevent out of band noise to become audible in case the PLL runs at its minimum frequency (e.g. when there is no SPDIF input signal).

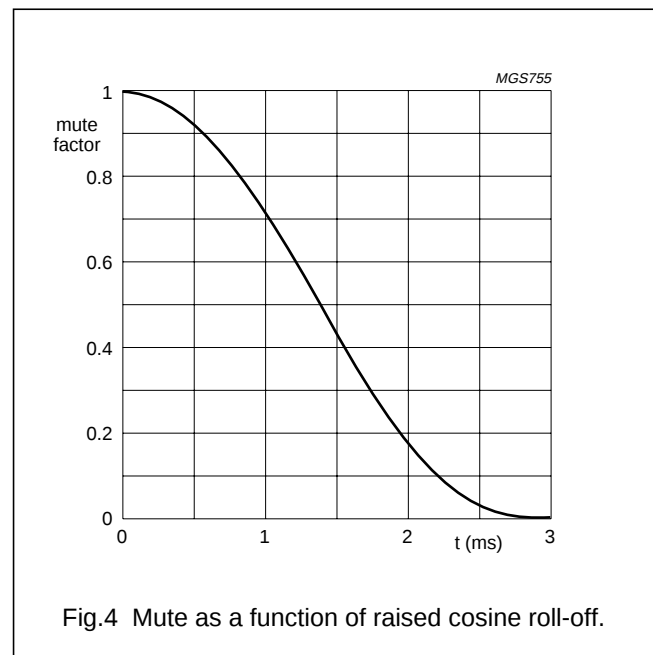
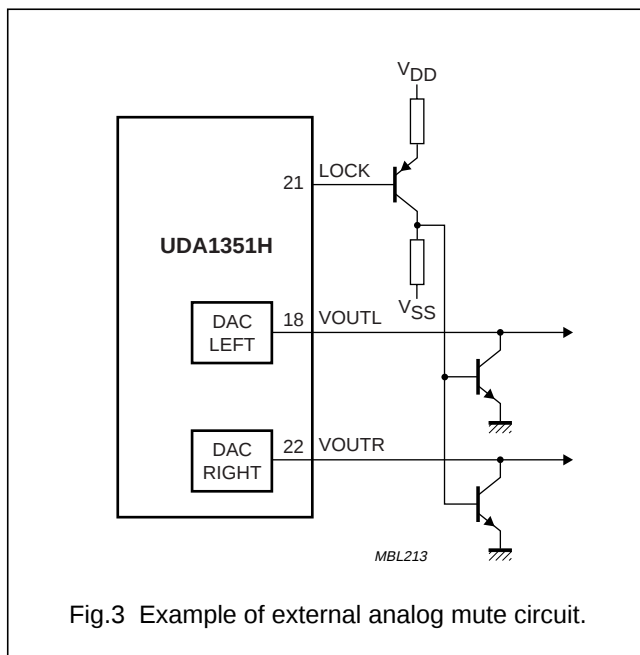
An example is given in Fig.3 where  $V_{DD}$  is the positive power supply and  $V_{SS}$  is the negative power supply.

## 8.3 Mute

The UDA1351H is equipped with a cosine roll-off mute in the DSP data path of the DAC part. Muting the DAC, by pin MUTE (in static mode) or via bit MT (in L3 mode) will result in a soft mute as presented in Fig.4. The cosine roll-off soft mute takes  $32 \times 32$  samples = 24 ms at a sampling frequency of 44.1 kHz.

When operating in the L3 control mode the device will mute on start-up. In L3 mode it is necessary to explicitly switch off the mute for audio output by means of the MT bit in the L3 register.

In the L3 mode pin MUTE does not have any function (the same holds for several other pins) and can either be left open-circuit (since it has an internal pull-down resistor) or be connected to ground.



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## 8.4 Auto mute

By default the outputs of the digital data output interface and the DAC will be muted until the IC is locked, regardless the level on pin MUTE (in static mode) or the state of bit MT of the sound feature register (in L3 mode). In this way only valid data will be passed to the outputs. This mute is done in the SPDIF interface and is a hard mute, not a cosine roll-off mute.

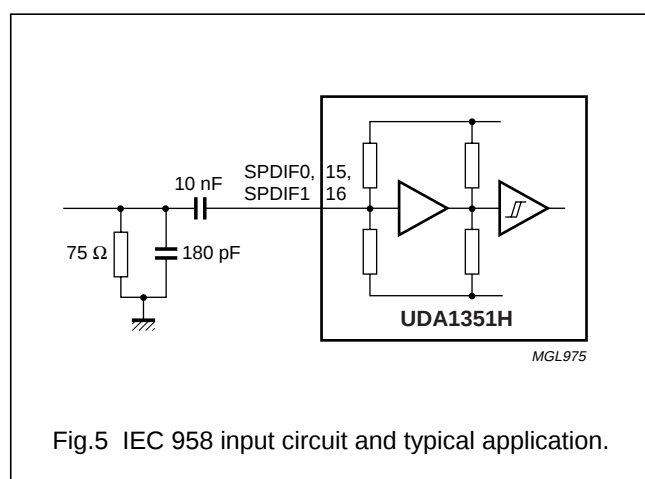
If needed, this muting can be bypassed by setting bit AutoMT to logic 0 via the L3 interface. As a result the IC will no longer mute during out-of-lock situations.

## 8.5 Data path

The UDA1351H data path consists of the slicer and the IEC 958 decoder, the digital data output and input interfaces, the audio feature processor, digital interpolator and noise shaper and the digital-to-analog converters.

## 8.5.1 IEC 958 INPUT

The UDA1351H IEC 958 decoder can select 1 out of 2 IEC 958 input channels. An on-chip amplifier with hysteresis amplifies the IEC 958 input signal to CMOS level (see Fig.5).



All 24 bits of data for left and right are extracted from the input bitstream as well as several of the IEC 958 key channel-status bits.

The extracted key parameters are:

- Pre-emphasis
- Audio sample frequency
- Two-channel PCM indicator
- Clock accuracy.

Both the lock indicator and the key channel status bits are accessible via the L3 interface.

The UDA1351H supports the following sample frequencies and data bit rates:

- $f_s = 32.0$  kHz, resulting in a data rate of 2.048 Mbits/s
- $f_s = 44.1$  kHz, resulting in a data rate of 2.8224 Mbits/s
- $f_s = 48.0$  kHz, resulting in a data rate of 3.072 Mbits/s
- $f_s = 64.0$  kHz, resulting in a data rate of 4.096 Mbits/s
- $f_s = 88.2$  kHz, resulting in a data rate of 5.6448 Mbits/s
- $f_s = 96.0$  kHz, resulting in a data rate of 6.144 Mbits/s.

The UDA1351H supports timing level I, II and III as specified by the IEC 958 standard.

## 8.5.2 SPDIF SELECTION PROCEDURE

**WARNING**

At switching between the two SPDIF inputs, the switching inside the UDA1351H is done instantly. It may occur that SPDIF words inside the SPDIF decoder of the UDA1351H get corrupted. When no action is taken, corrupted data can reach the FSDAC output.

In order to prevent noise at the FSDAC output when switching between the SPDIF inputs, the following procedures are recommended. This procedure uses an external analog mute circuit as shown in Fig.3.

- Static mode:
  - Activate the external analog mute circuit
  - Select the proper SPDIF input signal
  - Activate pin RESET to reset the PLL settings and the PLL will synchronize again to the new input signal
  - De-activate the external analog mute circuit.
- L3 mode:
  - Activate the external analog mute circuit
  - Select the proper SPDIF input signal via the L3 interface
  - Toggle bit RST\_PLL of the L3 interface to reset the PLL and the PLL will synchronize again to the new input signal
  - De-activate the external analog mute circuit.

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## 8.5.3 DIGITAL DATA OUTPUT AND INPUT INTERFACE

The digital data interface enables the exchange of digital data to and from an external signal processing device.

The digital output and input formats are identical by design. The possible formats are (see Fig.6):

- I<sup>2</sup>S-bus with a word length of up to 24 bits
- LSB-justified with a word length of 16 bits
- LSB-justified with a word length of 20 bits
- LSB-justified with a word length of 24 bits.

Important: the edge of the WS signal must fall on the negative edge of the BCK signal at all times for proper operation of the input and output interface (see Fig.9).

In the static pin control mode the format is selected by means of pins L3MODE and L3DATA. In the L3 control mode the format defaults to the I<sup>2</sup>S-bus settings and is programmable via the L3 interface.

The IEC 958 decoder provides the pre-emphasis information from the IEC 958 input bitstream to pins PREEM0 and PREEM1 and to the L3 interface register.

Controlling the de-emphasis is different for the 2 modes:

- Static pin control mode:
  - For IEC 958 input de-emphasis is automatically done, but for I<sup>2</sup>S-bus input de-emphasis is not possible.
- L3 control mode:
  - IEC 958 input: bit SPDSEL must be set to logic 1 and de-emphasis is done automatically
  - I<sup>2</sup>S-bus input: bit SPDSEL must be set to logic 0 and de-emphasis can be controlled via bits DE0 and DE1.

## 8.5.4 AUDIO FEATURE PROCESSOR

The audio feature processor automatically provides de-emphasis for the IEC 958 data stream in the static pin control mode and default mute at start-up in the L3 control mode. When used in the L3 control mode it provides the following additional features:

- Volume control using 6 bits
- Bass boost control using 4 bits
- Treble control using 2 bits
- Mode selection of the sound processing bass boost and treble filters: flat, minimum and maximum
- Soft mute control with raised cosine roll-off
- De-emphasis selection of the incoming data stream for  $f_s = 32.0$ , 44.1 and 48.0 kHz.

## 8.5.5 INTERPOLATOR

The UDA1351H includes an on-board interpolating filter which converts the incoming data stream from  $1f_s$  to  $128f_s$  by cascading a recursive filter and a FIR filter.

**Table 2** Interpolator characteristics

| PARAMETER        | CONDITIONS          | VALUE (dB) |
|------------------|---------------------|------------|
| Pass-band ripple | $0f_s$ to $0.45f_s$ | $\pm 0.03$ |
| Stop band        | $>0.65f_s$          | -50        |
| Dynamic range    | $0f_s$ to $0.45f_s$ | 115        |
| DC gain          | –                   | -3.5       |

## 8.5.6 NOISE SHAPER

The third-order noise shaper operates at  $128f_s$ . It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a filter stream digital-to-analog converter.

## 8.5.7 FILTER STREAM DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage.

The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC is scaled proportionally with the power supply voltage.

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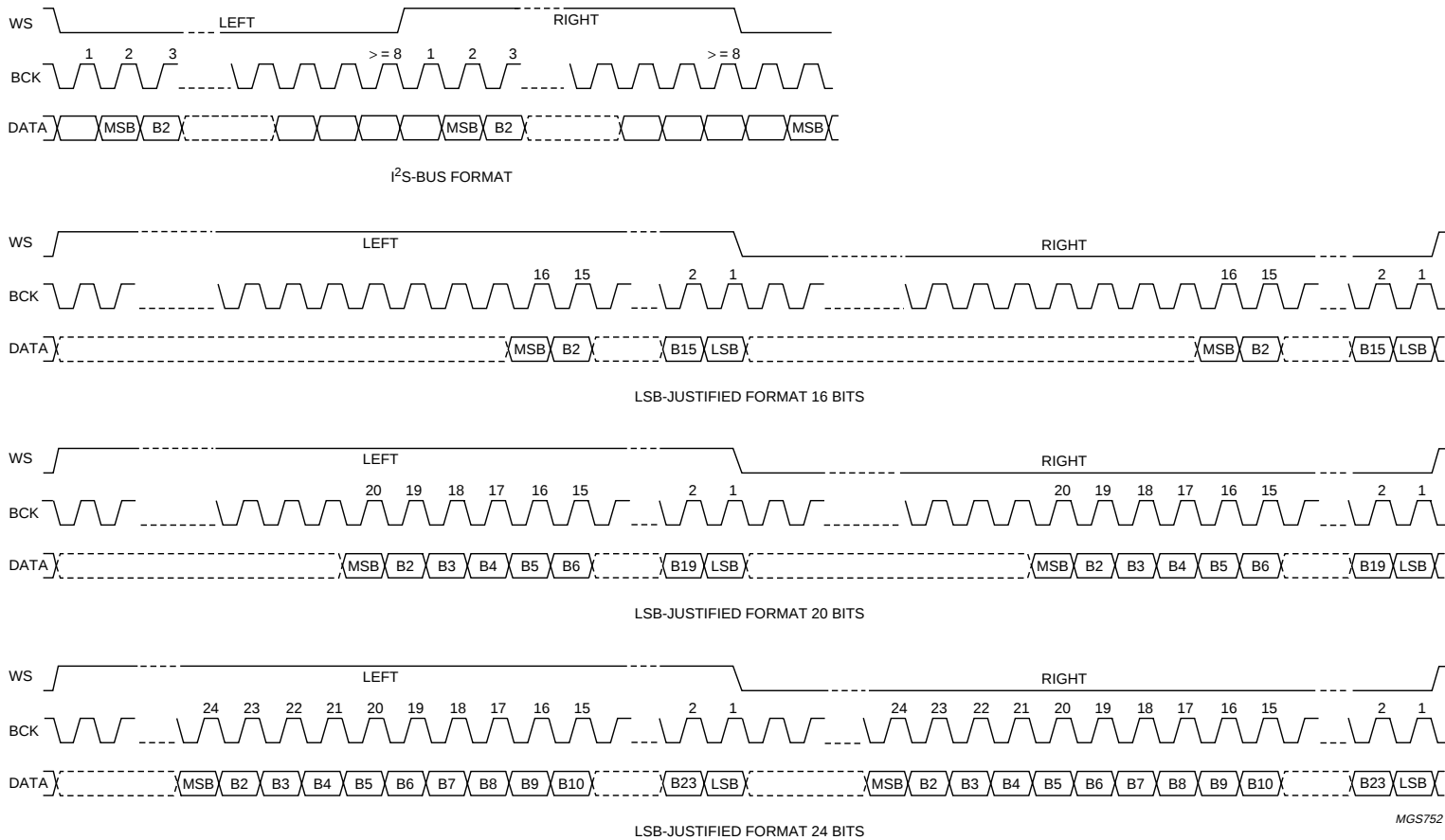


Fig.6 Digital data interface formats.

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## 8.6 Control

The UDA1351H can be controlled by means of static pins or via the L3 interface. For optimum use of the features of the UDA1351H the L3 control mode is recommended since only basic functions are available in the static pin control mode.

It should be noted that the static pin control mode and L3 control mode are mutual exclusive. In the static pin control mode pins L3MODE and L3DATA are used to select the format for the data output and input interface.

## 8.6.1 STATIC PIN CONTROL MODE

The default values for all non-pin controlled settings are identical to the default values at start-up in the L3 control mode.

**Table 3** Pin description of static pin control mode

| PIN                | NAME              | VALUE | FUNCTION                                                                          |
|--------------------|-------------------|-------|-----------------------------------------------------------------------------------|
| Mode selection pin |                   |       |                                                                                   |
| 35                 | SELSTATIC         | 1     | select static pin control mode; must be connected to V <sub>DD</sub>              |
| Input pins         |                   |       |                                                                                   |
| 1                  | RESET             | 0     | normal operation                                                                  |
|                    |                   | 1     | reset                                                                             |
| 6                  | L3CLOCK           | 0     | must be connected to V <sub>SSD</sub>                                             |
| 10 and 5           | L3MODE and L3DATA | 00    | select I <sup>2</sup> S-bus format for digital data interface                     |
|                    |                   | 01    | select LSB-justified format 16 bits for digital data interface                    |
|                    |                   | 10    | select LSB-justified format 20 bits for digital data interface                    |
|                    |                   | 11    | select LSB-justified format 24 bits for digital data interface                    |
| 12                 | MUTE              | 0     | normal operation                                                                  |
|                    |                   | 1     | mute active                                                                       |
| 13                 | SELCHAN           | 0     | select input SPDIF0 (channel 0)                                                   |
|                    |                   | 1     | select input SPDIF1 (channel 1)                                                   |
| 19                 | SELCLK            | 0     | slave to f <sub>s</sub> from IEC 958; master on data output and input interfaces  |
|                    |                   | 1     | slave to f <sub>s</sub> from digital data input interface                         |
| 20                 | SELSPDIF          | 0     | select data from digital data interface to DAC output                             |
|                    |                   | 1     | select data from IEC 958 decoder to DAC output                                    |
| Status pins        |                   |       |                                                                                   |
| 21                 | LOCK              | 0     | clock regeneration or IEC 958 decoder out-of-lock <b>or</b> non-PCM data detected |
|                    |                   | 1     | clock regeneration and IEC 958 decoder locked <b>plus</b> PCM data detected       |
| 30 and 42          | PREEM1 and PREEM0 | 00    | IEC 958 input: no pre-emphasis                                                    |
|                    |                   | 01    | IEC 958 input: f <sub>s</sub> = 32.0 kHz with pre-emphasis                        |
|                    |                   | 10    | IEC 958 input: f <sub>s</sub> = 44.1 kHz with pre-emphasis                        |
|                    |                   | 11    | IEC 958 input: f <sub>s</sub> = 48.0 kHz with pre-emphasis                        |
| Test pins          |                   |       |                                                                                   |
| 23                 | TC                | 0     | must be connected to digital ground (V <sub>SSD</sub> )                           |
| 34                 | TEST1             | 1     | must be connected to digital supply voltage (V <sub>DD</sub> )                    |
| 39                 | TEST2             | 0     | must be connected to digital ground (V <sub>SSD</sub> )                           |
| 44                 | RTCB              | 0     | must be connected to digital ground (V <sub>SSD</sub> )                           |

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## 8.6.2 L3 CONTROL MODE

The L3 control mode allows maximum flexibility in controlling the UDA1351H.

It should be noted that in the L3 control mode several base-line functions are still controlled by pins on the device and that on start-up in the L3 control mode the output is explicitly muted by bit MT via the L3 interface.

Also it should be noted that in using the L3 control mode, an initialization string is needed after power-up of the device for reliable operation.

**Table 4** Pin description in the L3 control mode

| PIN                | NAME              | VALUE | FUNCTION                                                      |
|--------------------|-------------------|-------|---------------------------------------------------------------|
| Mode selection pin |                   |       |                                                               |
| 35                 | SELSTATIC         | 0     | select L3 control mode; must be connected to V <sub>SSD</sub> |
| Input pins         |                   |       |                                                               |
| 1                  | RESET             | 0     | normal operation                                              |
|                    |                   | 1     | reset                                                         |
| 5                  | L3DATA            | –     | must be connected to the L3-bus                               |
| 6                  | L3CLOCK           | –     | must be connected to the L3-bus                               |
| 10                 | L3MODE            | –     | must be connected to the L3-bus                               |
| Status pins        |                   |       |                                                               |
| 21                 | LOCK              | 0     | clock regeneration or IEC 958 decoder out-of-lock             |
|                    |                   | 1     | clock regeneration and IEC 958 decoder locked                 |
| 30 and 42          | PREEM1 and PREEM0 | 00    | IEC 958 input: no pre-emphasis                                |
|                    |                   | 01    | IEC 958 input: f <sub>s</sub> = 32.0 kHz with pre-emphasis    |
|                    |                   | 10    | IEC 958 input: f <sub>s</sub> = 44.1 kHz with pre-emphasis    |
|                    |                   | 11    | IEC 958 input: f <sub>s</sub> = 48.0 kHz with pre-emphasis    |
| Test pins          |                   |       |                                                               |
| 23                 | TC                | 0     | must be connected to ground (V <sub>SSD</sub> )               |
| 34                 | TEST1             | 1     | must be connected to supply voltage (V <sub>DD</sub> )        |
| 39                 | TEST2             | 0     | must be connected to ground (V <sub>SSD</sub> )               |
| 44                 | RTCB              | 0     | must be connected to ground (V <sub>SSD</sub> )               |

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**8.7 L3 interface****8.7.1 GENERAL**

The UDA1351H has an L3 microcontroller interface and all the digital sound processing features and various system settings can be controlled by a microcontroller.

The controllable settings are:

- Restoring L3 defaults
- Power-on
- Selection of input channel, clock source, DAC input and external input format
- Selection of filter mode and settings of treble and bass boost
- Volume settings
- Selection of soft mute via cosine roll-off (only effective in L3 control mode) and bypass of auto mute
- Selection of de-emphasis.

The readable settings are:

- Mute status of interpolator
- PLL locked
- SPDIF input signal locked
- Audio Sample Frequency (ASF)
- Valid PCM data detected
- Pre-emphasis of the IEC 958 input signal
- ACCuracy of the Clock (ACC).

The exchange of data and control information between the microcontroller and the UDA1351H is LSB first and is accomplished through a serial hardware L3 interface comprising the following pins:

- L3DATA: data line
- L3MODE: mode line
- L3CLK: clock line.

The exchange of bytes via the L3 interface is LSB first.

The L3 format has 2 modes of operation:

- Address mode
- Data transfer mode.

The address mode is used to select a device for a subsequent data transfer. The address mode is characterized by L3MODE being LOW and a burst of 8 pulses on L3CLOCK, accompanied by 8 bits (see Fig.7).

The data transfer mode is characterized by L3MODE being HIGH and is used to transfer one or more bytes representing a register address, instruction or data.

Basically 2 types of data transfers can be defined:

- Write action: data transfer to the device
- Read action: data transfer from the device.

Remark: when the device is powered up, at least one L3CLOCK pulse must be given to the L3 interface to wake-up the interface before starting sending to the device (see Fig.7). This is only needed once after the device is powered up.

**8.7.2 DEVICE ADDRESSING**

The device address consists of 1 byte with:

- Bits 0 and 1 (called DOM bits) representing the type of data transfer (see Table 5)
- Bits 2 to 7 (address bits) representing a 6-bit device address.

**Table 5** Selection of data transfer

| DOM   |       | TRANSFER                   |
|-------|-------|----------------------------|
| BIT 0 | BIT 1 |                            |
| 0     | 0     | not used                   |
| 1     | 0     | not used                   |
| 0     | 1     | write data or prepare read |
| 1     | 1     | read data                  |

**8.7.3 REGISTER ADDRESSING**

After sending the device address, including Data Operating Mode (DOM) bits indicating whether the information is to be read or written, 1 data byte is sent using bit 0 to indicate whether the information will be read or written and bits 1 to 7 for the destination register address.

Basically there are 3 methods for register addressing:

1. Addressing for write data: bit 0 is logic 0 indicating a write action to the destination register, followed by bits 1 to 7 indicating the register address (see Fig.7)
2. Addressing for prepare read: bit 0 is logic 1 indicating that data will be read from the register (see Fig.8)
3. Addressing for data read action: in this case the device returns a register address prior to sending data from that register. When bit 0 is logic 0, the register address is valid; in case bit 0 is logic 1 the register address is invalid.

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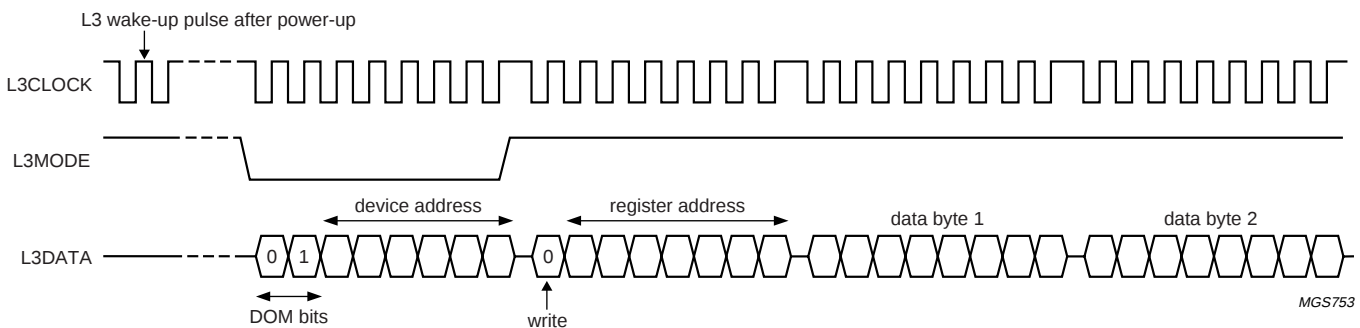


Fig.7 Data write mode (for L3 version 2).

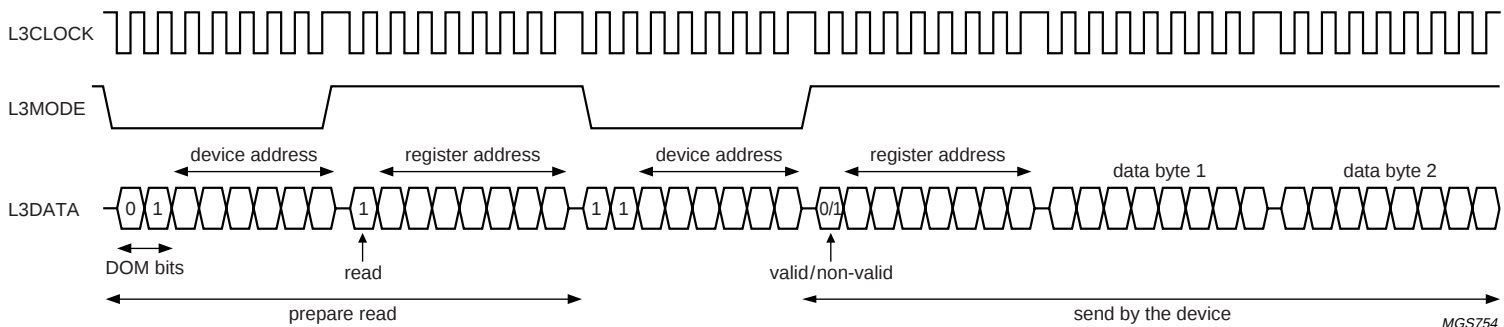


Fig.8 Data read mode.

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## 8.7.4 DATA WRITE MODE

The data write mode is explained in the signal diagram of Fig.7. For writing data to a device, 4 bytes must be sent (see Table 6):

1. One byte starting with '01' for signalling the write action to the device, followed by the device address ('011000' for the UDA1351H)
2. One byte starting with a '0' for signalling the write action, followed by 7 bits indicating the destination address in binary format with A6 being the MSB and A0 being the LSB
3. Two data bytes with D15 being the MSB and D0 being the LSB.

**Remark:** each time a new destination register address needs to be written, the device address must be sent again.

## 8.7.5 DATA READ MODE

For reading data from the device, first a prepare read must be done and then data read. The data read mode is explained in the signal diagram of Fig.8.

For reading data from a device, the following 6 bytes are involved (see Table 7):

1. One byte with the device address including '01' for signalling the write action to the device
2. One byte is sent with the register address from which data needs to be read; this byte starts with a '1', which indicates that there will be a read action from the register, followed again by 7 bits for the destination address in binary format with A6 being the MSB and A0 being the LSB
3. One byte with the device address including '11' is sent to the device; the '11' indicates that the device must write data to the microcontroller
4. One byte, sent by the device to the bus, with the (requested) register address and a flag bit indicating whether the requested register was valid (bit is logic 0) or invalid (bit is logic 1)
5. Two bytes, sent by the device to the bus, with the data information in binary format with D15 being the MSB and D0 being the LSB.

Table 6 L3 write data

| BYTE | L3 MODE       | ACTION           | FIRST IN TIME |       |       |       |       | LATEST IN TIME |       |       |
|------|---------------|------------------|---------------|-------|-------|-------|-------|----------------|-------|-------|
|      |               |                  | BIT 0         | BIT 1 | BIT 2 | BIT 3 | BIT 4 | BIT 5          | BIT 6 | BIT 7 |
| 1    | address       | device address   | 0             | 1     | 0     | 1     | 1     | 0              | 0     | 0     |
| 2    | data transfer | register address | 0             | A6    | A5    | A4    | A3    | A2             | A1    | A0    |
| 3    | data transfer | data byte 1      | D15           | D14   | D13   | D12   | D11   | D10            | D9    | D8    |
| 4    | data transfer | data byte 2      | D7            | D6    | D5    | D4    | D3    | D2             | D1    | D0    |

Table 7 L3 read data

| BYTE | L3 MODE       | ACTION           | FIRST IN TIME |       |       |       |       | LATEST IN TIME |       |       |
|------|---------------|------------------|---------------|-------|-------|-------|-------|----------------|-------|-------|
|      |               |                  | BIT 0         | BIT 1 | BIT 2 | BIT 3 | BIT 4 | BIT 5          | BIT 6 | BIT 7 |
| 1    | address       | device address   | 0             | 1     | 0     | 1     | 1     | 0              | 0     | 0     |
| 2    | data transfer | register address | 1             | A6    | A5    | A4    | A3    | A2             | A1    | A0    |
| 3    | address       | device address   | 1             | 1     | 0     | 1     | 1     | 0              | 0     | 0     |
| 4    | data transfer | register address | 0 or 1        | A6    | A5    | A4    | A3    | A2             | A1    | A0    |
| 5    | data transfer | data byte 1      | D15           | D14   | D13   | D12   | D11   | D10            | D9    | D8    |
| 6    | data transfer | data byte 2      | D7            | D6    | D5    | D4    | D3    | D2             | D1    | D0    |

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## 8.7.6 INITIALIZATION STRING

For proper and reliable operation it is needed that the UDA1351H is initialized in the L3 control mode. This is needed to have the PLL start up after power-up of the device under all conditions. The initialization string is given in Table 8.

**Table 8** L3 init string and set defaults after power-up.

| BYTE | L3 MODE       | ACTION       |                  | FIRST IN TIME |       |       |       |       | LATEST IN TIME |       |       |
|------|---------------|--------------|------------------|---------------|-------|-------|-------|-------|----------------|-------|-------|
|      |               |              |                  | BIT 0         | BIT 1 | BIT 2 | BIT 3 | BIT 4 | BIT 5          | BIT 6 | BIT 7 |
| 1    | address       | init string  | device address   | 0             | 1     | 0     | 1     | 1     | 0              | 0     | 0     |
| 2    | data transfer |              | register address | 0             | 1     | 0     | 0     | 0     | 0              | 0     | 0     |
| 3    | data transfer |              | data byte 1      | 0             | 0     | 0     | 0     | 0     | 0              | 0     | 0     |
| 4    | data transfer |              | data byte 2      | 0             | 0     | 0     | 0     | 0     | 0              | 1     | 1     |
| 5    | address       | set defaults | device address   | 0             | 1     | 0     | 1     | 1     | 0              | 0     | 0     |
| 6    | data transfer |              | register address | 0             | 1     | 1     | 1     | 1     | 1              | 1     | 1     |
| 7    | data transfer |              | data byte 1      | 0             | 0     | 0     | 0     | 0     | 0              | 0     | 0     |
| 8    | data transfer |              | data byte 2      | 0             | 0     | 0     | 0     | 0     | 0              | 0     | 0     |

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## 8.7.7 OVERVIEW OF L3 INTERFACE REGISTERS

**Table 9** UDA1351H register map

| ADDR              | FUNCTION                        | BIT |     |     |     |     |          |         |          |      |         |                  |                  |                  |                  |         |         |
|-------------------|---------------------------------|-----|-----|-----|-----|-----|----------|---------|----------|------|---------|------------------|------------------|------------------|------------------|---------|---------|
|                   |                                 | D15 | D14 | D13 | D12 | D11 | D10      | D9      | D8       | D7   | D6      | D5               | D4               | D3               | D2               | D1      | D0      |
| Writable settings |                                 |     |     |     |     |     |          |         |          |      |         |                  |                  |                  |                  |         |         |
| 00H               | system parameters               |     |     | PON |     |     | CHAN sel | IIS sel |          |      | SPD sel |                  | SFOR1            | SFOR0            |                  |         |         |
|                   | default                         |     |     | 1   |     |     | 0        | 0       |          |      | 1       |                  | 0                | 0                |                  |         |         |
| 10H               | sound features                  |     |     | M1  | M0  | BB3 | BB2      | BB1     | BB0      |      |         |                  | TR1              | TR0              | DE1              | DE0     | MT      |
|                   | default                         |     |     | 0   | 0   | 0   | 0        | 0       | 0        |      |         |                  | 0                | 0                | 0                | 0       | 1       |
| 11H               | volume control DAC              |     |     |     |     |     |          |         |          |      |         | VC5              | VC4              | VC3              | VC2              | VC1     | VC0     |
|                   | default                         |     |     |     |     |     |          |         |          |      |         | 0                | 0                | 0                | 0                | 0       | 0       |
| 40H               | multiplex parameters            |     |     |     |     |     |          |         |          |      |         |                  |                  |                  |                  | Auto MT | RST PLL |
|                   | default                         |     |     |     |     |     |          |         |          |      |         | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 1       | 0       |
| 7FH               | restore L3 defaults             |     |     |     |     |     |          |         |          |      |         |                  |                  |                  |                  |         |         |
| Readable settings |                                 |     |     |     |     |     |          |         |          |      |         |                  |                  |                  |                  |         |         |
| 18H               | interpolator parameters         |     |     |     |     |     |          |         |          |      |         |                  |                  |                  |                  |         | MT stat |
| 38H               | SPDIF input and lock parameters |     |     |     |     |     | PLL lock |         | SPD lock | ASF1 | ASF0    | PCM stat         |                  | PRE              |                  | ACC1    | ACC0    |

**Note**

1. When writing new settings via the L3 interface, these bits should always remain logic 0 (default value) to warrant correct operation.

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## 8.7.8 WRITABLE REGISTERS

## 8.7.8.1 Restoring L3 defaults

By writing to the 7FH register, all L3 control values are restored to their default values. Only the L3 interface is affected, the system will not be reset. Consequently readable registers, which are not reset, can be affected.

## 8.7.8.2 Power-on

A 1-bit value to switch the DAC on and off.

**Table 10** Power-on setting

| PON | FUNCTION                   |
|-----|----------------------------|
| 0   | power-down                 |
| 1   | power-on (default setting) |

## 8.7.8.3 Slicer input selection

A 1-bit value to select an IEC 958 input channel.

**Table 11** Slicer input selection

| CHAN sel | FUNCTION                                        |
|----------|-------------------------------------------------|
| 0        | IEC 958 input from pin SPDIF0 (default setting) |
| 1        | IEC 958 input from pin SPDIF1                   |

## 8.7.8.4 Clock source selection

A 1-bit value to select the source for clock regeneration, either from the IEC 958 input or digital data input interface. In the event that the IEC 958 input is used as a clock source the UDA1351H is clock master on the digital data output and input interfaces.

**Table 12** Clock source selection

| IIS sel | FUNCTION                                                             |
|---------|----------------------------------------------------------------------|
| 0       | slave to audio sampling frequency of IEC 958 input (default setting) |
| 1       | slave to audio sampling frequency of digital data input interface    |

## 8.7.8.5 DAC input selection

A 1-bit value to select the data source, either the IEC 958 input or the digital data input interface.

**Table 13** DAC input selection

| SPD sel | FUNCTION                             |
|---------|--------------------------------------|
| 0       | input from data input interface      |
| 1       | input from IEC 958 (default setting) |

## 8.7.8.6 Serial format selection

A 2-bit value to set the serial format for the digital data output and input interfaces.

**Table 14** Serial format settings

| SFOR1 | SFOR0 | FUNCTION                                |
|-------|-------|-----------------------------------------|
| 0     | 0     | I <sup>2</sup> S-bus (default settings) |
| 0     | 1     | LSB-justified, 16 bits                  |
| 1     | 0     | LSB-justified, 20 bits                  |
| 1     | 1     | LSB-justified, 24 bits                  |

## 8.7.8.7 Filter mode selection

A 2-bit value to program the mode for the sound processing filters of bass boost and treble.

**Table 15** Filter mode settings

| M1 | M0 | FUNCTION               |
|----|----|------------------------|
| 0  | 0  | flat (default setting) |
| 0  | 1  | minimum                |
| 1  | 0  |                        |
| 1  | 1  | maximum                |

## 8.7.8.8 Treble

A 2-bit value to program the treble setting in combination with the filter mode settings. At  $f_s = 44.1$  kHz the  $-3$  dB point for minimum setting is 3.0 kHz and the  $-3$  dB point for maximum setting is 1.5 kHz. The default value is '00'.

**Table 16** Treble settings

| TR1 | TR0 | LEVEL     |           |           |
|-----|-----|-----------|-----------|-----------|
|     |     | FLAT (dB) | MIN. (dB) | MAX. (dB) |
| 0   | 0   | 0         | 0         | 0         |
| 0   | 1   | 0         | 2         | 2         |
| 1   | 0   | 0         | 4         | 4         |
| 1   | 1   | 0         | 6         | 6         |

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## 8.7.8.9 Bass boost

A 4-bit value to program the bass boost setting in combination with the filter mode settings. At  $f_s = 44.1$  kHz the  $-3$  dB point for minimum setting is 250 Hz and the  $-3$  dB point for maximum setting is 300 Hz. The default value is '0000'.

**Table 17** Bass boost settings

| BB3 | BB2 | BB1 | BB0 | LEVEL     |           |           |
|-----|-----|-----|-----|-----------|-----------|-----------|
|     |     |     |     | FLAT (dB) | MIN. (dB) | MAX. (dB) |
| 0   | 0   | 0   | 0   | 0         | 0         | 0         |
| 0   | 0   | 0   | 1   | 0         | 2         | 2         |
| 0   | 0   | 1   | 0   | 0         | 4         | 4         |
| 0   | 0   | 1   | 1   | 0         | 6         | 6         |
| 0   | 1   | 0   | 0   | 0         | 8         | 8         |
| 0   | 1   | 0   | 1   | 0         | 10        | 10        |
| 0   | 1   | 1   | 0   | 0         | 12        | 12        |
| 0   | 1   | 1   | 1   | 0         | 14        | 14        |
| 1   | 0   | 0   | 0   | 0         | 16        | 16        |
| 1   | 0   | 0   | 1   | 0         | 18        | 18        |
| 1   | 0   | 1   | 0   | 0         | 18        | 20        |
| 1   | 0   | 1   | 1   | 0         | 18        | 22        |
| 1   | 1   | 0   | 0   | 0         | 18        | 24        |
| 1   | 1   | 0   | 1   | 0         | 18        | 24        |
| 1   | 1   | 1   | 0   | 0         | 18        | 24        |
| 1   | 1   | 1   | 1   | 0         | 18        | 24        |

## 8.7.8.10 De-emphasis

A 2-bit value to enable the digital de-emphasis filter.

**Table 18** De-emphasis selection

| DE1 | DE0 | FUNCTION                |
|-----|-----|-------------------------|
| 0   | 0   | other (default setting) |
| 0   | 1   | $f_s = 32.0$ kHz        |
| 1   | 0   | $f_s = 44.1$ kHz        |
| 1   | 1   | $f_s = 48.0$ kHz        |

## 8.7.8.11 Soft mute

A 1-bit value to enable the digital mute.

**Table 19** Soft mute selection

| MT | FUNCTION                 |
|----|--------------------------|
| 0  | no muting                |
| 1  | muting (default setting) |

## 8.7.8.12 Volume control

A 6-bit value to program the left and right channel volume attenuation. The range is from 0 to  $-60$  dB and  $-\infty$  dB in steps of 1 dB.

**Table 20** Volume settings

| VC5 | VC4 | VC3 | VC2 | VC1 | VC0 | VOLUME (dB) |
|-----|-----|-----|-----|-----|-----|-------------|
| 0   | 0   | 0   | 0   | 0   | 0   | 0           |
| 0   | 0   | 0   | 0   | 0   | 1   | 0           |
| 0   | 0   | 0   | 0   | 1   | 0   | -1          |
| 0   | 0   | 0   | 0   | 1   | 1   | -2          |
| :   | :   | :   | :   | :   | :   | :           |
| 1   | 1   | 0   | 0   | 1   | 1   | -51         |
| 1   | 1   | 0   | 1   | 0   | 0   |             |
| 1   | 1   | 0   | 1   | 0   | 1   | -52         |
| 1   | 1   | 0   | 1   | 1   | 0   |             |
| 1   | 1   | 0   | 1   | 1   | 1   | -54         |
| 1   | 1   | 1   | 0   | 0   | 0   |             |
| 1   | 1   | 1   | 0   | 0   | 1   | -57         |
| 1   | 1   | 1   | 0   | 1   | 0   |             |
| 1   | 1   | 1   | 0   | 1   | 1   |             |
| 1   | 1   | 1   | 1   | 0   | 0   | -60         |
| 1   | 1   | 1   | 1   | 0   | 1   |             |
| 1   | 1   | 1   | 1   | 1   | 0   | $-\infty$   |
| 1   | 1   | 1   | 1   | 1   | 1   |             |

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## 8.7.8.13 Auto mute

A 1-bit value to activate mute during out-of-lock. In normal operation the output is automatically hard muted when an out-of-lock situation is detected. Setting this bit to logic 0 will disable that function.

**Table 21** Auto mute setting

| Auto MT | FUNCTION                                         |
|---------|--------------------------------------------------|
| 0       | do not mute output during out-of-lock            |
| 1       | mute output during out-of-lock (default setting) |

## 8.7.8.14 PLL reset

A 1-bit value to reset the PLL. This is the bit which is set in the initialization string. When this bit is asserted, the PLL will be reset and the output clock of the PLL will be forced to its lowest value, which is in the area of a few MHz.

**Table 22** PLL reset

| RST PLL | FUNCTION                   |
|---------|----------------------------|
| 0       | normal operation (default) |
| 1       | PLL is reset               |

## 8.7.9 READABLE REGISTERS

## 8.7.9.1 Mute status

A 1-bit value indicating whether the interpolator is muting or not muting.

**Table 23** Interpolator mute status

| MT stat | FUNCTION  |
|---------|-----------|
| 0       | no muting |
| 1       | muting    |

## 8.7.9.2 PLL lock detection

A 1-bit value indicating that the clock regeneration is locked.

**Table 24** PLL lock indication

| PLL lock | FUNCTION    |
|----------|-------------|
| 0        | out-of-lock |
| 1        | locked      |

## 8.7.9.3 SPDIF lock detection

A 1-bit value indicating the IEC 958 decoder is locked and is decoding correct data.

**Table 25** SPDIF lock detection

| SPD lock | FUNCTION                                   |
|----------|--------------------------------------------|
| 0        | not locked <b>or</b> non-PCM data detected |
| 1        | locked <b>and</b> PCM data detected        |

## 8.7.9.4 Audio sample frequency detection

A 2-bit value indicating the audio sample frequency of the IEC 958 input signal.

**Table 26** Audio sample frequency detection

| ASF1 | ASF0 | FUNCTION  |
|------|------|-----------|
| 0    | 0    | 44.1 kHz  |
| 0    | 1    | undefined |
| 1    | 0    | 48.0 kHz  |
| 1    | 1    | 32.0 kHz  |

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## 8.7.9.5 PCM detection

A 1-bit value which indicates whether the IEC 958 input contains PCM audio data or other binary data.

**Table 27** Two-channel PCM input detection

| PCM stat | FUNCTION                         |
|----------|----------------------------------|
| 0        | input with 2 channel PCM data    |
| 1        | input without 2 channel PCM data |

## 8.7.9.6 Pre-emphasis detection

A 1-bit value which indicates whether the pre-emphasis bit was set on the IEC 958 input signal or not set.

**Table 28** Pre-emphasis detection

| PRE | FUNCTION        |
|-----|-----------------|
| 0   | no pre-emphasis |
| 1   | pre-emphasis    |

## 8.7.9.7 Clock accuracy detection

A 2-bit value indicating the timing accuracy of the IEC 958 input signal is conforming to the IEC 958 specification.

**Table 29** Input signal accuracy detection

| ACC1 | ACC0 | FUNCTION  |
|------|------|-----------|
| 0    | 0    | level II  |
| 0    | 1    | level I   |
| 1    | 0    | level III |
| 1    | 1    | undefined |

## 9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL         | PARAMETER                      | CONDITIONS                               | MIN.  | MAX.  | UNIT |
|----------------|--------------------------------|------------------------------------------|-------|-------|------|
| $V_{DD}$       | supply voltage                 | note 1                                   | 2.7   | 5.0   | V    |
| $T_{xtal}$     | crystal temperature            |                                          | -25   | +150  | °C   |
| $T_{stg}$      | storage temperature            |                                          | -65   | +125  | °C   |
| $T_{amb}$      | ambient temperature            |                                          | -40   | +85   | °C   |
| $V_{es}$       | electrostatic handling voltage | Human Body Model (HBM); note 2           | -2000 | +2000 | V    |
|                |                                | Machine Model (MM)                       | -200  | +200  | V    |
| $I_{lu(prot)}$ | latch-up protection current    | note 3                                   | —     | 200   | mA   |
| $I_{sc(DAC)}$  | short-circuit current of DAC   | note 4                                   |       |       |      |
|                |                                | output short-circuited to $V_{SSA(DAC)}$ | —     | 482   | mA   |
|                |                                | output short-circuited to $V_{DDA(DAC)}$ | —     | 346   | mA   |

## Notes

1. All  $V_{DD}$  and  $V_{SS}$  connections must be made to the same power supply.
2. JEDEC class 2 compliant, except pin  $V_{SSA(PLL)}$  which can withstand ESD pulses of -1600 to +1600 V.
3. Latch-up test at  $T_{amb} = 125$  °C and  $V_{DD} = 3.6$  V.
4. Short-circuit test at  $T_{amb} = 0$  °C and  $V_{DD} = 3$  V. DAC operation after short-circuiting cannot be warranted.

## 10 THERMAL CHARACTERISTICS

| SYMBOL        | PARAMETER                                   | CONDITIONS  | VALUE | UNIT |
|---------------|---------------------------------------------|-------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 63    | K/W  |

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**11 CHARACTERISTICS**

$V_{DDD} = V_{DDA} = 3.0\text{ V}$ ; IEC 958 input with  $f_s = 48.0\text{ kHz}$ ;  $T_{amb} = 25\text{ °C}$ ;  $R_L = 5\text{ k}\Omega$ ; all voltages measured with respect to ground; unless otherwise specified.

| SYMBOL                              | PARAMETER                       | CONDITIONS                                | MIN.                 | TYP.                 | MAX.                  | UNIT |
|-------------------------------------|---------------------------------|-------------------------------------------|----------------------|----------------------|-----------------------|------|
| Supplies; note 1                    |                                 |                                           |                      |                      |                       |      |
| V <sub>DDA</sub>                    | analog supply voltage           |                                           | 2.7                  | 3.0                  | 3.6                   | V    |
| V <sub>DDA(DAC)</sub>               | analog supply voltage for DAC   |                                           | 2.7                  | 3.0                  | 3.6                   | V    |
| V <sub>DDA(PLL)</sub>               | analog supply voltage for PLL   |                                           | 2.7                  | 3.0                  | 3.6                   | V    |
| V <sub>DDD</sub>                    | digital supply voltage          |                                           | 2.7                  | 3.0                  | 3.6                   | V    |
| V <sub>DDD(C)</sub>                 | digital supply voltage for core |                                           | 2.7                  | 3.0                  | 3.6                   | V    |
| I <sub>DDA(DAC)</sub>               | analog supply current of DAC    | power-on                                  | –                    | 8.0                  | –                     | mA   |
|                                     |                                 | power-down                                | –                    | 750                  | –                     | μA   |
| I <sub>DDA(PLL)</sub>               | analog supply current of PLL    | at 48 kHz                                 | –                    | 0.7                  | –                     | mA   |
|                                     |                                 | at 96 kHz                                 | –                    | 1.0                  | –                     | mA   |
| I <sub>DDD(C)</sub>                 | digital supply current of core  | at 48 kHz                                 | –                    | 16.0                 | –                     | mA   |
|                                     |                                 | at 96 kHz                                 | –                    | 24.5                 | –                     | mA   |
| I <sub>DDD</sub>                    | digital supply current          | at 48 kHz                                 | –                    | 2.0                  | –                     | mA   |
|                                     |                                 | at 96 kHz                                 | –                    | 3.0                  | –                     | mA   |
| P                                   | power consumption at 48 kHz     | DAC in playback mode                      | –                    | 80                   | –                     | mW   |
|                                     |                                 | DAC in Power-down mode                    | –                    | 58                   | –                     | mW   |
|                                     | power consumption at 96 kHz     | DAC in playback mode                      | –                    | 109                  | –                     | mW   |
|                                     |                                 | DAC in Power-down mode                    | –                    | 87                   | –                     | mW   |
| Digital input pins                  |                                 |                                           |                      |                      |                       |      |
| V <sub>IH</sub>                     | HIGH-level input voltage        |                                           | 0.8V <sub>DD</sub>   | –                    | V <sub>DD</sub> + 0.5 | V    |
| V <sub>IL</sub>                     | LOW-level input voltage         |                                           | –0.5                 | –                    | +0.2V <sub>DD</sub>   | V    |
| V <sub>hys(RESET)</sub>             | hysteresis voltage on pin RESET |                                           | –                    | 0.8                  | –                     | V    |
| I <sub>LI</sub>                     | input leakage current           |                                           | –                    | –                    | 10                    | μA   |
| C <sub>i</sub>                      | input capacitance               |                                           | –                    | –                    | 10                    | pF   |
| R <sub>pu(int)</sub>                | internal pull-up resistance     |                                           | 16                   | 33                   | 78                    | kΩ   |
| R <sub>pd(int)</sub>                | internal pull-down resistance   |                                           | 16                   | 33                   | 78                    | kΩ   |
| Digital output pins                 |                                 |                                           |                      |                      |                       |      |
| V <sub>OH</sub>                     | HIGH-level output voltage       | I <sub>OH</sub> = –2 mA                   | 0.85V <sub>DD</sub>  | –                    | –                     | V    |
| V <sub>OL</sub>                     | LOW-level output voltage        | I <sub>OL</sub> = 2 mA                    | –                    | –                    | 0.4                   | V    |
| I <sub>L(max)</sub>                 | maximum load current            |                                           | –                    | 3                    | –                     | mA   |
| Digital-to-analog converter; note 2 |                                 |                                           |                      |                      |                       |      |
| V <sub>ref</sub>                    | reference voltage               | measured with respect to V <sub>SSA</sub> | 0.45V <sub>DDA</sub> | 0.50V <sub>DDA</sub> | 0.55V <sub>DDA</sub>  | V    |
| V <sub>o(rms)</sub>                 | output voltage (RMS value)      | note 3                                    | –                    | 900                  | –                     | mV   |

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| SYMBOL                | PARAMETER                                            | CONDITIONS                                 | MIN. | TYP. | MAX. | UNIT       |
|-----------------------|------------------------------------------------------|--------------------------------------------|------|------|------|------------|
| (THD + N)/S           | total harmonic distortion-plus-noise to signal ratio | $f_i = 1.0$ kHz tone at 48 kHz             | –    | –90  | –85  | dB         |
|                       |                                                      | at 0 dB                                    | –    | –60  | –55  | dB         |
|                       |                                                      | $f_i = 1.0$ kHz tone at 96 kHz             | –    | –85  | –80  | dB         |
|                       |                                                      | at 0 dB                                    | –    | –58  | –53  | dB         |
| S/N                   | signal-to-noise ratio at 48 kHz                      | $f_i = 1.0$ kHz tone; code = 0; A-weighted | 95   | 100  | –    | dB         |
|                       | signal-to-noise ratio at 96 kHz                      | $f_i = 1.0$ kHz tone; code = 0; A-weighted | 95   | 100  | –    | dB         |
| $\alpha_{CS}$         | channel separation                                   | $f_i = 1.0$ kHz tone                       | –    | 96   | –    | dB         |
| $\Delta V_0$          | unbalance of output voltages                         | $f_i = 1.0$ kHz tone                       | 0.4  | 0.1  | –    | dB         |
| <b>IEC 958 inputs</b> |                                                      |                                            |      |      |      |            |
| $V_{i(p-p)}$          | AC input voltage (peak-to-peak value)                |                                            | 0.2  | 0.5  | 3.3  | V          |
| $R_i$                 | input resistance                                     |                                            | –    | 6    | –    | k $\Omega$ |
| $V_{hys}$             | hysteresis voltage                                   |                                            | –    | 40   | –    | mV         |

**Notes**

1. All supply pins  $V_{DD}$  and  $V_{SS}$  must be connected to the same external power supply unit.
2. When the DAC must drive a higher capacitive load (above 50 pF), then a series resistor of 100  $\Omega$  must be used in order to prevent oscillations in the output stage of the operational amplifier.
3. The output voltage of the DAC is proportional to the DAC power supply voltage.

**12 TIMING CHARACTERISTICS**

$V_{DD} = V_{DDA} = 2.7$  to  $3.6$  V;  $T_{amb} = -40$  to  $+85$  °C;  $R_L = 5$  k $\Omega$ ; all voltages measured with respect to ground; unless otherwise specified.

| SYMBOL                                  | PARAMETER            | CONDITIONS                                      | MIN. | TYP. | MAX.               | UNIT |
|-----------------------------------------|----------------------|-------------------------------------------------|------|------|--------------------|------|
| Device reset                            |                      |                                                 |      |      |                    |      |
| t <sub>rst</sub>                        | reset active time    |                                                 | –    | 250  | –                  | μs   |
| PLL lock time                           |                      |                                                 |      |      |                    |      |
| t <sub>lock</sub>                       | time to lock         | f <sub>s</sub> = 32.0 kHz                       | –    | 85.0 | –                  | ms   |
|                                         |                      | f <sub>s</sub> = 44.1 kHz                       | –    | 63.0 | –                  | ms   |
|                                         |                      | f <sub>s</sub> = 48.0 kHz                       | –    | 60.0 | –                  | ms   |
|                                         |                      | f <sub>s</sub> = 96.0 kHz                       | –    | 40.0 | –                  | ms   |
| I <sup>2</sup> S-bus timing (see Fig.9) |                      |                                                 |      |      |                    |      |
| T <sub>cy(BCK)</sub>                    | bit clock cycle time | T <sub>s</sub> = cycle time of sample frequency | –    | –    | 1/64T <sub>s</sub> | s    |
| t <sub>BCKH</sub>                       | bit clock HIGH time  |                                                 | 140  | –    | 280                | ns   |
| t <sub>BCKL</sub>                       | bit clock LOW time   |                                                 | 140  | –    | 280                | ns   |
| t <sub>r</sub>                          | rise time            |                                                 | –    | –    | 20                 | ns   |

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| SYMBOL                                                          | PARAMETER                                            | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------------------------------------------------------|------------------------------------------------------|------------|------|------|------|------|
| $t_f$                                                           | fall time                                            |            | –    | –    | 20   | ns   |
| $t_{su(WS)}$                                                    | set-up time word select                              |            | 20   | –    | –    | ns   |
| $t_{h(WS)}$                                                     | hold time word select                                |            | 10   | –    | –    | ns   |
| $t_{su(DATAI)}$                                                 | set-up time data input                               |            | 20   | –    | –    | ns   |
| $t_{h(DATAI)}$                                                  | hold time data input                                 |            | 0    | –    | –    | ns   |
| $t_{h(DATAO)}$                                                  | hold time data output                                |            | 0    | –    | –    | ns   |
| $t_{d(DATAO-BCK)}$                                              | data output to bit clock delay                       |            | –    | –    | 80   | ns   |
| $t_{d(DATAO-WS)}$                                               | data output to word select delay                     |            | –    | –    | 80   | ns   |
| <b>Microcontroller L3 interface timing</b> (see Figs 10 and 11) |                                                      |            |      |      |      |      |
| $T_{cy(CLK)(L3)}$                                               | L3CLOCK cycle time                                   |            | 500  | –    | –    | ns   |
| $t_{CLK(L3)H}$                                                  | L3CLOCK HIGH time                                    |            | 250  | –    | –    | ns   |
| $t_{CLK(L3)L}$                                                  | L3CLOCK LOW time                                     |            | 250  | –    | –    | ns   |
| $t_{su(L3)A}$                                                   | L3MODE set-up time in address mode                   |            | 190  | –    | –    | ns   |
| $t_{h(L3)A}$                                                    | L3MODE hold time in address mode                     |            | 190  | –    | –    | ns   |
| $t_{su(L3)D}$                                                   | L3MODE set-up time in data transfer mode             |            | 190  | –    | –    | ns   |
| $t_{h(L3)D}$                                                    | L3MODE hold time in data transfer mode               |            | 190  | –    | –    | ns   |
| $t_{stp(L3)}$                                                   | L3MODE stop time in data transfer mode               |            | 190  | –    | –    | ns   |
| $t_{su(L3)DA}$                                                  | L3DATA set-up time in address and data transfer mode |            | 190  | –    | –    | ns   |
| $t_{h(L3)DA}$                                                   | L3DATA hold time in address and data transfer mode   |            | 30   | –    | –    | ns   |
| $t_{su(L3)R}$                                                   | L3DATA set-up time in data transfer mode             | read mode  | 50   | –    | –    | ns   |
| $t_{h(L3)R}$                                                    | L3DATA hold time in data transfer mode               | read mode  | 360  | –    | –    | ns   |

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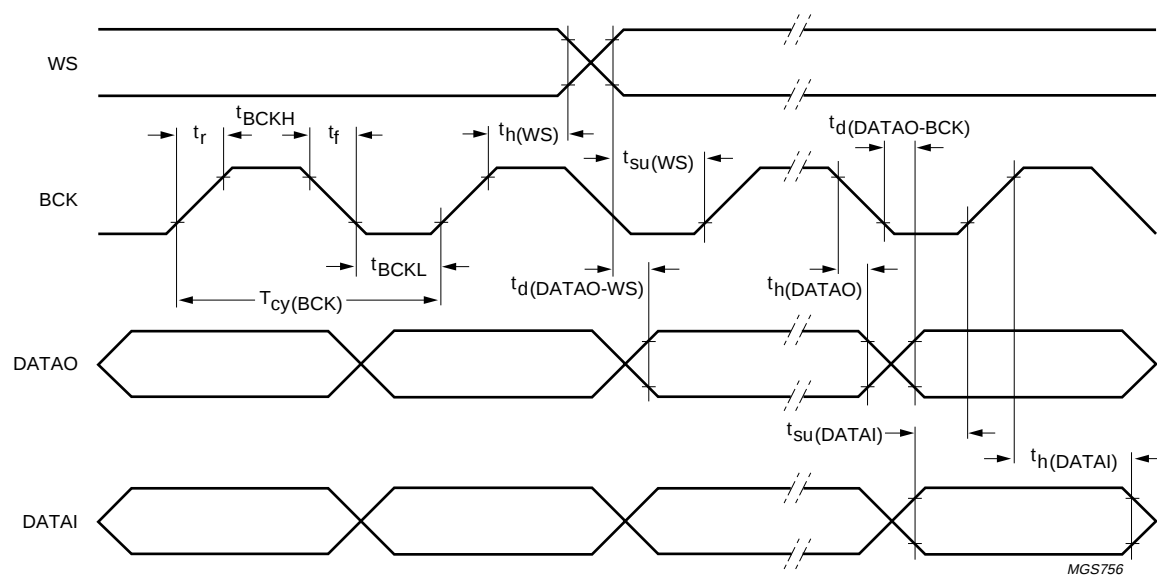


Fig.9 I<sup>2</sup>S-bus timing of output and input interface.

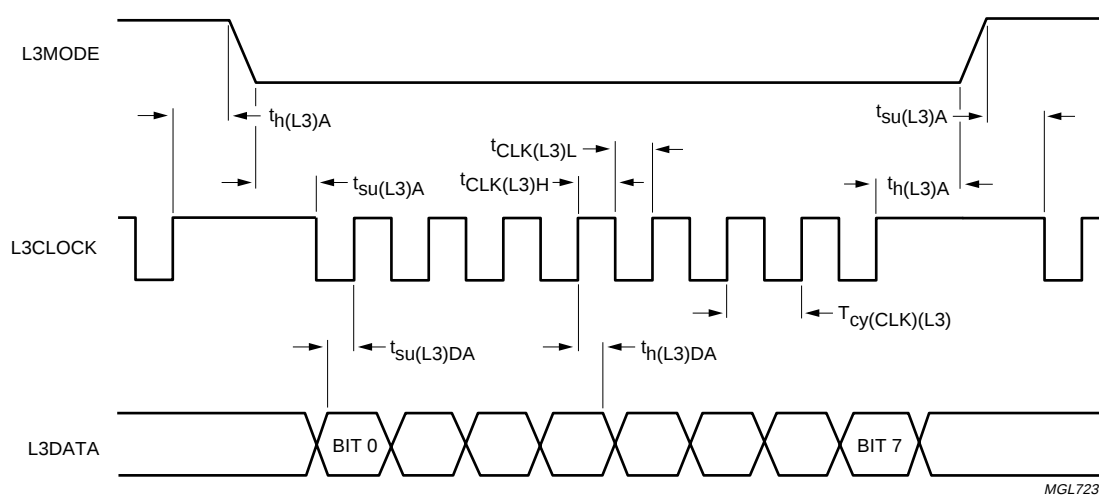


Fig.10 Timing for address mode.

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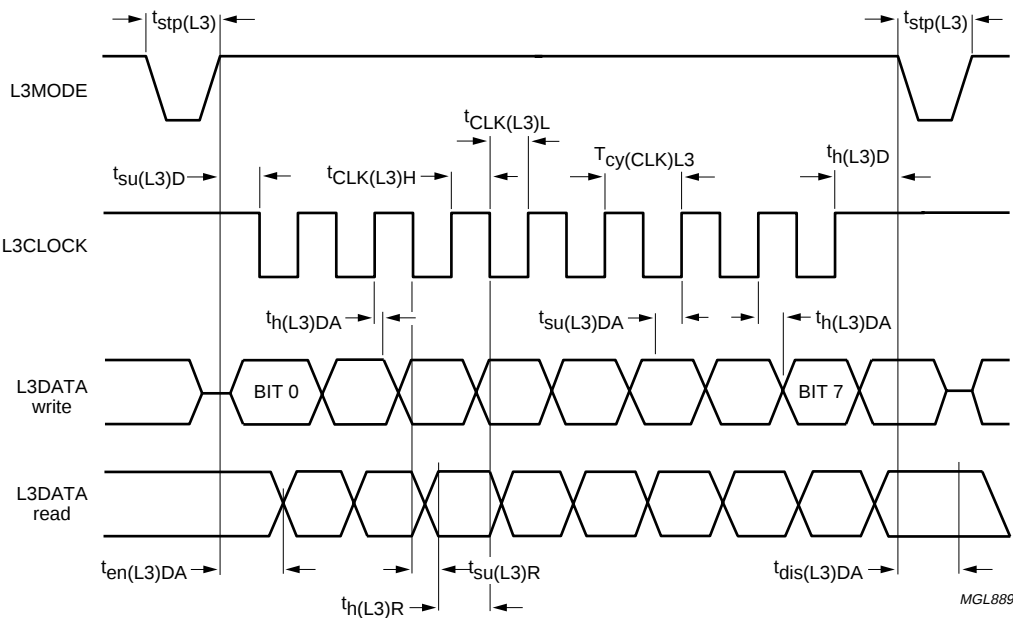


Fig.11 Timing for data transfer mode.

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### 13 APPLICATION INFORMATION

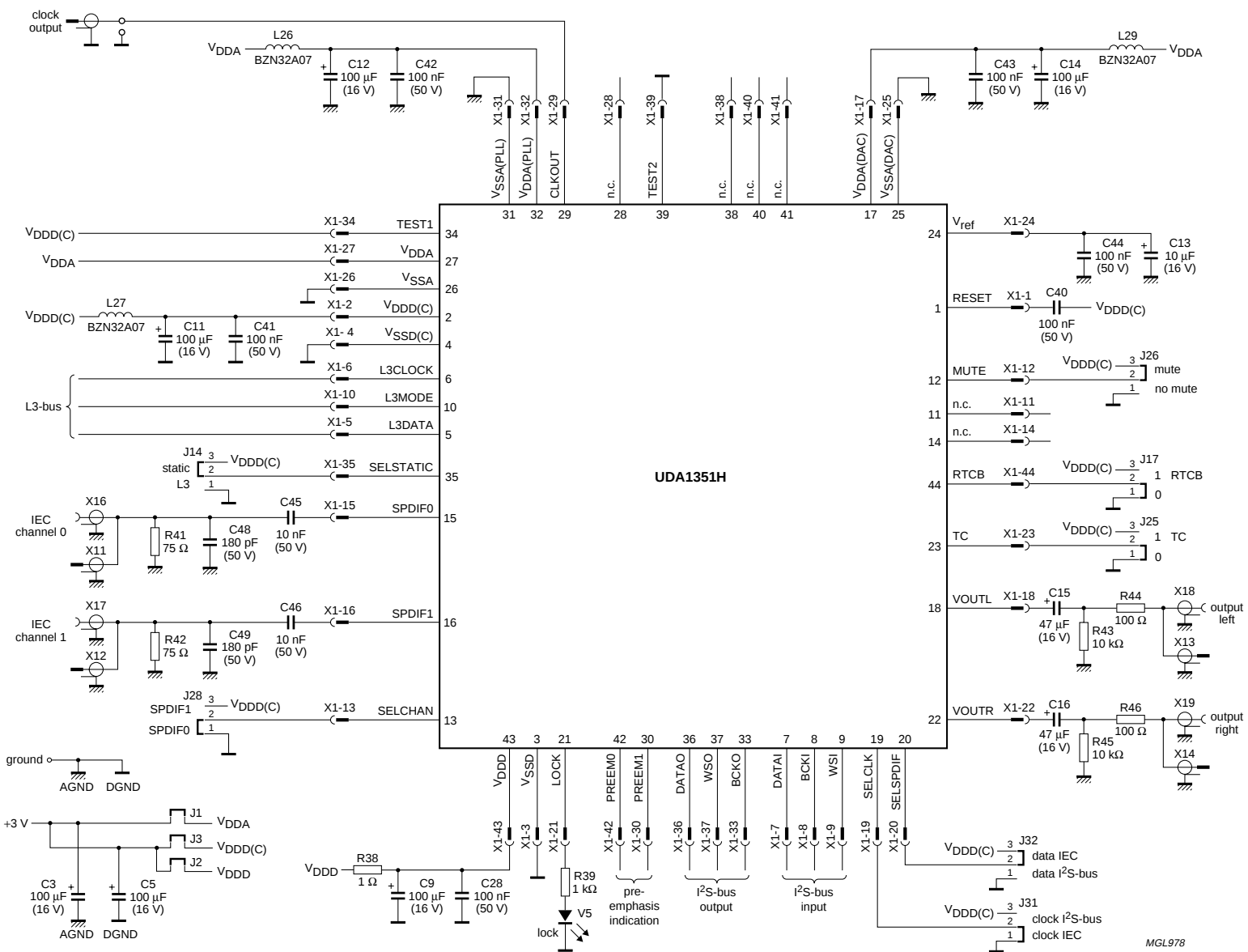


Fig.12 Test and application diagram.

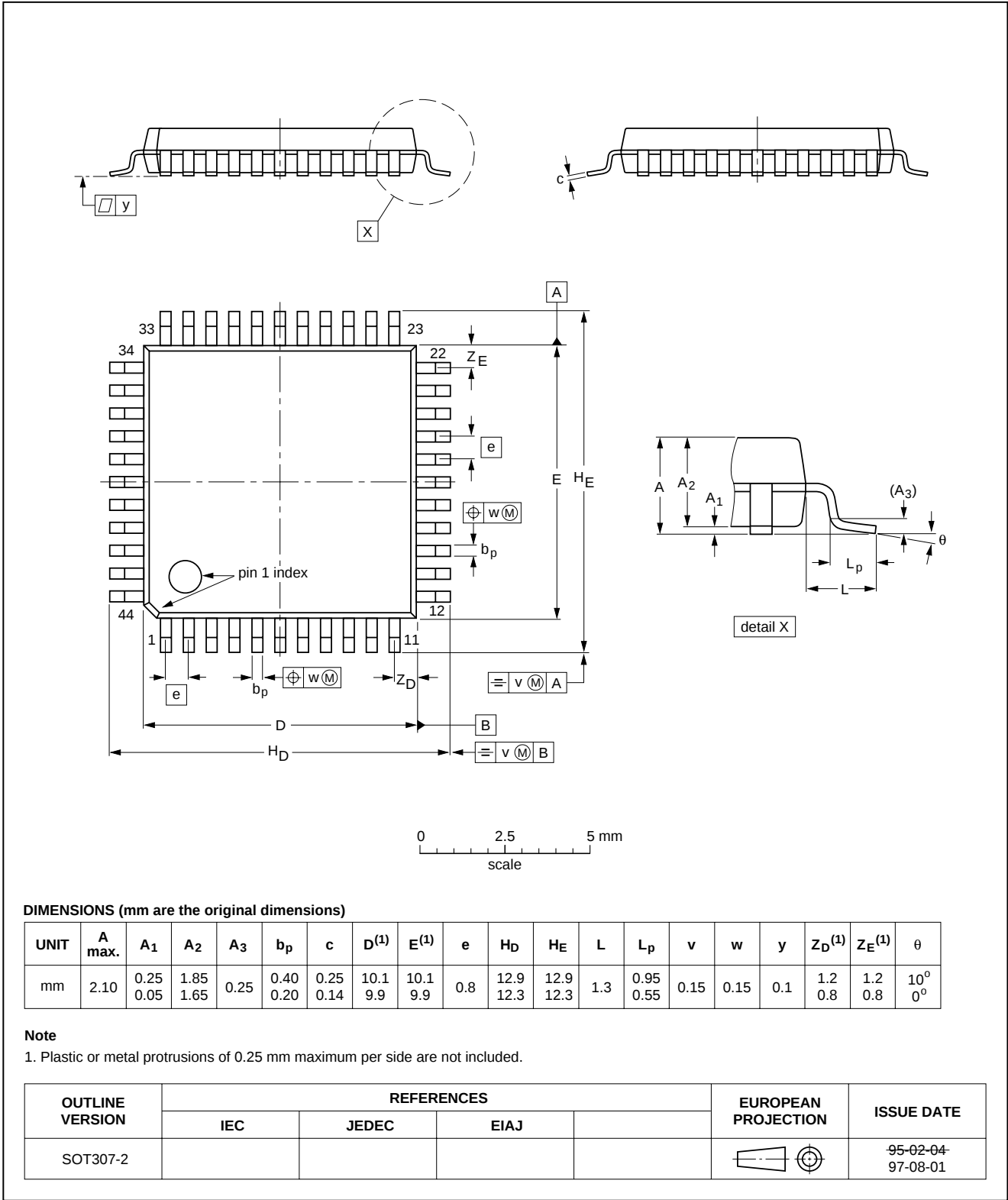
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14 PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2



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## 15 SOLDERING

### 15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

### 15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

### 15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### 15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## 15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE                                      | SOLDERING METHOD                  |                       |
|----------------------------------------------|-----------------------------------|-----------------------|
|                                              | WAVE                              | REFLOW <sup>(1)</sup> |
| BGA, LFBGA, SQFP, TFBGA                      | not suitable                      | suitable              |
| HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS | not suitable <sup>(2)</sup>       | suitable              |
| PLCC <sup>(3)</sup> , SO, SOJ                | suitable                          | suitable              |
| LQFP, QFP, TQFP                              | not recommended <sup>(3)(4)</sup> | suitable              |
| SSOP, TSSOP, VSO                             | not recommended <sup>(5)</sup>    | suitable              |

## Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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## 16 DATA SHEET STATUS

| DATA SHEET STATUS         | PRODUCT STATUS | DEFINITIONS <sup>(1)</sup>                                                                                                                                                                                                                                 |
|---------------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Objective specification   | Development    | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.                                                                                                          |
| Preliminary specification | Qualification  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification     | Production     | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.                                                       |

**Note**

1. Please consult the most recently issued data sheet before initiating or completing a design.

## 17 DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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96 kHz IEC 958 audio DAC

UDA1351H

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**NOTES**

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Printed in The Netherlands

735303/25/02/pp36

Date of release: 2000 Jul 27

Document order number: 9397 750 07236

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