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Electronic Components Sourcing Information

Product Reference Information

Part Number:	PMXB65ENE,147
Manufacturer:	NXP USA Inc.
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nxp-usa-inc/pmx65ene-147.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



PMXB65ENE

30 V, N-channel Trench MOSFET

3 November 2016

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Leadless ultra small and thin SMD plastic package: $1.1 \times 1.0 \times 0.37$ mm
- Exposed drain pad for excellent thermal conduction
- ElectroStatic Discharge (ESD) protection 1 kV
- Very low Drain-Source on-state resistance $R_{DSon} = 44$ m Ω

3. Applications

- Low-side load switch and charging switch for portable devices
- Power management in battery-driven portables
- LED driver
- DC-to-DC converters

4. Quick reference data

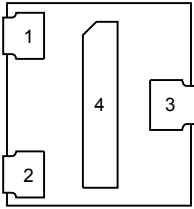
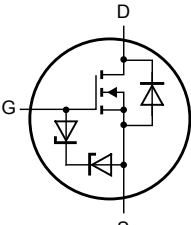
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25$ °C		-	-	30	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$V_{GS} = 10$ V; $T_{amb} = 25$ °C	[1]	-	-	3.2	A
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 3.2$ A; $T_j = 25$ °C		-	44	67	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view DFN1010D-3 (SOT1215)	 017aaa255
2	S	source		
3	D	drain		
4	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMXB65ENE	DFN1010D-3	DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body 1.1 x 1.0 x 0.37 mm	SOT1215

7. Marking

Table 4. Marking codes

Type number	Marking code
PMXB65ENE	00 10 00

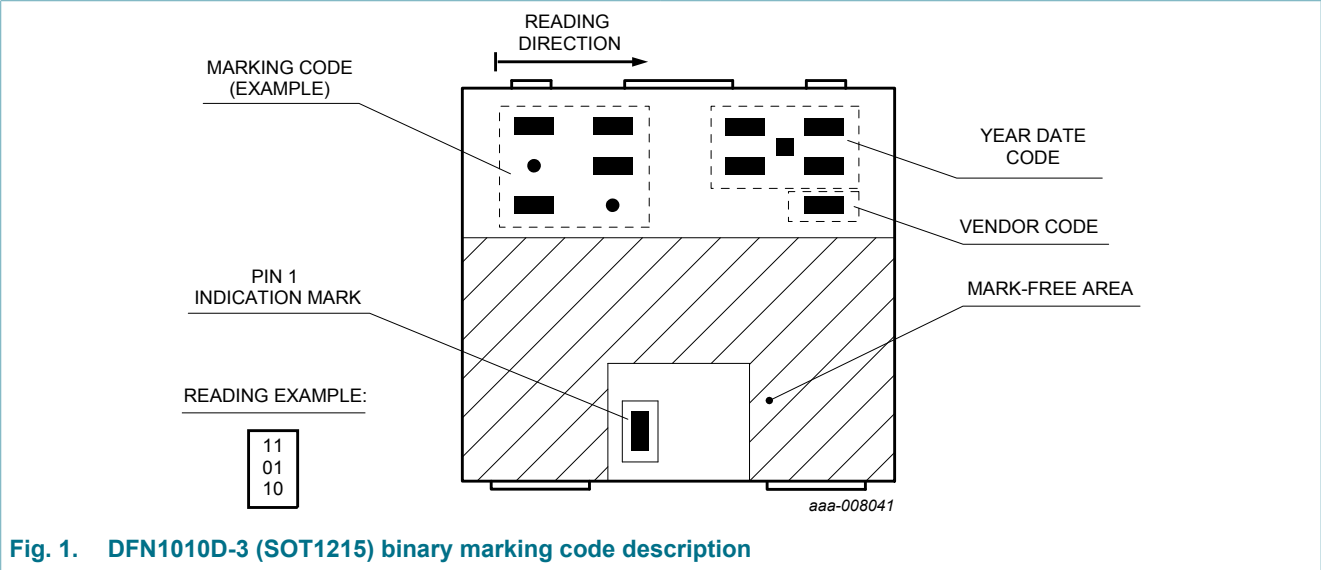


Fig. 1. DFN1010D-3 (SOT1215) binary marking code description

8. Limiting values

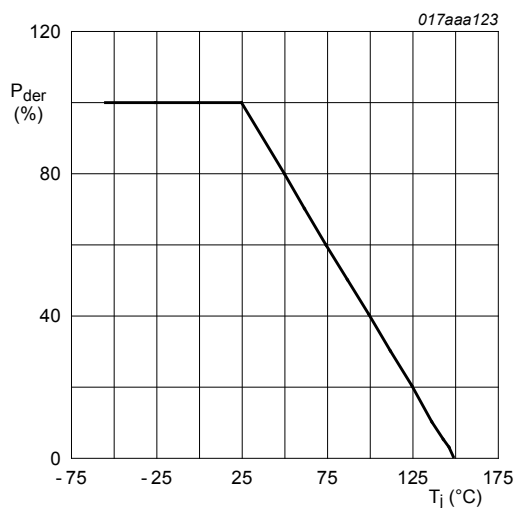
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	30	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	3.2	A
		$V_{GS} = 10\text{ V}; T_{amb} = 100\text{ }^{\circ}\text{C}$	[1]	-	2.5	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	12.8	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	-	0.4	W
			[1]	-	1.07	W
		$T_{sp} = 25\text{ }^{\circ}\text{C}$		-	8.33	W
T_j	junction temperature			-55	150	$^{\circ}\text{C}$
T_{amb}	ambient temperature			-55	150	$^{\circ}\text{C}$
T_{stg}	storage temperature			-65	150	$^{\circ}\text{C}$
Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	0.9	A

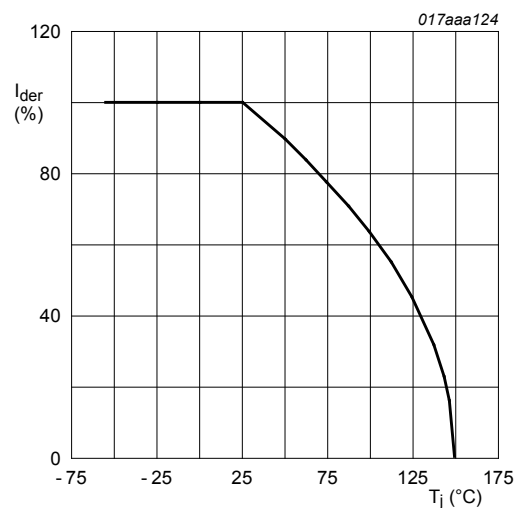
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



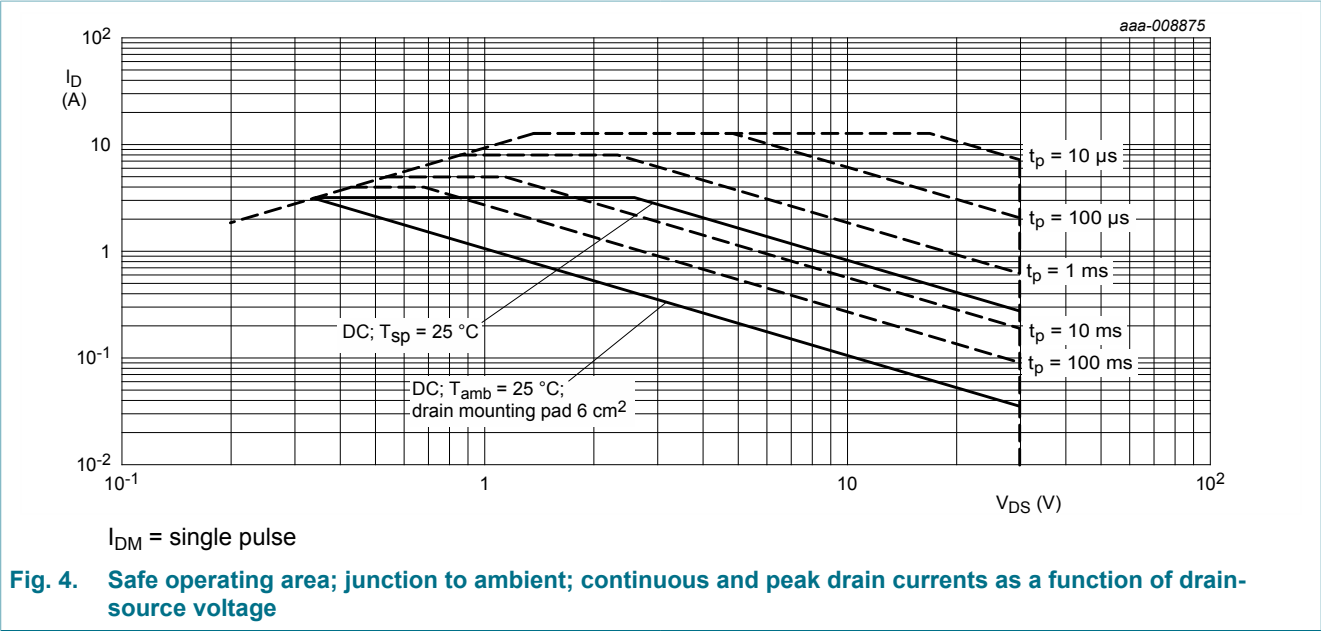
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig. 2. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig. 3. Normalized continuous drain current as a function of junction temperature

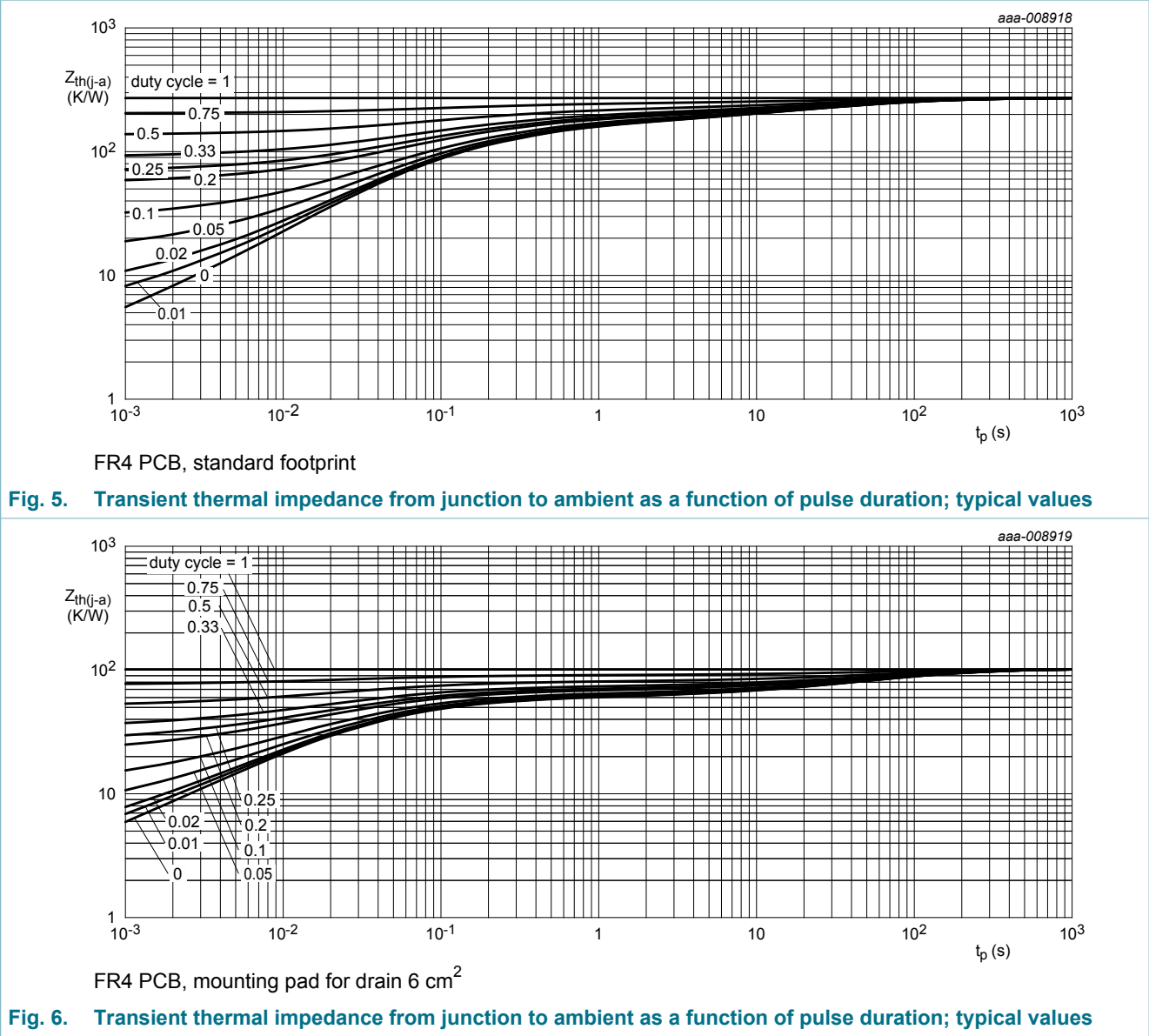


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	271	312	K/W
			[2]	-	102	117	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	10	15	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		30	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = 250 μA; V _{DS} =V _{GS} ; T _j = 25 °C		1	1.4	2	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V; T _j = 25 °C		-	-	1	μA
I _{GSS}	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -16 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-10	μA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-1	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 3.2 A; T _j = 25 °C		-	44	67	mΩ
		V _{GS} = 10 V; I _D = 3.2 A; T _j = 150 °C		-	71	107	mΩ
		V _{GS} = 4.5 V; I _D = 2.9 A		-	56	79	mΩ
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 3.2 A; T _j = 25 °C		-	26	-	S
R _G	gate resistance	f = 1 MHz		-	1	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = 15 V; I _D = 3.2 A; V _{GS} = 10 V; T _j = 25 °C		-	6	11	nC
Q _{GS}	gate-source charge			-	0.7	-	nC
Q _{GD}	gate-drain charge			-	0.9	-	nC
C _{iss}	input capacitance	V _{DS} = 15 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	295	-	pF
C _{oss}	output capacitance			-	40	-	pF
C _{rss}	reverse transfer capacitance			-	31	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 15 V; I _D = 3.2 A; V _{GS} = 10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	3	-	ns
t _r	rise time			-	12	-	ns
t _{d(off)}	turn-off delay time			-	11	-	ns
t _f	fall time			-	3	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 0.9 A; V _{GS} = 0 V; T _j = 25 °C		-	0.8	1.2	V

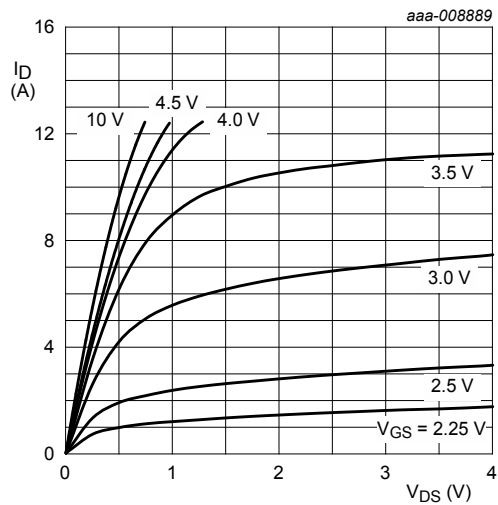


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

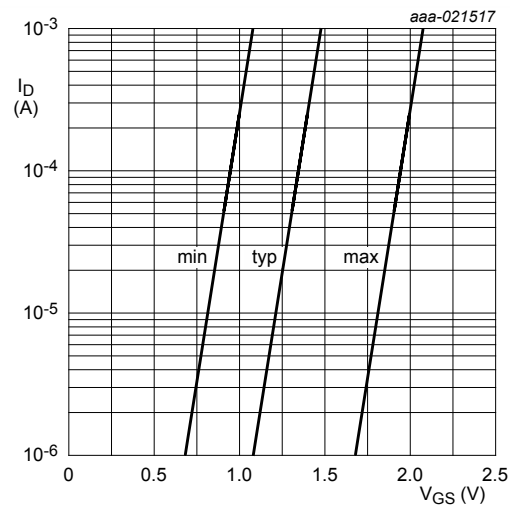


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

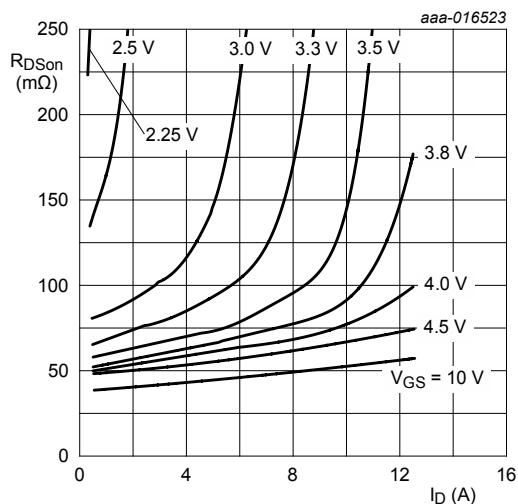


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

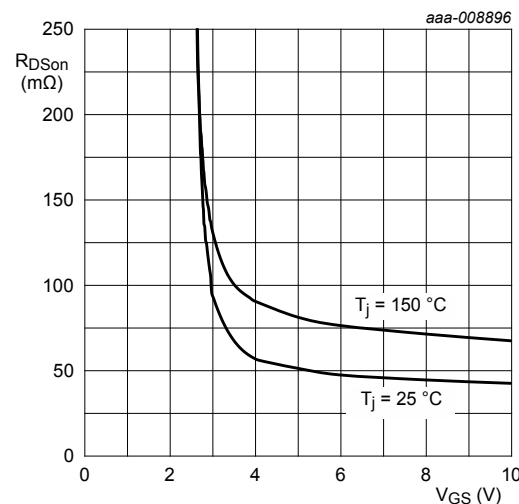
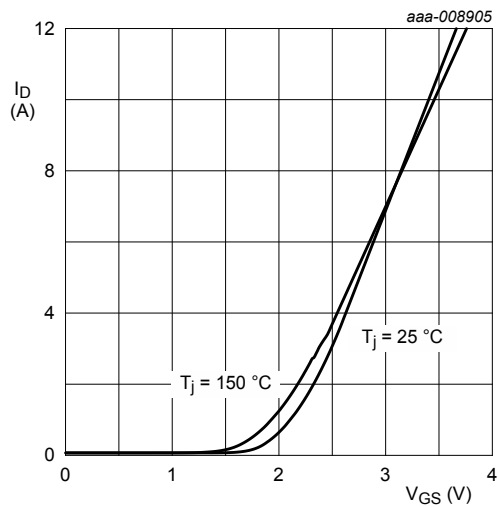
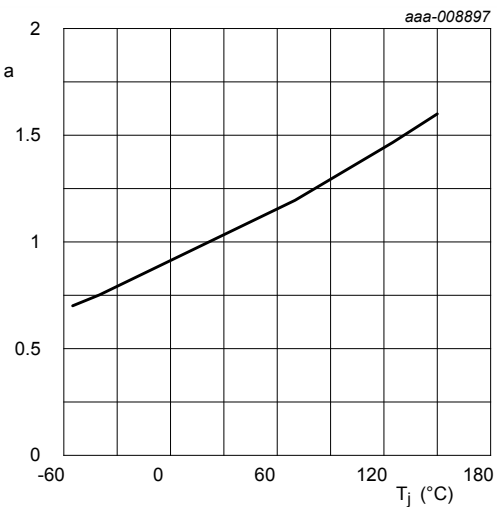


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



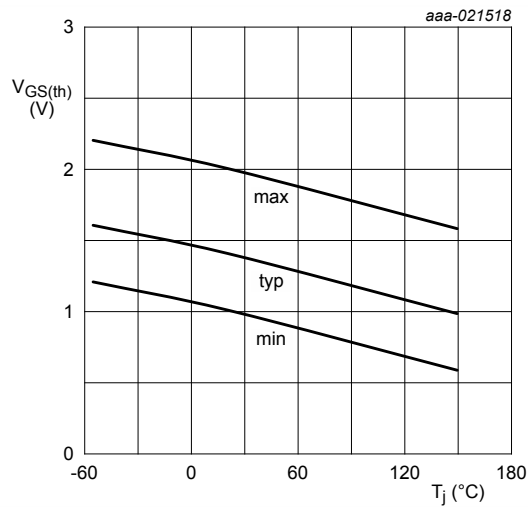
$V_{DS} > I_D \times R_{DSon}$

Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values



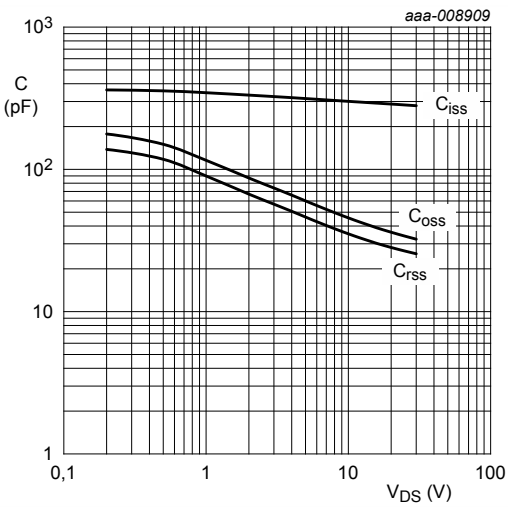
$$a = \frac{R_{DSon}}{R_{DSon}(25\text{ °C})}$$

Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values



$I_D = 0.25\text{ mA}; V_{DS} = V_{GS}$

Fig. 13. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

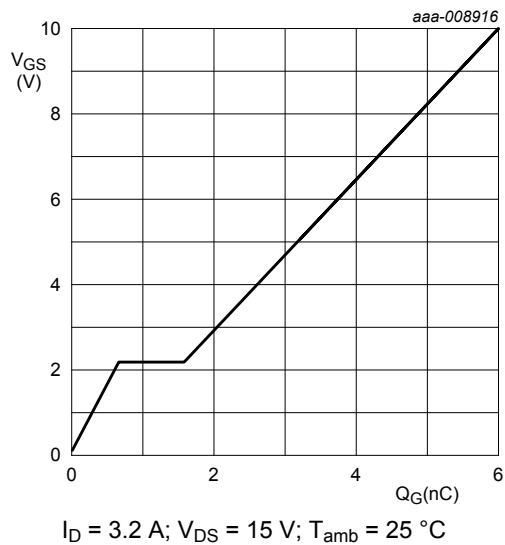


Fig. 15. Gate-source voltage as a function of gate charge; typical values

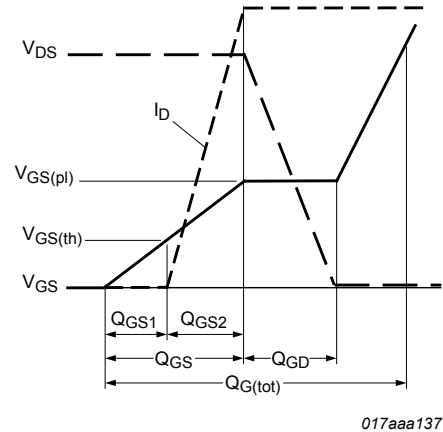


Fig. 16. MOSFET transistor: Gate charge waveform definitions

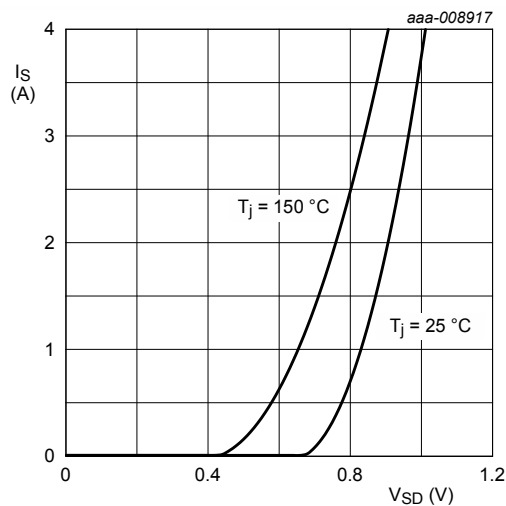


Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

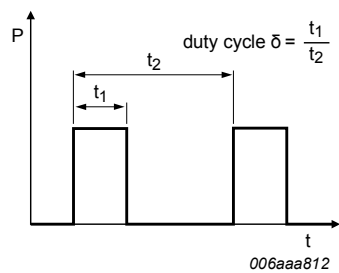
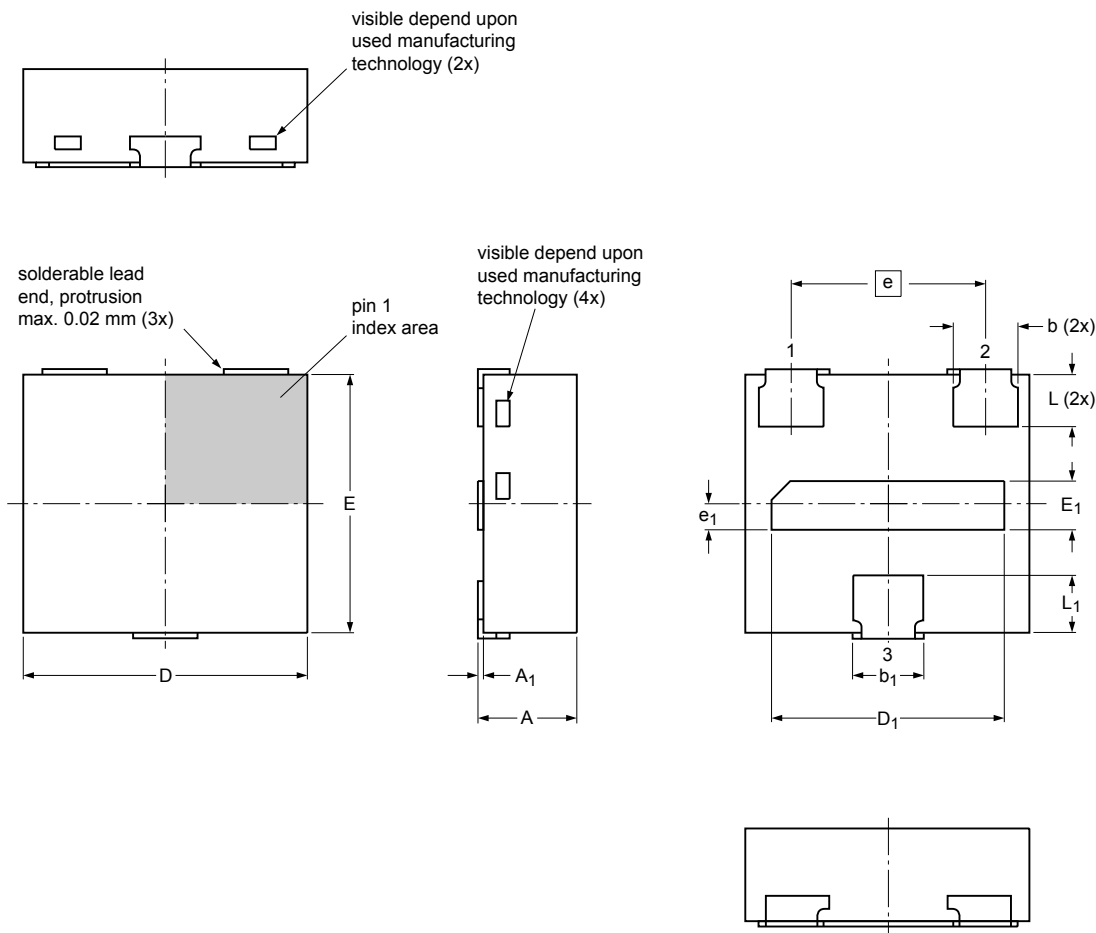


Fig. 18. Duty cycle definition

12. Package outline

DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads;
3 terminals; body: 1.1 x 1.0 x 0.37 mm

SOT1215



0 1 mm

scale

Dimensions (mm are the original dimensions)

Unit	A	A ₁	b	b ₁	D	D ₁	E	E ₁	e	e ₁	L	L ₁
min	0.34		0.22	0.245	1.05	0.87	0.95	0.16			0.17	0.195
mm	nom		0.25	0.275	1.10	0.90	1.00	0.19	0.75	0.1	0.20	0.225
	max	0.40	0.30	0.325	1.15	0.95	1.05	0.24			0.25	0.275

Note
1. Dimension A is including plating thickness.

sot1215_po

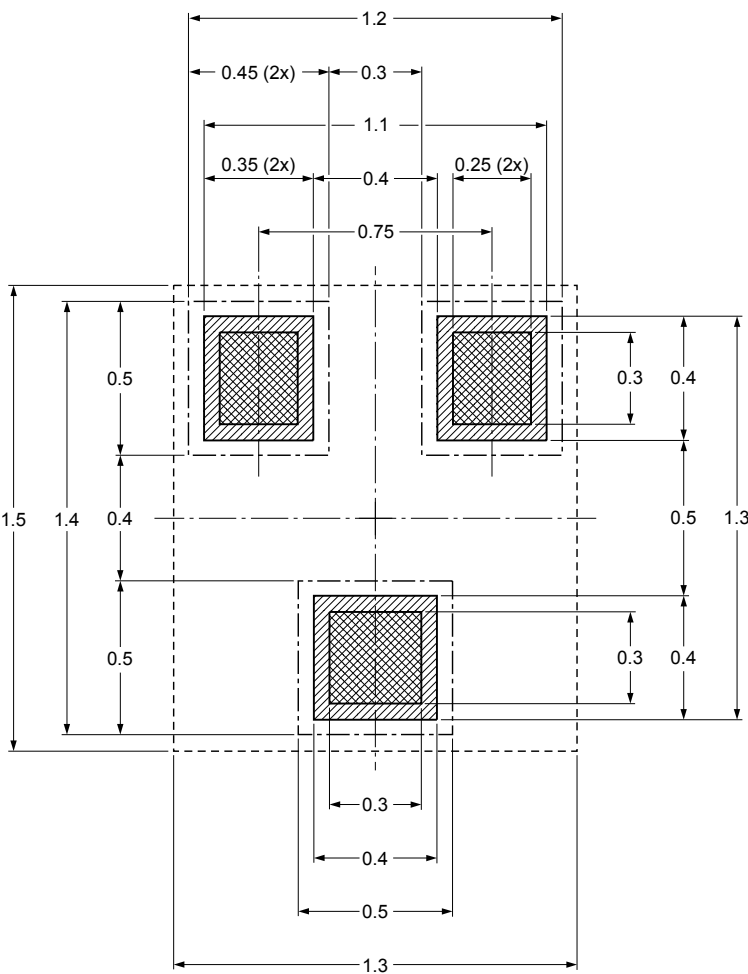
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1215						-13-03-05- 13-03-06

Fig. 19. Package outline DFN1010D-3 (SOT1215)

13. Soldering

Footprint information for reflow soldering of DFN1010D-3 package

SOT1215



-  solder land
-  solder land plus solder paste
-  occupied area
-  solder resist

Dimensions in mm

Issue date ~~12-11-23~~
13-03-06

sot1215_fr

Fig. 20. Reflow soldering footprint for DFN1010D-3 (SOT1215)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMXB65ENE v.4	20161103	Product data sheet	-	PMXB65ENE v.3
Modifications:	Maximum value of gate-source threshold voltage revised			
PMXB65ENE v.3	20150520	Product data sheet	-	PMXB65ENE v.2
PMXB65ENE v.2	20130924	Product data sheet	-	PMXB65ENE v.1
PMXB65ENE v.1	20130910	Product data sheet	-	-

15. Legal information

Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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