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Manufacturer:	NXP USA Inc.
Package:	Please confirm with sales
Availability:	Please confirm with sales

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<https://antrexco.com/product/details/nxp-usa-inc/pmn25en-115.html>

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The original manufacturer datasheet follows from the next page.

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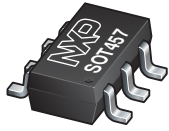
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PMN25EN

30 V, 6.2 A N-channel Trench MOSFET

Rev. 1 — 29 August 2011

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) small Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Logic level compatible
- Trench MOSFET technology
- Very fast switching

1.3 Applications

- Relay driver
- Low-side loadswitch
- High-speed line driver
- Switching circuits

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	30	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	6.2	A
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 6.2\text{ A}; T_j = 25\text{ °C}$	-	20	23	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	SOT457 (TSOP6)	017aaa253
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		



3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PMN25EN	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code
PMN25EN	T8

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

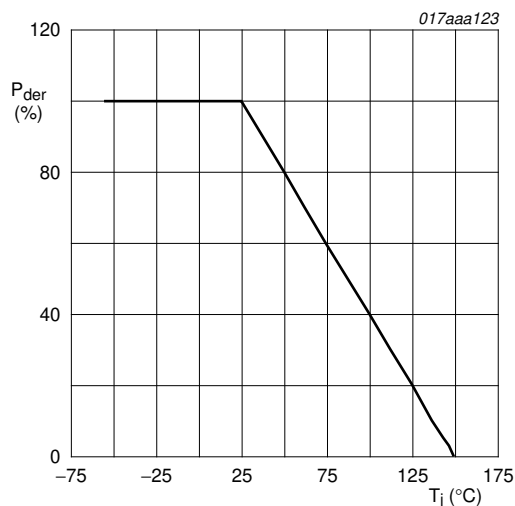
Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C	-	30	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C	[1]	6.2	A
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	3.9	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs	-	25	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	540	mW
			[1]	1385	mW
		T _{sp} = 25 °C	-	6250	mW
T _j	junction temperature		-55	150	°C
T _{amb}	ambient temperature		-55	150	°C
T _{stg}	storage temperature		-65	150	°C

Source-drain diode

I _S	source current	T _{amb} = 25 °C	[1]	1.4	A
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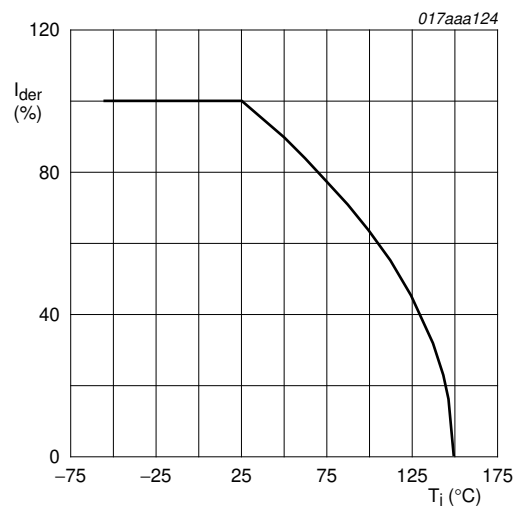
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



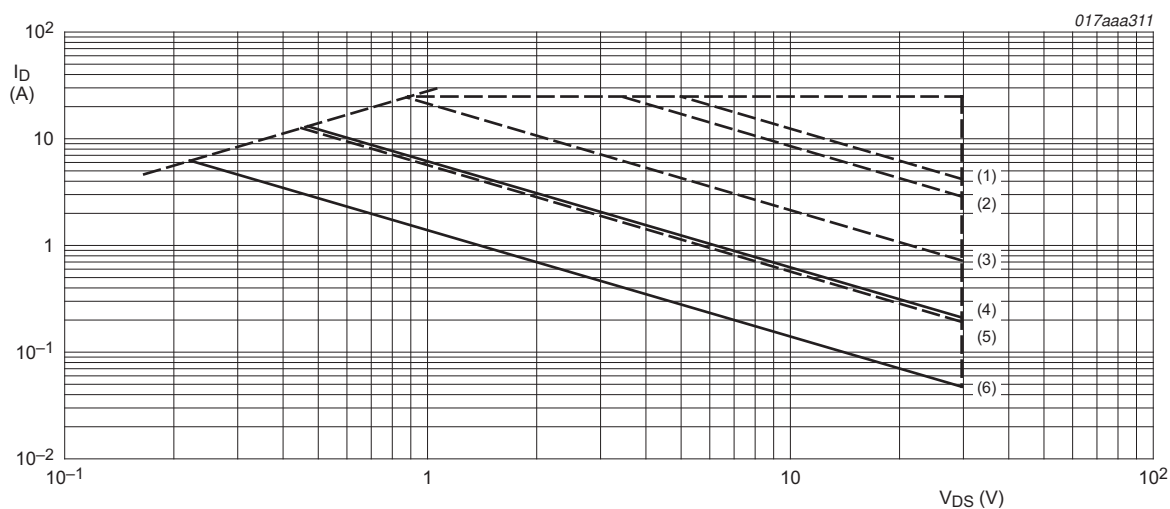
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} = single pulse

(1) $t_p = 100 \mu s$

(2) $t_p = 1 ms$

(3) $t_p = 10 ms$

(4) DC; $T_{sp} = 25 ^\circ C$

(5) $t_p = 100 ms$

(6) DC; $T_{amb} = 25 ^\circ C$; drain mounting pad $6 cm^2$

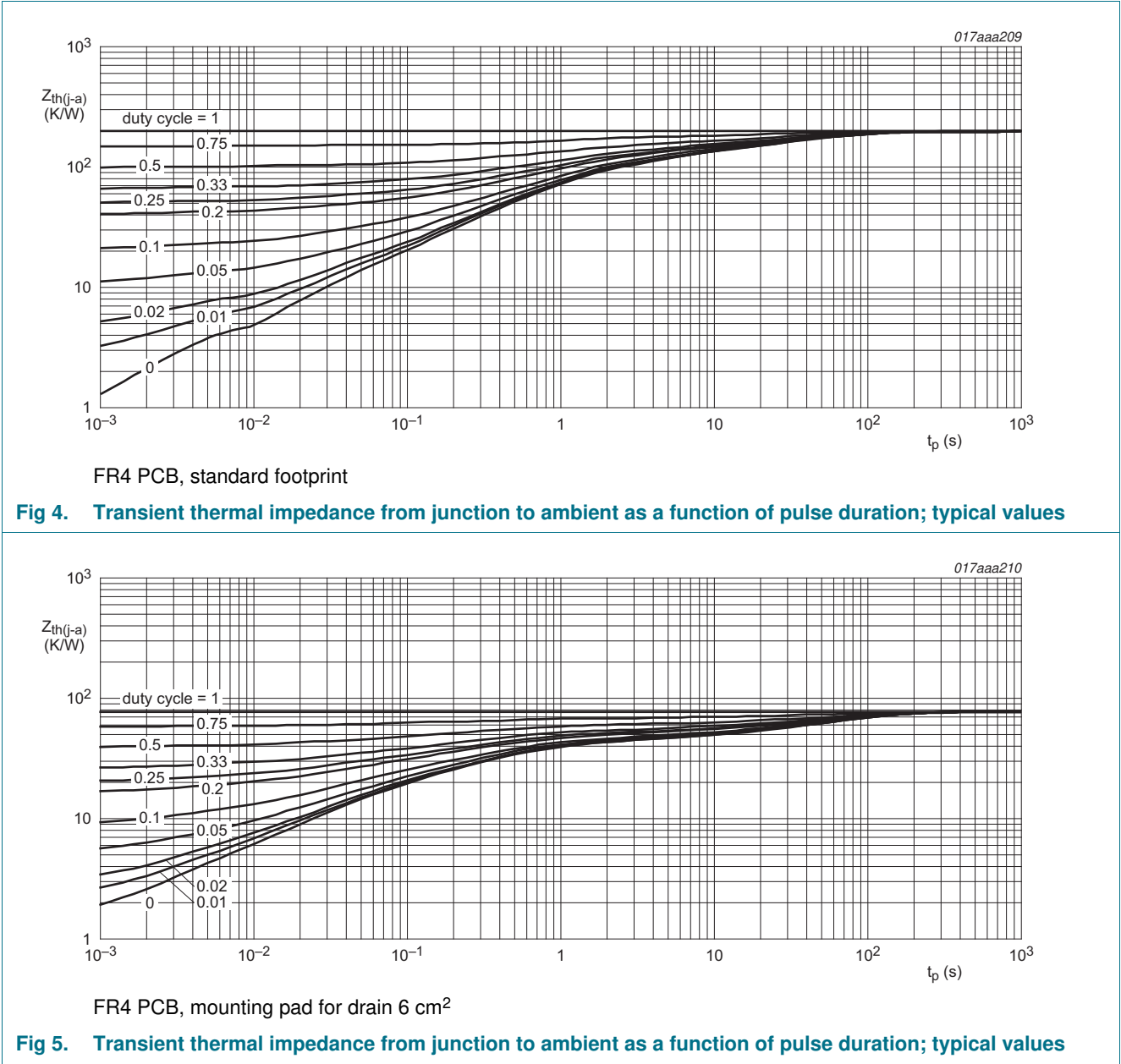
Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	200	230 K/W
			[2]	-	78 90	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	15	20	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².



7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	30	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; T _j = 25 °C	1	1.5	2.5	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V; T _j = 25 °C	-	-	1	μA
		V _{DS} = 30 V; V _{GS} = 0 V; T _j = 150 °C	-	-	10	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 6.2 A; T _j = 25 °C	-	20	23	mΩ
		V _{GS} = 10 V; I _D = 6.2 A; T _j = 150 °C	-	31	36	mΩ
		V _{GS} = 4.5 V; I _D = 5.4 A; T _j = 25 °C	-	24	31	mΩ
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 6.2 A; T _j = 25 °C	-	18	-	S
Dynamic characteristics						
Q _{G(tot)}	total gate charge	V _{DS} = 15 V; I _D = 6 A; V _{GS} = 10 V; T _j = 25 °C	-	9.6	11	nC
Q _{GS}	gate-source charge		-	1.5	-	nC
Q _{GD}	gate-drain charge		-	1.5	-	nC
C _{iss}	input capacitance	V _{DS} = 15 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C	-	492	-	pF
C _{oss}	output capacitance		-	115	-	pF
C _{rss}	reverse transfer capacitance		-	54	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 15 V; V _{GS} = 10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C; I _D = 6 A	-	5	-	ns
t _r	rise time		-	28	-	ns
t _{d(off)}	turn-off delay time		-	94	-	ns
t _f	fall time		-	40	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 1.4 A; V _{GS} = 0 V; T _j = 25 °C	-	0.78	1.2	V

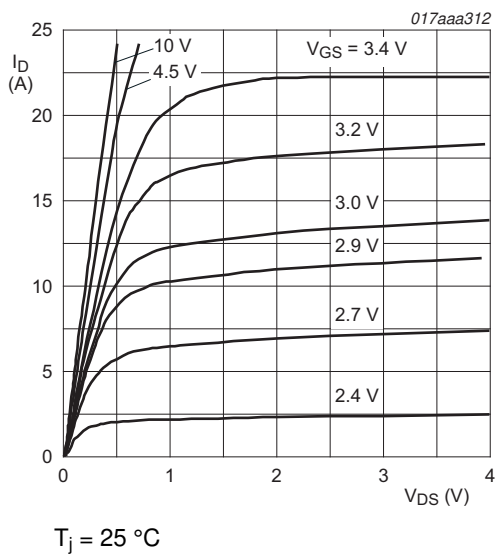


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

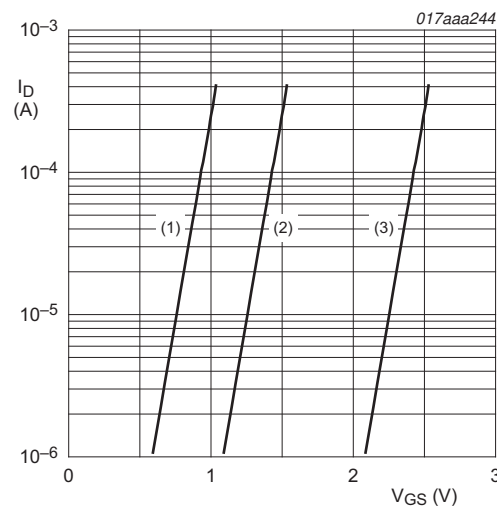
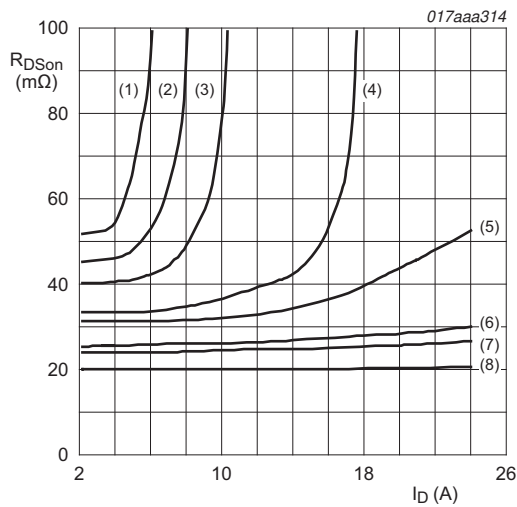


Fig 7. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25\text{ °C}$

(1) $V_{GS} = 2.7\text{ V}$

(2) $V_{GS} = 2.8\text{ V}$

(3) $V_{GS} = 2.9\text{ V}$

(4) $V_{GS} = 3.2\text{ V}$

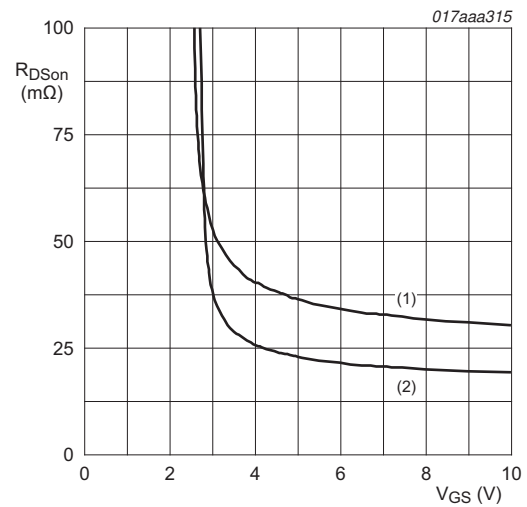
(5) $V_{GS} = 3.4\text{ V}$

(6) $V_{GS} = 4.0\text{ V}$

(7) $V_{GS} = 4.5\text{ V}$

(8) $V_{GS} = 10\text{ V}$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values

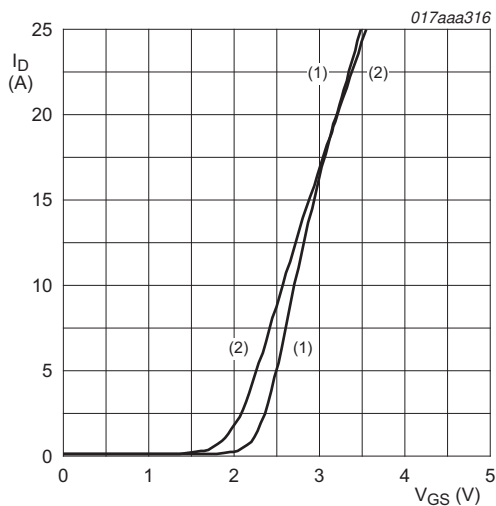


$I_D = 6.0\text{ A}$

(1) $T_j = 150\text{ °C}$

(2) $T_j = 25\text{ °C}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

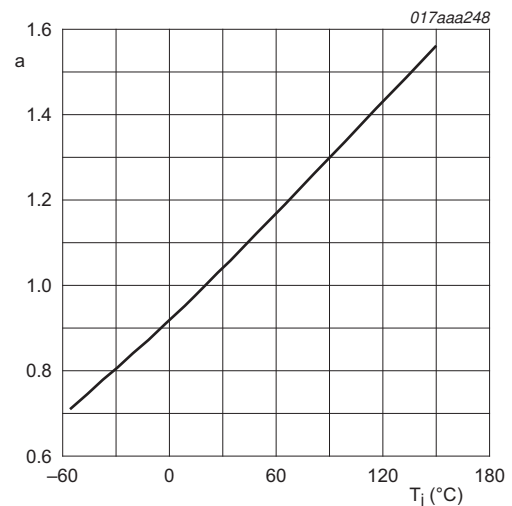


$V_{DS} > I_D \times R_{DS(on)}$

(1) $T_j = 25\text{ °C}$

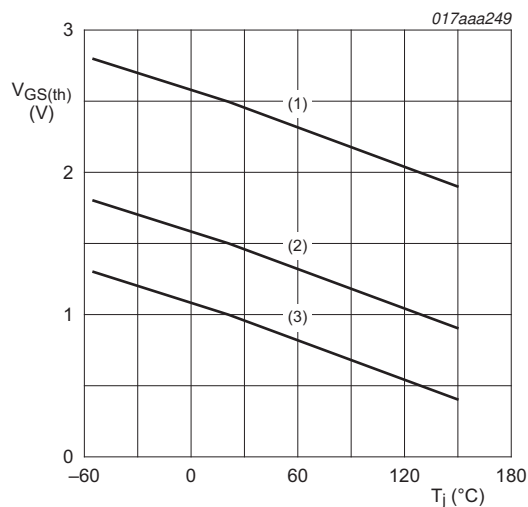
(2) $T_j = 150\text{ °C}$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



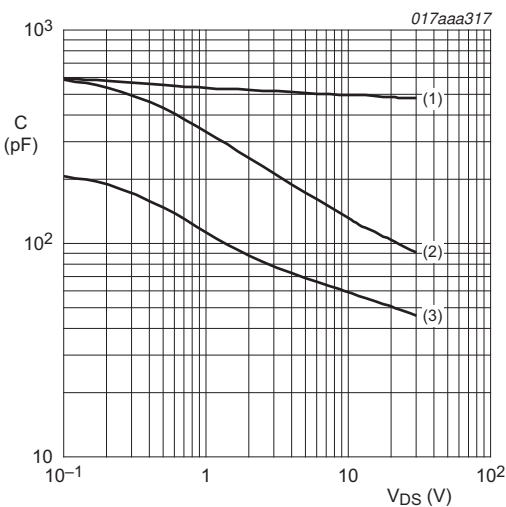
$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25\text{ °C})}$$

Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



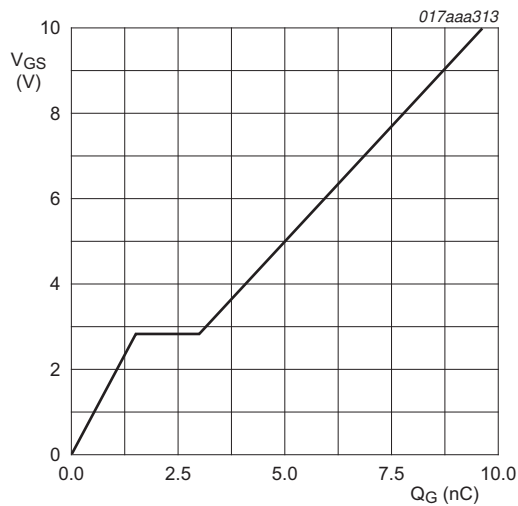
$I_D = 0.25 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature



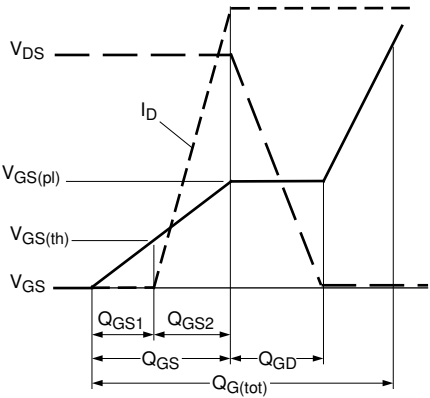
$f = 1 \text{ MHz}$; $V_{GS} = 0 \text{ V}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



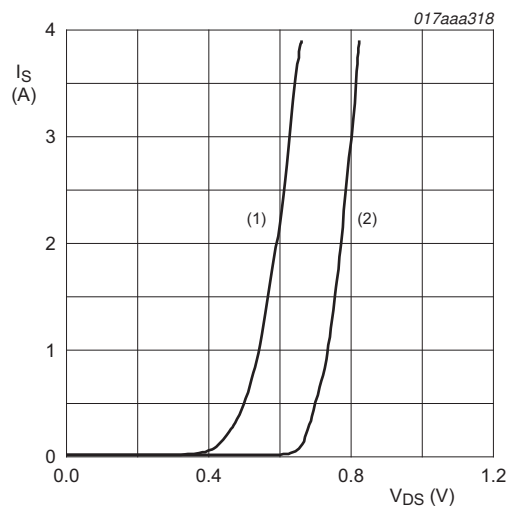
$I_D = 6 \text{ A}$; $V_{DS} = 10 \text{ V}$; $T_{amb} = 25 \text{ °C}$

Fig 14. Gate-source voltage as a function of gate charge; typical values



017aaa137

Fig 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$
(1) $T_j = 150\text{ }^{\circ}\text{C}$
(2) $T_j = 25\text{ }^{\circ}\text{C}$

Fig 16. Source current as a function of source-drain voltage; typical values

8. Test information

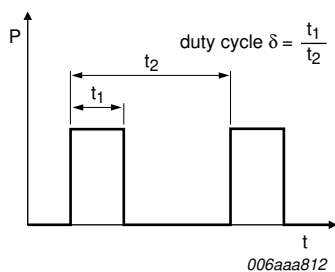


Fig 17. Duty cycle definition

9. Package outline

Plastic surface-mounted package (TSOP6); 6 leads SOT457

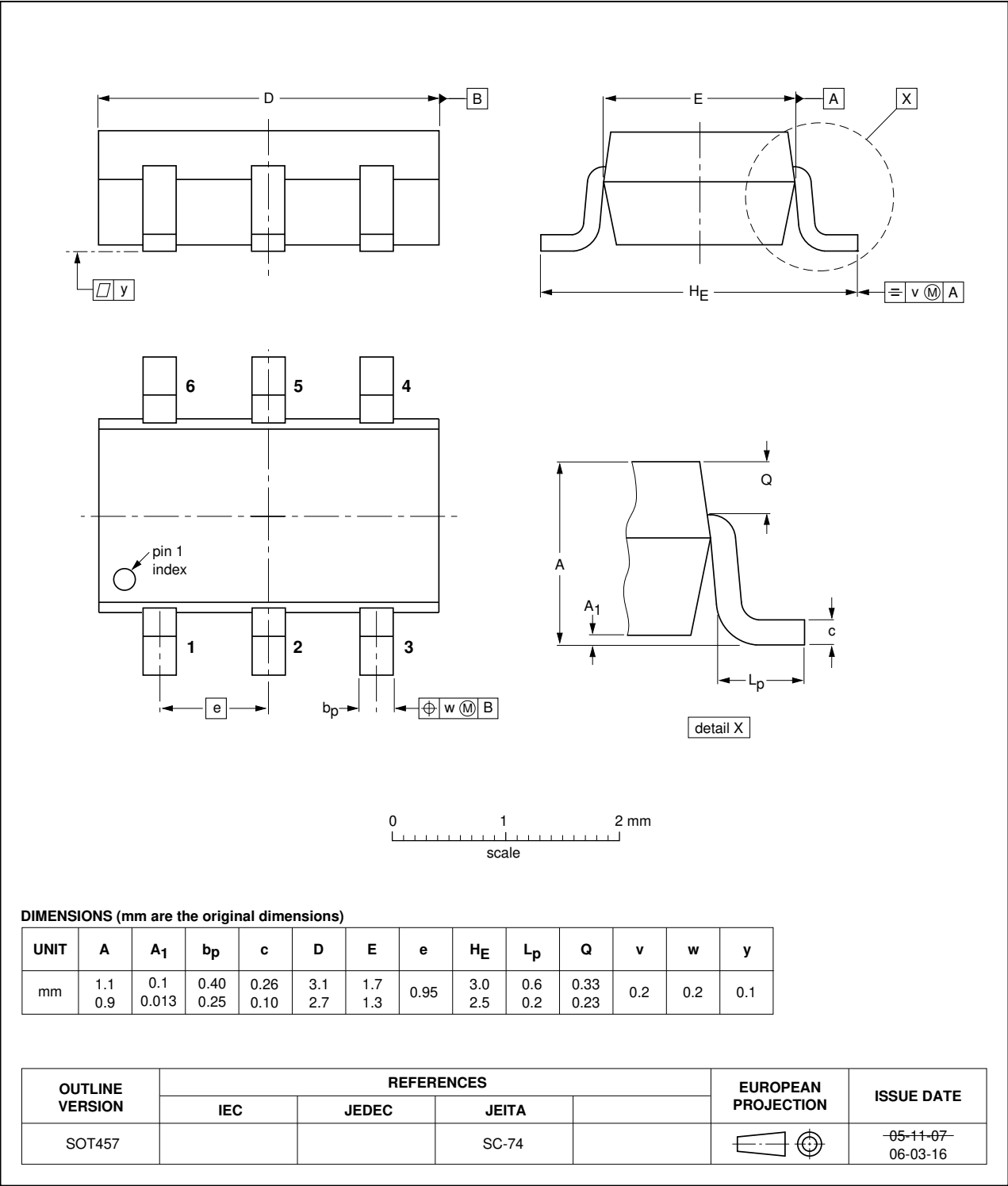


Fig 18. Package outline SOT457 (TSOP6)

10. Soldering

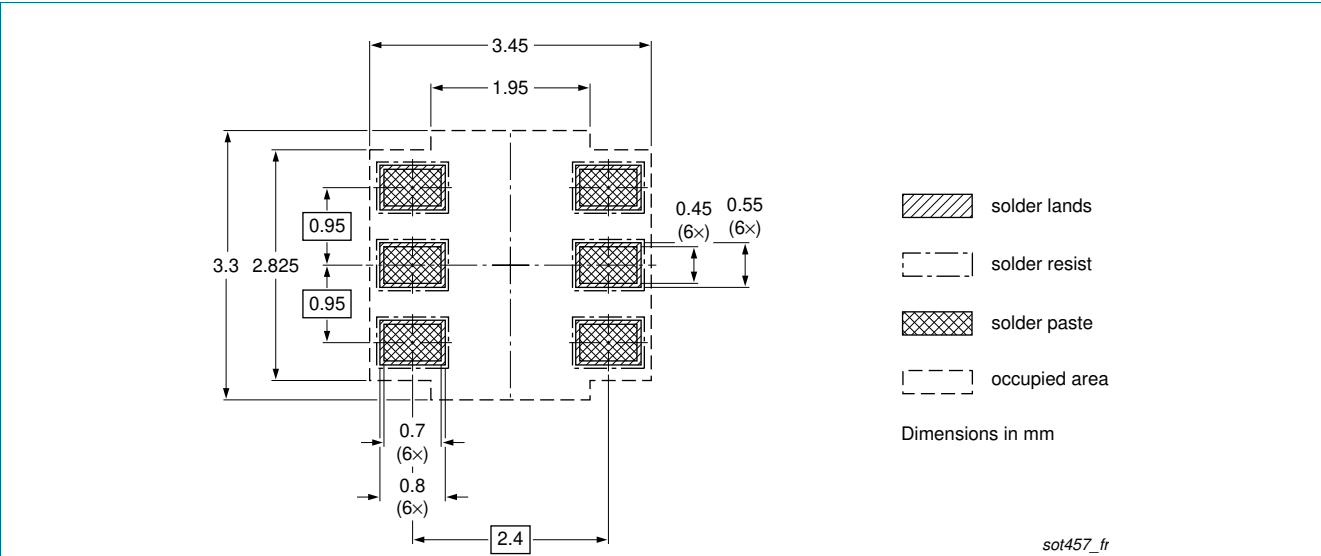


Fig 19. Reflow soldering footprint for SOT457 (TSOP6)

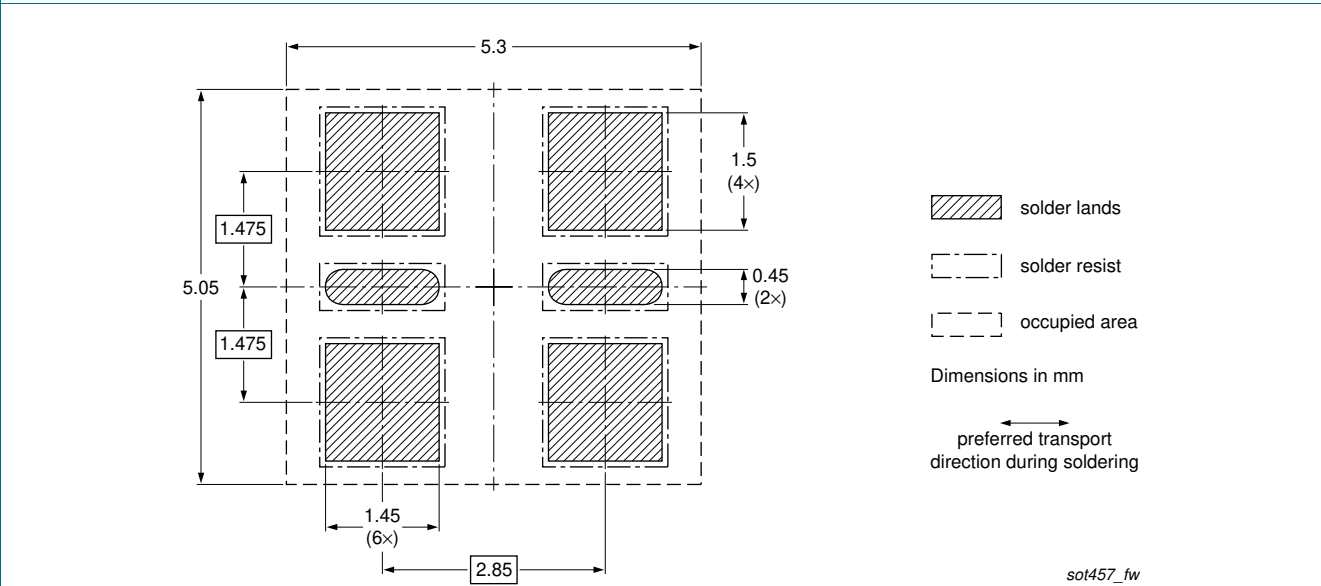


Fig 20. Wave soldering footprint for SOT457 (TSOP6)

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMN25EN v.1	20110829	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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