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Electronic Components Sourcing Information

Product Reference Information

Part Number:	PMGD130UN,115
Manufacturer:	NXP USA Inc.
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nxp-usa-inc/pmgd130un-115.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

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Kind regards,

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PMGD130UN

20 V, dual N-channel Trench MOSFET

Rev. 1 — 1 June 2012

Product data sheet

1. Product profile

1.1 General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology

1.3 Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

1.4 Quick reference data

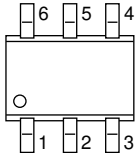
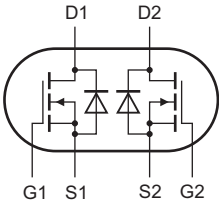
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	20	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = 4.5\text{ V}$; $T_{amb} = 25\text{ °C}$; $t \leq 5\text{ s}$	[1]	-	1.3	A
Static characteristics (per transistor)						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$; $I_D = 1.2\text{ A}$; $T_j = 25\text{ °C}$	-	118	145	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 SOT363 (TSSOP6)	 017aaa254
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMGD130UN	TSSOP6	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PMGD130UN	U8%

[1] % = placeholder for manufacturing site code

5. Limiting values

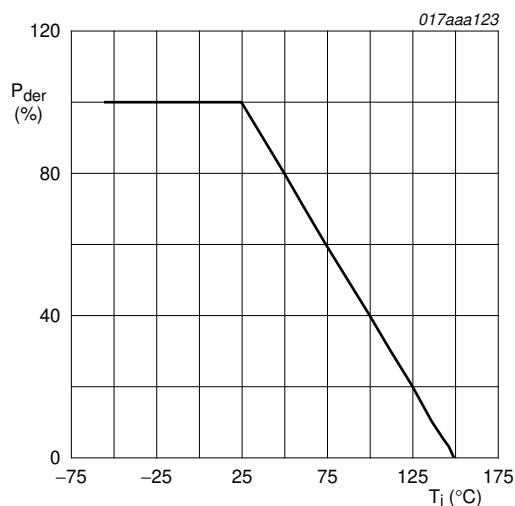
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor					
V _{DS}	drain-source voltage	T _j = 25 °C	-	20	V
V _{GS}	gate-source voltage		-8	8	V
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	1.3	A
		V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	1.2	A
		V _{GS} = 4.5 V; T _{amb} = 100 °C	[1]	0.7	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs	-	4.8	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	260	mW
			[1]	310	mW
		T _{sp} = 25 °C	-	905	mW
Source-drain diode					
I _S	source current	T _{amb} = 25 °C	[1]	0.7	A
Per device					
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	390	mW
T _j	junction temperature		-55	150	°C
T _{amb}	ambient temperature		-55	150	°C
T _{stg}	storage temperature		-65	150	°C

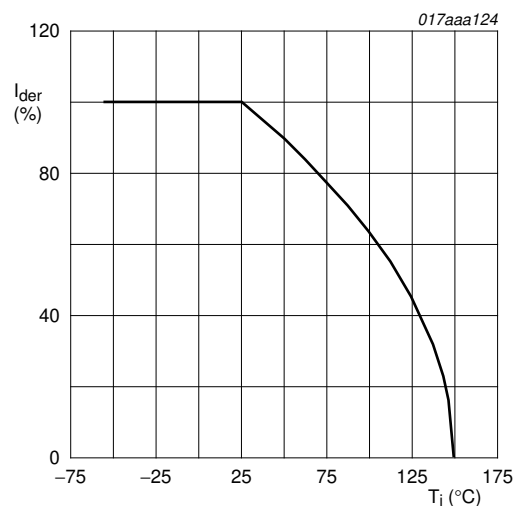
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of junction temperature

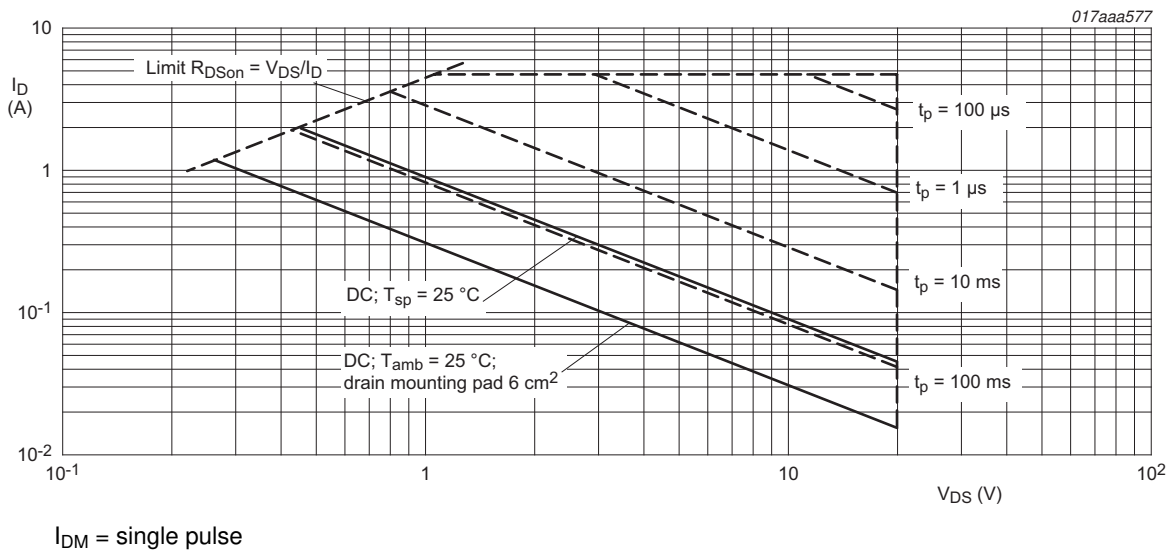


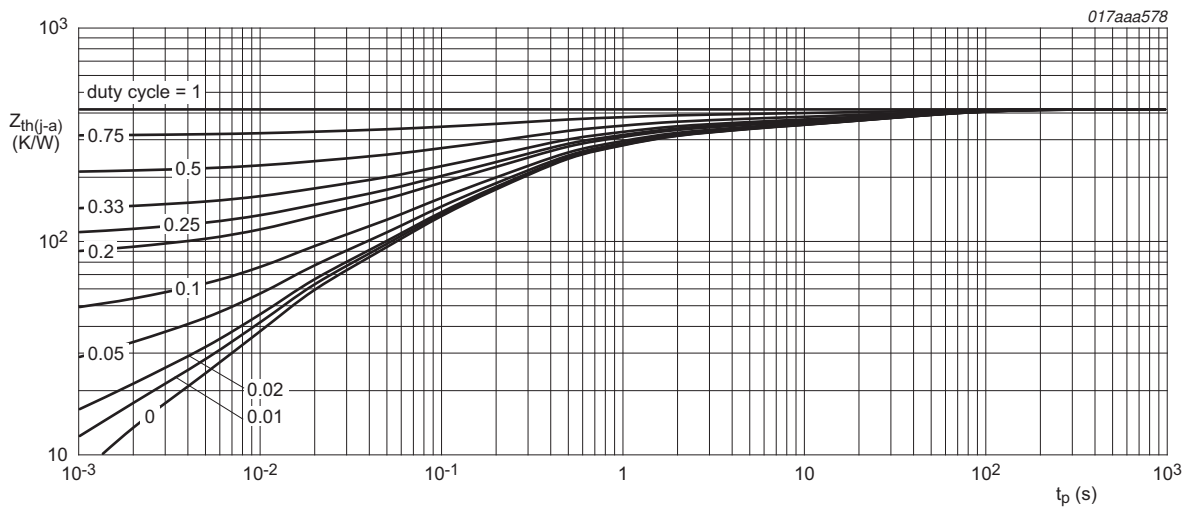
Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

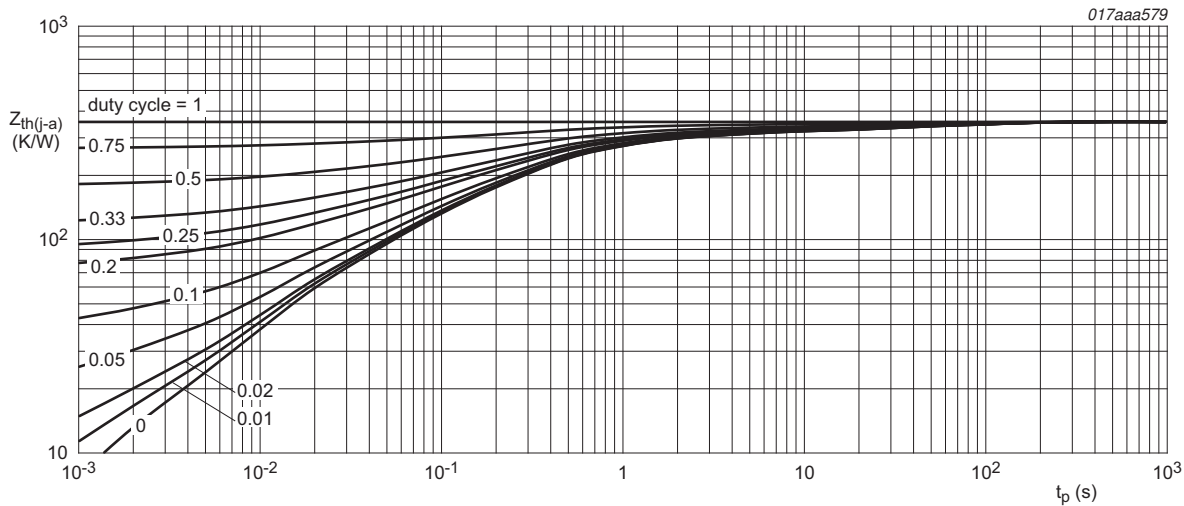
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	417	K/W
			[2]	-	352	K/W
			[3]	-	295	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point		-	120	138	K/W
Per device						
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	320	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm², t ≤ 5 s.



FR4 PCB, standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm²

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics (per transistor)						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250\ \mu\text{A}$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ\text{C}$	0.4	0.7	1	V
I_{DSS}	drain leakage current	$V_{DS} = 20\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 20\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 150\ ^\circ\text{C}$	-	-	10	μA
I_{GSS}	gate leakage current	$V_{GS} = 8\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -8\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}$; $I_D = 1.2\ \text{A}$; $T_j = 25\ ^\circ\text{C}$	-	118	145	m Ω
		$V_{GS} = 4.5\ \text{V}$; $I_D = 1.2\ \text{A}$; $T_j = 150\ ^\circ\text{C}$	-	179	220	m Ω
		$V_{GS} = 2.5\ \text{V}$; $I_D = 1\ \text{A}$; $T_j = 25\ ^\circ\text{C}$	-	155	204	m Ω
		$V_{GS} = 1.8\ \text{V}$; $I_D = 0.25\ \text{A}$; $T_j = 25\ ^\circ\text{C}$	-	213	318	m Ω
g_{fs}	forward transconductance	$V_{DS} = 10\ \text{V}$; $I_D = 1.2\ \text{A}$; $T_j = 25\ ^\circ\text{C}$	-	4.1	-	S
Dynamic characteristics (per transistor)						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 10\ \text{V}$; $I_D = 1.2\ \text{A}$; $V_{GS} = 4.5\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	0.88	1.3	nC
Q_{GS}	gate-source charge		-	0.12	-	nC
Q_{GD}	gate-drain charge		-	0.26	-	nC
C_{iss}	input capacitance	$V_{DS} = 10\ \text{V}$; $f = 1\ \text{MHz}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	83	-	pF
C_{oss}	output capacitance		-	38	-	pF
C_{rss}	reverse transfer capacitance		-	27	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10\ \text{V}$; $I_D = 1.2\ \text{A}$; $V_{GS} = 4.5\ \text{V}$; $R_{G(ext)} = 6\ \Omega$; $T_j = 25\ ^\circ\text{C}$	-	5	-	ns
t_r	rise time		-	17	-	ns
$t_{d(off)}$	turn-off delay time		-	17	-	ns
t_f	fall time		-	7	-	ns
Source-drain diode (per transistor)						
V_{SD}	source-drain voltage	$I_S = 0.7\ \text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	0.8	1.2	V

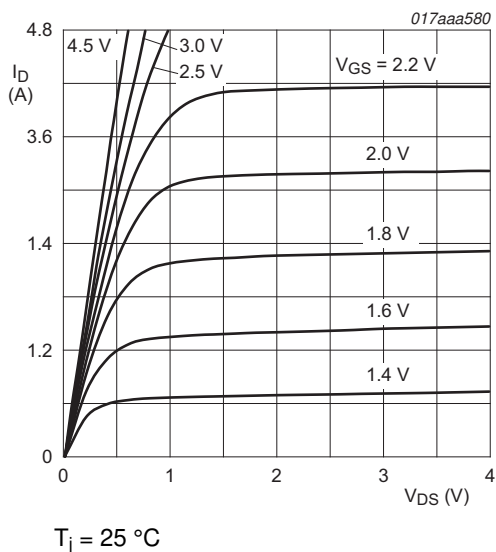


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

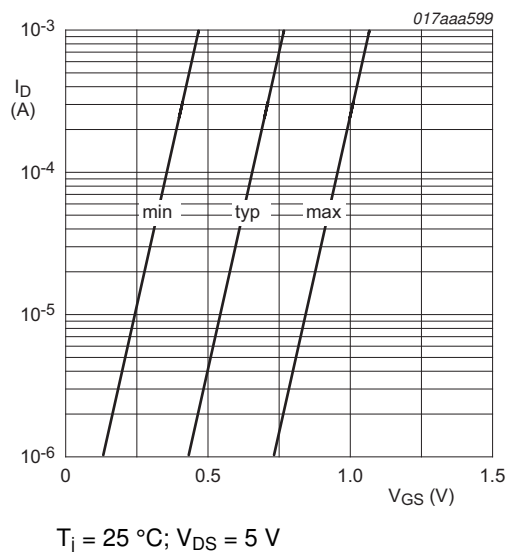


Fig 7. Sub-threshold drain current as a function of gate-source voltage

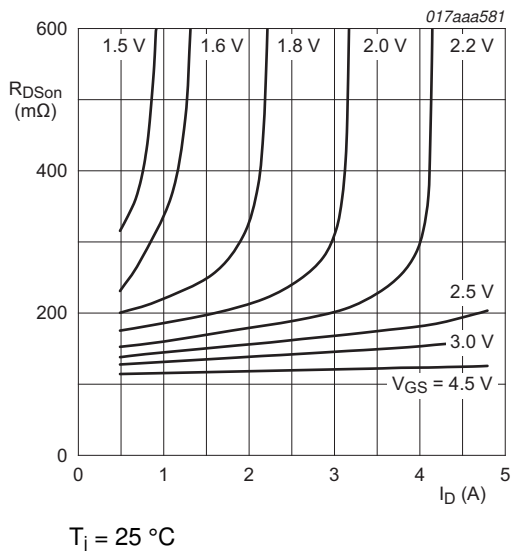


Fig 8. Drain-source on-state resistance as a function of drain current; typical values

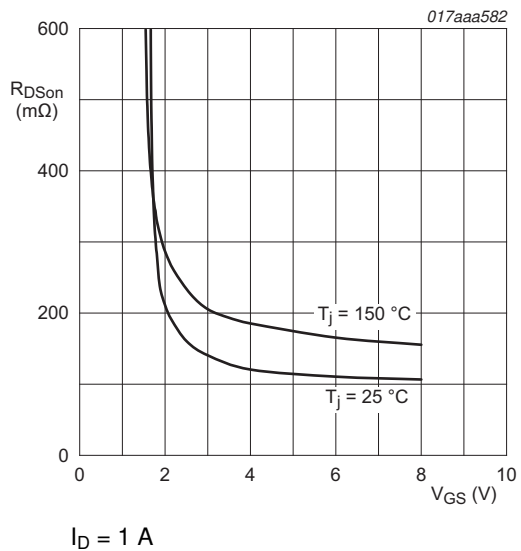


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

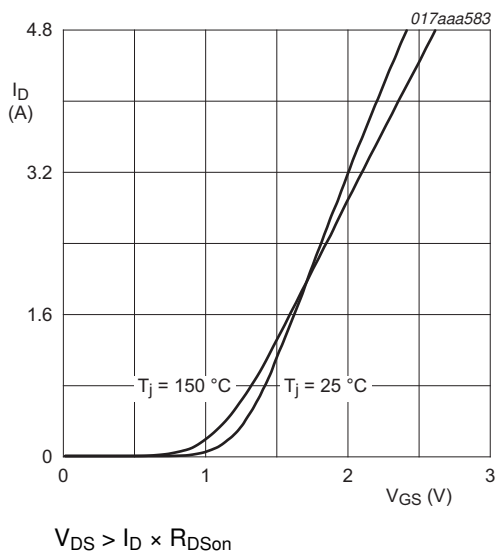


Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

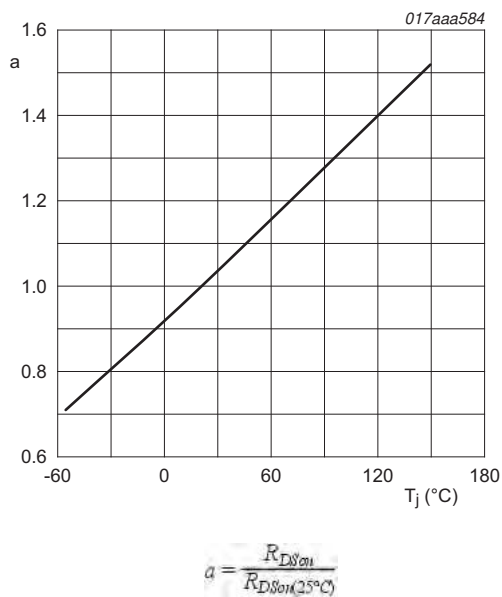
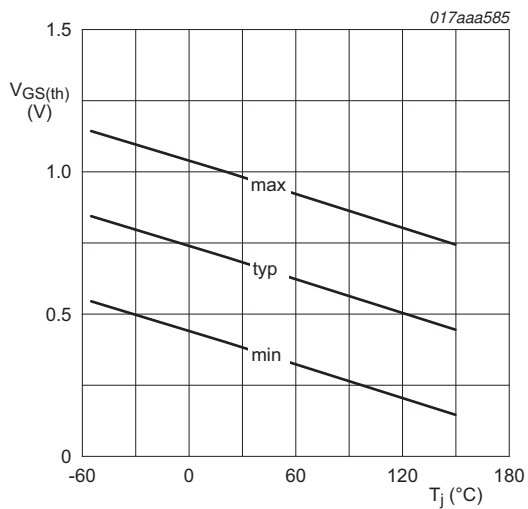
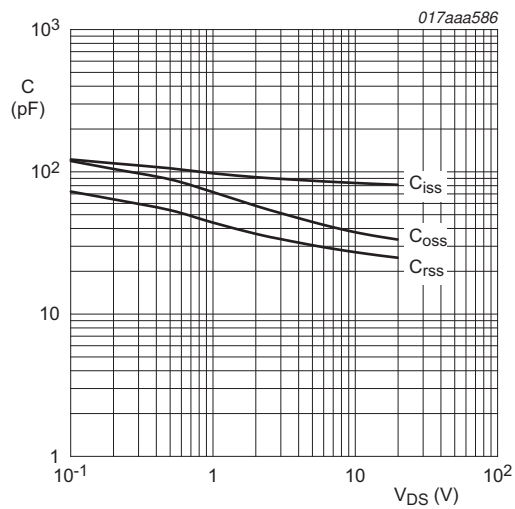


Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



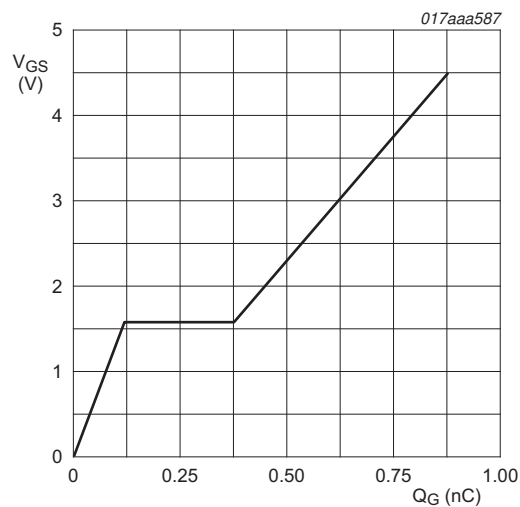
$I_D = 0.25\text{ mA}$; $V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}$; $V_{GS} = 0\text{ V}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 1.2$ A; $V_{DS} = 10$ V; $T_{amb} = 25$ °C

Fig 14. Gate-source voltage as a function of gate charge; typical values

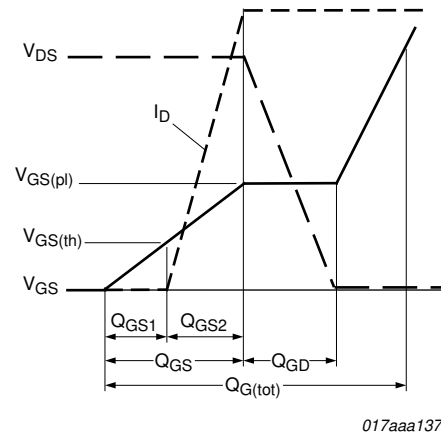
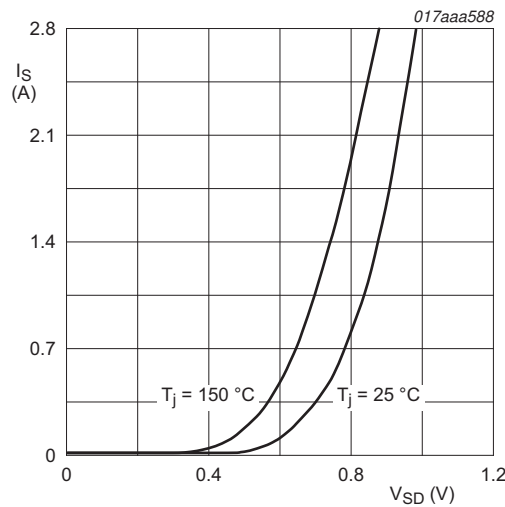


Fig 15. Gate charge waveform definitions



$V_{GS} = 0$ V

Fig 16. Source current as a function of source-drain voltage; typical values

8. Test information

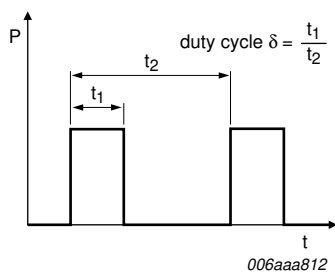


Fig 17. Duty cycle definition

9. Package outline

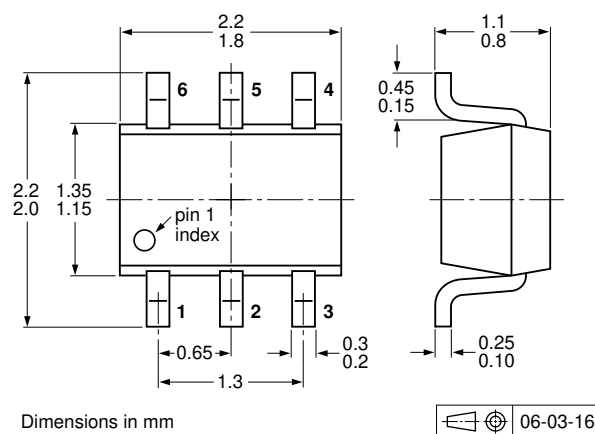


Fig 18. Package outline SOT363 (TSSOP6)

10. Soldering

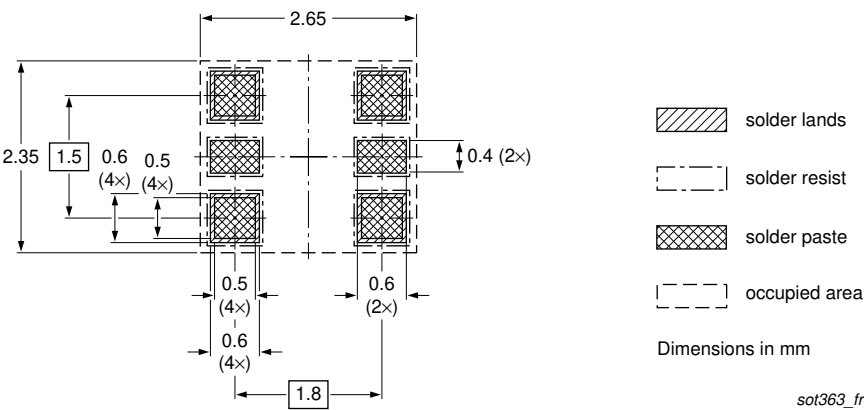


Fig 19. Reflow soldering footprint for SOT363 (TSSOP6)

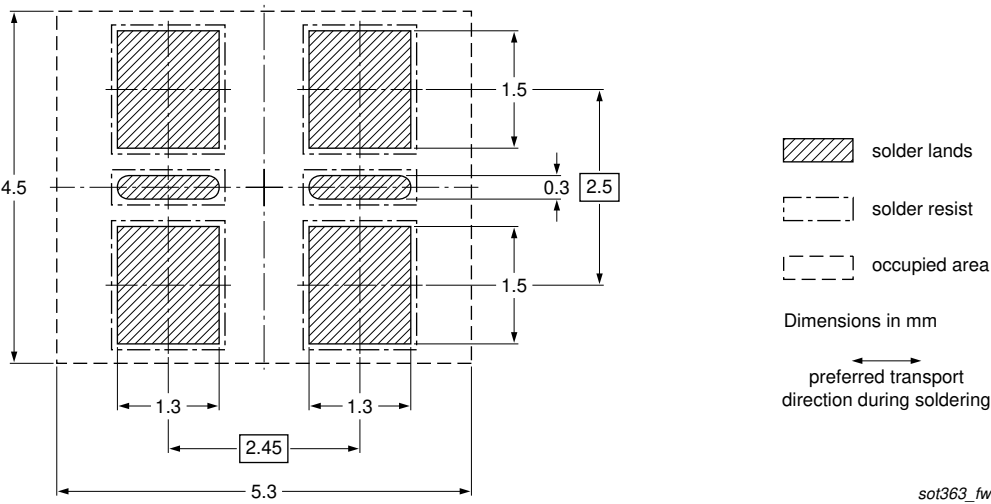


Fig 20. Wave soldering footprint for SOT363 (TSSOP6)

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMGD130UN v.1	20120601	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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