

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	PHD96NQ03LT,118
Manufacturer:	NXP USA Inc.
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nxp-usa-inc/phd96nq03lt-118.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

PHD96NQ03LT

N-channel TrenchMOS logic level FET

Rev. 06 — 15 March 2010

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Simple gate drive required due to low gate charge

1.3 Applications

- DC-to-DC convertors

1.4 Quick reference data

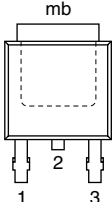
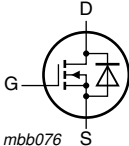
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	25	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 1 and 3	-	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	115	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}$; $I_D = 50\text{ A}$; $V_{DS} = 15\text{ V}$; $T_j = 25\text{ °C}$; see Figure 11	-	8.4	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 9	-	4.2	4.95	mΩ
		$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 9 and 10	-	5.6	7.5	mΩ



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain [1]		
3	S	source		
mb	D	mounting base; connected to drain		

SOT428 (DPAK)

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PHD96NQ03LT	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

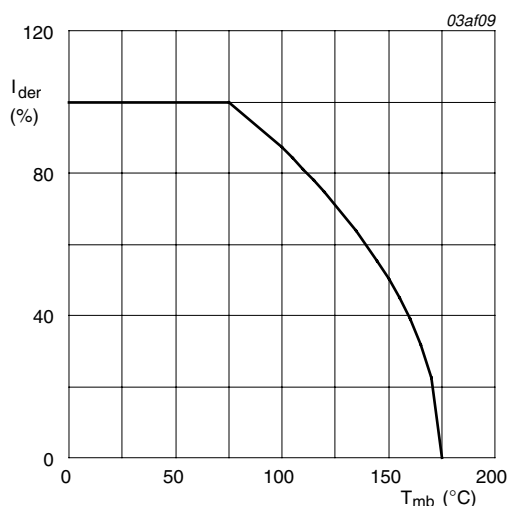
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	25	V
V_{DGR}	drain-gate voltage	$T_j \leq 175\text{ °C}$; $T_j \geq 25\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	65	A
		$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 and 3	-	75	A
I_{DM}	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$; see Figure 3	-	240	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	115	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C

Source-drain diode

I_S	source current	$T_{mb} = 25\text{ °C}$	-	75	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	240	A

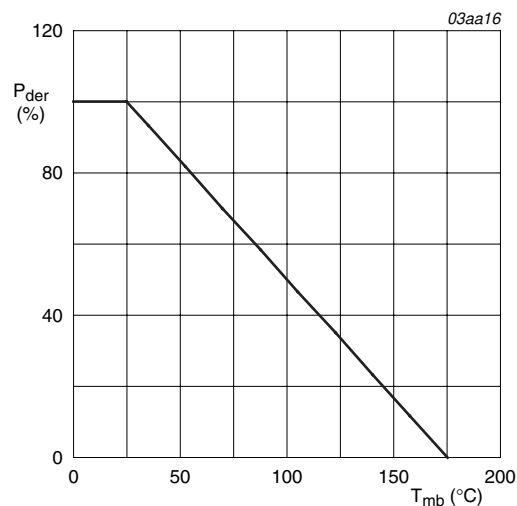
Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 43\text{ A}$; $V_{sup} \leq 15\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $t_p = 0.25\text{ ms}$; unclamped	-	185	mJ
$I_{DS(AL)S}$	non-repetitive drain-source avalanche current	$V_{GS} = 10\text{ V}$; $V_{sup} \leq 15\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $T_{j(\text{init})} = 25\text{ °C}$; unclamped	-	75	A



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

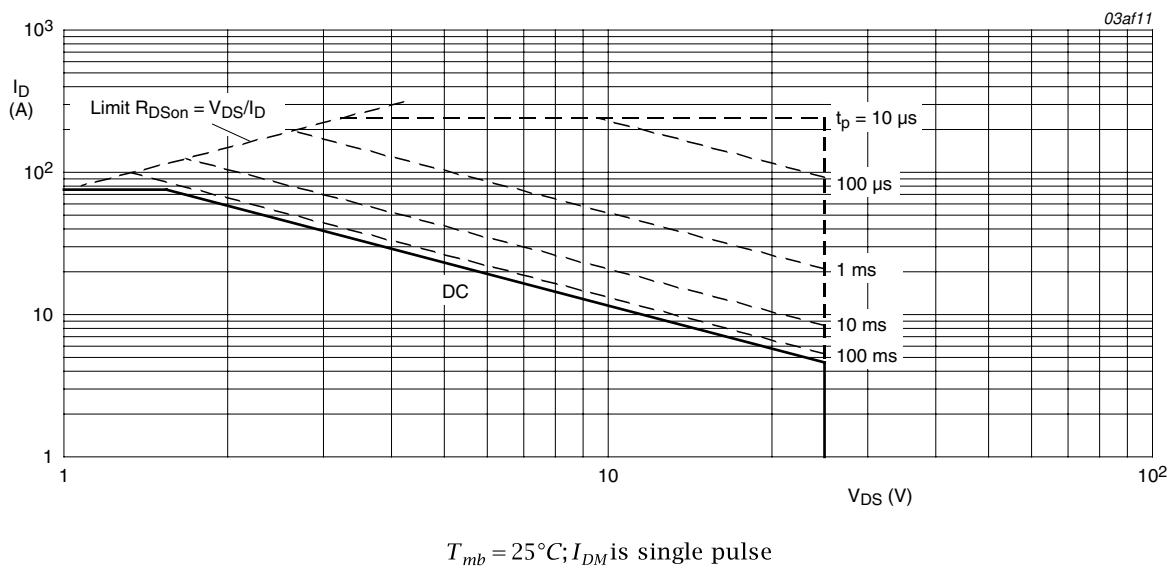


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	75	-	K/W

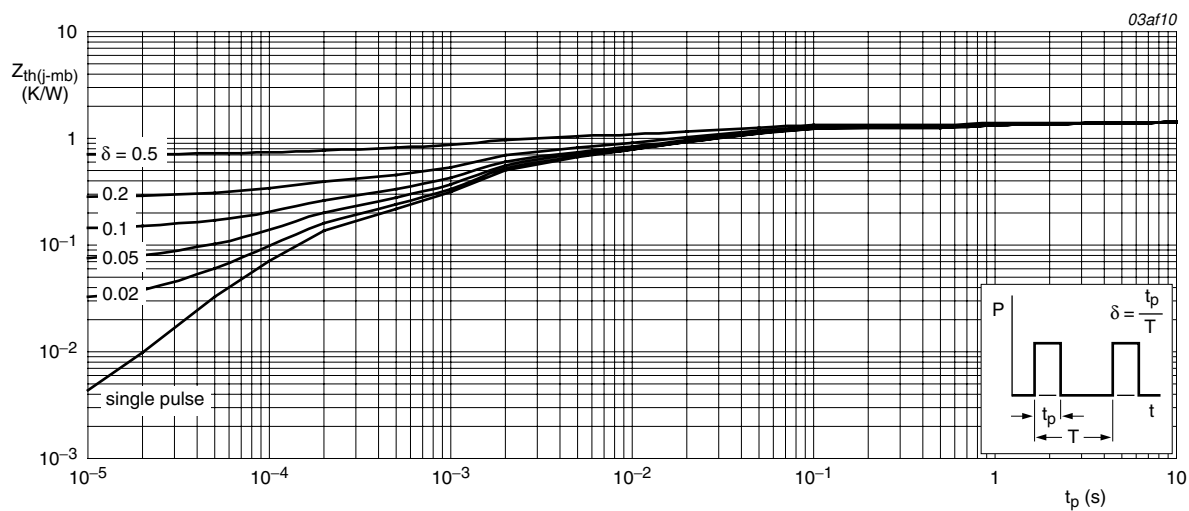


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _j = -55 °C	22	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _j = 25 °C	25	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 8	0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 8	-	-	2.3	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 8	1	1.5	2	V
I _{DSS}	drain leakage current	V _{DS} = 25 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	1	μA
		V _{DS} = 25 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 15 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
		V _{GS} = -15 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; see Figure 9 and 10	-	10	13.5	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 9	-	4.2	4.95	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; see Figure 9 and 10	-	5.6	7.5	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 50 A; V _{DS} = 15 V; V _{GS} = 5 V; T _j = 25 °C; see Figure 11	-	26.7	-	nC
Q _{GS}	gate-source charge		-	8.5	-	nC
Q _{GD}	gate-drain charge		-	8.4	-	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 12	-	2200	-	pF
C _{oss}	output capacitance		-	725	-	pF
C _{rss}	reverse transfer capacitance		-	290	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 15 V; R _L = 1.2 Ω; V _{GS} = 5 V; R _{G(ext)} = 5.6 Ω; T _j = 25 °C; I _D = 12.5 A	-	18	-	ns
t _r	rise time		-	70	-	ns
t _{d(off)}	turn-off delay time		-	75	-	ns
t _f	fall time		-	70	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 13	-	0.9	1.2	V
t _{rr}	reverse recovery time	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 25 V; T _j = 25 °C	-	43	-	ns
Q _r	recovered charge		-	40	-	nC

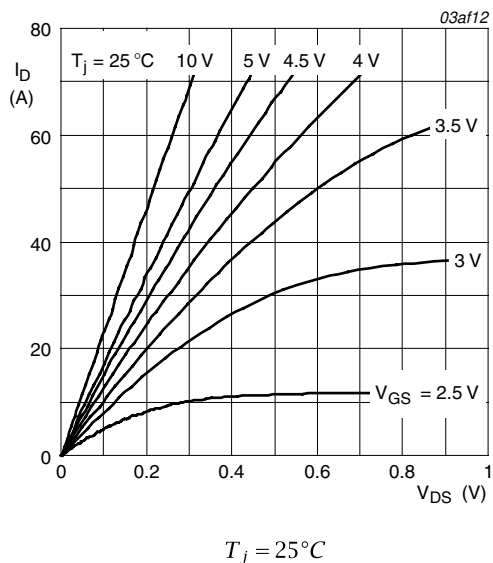


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

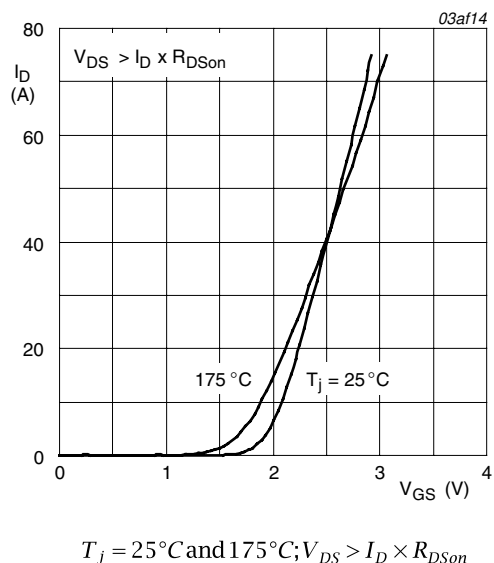


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

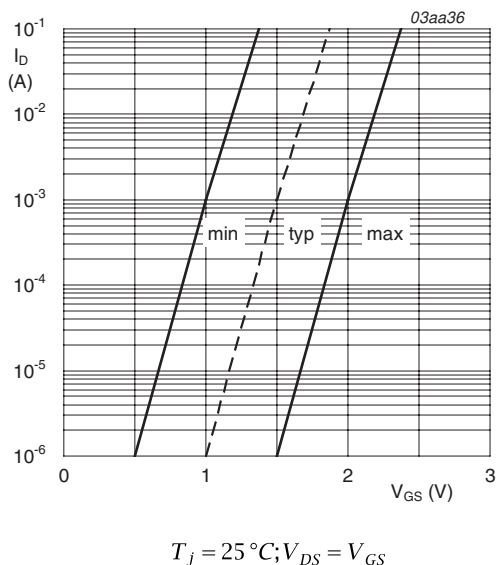


Fig 7. Sub-threshold drain current as a function of gate-source voltage

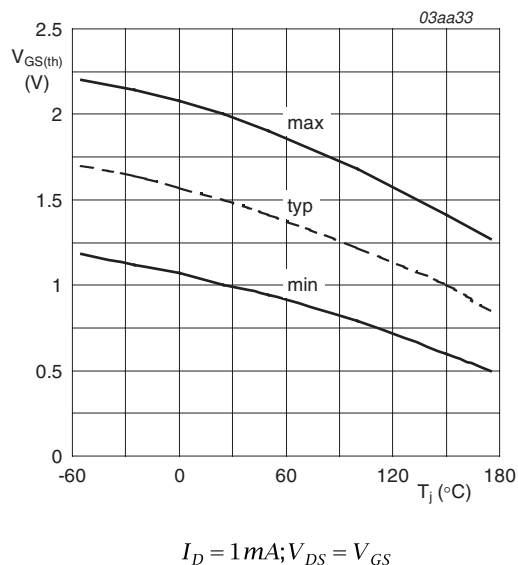


Fig 8. Gate-source threshold voltage as a function of junction temperature

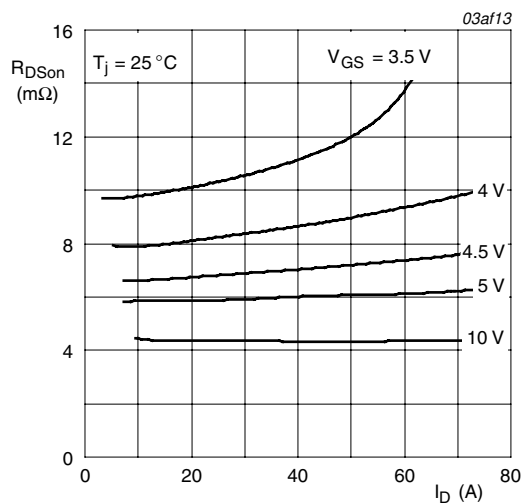
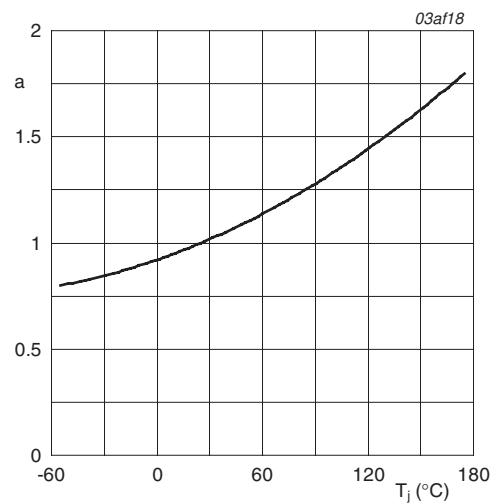


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature

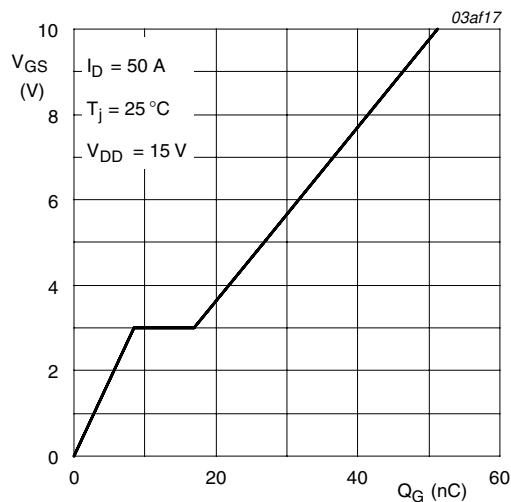


Fig 11. Gate-source voltage as a function of gate charge; typical values

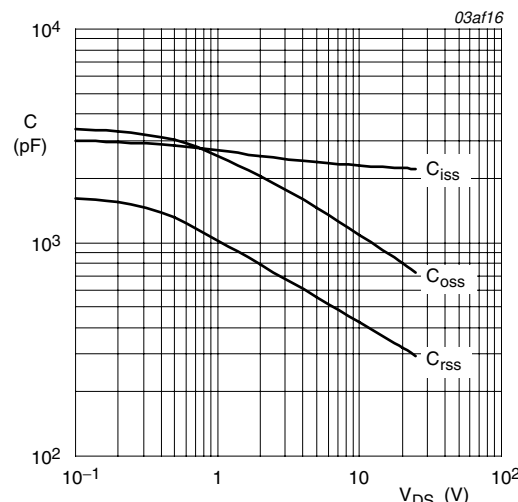
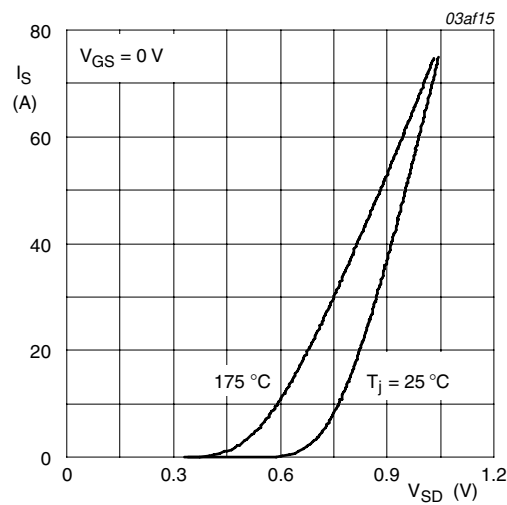


Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25\text{ °C}$ and $175\text{ °C}; V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) SOT428

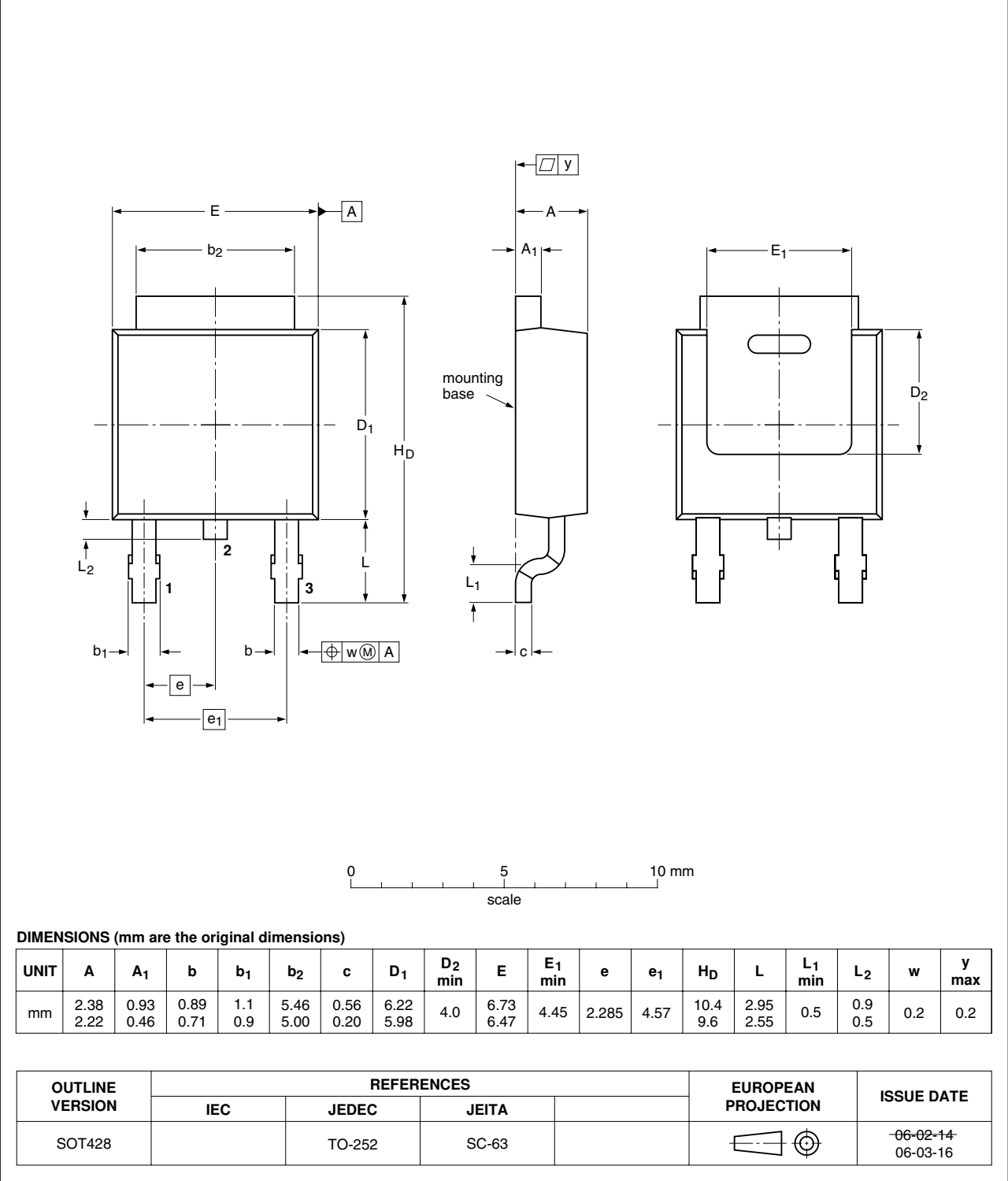


Fig 14. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD96NQ03LT_6	20100315	Product data sheet	-	PHP96NQ03LT-05
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate.			
PHP96NQ03LT-05 (9397 750 09666)	20020605	Product data	-	PHP96NQ03LT-04
PHP96NQ03LT-04	20020220	Product data	-	PHP96NQ03LT-03
PHP96NQ03LT-03	20011023	Product data	-	PHP96NQ03LT-02
PHP96NQ03LT-02	20011008	Product data	-	PHP96NQ03LT-01
PHP96NQ03LT-01	20010716	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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11. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	3
5	Thermal characteristics	4
6	Characteristics	5
7	Package outline	9
8	Revision history	10
9	Legal information	11
9.1	Data sheet status	11
9.2	Definitions	11
9.3	Disclaimers	11
9.4	Trademarks	12
10	Contact information	12

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