

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: MCXN547VNLT
Manufacturer: NXP USA Inc.
Package: -
Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nxp-usa-inc/mcxn547vnl.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

MCXN23x

Arm® Cortex®-M33 150MHz 32-bit MCU, up to 1MB Flash

Rev. 3 — 21 January 2025

Product Data Sheet

Features

- Arm Cortex-M33 150MHz with 618 CoreMark® (4.12 CoreMark/MHz)
- Up to 1MB Flash, 352 KB SRAM
- Platform Security with EdgeLock® Secure Enclave, Core Profile
- - 40 °C to + 125 °C temperature range
- Down to 50 µA/MHz active current, 3.0 µA Power down mode with RTC enabled and 352 KB SRAM retention, 1.5 µA Deep Power-down mode with RTC active and 32 KB SRAM

Cores

- Arm 32-bit Cortex-M33 CPU with TrustZone®, MPU, FPU, SIMD, ETM and CTI

Processing Accelerators

- SmartDMA (co-processor for applications such as parallel camera interface and keypad scanning)

Memories

- Up to 1 MB (2 x 512KB Bank) on chip Flash memory supporting Flash Swap and Read While Write, with ECC (support one bit correction and two bits detection)
- Cache Engine with 16 KB RAM
- Up to 352 KB RAM, configurable as up to 288 KB with ECC (support one bit correction and two bits detection)
- Up to 4x 8 KB ECC RAM can be retained down to VBAT mode
- 256 KB ROM with secure bootloader

Security

- EdgeLock Secure Enclave, Core Profile
 - Cryptographic services (incl. AES-256, SHA-2, ECC NIST P-256, TRNG and key generation/derivation)
 - Secure key store with key usage policies (protection of platform integrity, manufacturing and applications keys)
 - Device Unique Identity based on Physically Unclonable Function (PUF)
 - Device Attestation with support of Device Identifier Composition Engine (DICE)
 - Secure connection and TLS support
 - Key management over-the-air with pre-integration of NXP EdgeLock 2GO
- EdgeLock Accelerator (Public Key Cryptography)
- Immutable secure boot code in ROM
- Dual Secure Boot Mode (asymmetric mode and fast, post-quantum secure symmetric mode)
- Secure firmware update support
- Device lifecycle management including secure authenticated debug

MCXN23x



184VFBGA

9 x 9 x 0.86 mm,
0.5 mm



100HLQFP

14 x 14 x 1.4 mm,
0.5 mm



172HDQFP

16 x 16 x 1.65 mm, 0.65 mm



- High-performance on-the-fly memory encryption with additional authentication for internal Flash
- Implicit-protected Flash Region (IFR)
- Security Monitoring:
 - 2x Code Watchdog
 - Intrusion and Tamper Response Controller (ITRC)
 - 6 Active and Passive Tamper Pin Detect
 - Voltage, Temperature, Light and Clock Tamper Detect
 - Voltage glitch detect
- Secure manufacturing and IP theft protection in untrusted factory
- Arm TrustZone for Cortex-M

Low-Power Performance

- Active: down to 50 μ A/MHz
- Deep Sleep: 124 μ A, (full 352 KB SRAM retention, 3.3 V @25 C)
- Power Down: 2.39 μ A, (full 352 KB SRAM retention, 3.3 V, @25 C)
- Deep Power Down: 1.5 μ A, 5.6 ms wake-up (RTC enabled and 32 KB RAM and Reset pin enabled, @25 C)

System and Clocks

- 144 MHz free-running oscillator (FRO144M)
- 12 MHz free-running oscillator (FRO12M)
- 16 KHz free-running oscillator (FRO16K)
- 32 KHz low-power crystal oscillator
- Up to 50 MHz low-power crystal oscillator
- 2 x phase-locked loop
- Hardware and Software Watchdogs
- Two asynchronous DMA modules (1x 16-channels, 1x 8-channels)

Communication Interfaces for Connectivity

- 8 x Low-Power Flexcomms each supports SPI, I2C, UART
- USB High-speed (Host/Device) with on-chip HS PHY
- 2x FlexCAN with FD
- 2x I3C

Human-Machine Interfaces

- 1x FlexIO programmable as a variety of serial and parallel interfaces, including but not limited to display driver and camera interface
- 2x Serial Audio Interface (SAI)
- Digital PDM Microphone
 - allows connection of up to 4 MEMS microphones with PDM output

Advanced Motor Control

- 2x FlexPWM each with 4 sub-modules, providing 12 PWM outputs (no Nanoedge module)
- 2x Quadrature Decoder(QDC)

- 1x Event Generator (AND/OR/INVERT) module support up to 8 output trigger

Analog

- 2x 16-bit ADC, supporting 4 parallel conversions
 - Each ADC can be used as two single end input ADC, or one differential input ADC
 - up to 2 Msps in 16-bit mode, and 3.15 Msps in 12-bit mode
 - up to 61 ADC Input channels (depending on the package)
 - one integrated temperature sensor per ADC
- Two High-speed Comparators with 11 input pins and 8-bit DAC as internal reference
- 2x CMP is functional down to Deep Power Down mode
- Highly accurate VREF $\pm 0.2\%$ and 15 ppm/deg C drift

Timers

- Five 32-bit standard general-purpose asynchronous timers/counters, which support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests.
- Low-Power Timer
- Frequency measurement timer
- Multi-Rate Timer
- Windowed Watchdog Timer
- RTC with calendar
- Wake Timer
- Micro-Tick Timer (UTICK)
- OS Event Timer

General-purpose input/outputs

- Up to 106 GPIOs
- 1.2 V support at reduced performance (available only on Fast pads)
- Five independent IO power rings
- 100 MHz IO on P2 and P3
- Up to 28-pin wake-up sources function down to deep power-down mode
- Support 1.71 V~3.6 V IO supply range

Power Management

- Integrated voltage regulator
 - Buck DC-DC, Core LDO, other LDOs
- Separate AON domain on VDD_BAT pin
- Operating voltage: 1.71 V to 3.6 V
- IOs: 1.71 V-3.6 V full-performance

Target Applications

Industrial

- Energy Storage and Management System
- Smart Metering
- Factory Automation

- Industrial HMI
- Mobile Robotics Ecosystem
- Motion Control and Robotics
- Motor Drives
- Brushless DC Motor (BLDC) Control
- Permanent Magnet Synchronous Motor (PMSM)
- Edge AI/ML Anomaly Detection and Predictive Maintenance

Smart Home

- Home Control Panel
- Home Security and Surveillance
- Major Home Appliances
- Robotic Appliance
- Smart Speaker
- Soundbar
- Gaming Accessories
- Smart Lighting
- Smart Power Socket and Light Switch

Table 1. Ordering information¹

Orderable Part Number ^{2,3}	Marking ⁴	Embedded Memory		Features			Package	
		Flash (KB)	SRAM (KB)	Tamper Pins (max)	GPIOs (max)	SRAM PUF	Pin Count	Type
(P)MCXN236VKLT	(P)MCXN236V	1024	352	2	74	Y	100	HLQFP
(P)MCXN235VKLT	(P)MCXN235V	512	192	2	74	Y	100	HLQFP
(P)MCXN236VDFT	(P)MCXN236V	1024	352	6	106	Y	184	VFBGA
(P)MCXN235VDFT	(P)MCXN235V	512	192	6	106	Y	184	VFBGA
(P)MCXN236VPBT	(P)MCXN236V	1024	352	6	103	Y	172	HDQFP
(P)MCXN235VPBT	(P)MCXN235V	512	192	6	103	Y	172	HDQFP

1. Devices with prefix "P" are pre-qualification devices. Fully qualified general market flow devices will not include this "P" prefix.
2. To confirm current availability of orderable part numbers, go to <http://www.nxp.com> and perform a part number search.
3. Previous HLQFP parts with suffix VNLT (MCXNxxxVNLT) have been deprecated and are replaced with VKLT suffix (MCXNxxxVKLT).
4. As marked on package

Table 2. Device Revision Number

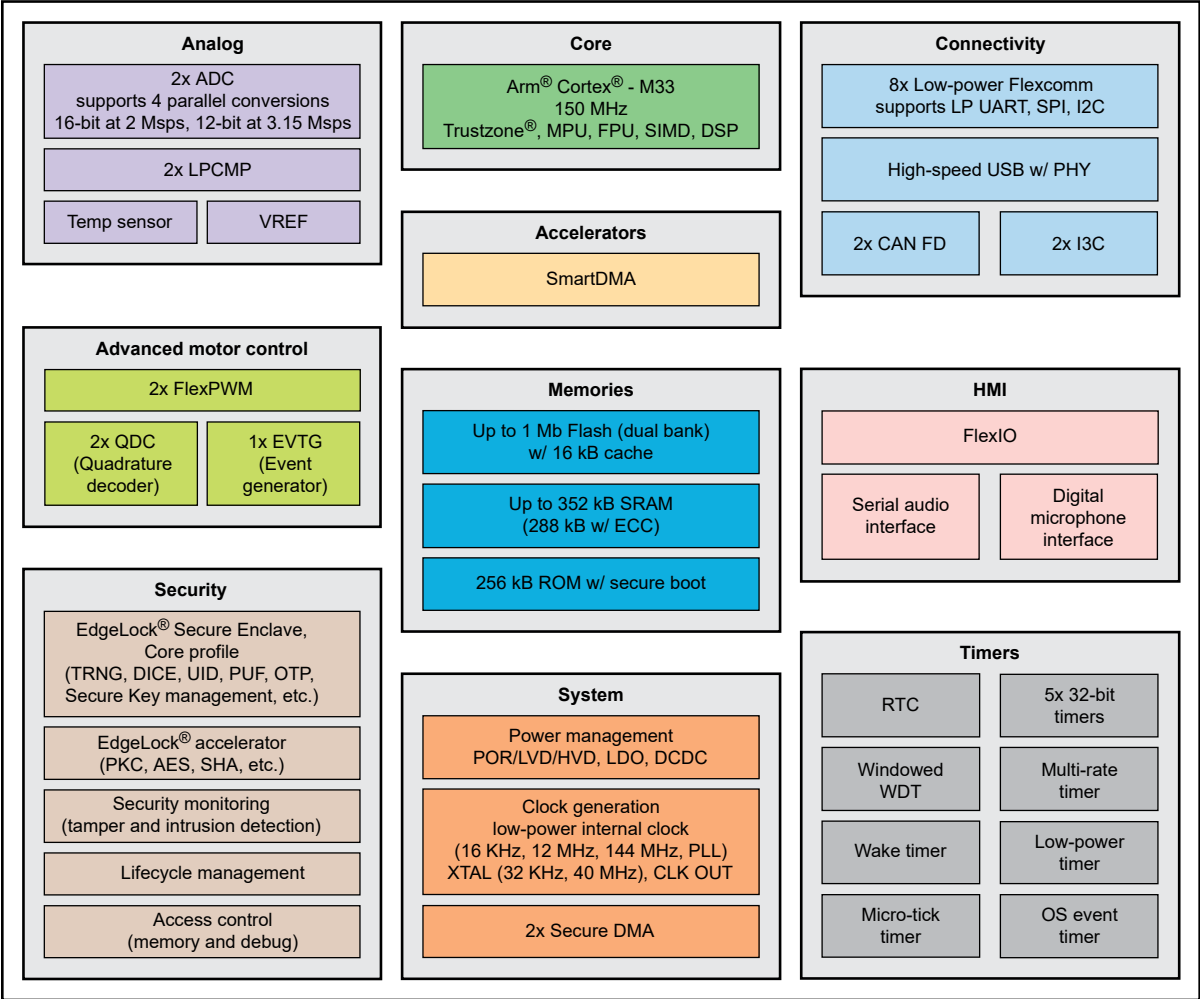
Device Mask Set Number	SYSCON[DIEID]	JTAG ID Register[PRN]
0P21K	0x0059D9A0	0x0726502B

Table 3. Related Resources

Type	Description	Resource
Fact Sheet	The Fact Sheet gives overview of the product key features and its uses.	Fact sheet
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	MCXN23xRM
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	MCXN23x_0P21K
Package drawing	Package dimensions are provided in package drawings.	• HLQFP 100-pin: 98ASA02131D • BGA 184-pin: 98ASA01888D • HDQFP 172-pin: 98ASA01107D
Software development kit	MCUXpresso SDK. An open source software development kit (SDK) built specifically for your processor and evaluation board selections.	http://www.nxp.com/mcuxpresso

NOTE

The EdgeLock Secure Subsystem (ELS) is also known as EdgeLock Secure Enclave, Core Profile (ELE). This document uses the ELS name, but other materials might refer to this module as EdgeLock Secure Enclave, Core Profile or ELE.



aaa-058841

Figure 1. MCXN23x Block diagram

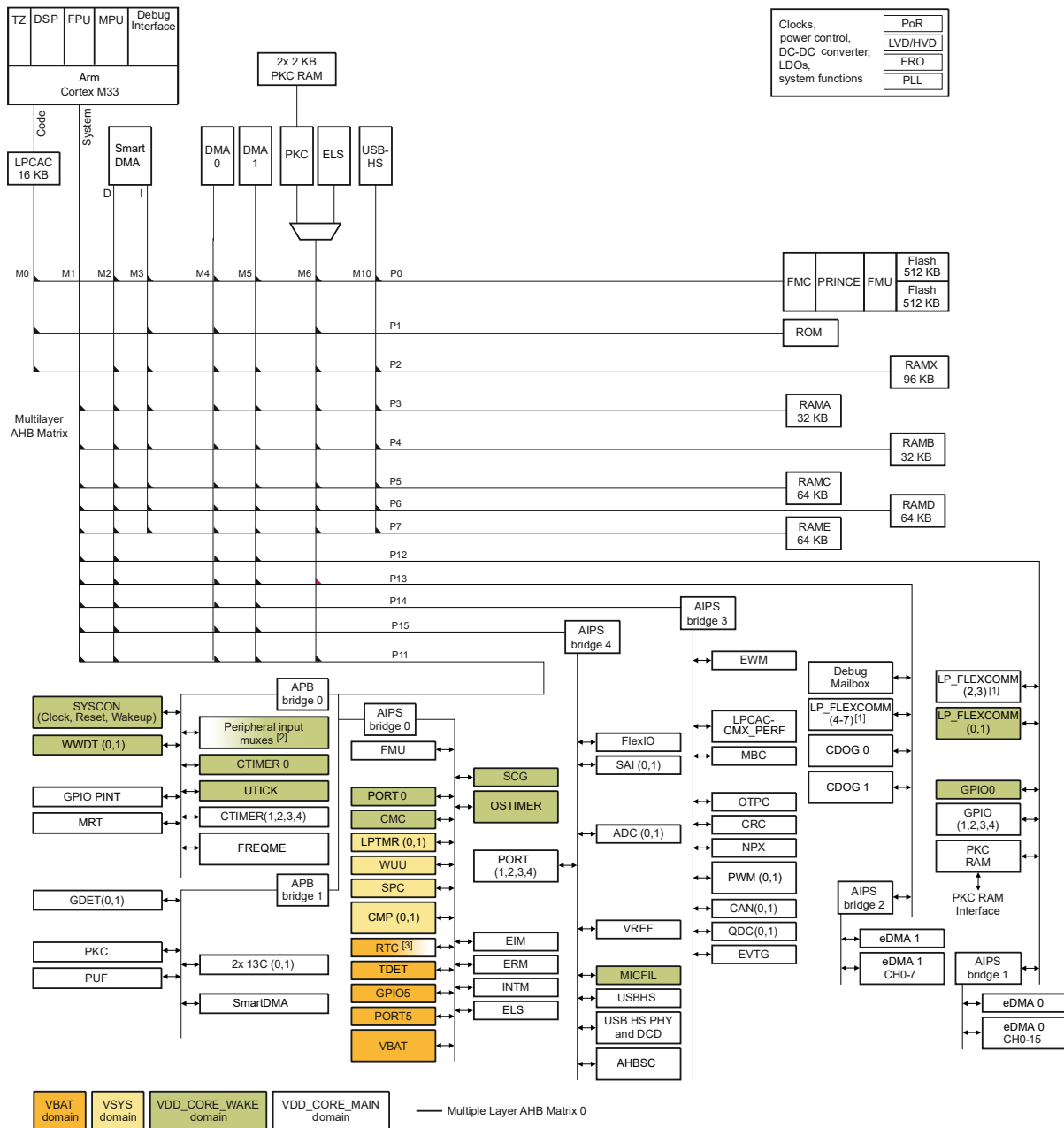


Figure 2. MCXN23x Architecture

NOTE

Flash and bus masters, including eDMA, USB HS (USB1), PKC, S50 have registers. The registers can be accessed from APB or AIPS bridge.

1 Feature Comparison

Table 4. Feature Comparison

Features		MCXN236	MCXN235
	Package	VFBGA184, HLQFP100, HDQFP172	VFBGA184, HLQFP100, HDQFP172
CPU Core Platform	M33 @150 MHz	1	1
Flash¹	Flash ECC	Upto 1 MB	Upto 512 KB
Memory	SRAM1	Upto 320 K no ECC	Upto 160 K no ECC
	SRAM ECC	32 K	32 K
Security	Secure Key Management	PUF/UDF	PUF/UDF
	Secure Subsystem	Y	Y
	Anti Tamper Pin ²	6	6
Analog peripherals	ADC	2	2
	ADC channel number	VFBGA184 (DF)	61
		HLQFP100 (KL)	41
		HDQFP172 (PB)	59
	Low power comparator (LPCMP)	2	2
	Accurate Vref	Y	Y
Serial Interfaces	I3C (I2C back compatible)	2	2
	USB HS	Y	Y
	CAN w/wo FD	2	2
	SAI	4 ch	4 ch
	Flexcom	8	8
Human Machine Interface	Flexible I/O (FlexIO)	1	1
	DMIC	4 ch	4 ch
Motor Control Subsystem	FlexPWM	2	2
	Quadrature decoder (QDC)	2	2
Timers	RTC	1	1
	32-bit timer (Ctimer)	5	5
	Multi-Rate Timer (MRT)	1	1
	Micro-tick Timer (UTICK)	1	1
	Windowed watchdog timer (WWDT)	1	1
	Low power timer (LPTMR)	1	1

Table continues on the next page...

Table 4. Feature Comparison....continued

Features		MCXN236	MCXN235
	Wake timer	1	1
	OS Timer	1	1

1. For more details, please refer to Table 1
2. Only 2 Anti Tamper pins available on 100 HLQFP packages

2 Ratings

2.1 Thermal handling ratings

Table 5. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	–55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

2.2 Moisture handling ratings

Table 6. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

2.3 ESD handling ratings

Table 7. ESD and Latch-up ratings

Description	Rating	Notes
Electrostatic discharge voltage, human body model	+/-2000 V	1
Electrostatic discharge voltage, charged-device model	+/-500 V	2
Electrostatic discharge voltage, charged device model (corner pins)	+/-750 V	
Latch-up immunity level (Class II at 125 °C junction temperature)	Immunity Level A	3

1. Determined according to ANSI/ESDA/JEDEC Standard JS-001-2023, For Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM) - Component Level.
2. Determined according to ANSI/ESDA/JEDEC Standard JS-002-2022, For Electrostatic Discharge Sensitivity Testing, Charged Device Model (CDM) - Device Level
3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

2.4 Voltage and current maximum ratings

The table below shows the absolute minimum and maximum ratings for the device. If the values are violated, the device could be damaged. See [Voltage and current operating requirements](#) for operating requirements, and [Terminology and guidelines](#) for definitions of terms.

Table 8. Voltage and current maximum ratings

Symbol	Description	Min.	Max.	Unit
VDD_CORE	Supply voltage for most digital domains	−0.3	1.26	V
VDD_SYS	Supply voltage for on-board regulators, LVD / HVDs, and clock sources	−0.3	1.98 ¹	V
VDD_DCDC	Supply voltage for DCDC regulator	−0.3	3.63	V
VDD_LDO_SYS	Supply voltage for LDO_SYS regulator	−0.3	3.63	V
VDD_LDO_CORE	Supply voltage for LDO_CORE regulator	−0.3	3.63	V
VDD	Supply voltage for Port 0, Port 1, Flash arrays	−0.3	3.63	V
VDD_P2	Supply voltage for Port 2	−0.3	3.63	V
VDD_P3	Supply voltage for Port 3	−0.3	3.63	V
VDD_P4	Supply voltage for Port 4	−0.3	3.63	V
VDD_BAT	Supply voltage for VBAT domain and Port 5	−0.3	3.63	V
VDD_ANA	Supply voltage for analog modules	−0.3	3.63	V
VDD_USB	Supply voltage for USB analog	−0.3	3.63	V
V _{USB1_VBUS}	USB1_VBUS input voltage	−0.3	5.5	V
V _{USB1_Dx}	USB1_DP and USB1_DM input voltage	−0.3	3.63	V
V _{DIO}	Digital input voltage	−0.3	VDD_Px + 0.3	V
V _{AIO}	Analog input voltage ²	−0.3	VDD_ANA + 0.3	V
I _{DD}	Digital supply current	—	100 ³	mA
I _D	Maximum current single pin limit (digital output pins)	−25	25	mA
V _{REFH}	ADC reference voltage high	VSS_P4 −0.1	VDD_ANA + 0.1	V
V _{REFL}	ADC reference voltage low	VSS_P4 −0.1	VSS_P4 + 0.1	V

1. The part will support 2.75 V for up to 20 s over lifetime to allow for fuse programming
2. Analog pins are defined as pins that do not have an associated general-purpose I/O port function.
3. This limit is per supply pin. This includes all power pins, including, VDD_CORE, VDD_SYS, VDD_LDO_SYS, VDD_LDO_CORE, VDD, VDD_Px, VDD_ANA, VDD_USB, and VDD_BAT

2.5 Required Power-On-Reset (POR) Sequencing

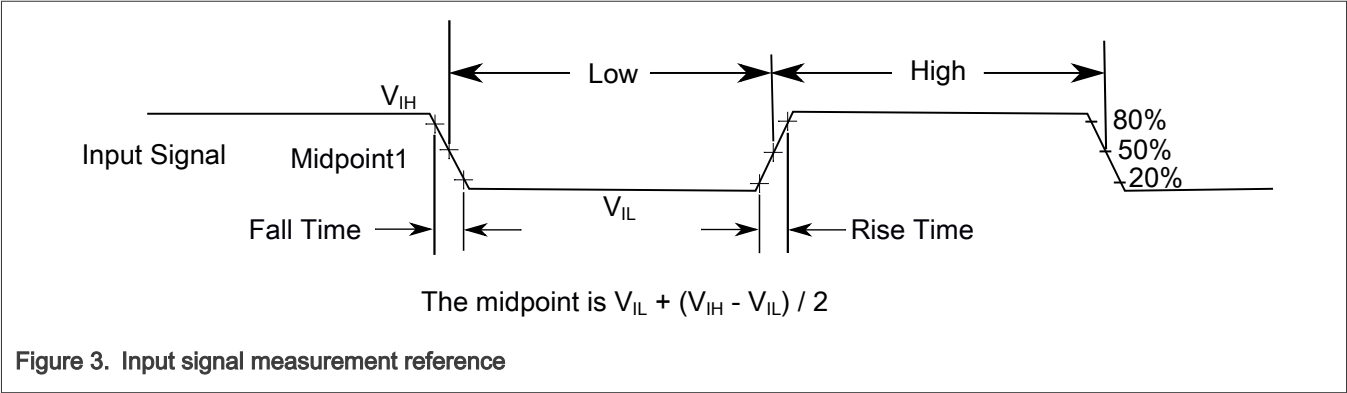
- Secondary IO supplies (VDD_P2/VDD_P3/VDD_P4) must implement one of the following:
 - Must be shorted with VDD (eg: single supply system), or
 - Must ramp after VDD_SYS

- VDD_CORE must ramp after VDD
- VDD_P4 and VDD_ANA must be same voltage
- VDD_BAT must ramp before or with VDD_SYS

3 General

3.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



3.2 Nonswitching electrical specifications

3.2.1 Voltage and current operating requirements

Table 9. Voltage and current operating requirements

Symbol	Description	Min.	Typ	Max.	Unit	Notes
VDD_CORE	Supply voltage for most digital domains				V	1
	• Mid voltage	0.95	1.0	1.05		
	• Normal voltage	1.045	1.1	1.155		
	• Overdrive voltage	1.14	1.2	1.26		
VDD_SYS	Supply voltage for on-board regulators, LVD / HVDs, and clock sources				V	
	• Normal mode	1.71		1.98		
	• Fuse Programming	2.25		2.75		
VDD_DCDC	Supply voltage DCDC regulator	1.71		3.6	V	2
VDD_LDO_SYS	Supply voltage for LDO_SYS regulator	1.86		3.6	V	
VDD_LDO_CORE	Supply voltage for LDO_CORE regulator	1.71		3.6	V	

Table continues on the next page...

Table 9. Voltage and current operating requirements...continued

Symbol	Description	Min.	Typ	Max.	Unit	Notes
VDD	Supply Voltage for Port 0, Port 1, Flash, and CMPx	1.71		3.6	V	
VDD_P2	Supply voltage for Port 2	1.14 1.71		1.32 3.6	V	3,4
VDD_P3	Supply voltage for Port 3	1.14 1.71		1.32 3.6	V	3,5,4
VDD_P4	Supply voltage for Port 4	1.71		3.6	V	6,4
VDD_BAT	Supply voltage for VBAT domain	1.71		3.6	V	
VDD_ANA	Supply voltage for analog modules	VDD_P4		VDD_P4	V	7
VSS - VSS_ANA	VSS-to-VSS_ANA differential voltage	-0.1		0.1	V	
VDD_USB	Supply voltage for USB analog	3.0		3.6	V	8
V _{IH}	Input high voltage • 1.71 V ≤ VDD_Px ≤ 3.6 V • 1.14 V ≤ VDD_Px ≤ 1.32 V	0.7 × VDD_Px 0.7 × VDD_Px		— —	V	3
V _{IL}	Input low voltage • 1.71 V ≤ VDD_Px ≤ 3.6 V • 1.14 V ≤ VDD_Px ≤ 1.32 V	— —		0.3 × VDD_Px 0.3 × VDD_Px	V	3
V _{HYS}	Input hysteresis • Slow I/O • Medium I/O • Fast I/O	0.1 × VDD_Px 0.1 × VDD_Px 0.04 × VDD_Px		—	V	
I _{ICIO}	IO pin DC injection current — per pin • V _{IN} < VSS-0.3 V (negative current injection) • V _{IN} > VDD+0.3 V (positive current injection)	-3 —		— +3	mA	9
I _{ICont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	-25		—	mA	

Table continues on the next page...

Table 9. Voltage and current operating requirements...continued

Symbol	Description	Min.	Typ	Max.	Unit	Notes
	• Positive current injection	—		+25		
V _{ODPU}	Open drain pullup voltage level	VDD_Px		VDD_Px	V	10

- To avoid triggering the glitch detect modules on this device, it is important that the VDD_CORE voltage matches the configuration of the GDET modules. See the GDET chapter in the Security Reference Manual for details.
- If DCDC is unused, then input supply should be tied to GND through a 10 kΩ resistor.
- Operation at 1.2 V is allowed on Port P2/P3 pins only with the following restrictions:
 - VDD_CORE must be less than or equal to the VDD_Px voltage
 - VDD_SYS must be powered on before VDD_Px is powered and VDD_SYS must not be powered off before powering off VDD_Px.
- If this voltage rail is not tied to VDD, it must ramp after VDD_SYS
- If none of the Port 3 pins are being used, then the VDD_P3 can be left floating.
- VDD_P4 should be powered up with VDD_ANA and to the same voltage level as VDD_ANA
- VDD_ANA may deviate from VDD_P4 by ± 0.1 V provided it is still within range of 1.71 V - 3.6 V
- USB HS is not supported when VDD_CORE < 1.1 V
- All I/O pins are internally clamped to VSS and VDD_Px through an ESD protection diode. If VIN is greater than VDD_Px_MIN(=VSS-0.3 V) or is less than VDD_Px_MAX(=VDD_Px + 0.3 V), then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (-0.3 - VIN)/(-I_{ICIOmin})$. The positive injection current limiting resistor is calculated as $R = (VIN - VDD_Px_MAX)/I_{ICIOmax}$. The actual resistor should be an order of magnitude higher to tolerate transient voltages.
- Open drain outputs must be pulled to whichever supply voltage corresponds to that IO, VDD_Px as appropriate.

3.2.2 HVD, LVD, and POR operating requirements

The device includes low-voltage detection (LVD) and high-voltage detection (HVD) power supervisor circuits for following power supplies:

- VDD
- VDD_CORE
- VDD_SYS

For VDD_SYS, it has Power-on-reset (POR) power supervisor circuits.

Table 10. VDD supply HVD, LVD, and POR Operating Requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{HVDH_VDD}	VDD Rising high-voltage detect threshold (HVD assertion)	3.730	3.810	3.890	V	
V _{HVDH_HYS_VDD}	VDD High-voltage inhibit reset/recover hysteresis	—	38	—	mV	
V _{LVDH_VDD}	VDD Falling low-voltage detect threshold (LVD assertion) - high range (VD_IO_CFG[LVSEL] = 0b)	2.567	2.619	2.673	V	
V _{LVDH_HYS_VDD}	VDD Low-voltage inhibit reset/recover hysteresis - high range	—	27	—	mV	
V _{LVDL_VDD}	VDD Falling low-voltage detect threshold (LVD assertion) - low range (VD_IO_CFG[LVSEL] = 1b)	1.618	1.651	1.684	V	

Table continues on the next page...

Table 10. VDD supply HVD, LVD, and POR Operating Requirements...continued

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{LVDV_HYS_VDD}	VDD Low-voltage inhibit reset/recover hysteresis - low range	—	16	—	mV	

Table 11. VDD_CORE supply HVD and LVD Operating Requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{HVD_CORE}	VDD_CORE Rising high-voltage detect threshold (HVD assertion) Target VDD_CORE = 1.0 V Target VDD_CORE = 1.1 V Target VDD_CORE = 1.2 V	1.260	1.285	1.311	V	1
V _{HVD_HYS_CORE}	VDD_CORE High-voltage inhibit reset/recover hysteresis Target VDD_CORE = 1.0 V Target VDD_CORE = 1.1 V Target VDD_CORE = 1.2 V	—	13	—	mV	1
V _{LVD_CORE}	VDD_CORE Falling low-voltage detect threshold (LVD assertion) Target VDD_CORE = 1.0 V Target VDD_CORE = 1.1 V Target VDD_CORE = 1.2 V	0.899 0.989 1.078	0.917 1.009 1.1	0.936 1.029 1.123	V	
V _{LVD_HYS_CORE}	VDD_CORE Low-voltage inhibit reset/recover hysteresis Target VDD_CORE = 1.0 V Target VDD_CORE = 1.1 V Target VDD_CORE = 1.2 V	— — —	9 10 11	— — —	mV	

1. Same value applies to all conditions.

Table 12. VDD_SYS supply HVD and LVD Operating Requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{HVD_SYS}	VDD_SYS Rising high-voltage detect threshold (HVD assertion) Target VDD_SYS = 1.8 V	2.035	2.077	2.120	V	1
V _{HVD_HYS_SYS}	VDD_SYS High-voltage inhibit reset/recover hysteresis	—	20	—	mV	
V _{POR_SYS}	Falling VDD_SYS POR detect voltage (POR assertion)	0.8	1.0	1.5	V	

Table continues on the next page...

Table 12. VDD_SYS supply HVD and LVD Operating Requirements...continued

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVD_SYS}	VDD_SYS Falling low-voltage detect threshold (LVD assertion) Target VDD_SYS = 1.8 V	1.616	1.649	1.683	V	
$V_{LVD_HYS_SYS}$	VDD_SYS Low-voltage inhibit reset/recover hysteresis	—	17	—	mV	

1. When fuses are being programmed VDD_SYS is raised to 2.5V nominal. This is outside the HVD bounds, so HVD detection for VDD_SYS must be disabled when programming fuses

Table 13. VBAT supply POR Operating Requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VBAT_POR_SYS	Falling VBAT POR detect voltage (POR assertion)	0.689	—	1.36	V	1

1. Guaranteed by design. Not tested in production.

3.2.3 Voltage and current operating behaviors

Table 14. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive strength $2.7\text{ V} \leq VDD_Px \leq 3.6\text{ V}$, $I_{OH} = 4\text{ mA}$ $1.71\text{ V} \leq VDD_Px < 2.7\text{ V}$, $I_{OH} = 2.5\text{ mA}$ $1.14\text{ V} \leq VDD_Px < 1.32\text{ V}$, $I_{OH} = 0.5\text{ mA}$	$VDD_Px - 0.5$ $VDD_Px - 0.5$ $VDD_Px - 0.5$	— — —	— — —	V V V	1
V_{OH}	Output high voltage — High drive strength $2.7\text{ V} \leq VDD_Px \leq 3.6\text{ V}$, $I_{OH} = 6\text{ mA}$ $1.71\text{ V} \leq VDD_Px < 2.7\text{ V}$, $I_{OH} = 3.75\text{ mA}$ $1.14\text{ V} \leq VDD_Px < 1.32\text{ V}$, $I_{OH} = 0.75\text{ mA}$	$VDD_Px - 0.5$ $VDD_Px - 0.5$ $VDD_Px - 0.5$	— — —	— — —	V V V	2,1
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — Normal drive strength $2.7\text{ V} \leq VDD_Px \leq 3.6\text{ V}$, $I_{OL} = 4\text{ mA}$ $1.71\text{ V} \leq VDD_Px < 2.7\text{ V}$, $I_{OL} = 2.5\text{ mA}$ $1.14\text{ V} \leq VDD_Px < 1.32\text{ V}$, $I_{OL} = 0.5\text{ mA}$	— — —	— — —	0.5 0.5 0.5	V V V	3,1
V_{OL}	Output low voltage — High drive strength $2.7\text{ V} \leq VDD_Px \leq 3.6\text{ V}$, $I_{OL} = 6\text{ mA}$ $1.71\text{ V} \leq VDD_Px < 2.7\text{ V}$, $I_{OL} = 3.75\text{ mA}$	— —	— —	0.5 0.5	V V	1,3

Table continues on the next page...

Table 14. Voltage and current operating behaviors...continued

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• $1.14\text{ V} \leq \text{VDD_Px} < 1.32\text{ V}$, $I_{OH} = 0.75\text{ mA}$	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	—	1	μA	4
I_{IN}	Input leakage current (per pin) at 25 °C	—	—	0.025	μA	4
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	—	1	μA	
R_{PU}	Internal pullup resistors	33	50	75	k Ω	
R_{PU} (I3C)	Internal pullup resistors	1.11	1.2	2.83	k Ω	5
R_{PD}	Internal pulldown resistors	33	50	75	k Ω	
R_{HPU}	High-resistance pullup option (PCR _x [PV] = 1)	0.67	1.0	1.5	M Ω	6
R_{HPD}	High-resistance pulldown option (PCR _x [PV] = 1)	0.67	1.0	1.5	M Ω	6
V_{BG}	Bandgap voltage reference voltage	0.98	1.0	1.02	V	

1. The 1.14 V – 1.32 V range only applies to port P2 / P3 pins.
2. AON and RESET_B pins are always configured in high drive mode
3. Open drain outputs must be pulled to VDD_Px.
4. Measured at VDD_Px = 3.6 V.
5. Only pins with +I3C add-on support this option
6. Only AON pins and RESET_B pin support this option.

3.2.4 On-chip regulator electrical specifications

3.2.4.1 DCDC converter specifications

Table 15. DCDC Converter Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD_DCDC}	DCDC input voltage	1.71	—	3.6	V	1
V_{DCDC_LX}	DCDC output voltage 1.2 V range	0.85	—	1.21	V	1, 2
I_{LOAD}	DCDC load current					3
	• Normal drive strength	—	—	105	mA	
	• FREQ_CNTRL_ON=1	—	—	45	mA	
	• Low drive strength	—	—	15	mA	
LX	DCDC inductor value	0.47	1	2.2	μH	4
ESR	External inductor equivalent series resistance	—	110	—	m Ω	5
C_{OUT}	DCDC capacitance value	6	22	30	μF	6
V_{RIPPLE}	DCDC voltage ripple	—	1	—	%	

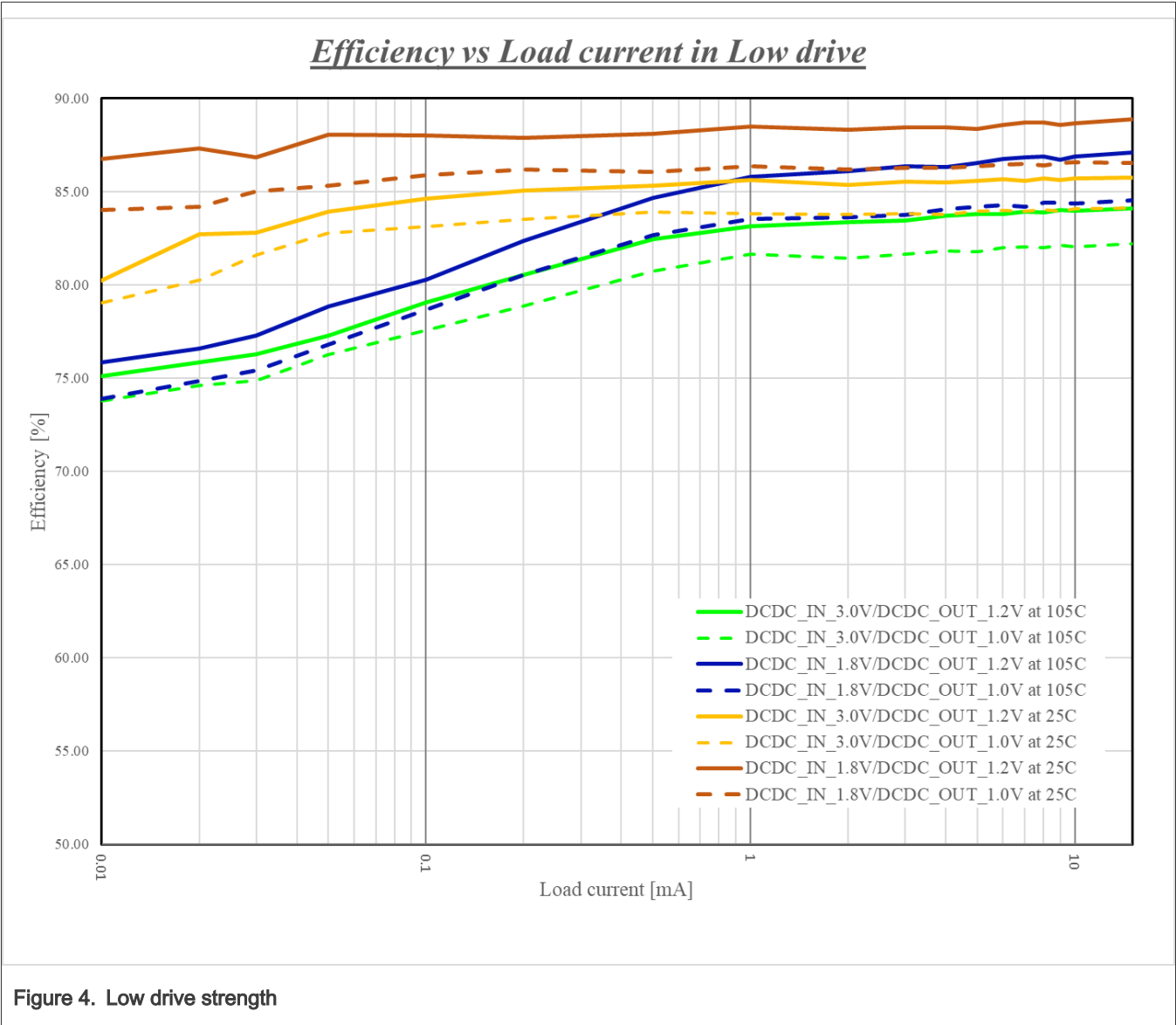
Table continues on the next page...

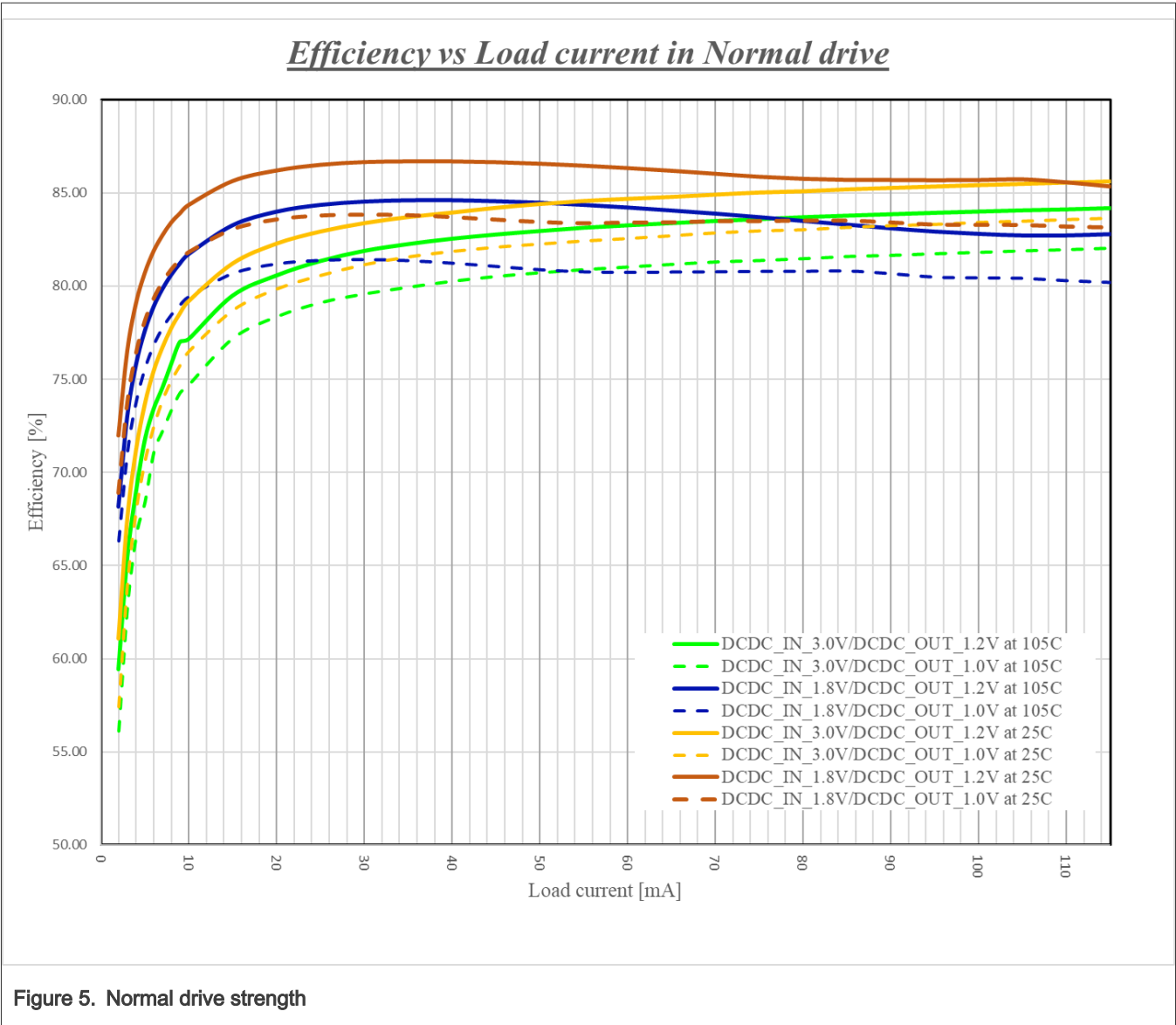
Table 15. DCDC Converter Specifications...continued

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	- In normal drive strength - In low drive strength	—	25	—	mV	
T_startup	DCDC startup time	—	100	—	μs	
f_burst	DCDC switching frequency	3	5	8	MHz	7
f_burst_acc	DCDC burst frequency accuracy	—	10	—	%	8

1. The VDD_DCDC input supply to the system DCDC must be at least 500 mV higher than the desired output at DCDC_LX to achieve the stated efficiency. VDD_DCDC can be as low as 300 mV above the desired output voltage but the efficiency will be reduced.
2. The system DCDC converter generates 1.2 V at DCDC_LX by default. The DCDC is used to power VDD_CORE.
3. The maximum load current during boot up shall not exceed 60 mA.
4. Recommended inductor value is 1 μH to 1.5 μH. If the inductor is < 1 μH, the DCDC efficiency is not guaranteed.
5. The maximum recommended ESR is 250 mΩ (not a hard limit).
6. The variation in capacitance of the capacitor at DCDC_LX due to aging, temperature, and voltage degradation must not exceed the Min./Max. values.
7. FREQ_CNTRL_ON = 1. This range is for 1 μH inductor.
8. FREQ_CNTRL_ON = 1.

3.2.4.2 DCDC efficiency plots





3.2.4.3 LDO_SYS electrical specifications

Table 16. LDO_SYS electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_LDO_SYS	LDO_SYS input supply voltage		—		V	1,2
	• Normal Drive mode	1.95		3.6		
	• Passthrough mode	1.86		1.98		
VOUT_SYS	LDO_SYS regulator output voltage				V	3,4,2
	Normal drive strength mode	2.25	2.5	2.75		
	Fuse programming mode					

Table continues on the next page...

Table 16. LDO_SYS electrical specifications...continued

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
LDO_SYS_DROPOUT	LDO_SYS dropout voltage				mV	1, 2
	• Normal drive strength mode	—	—	150		
	• Fuse programming mode ⁵	—	—	500		
	• Pass through mode ⁶	—	—	60		
I _{LOAD}	LDO_SYS maximum load current					
	• Normal drive strength mode	—	—	50		
	• Low drive strength mode	—	—	2		
	• Fuse programming mode	—	—	40	mA	
I _{DD}	LDO_SYS power consumption					7
	• Normal drive strength mode	—	100	—	μA	
	• Low drive strength mode	—	70	—	nA	
C _{OUT}	External output capacitor	1.4	2.2	4.0	μF	
ESR	External output capacitor equivalent series resistance	—	30	—	mΩ	
I _{INRUSH}	LDO_SYS inrush current	—	—	100 ⁸	mA	

1. Regulator will automatically switch to passthrough mode with the supply is below 1.95 V.
2. VDD_LDO_SYS must be at least 150 mV higher than the desired VOUT_SYS.
3. The LDO_SYS converter generates 1.8 V by default at VOUT_SYS. VOUT_SYS can be used to power VDD_SYS, VDD_Px, VDD_ANA, and external components as long as the max I_{LOAD} is not exceeded.
4. VOUT_SYS and VDD_SYS are connected together within the package
5. Maximum current load in fuse programming mode is 40 mA
6. Maximum current load during pass through mode = 50 mA
7. In normal mode, LDO_SYS draws ~100 μA for every 20 mA of load current.
8. This value is for a 1.5 μF external output capacitor. This value would increase with higher load capacitor.

3.2.4.4 LDO_CORE electrical specifications

Table 17. LDO_CORE electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_LDO_CORE	LDO_CORE input supply voltage	1.71	—	3.6	V	1
VOUT_CORE	LDO_CORE regulator output voltage				V	2
	• Normal drive strength					
	— Mid drive	0.95	1	1.05		
	— Normal drive	1.045	1.1	1.155		
	— Over drive	1.14	1.2	1.26		
	• Low drive strength					

Table continues on the next page...

Table 17. LDO_CORE electrical specifications...continued

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	— Mid drive	0.95	1	1.05		
	— Normal drive	1.045	1.1	1.155		
I_{LOAD}	LDO_CORE max load current - Normal drive strength $T_j = -40\text{ }^{\circ}\text{C}$ $T_j = 27\text{ }^{\circ}\text{C}$ $T_j = 125\text{ }^{\circ}\text{C}$ - Low drive strength $-40\text{ }^{\circ}\text{C} < T_j < 125\text{ }^{\circ}\text{C}$					
		—	—	90		
		—	—	100		
		—	—	115		
		—	—	28	mA	
I_{INRUSH}	LDO_CORE inrush current	—	—	500	mA	3

1. To bypass LDO_CORE, tie VDD_LDO_CORE to VDD_CORE
2. VOUT_CORE and VDD_CORE are connected together in package
3. This value is for 4.7 μF external output capacitor. This value would increase with higher load capacitor

Table 18. LDO_CORE external device electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
C_{OUT}	External output capacitor	3.7	4.7	10	μF	
C_{DEC}	External output decoupling capacitor	—	0.1	—	μF	
ESR	External output capacitor equivalent series resistance	—	10	—	m Ω	

3.2.5 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration:

- CPU clock = 48 MHz
- AHB clock = 48 MHz
- Clock source = Fast internal reference clock (FIRC)

All specifications in the following table were measured from the initiation of an external pin event to the execution code (unless otherwise stated).

All specifications in the following table assume this SPC configuration:

- SPC->LPWKUP_DELAY[LPWKUP_DELAY] = 0x00 and the Core voltage level is configured for the same level in active and low power mode (SPC->ACTIVE_CFG[DCDC_VDD_LVL] = SPC->ACTIVE_CFG[CORELDO_VDD_LVL] = SPC->LP_CFG[DCDC_VDD_LVL] = SPC->LP_CFG[CORELDO_VDD_LVL]).

Table 19. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time to execution of the first instruction (measured from the point	—	6.8	6.9	ms	1, 2, 3, 4

Table continues on the next page...

Table 19. Power mode transition operating behaviors...continued

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	where VDD and VDD_SYS reach 1.8V) across the operating temperature range of the chip.					
t _{SLEEP}	SLEEP → ACTIVE	—	0.22	0.25	μs	3, 4, 5
t _{DSLEEP}	DEEP SLEEP → ACTIVE	—	8.7	9.8	μs	3, 4, 5
t _{PWDN}	POWER DOWN → ACTIVE	—	9.8	11.1	μs	3, 4, 5
t _{DPWDN}	Deep Power DOWN → ACTIVE	—	5.6	5.8	ms	1, 2, 3, 4, 5

1. Boot configuration 144 MHz
2. Measured using ROM version v4.0
3. Based on characterization of typical units. Not tested in production
4. Max value is mean + 3 sigma of tested values at the worst case of ambient temperature range and VDD 1.71 V to 3.6 V. Max values are based on characterization but not covered by test limits in production
5. WFE used for low-power mode entry

3.2.6 Power consumption operating behaviors

The MCXN23x device has multiple power supplies that can be connected in different configurations, where the total current consumption of the device is the accumulative result of each individual power supply's current consumption. The Core domain is provided by the noted source (either DCDC or LDO), the voltage for the System domain is provided by the LDO_SYS (except for LDO @ 1.8V), voltage for the I/O rails is provided by the same external source powering the Core domain regulator and System domain regulator, and the VBAT domain is also provided by the same external source.

When calculating the total MCU current consumption the following considerations should be made:

- Specifications below only include power for the MCU itself
- VDD_USB current draw are not included
- On top of the device's IDD current consumption, external loads applied to pins of the device need to be considered
- Efficiency of regulators (on-chip or off-chip) used to generate supply voltages should be considered

3.2.6.1 Power Consumption Operating Behaviors

NOTE

The data for 125C is just a reference without considering Tj

Appendix A : Active IDD

Table 20. DCDC @ 3.3 V

Flash, LPCAC cases					
Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units
IDD_ACT_OD_1	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	7.43	10.35	mA
		105	10.56	24.53	
		125	13.12	34.08	

Table continues on the next page...

Table 20. DCDC @ 3.3 V...continued

Flash, LPCAC cases					
Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units
IDD_ACT_SD_1	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	4.99	7.91	mA
		105	7.35	13.65	
		125	9.33	18.77	
IDD_ACT_MD_1	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	2.30	5.22	mA
		105	4.04	10.34	
		125	5.54	14.99	
IDD_ACT_LP_1	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	0.58	3.50	mA
		105	2.33	8.63	
		125	3.83	13.28	
IDD_CM_OD_1	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	8.93	11.85	mA
		105	12.24	26.21	
		125	14.85	35.81	
IDD_CM_SD_1	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	5.76	8.67	mA
		105	8.24	14.53	
		125	10.22	19.67	
IDD_CM_MD_1	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	2.63	5.55	mA
		105	4.38	10.68	
		125	5.89	15.34	
IDD_CM_LP_1	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	0.67	3.58	mA
		105	2.42	8.72	
		125	3.92	13.37	
IDD_ACT_OD_2	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks enabled	25	19.00	21.92	mA
		105	22.57	36.54	
		125	25.28	46.24	
IDD_ACT_SD_2	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks enabled	25	11.47	14.39	mA
		105	14.05	28.02	
		125	16.10	37.06	
IDD_ACT_MD_2	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks enabled	25	4.89	7.81	mA
		105	6.71	13.01	
		125	8.23	17.68	

Table continues on the next page...

Table 20. DCDC @ 3.3 V...continued

Flash, LPCAC cases					
Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units
IDD_ACT_LP_2	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the SIRC at 12 MHz; All peripheral clocks enabled	25	1.24	4.16	mA
		105	3.01	9.30	
		125	4.50	13.95	
IDD_CM_OD_2	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks enabled	25	20.51	23.43	mA
		105	24.26	38.23	
		125	27.02	47.98	
IDD_CM_SD_2	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks enabled	25	12.28	15.20	mA
		105	14.90	28.87	
		125	16.94	37.90	
IDD_CM_MD_2	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks enabled	25	5.23	8.15	mA
		105	7.05	13.35	
		125	8.57	18.02	
IDD_CM_LP_2	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the SIRC at 12 MHz; All peripheral clocks enabled	25	1.32	4.24	mA
		105	3.10	9.40	
		125	4.59	14.04	

1. Based on characterization of typical units. Not tested in production

2. Based on characterization of typical numbers + 3 sigma. Not tested in production

Table 21. LDO @ 1.8 V

Flash, LPCAC cases					
Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units
IDD_ACT_OD_1	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	15.19	18.19	mA
		105	21.44	45.35	
		125	26.23	61.12	
IDD_ACT_SD_1	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	10.10	12.13	mA
		105	15.23	34.82	
		125	19.23	47.74	
IDD_ACT_MD_1	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	4.64	6.38	mA
		105	8.75	21.90	
		125	12.03	31.76	

Table continues on the next page...

Table 21. LDO @ 1.8 V...continued

Flash, LPCAC cases					
Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units
IDD_ACT_LP_1	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	1.36	3.09	mA
		105	5.38	18.53	
		125	8.62	28.34	
IDD_CM_OD_1	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	18.59	21.48	mA
		105	25.20	49.47	
		125	30.10	65.49	
IDD_CM_SD_1	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	12.01	14.08	mA
		105	17.39	37.00	
		125	21.35	49.86	
IDD_CM_MD_1	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	5.55	7.05	mA
		105	9.67	25.71	
		125	12.94	36.14	
IDD_CM_LP_1	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	1.57	3.31	mA
		105	5.62	18.77	
		125	8.87	28.59	
IDD_ACT_OD_2	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks enabled	25	41.61	45.21	mA
		105	48.44	73.34	
		125	53.46	89.45	
IDD_ACT_SD_2	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks enabled	25	26.16	28.43	mA
		105	31.58	51.62	
		125	35.69	64.75	
IDD_ACT_MD_2	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks enabled	25	11.60	13.25	mA
		105	15.81	31.99	
		125	19.12	42.47	
IDD_ACT_LP_2	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the SIRC at 12 MHz; All peripheral clocks enabled	25	3.07	4.80	mA
		105	7.14	20.29	
		125	10.39	30.11	
IDD_CM_OD_2	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks enabled	25	45.01	48.50	mA
		105	52.16	77.35	
		125	57.28	93.61	

Table continues on the next page...

Table 21. LDO @ 1.8 V...continued

Flash, LPCAC cases					
Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units
IDD_CM_SD_2	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks enabled	25	28.15	30.41	mA
		105	33.62	53.62	
		125	37.78	66.80	
IDD_CM_MD_2	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks enabled	25	12.50	14.22	mA
		105	16.70	32.95	
		125	20.08	43.37	
IDD_CM_LP_2	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the SIRC at 12 MHz; All peripheral clocks enabled	25	3.29	5.02	mA
		105	7.37	20.52	
		125	10.62	30.35	
RAM w Cache cases					
IDD_ACT_OD_5	While(1) executing on CPU0 from RAM; Cache Enabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	17.95	20.67	mA
		105	23.99	45.12	
		125	28.57	58.72	
IDD_ACT_SD_5	While(1) executing on CPU0 from RAM; Cache Enabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	11.63	13.62	mA
		105	16.48	33.58	
		125	20.26	44.55	
IDD_ACT_MD_5	While(1) executing on CPU0 from RAM; Cache Enabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	5.29	7.02	mA
		105	9.10	22.25	
		125	12.18	31.90	
IDD_ACT_LP_5	While(1) executing on CPU0 from RAM; Cache Enabled; Core voltage at 1.0V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	1.56	3.29	mA
		105	5.29	18.44	
		125	8.32	28.05	

1. Based on characterization of typical units. Not tested in production

2. Based on characterization of typical numbers + 3 sigma. Not tested in production

Table 22. LDO @ 3.3 V

Flash, LPCAC cases					
Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units
IDD_ACT_OD_1	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	15.30	18.29	mA
		105	22.06	46.11	

Table continues on the next page...

Table 22. LDO @ 3.3 V...continued

Flash, LPCAC cases					
Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units
		125	27.56	60.47	
IDD_ACT_SD_1	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	10.22	12.31	mA
		105	15.74	35.10	
		125	20.30	46.70	
IDD_ACT_MD_1	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	4.75	6.49	mA
		105	9.15	22.30	
		125	12.87	32.59	
IDD_ACT_LP_1	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	1.37	3.10	mA
		105	5.66	18.81	
		125	9.31	29.04	
IDD_CM_OD_1	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	18.73	21.65	mA
		105	25.89	50.31	
		125	31.50	65.08	
IDD_CM_SD_1	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	12.13	14.20	mA
		105	17.83	37.15	
		125	22.48	48.88	
IDD_CM_MD_1	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	5.66	7.39	mA
		105	10.05	23.20	
		125	13.79	33.52	
IDD_CM_LP_1	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	1.58	3.32	mA
		105	5.90	19.05	
		125	9.55	29.28	
IDD_ACT_OD_2	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks enabled	25	41.77	45.45	mA
		105	49.33	75.07	
		125	55.16	90.32	
IDD_ACT_SD_2	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks enabled	25	26.29	28.59	mA
		105	32.24	52.39	
		125	36.97	64.43	
IDD_ACT_MD_2	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks enabled	25	11.71	13.45	mA
		105	16.27	29.41	

Table continues on the next page...

Table 22. LDO @ 3.3 V...continued

Flash, LPCAC cases					
Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units
		125	20.02	39.75	
IDD_ACT_LP_2	While(1) executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the SIRC at 12 MHz; All peripheral clocks enabled	25	3.08	4.81	mA
		105	7.44	20.59	
		125	11.10	30.82	
IDD_CM_OD_2	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks enabled	25	45.20	48.81	mA
		105	53.12	79.22	
		125	59.06	94.77	
IDD_CM_SD_2	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks enabled	25	28.30	30.68	mA
		105	34.34	54.59	
		125	39.07	66.62	
IDD_CM_MD_2	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks enabled	25	12.67	14.40	mA
		105	17.15	30.29	
		125	20.94	40.66	
IDD_CM_LP_2	CoreMark executing on CPU0 from Flash; Cache Enabled; Core voltage at 1.0V; Clocked from the SIRC at 12 MHz; All peripheral clocks enabled	25	3.30	5.03	mA
		105	7.68	20.83	
		125	11.33	31.05	
RAM w Cache cases					
IDD_ACT_OD_5	While(1) executing on CPU0 from RAM; Cache Enabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	18.01	21.04	mA
		105	24.62	47.68	
		125	29.63	63.38	
IDD_ACT_SD_5	While(1) executing on CPU0 from RAM; Cache Enabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	11.70	13.81	mA
		105	16.98	35.52	
		125	21.10	48.11	
IDD_ACT_MD_5	While(1) executing on CPU0 from RAM; Cache Enabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	5.37	7.11	mA
		105	9.51	22.66	
		125	12.85	32.58	
IDD_ACT_LP_5	While(1) executing on CPU0 from RAM; Cache Enabled; Core voltage at 1.0V; Clocked from the SIRC at 12 MHz; All peripheral clocks disabled	25	1.55	3.28	mA
		105	5.58	18.73	
		125	8.87	28.59	
Flash w/o LPCAC cases					

Table continues on the next page...

Table 22. LDO @ 3.3 V...continued

Flash, LPCAC cases					
Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units
IDD_CM_OD_6	CoreMark executing on CPU0 from Flash; Cache Disabled; Core voltage at 1.2V; Clocked from PLL0 at 150 MHz; All peripheral clocks disabled	25	20.82	23.87	mA
		105	28.22	52.90	
		125	33.86	67.91	
IDD_CM_SD_6	CoreMark executing on CPU0 from Flash; Cache Disabled; Core voltage at 1.1V; Clocked from PLL0 at 100 MHz; All peripheral clocks disabled	25	13.26	15.47	mA
		105	19.12	38.68	
		125	23.72	50.47	
IDD_CM_MD_6	CoreMark executing on CPU0 from Flash; Cache Disabled; Core voltage at 1.0V; Clocked from the FIRC at 48 MHz; All peripheral clocks disabled	25	6.06	7.79	mA
		105	10.60	23.75	
		125	14.31	34.03	

1. Based on characterization of typical units. Not tested in production

2. Based on characterization of typical numbers + 3 sigma. Not tested in production

Appendix B : Static IDD

Table 23. DCDC @ 3.3V

Flash, LPCAC cases						
Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units	Notes
IDD_SLEEP	Core_Main in Sleep; Core_Wake in Sleep; IVS disabled; All RAM retained; Core voltage at 1.0V; Core clocked at 48MHz by FIRC; All regulators in Normal mode	25	1.48	2.23	mA	
		105	3.22	14.14		
		125	4.67	21.05		
IDD_SLEEP_LP	Core_Main in Sleep; Core_Wake in Sleep; IVS disabled; All RAM retained; Core voltage at 1.0V; Core clocked at 48MHz by FIRC; Core regulator in low power mode, System regulator in Normal mode	25	1.12	1.87	mA	
		105	2.91	13.83		
		125	4.39	20.77		
IDD_DSLEEP_OD	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS disabled; All HVD/LVD enabled; Core voltage at 1.2V; All RAM retained; All regulators in Normal mode	25	0.80	1.74	mA	
		105	3.38	14.30		
		125	5.41	21.78		
IDD_DSLEEP_MD	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS disabled; All HVD/LVD enabled; Core voltage at 1.0V; All RAM retained; All regulators in Normal mode	25	0.66	1.41	mA	
		105	2.13	13.04		
		125	3.34	19.71		

Table continues on the next page...

Table 23. DCDC @ 3.3V...continued

Flash, LPCAC cases						
Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units	Notes
IDD_DSLEEP_IVS	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; Core voltage at 1.0V; All RAM retained; All regulators in Normal mode	25	0.66	1.41	mA	
		105	2.11	13.03		
		125	3.32	19.69		
IDD_DSLEEP_LP	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; All RAM retained; Core voltage at 1.0V; All Regulators in low power mode	25	0.12	0.88	mA	
		105	1.61	12.53		
		125	2.83	19.20		
IDD_PDOWN_64K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 64KB RAM retained; Core voltage at 1.0V; All regulators in low power mode	25	2.01	-	µA	
		105	20.32	-		
		125	42.58	-		
IDD_PDOWN_128K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 128KB RAM retained; Core voltage at 1.0V; All regulators in low power mode	25	2.23	-	µA	
		105	25.09	-		
		125	51.45	-		
IDD_PDOWN_OD	Core_Main in Power Down; Core_Wake in Power Down; IVS disabled; All HVD/LVD enabled; Core voltage at 1.2V; No RAM retained; All regulators in Normal mode	25	546.72	-	µA	
		105	570.68	-		
		125	594.70	-		
IDD_PDOWN_MD	Core_Main in Power Down; Core_Wake in Power Down; IVS disabled; All HVD/LVD enabled; Core voltage at 1.0V; No RAM retained; All regulators in Normal mode	25	541.89	-	µA	
		105	562.40	-		
		125	581.88	-		
IDD_PDOWN_IVS	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD enabled; Core voltage at 1.0V; No RAM retained; All regulators in Normal mode	25	541.81	-	µA	
		105	557.82	-		
		125	576.44	-		
IDD_PDOWN_WK_DS	Core_Main in Power Down; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; No RAM retained; Core voltage at 1.0V; All regulators in low power mode	25	21.27	-	µA	
		105	155.62	-		
		125	246.66	-		
IDD_PDOWN_RET_0V7	Core_Main in Power Down; Core_Wake in Power Down; IVS disabled; All HVD/LVD disabled; Core voltage at 0.7V; All RAM retained; All regulators in low power mode	25	2.52	-	µA	
		105	34.16	-		
		125	72.71	-		
IDD_DPDOWN_0	Core_Main in Deep Power Down; Core_Wake in Deep Power Down; IVS powered down; All HVD/LVD disabled; No RAM retained; DCDC output disabled; Core regulator in low power mode, System regulator in Normal mode	25	120.43	-	µA	
		105	130.97	-		
		125	140.61	-		

Table continues on the next page...

Table 23. DCDC @ 3.3V...continued

Flash, LPCAC cases						
Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units	Notes
IDD_DPDOWN_LP	Core_Main in Deep Power Down; Core_Wake in Deep Power Down; IVS powered down; All HVD/LVD disabled; No RAM retained; DCDC output disabled; All regulators in low power mode	25	0.81	-	µA	
		105	8.28	-		
		125	17.44	-		
IDD_DPDOWN_OSC32K	Core_Main in Deep Power Down; Core_Wake in Deep Power Down; IVS powered down; All HVD/LVD disabled; No RAM retained; DCDC output disabled; All regulators in low power mode; OSC32K enabled	25	1.13	-	µA	
		105	8.56	-		
		125	17.76	-		
IDD_DPDOWN_FRO16K	Core_Main in Deep Power Down; Core_Wake in Deep Power Down; IVS powered down; All HVD/LVD disabled; No RAM retained; All regulators in low power mode; FRO16K enabled	25	0.87	-	µA	
		105	8.36	-		
		125	17.50	-		
IDD_DPDOWN_32K	Core_Main in Deep Power Down; Core_Wake in Deep Power Down; IVS powered down; All HVD/LVD disabled; No RAM retained; All regulators in low power mode; 32KB VBAT SRAM retained	25	1.28	-	µA	
		105	15.10	-		
		125	31.66	-		
IDD_VBAT_0	VBAT mode; DCDC output disabled	25	0.21	-	µA	3
		105	2.25	-		
		125	4.66	-		
IDD_VBAT_32K	VBAT mode; DCDC output disabled; 32KB VBAT SRAM retained	25	0.70	-	µA	3
		105	9.08	-		
		125	16.13	-		
IDD_VBAT_8K	VBAT mode; DCDC output disabled; 8KB VBAT SRAM retained	25	0.44	-	µA	3
		105	4.13	-		
		125	8.47	-		
IDD_VBAT_OSC32K	VBAT mode; DCDC output disabled; RTC enabled and clocked from OSC32K	25	1.04	-	µA	3
		105	3.02	-		
		125	5.48	-		
IDD_VBAT_FRO16K	VBAT mode; DCDC output disabled; RTC enabled and clocked from FRO16K	25	0.51	-	µA	3
		105	2.56	-		
		125	4.96	-		

1. Based on characterization of typical units. Not tested in production

2. Based on characterization of typical numbers + 3 sigma. Not tested in production

3. Power measurements for IDD_VBATx symbols are attained after turning off external power supplies to all domains, except VDD_BAT

Table 24. LDO @ 1.8V

Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units	Notes
IDD_SLEEP	Core_Main in Sleep; Core_Wake in Sleep; IVS disabled; All RAM retained; Core voltage at 1.0V; Core clocked at 48MHz by FIRC; All regulators in Normal mode	25	2.59	3.89	mA	
		105	6.73	21.95		
		125	9.99	32.25		
IDD_SLEEP_LP	Core_Main in Sleep; Core_Wake in Sleep; IVS disabled; All RAM retained; Core voltage at 1.0V; Core clocked at 48MHz by FIRC; Core regulator in low power mode, System regulator in Normal mode	25	2.45	3.69	mA	
		105	6.56	20.65		
		125	9.80	30.71		
IDD_DSLEEP_O D	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS disabled; All HVD/LVD enabled; Core voltage at 1.2V; All RAM retained; All regulators in Normal mode	25	0.77	2.83	mA	
		105	6.15	26.62		
		125	10.12	39.91		
IDD_DSLEEP_M D	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS disabled; All HVD/LVD enabled; Core voltage at 1.0V; All RAM retained; All regulators in Normal mode	25	0.49	1.57	mA	
		105	4.01	16.44		
		125	6.74	25.11		
IDD_DSLEEP_IV S	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; Core voltage at 1.0V; All RAM retained; All regulators in Normal mode	25	0.49	1.56	mA	
		105	3.98	16.38		
		125	6.69	25.00		
IDD_DSLEEP_LP	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; All RAM retained; Core voltage at 1.0V; All Regulators in low power mode	25	0.30	1.35	mA	
		105	3.74	15.91		
		125	6.42	24.35		
IDD_PDOWN_LP	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; No RAM retained; Core voltage at 1.0V; All regulators in low power mode	25	2.64	-	µA	
		105	23.18	-		
		125	46.93	-		
IDD_PDOWN_W K_DS	Core_Main in Power Down; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; No RAM retained; Core voltage at 1.0V; All regulators in low power mode	25	49.52	-	µA	
		105	347.91	-		
		125	536.02	-		
IDD_PDOWN_32 K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 32KB RAM retained; Core voltage at 1.0V; All regulators in low power mode	25	2.90	-	µA	
		105	28.86	-		
		125	58.55	-		
IDD_PDOWN_64 K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 64KB RAM retained; Core voltage at 1.0V; All regulators in low power mode	25	3.16	-	µA	
		105	33.67	-		
		125	68.57	-		

Table continues on the next page...

Table 24. LDO @ 1.8V...continued

Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units	Notes
IDD_PDOWN_128K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 128KB RAM retained; Core voltage at 1.0V; All regulators in low power mode	25	3.71	-	µA	
		105	43.58	-		
		125	89.12	-		
IDD_PDOWN_OD	Core_Main in Power Down; Core_Wake in Power Down; IVS disabled; All HVD/LVD enabled; Core voltage at 1.2V; No RAM retained; All regulators in Normal mode	25	197.65	-	µA	
		105	244.88	-		
		125	282.08	-		
IDD_PDOWN_MD	Core_Main in Power Down; Core_Wake in Power Down; IVS disabled; All HVD/LVD enabled; Core voltage at 1.0V; No RAM retained; All regulators in Normal mode	25	188.24	-	µA	
		105	228.31	-		
		125	260.26	-		
IDD_PDOWN_IVS	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD enabled; Core voltage at 1.0V; No RAM retained; All regulators in Normal mode	25	184.34	-	µA	
		105	218.59	-		
		125	245.66	-		

1. Based on characterization of typical units. Not tested in production

2. Based on characterization of typical numbers + 3 sigma. Not tested in production

Table 25. LDO @ 3.3V

Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units	Notes
IDD_SLEEP	Core_Main in Sleep; Core_Wake in Sleep; IVS disabled; All RAM retained; Core voltage at 1.0V; Core clocked at 48MHz by FIRC; All regulators in Normal mode	25	2.69	3.98	mA	
		105	7.13	21.93		
		125	10.78	31.11		
IDD_SLEEP_LP	Core_Main in Sleep; Core_Wake in Sleep; IVS disabled; All RAM retained; Core voltage at 1.0V; Core clocked at 48MHz by FIRC; Core regulator in low power mode, System regulator in Normal mode	25	2.54	3.77	mA	
		105	6.95	20.64		
		125	10.58	29.60		
IDD_DSLEEP_OD	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS disabled; All HVD/LVD enabled; Core voltage at 1.2V; All RAM retained; All regulators in Normal mode	25	0.87	2.91	mA	
		105	6.62	26.65		
		125	11.04	38.67		
IDD_DSLEEP_MD	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS disabled; All HVD/LVD enabled; Core voltage at 1.0V; All RAM retained; All regulators in Normal mode	25	0.59	1.66	mA	
		105	4.35	16.34		
		125	7.37	23.99		

Table continues on the next page...

Table 25. LDO @ 3.3V...continued

Symbol	Description	Temp, Ta (°C)	Typ ¹	Max ²	Units	Notes
IDD_DSLEEP_IVS	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; No RAM retained;	25	0.58	1.65	mA	
		105	4.31	16.29		
		125	7.31	23.89		
IDD_DSLEEP_LP	Core_Main in Deep Sleep; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; All RAM retained; Core voltage at 1.0V; All Regulators in low power mode	25	0.30	1.35	mA	
		105	3.98	15.74		
		125	6.95	23.16		
IDD_PDOWN_OD	Core_Main in Power Down; Core_Wake in Power Down; IVS disabled; All HVD/LVD enabled; Core voltage at 1.2V; No RAM retained; All regulators in Normal mode	25	293.67	-	µA	
		105	345.66	-		
		125	387.99	-		
IDD_PDOWN_MD	Core_Main in Power Down; Core_Wake in Power Down; IVS disabled; All HVD/LVD enabled; Core voltage at 1.0V; No RAM retained; All regulators in Normal mode	25	283.97	-	µA	
		105	328.80	-		
		125	364.75	-		
IDD_PDOWN_IVS	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD enabled; Core voltage at 1.0V; No RAM retained; All regulators in Normal mode	25	280.45	-	µA	
		105	318.48	-		
		125	349.63	-		
IDD_PDOWN_LP	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; No RAM retained; Core voltage at 1.0V; All regulators in low power mode	25	2.93	-	µA	
		105	26.20	-		
		125	54.08	-		
IDD_PDOWN_WK_DS	Core_Main in Power Down; Core_Wake in Deep Sleep; IVS enabled; All HVD/LVD disabled; No RAM retained; Core voltage at 1.0V; All regulators in low power mode	25	50.05	-	µA	
		105	364.71	-		
		125	571.47	-		
IDD_PDOWN_32K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 32KB RAM retained; Core voltage at 1.0V; All regulators in low power mode	25	3.24	-	µA	
		105	32.23	-		
		125	66.76	-		
IDD_PDOWN_64K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 64KB RAM retained; Core voltage at 1.0V; All regulators in low power mode	25	3.44	-	µA	
		105	37.44	-		
		125	77.80	-		
IDD_PDOWN_128K	Core_Main in Power Down; Core_Wake in Power Down; IVS enabled; All HVD/LVD disabled; 128KB RAM retained; Core voltage at 1.0V; All regulators in low power mode	25	4.02	-	µA	
		105	48.16	-		
		125	100.33	-		

1. Based on characterization of typical units. Not tested in production

2. Based on characterization of typical numbers + 3 sigma. Not tested in production

3.2.7 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

3.2.8 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to <http://www.nxp.com>.
2. Perform a keyword search for “EMC design”.

3.2.9 Capacitance attributes

Table 26. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN_A}	Input capacitance: analog pins	—	7	pF
C _{IN_D}	Input capacitance: digital pins	—	7	pF

3.3 Switching specifications

3.3.1 Device clock specifications

Table 27. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
f _{LPTMR}	LPTMR clock	—	25	MHz	
Overdrive mode					
f _{CPU}	CPU clock (CPU_CLK)	—	150	MHz	¹
f _{AHB}	AHB clock (AHB_CLK)	—	150	MHz	
f _{SLOW}	Slow clock (SLOW_CLK)	—	37.5	MHz	
Standard Drive mode					
f _{CPU}	CPU clock (CPU_CLK)	—	100	MHz	
f _{AHB}	AHB clock (AHB_CLK)	—	100	MHz	
f _{SLOW}	Slow clock (SLOW_CLK)	—	25	MHz	
Mid-Drive mode					
f _{CPU}	CPU clock (CPU_CLK)	—	50	MHz	
f _{AHB}	AHB clock (AHB_CLK)	—	50	MHz	
f _{SLOW}	Slow clock (SLOW_CLK)	—	12.5	MHz	

1. The maximum value of system clock, core clock, AHB clock, and flash clock under normal run mode can be 2 % higher than the specified maximum frequency when FRO144M is used as the clock source.

3.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPUART, LPTMR, CAN, LPI2C, LPI3C, LPSPI, or FlexIO functions.

NOTE

Pad types are specified in the pinout spreadsheet attached to this document.

Table 28. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (passive filter enabled) — Synchronous path	Largest of 1.5 and 150	—	AHB clock cycles ns	^{1, 2}
GPIO pin interrupt pulse width (passive filter disabled)— Synchronous path	1.5	—	AHB clock cycles	^{1, 2}
GPIO pin interrupt pulse width (passive filter enabled) — Asynchronous path	150	—	ns	^{1, 3}
GPIO pin interrupt pulse width (passive filter disabled) — Asynchronous path	50	—	ns	^{1, 3}
AON pins and RESET_B pin interrupt pulse width (passive filter enabled)— Asynchronous path	330	—	ns	^{1, 4}
AON pins and RESET_B pin interrupt pulse width (passive filter disabled)—Asynchronous path	10	—	ns	¹
Port rise/fall time				
Slow I/O pins			ns	⁵
• $2.7 \leq VDD_{Px} \leq 3.6$ V — Fast slew rate (SRE = 0; DSE = 0) — Slow slew rate (SRE = 1; DSE = 0) • $1.71 \leq VDD_{Px} < 2.7$ V — Fast slew rate (SRE = 0; DSE = 1) — Slow slew rate (SRE = 1; DSE = 1)	2.5 4.6	7 15		
Fast I/O pins			ns	^{8,9}
• $2.7 \leq VDD_{Px} \leq 3.6$ V — Fast slew rate (SRE = 0; DSE = 0)⁶ — Slow slew rate (SRE = 1; DSE = 0)⁶ • $1.71 \leq VDD_{Px} < 2.7$ V — Fast slew rate (SRE = 0; DSE = 1)⁶ — Slow slew rate (SRE = 1; DSE = 1)⁶ • $1.14 \leq VDD_{Px} < 1.32$ V — Fast slew rate (SRE = 0; DSE = 1)⁷ — Slow slew rate (SRE = 1; DSE = 1)⁷	0.8 0.9 0.5 0.6 2 2	2 2.5 2 2.5 7 8		
Medium I/O pins				⁵

Table continues on the next page...

Table 28. General switching specifications...continued

Description	Min.	Max.	Unit	Notes
• $2.7 \leq VDD_{Px} \leq 3.6$ V — Fast slew rate (SRE = 0; DSE = 0) — Slow slew rate (SRE = 1; DSE = 0) • $1.71 \leq VDD_{Px} < 2.7$ V — Fast slew rate (SRE = 0; DSE = 1) — Slow slew rate (SRE = 1; DSE = 1)	1.500 2.071	3.322 4.864	ns	
• $2.7 \leq VDD_{Px} \leq 3.6$ V • $1.71 \leq VDD_{Px} < 2.7$ V	3 3.6	8 20	ns	10

1. This is the shortest pulse that is guaranteed to be recognized.
2. Synchronous path is used in active and sleep mode for pin functions other than WUU. Pins configured as WUU use asynchronous path in all power modes.
3. Asynchronous path is used deep sleep, power down, and deep power down modes.
4. The passive filter is always enabled for the RESET_B pin.
5. Load is 25 pF. Drive strength and slew rate are configured using PORTx_PCRn[DSE] and PORTx_PCRn[SRE].
6. 15 pF lumped load.
7. 25 pF lumped load
8. These are Port 3 and Port 2 pins.
9. Uses default configuration for NCAL and PCAL in PORTS.
10. Load is 25 pF.

3.4 Thermal specifications

3.4.1 Thermal operating requirements

Table 29. Thermal operating requirements

Symbol	Description	Min.	Typical	Max.	Unit	Notes
T_A	Ambient temperature	–40	25	125	°C	1
T_J	Die junction temperature maximum	–	–	125	°C	2, 3, 4

1. The device may operate at maximum T_A rating as long as T_J maximum of 125 °C is not exceeded. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.
2. The device operating specification is not guaranteed beyond 125 °C T_J .
3. The maximum operating requirement applies to all chapters unless otherwise specifically stated.
4. Operating at maximum conditions for extended periods may affect device reliability. Refer to Product Lifetime Usage application note (AN14273)

3.4.2 Thermal attributes

Table 30. Thermal attributes

Board type ¹	Symbol	Description	100 HLQFP	184 BGA	172 HDQFP	Unit	Notes
2s2p	$R_{\theta JA}$	Junction to Ambient Thermal resistance,	32.1	48.6	43.4	°C/W	2

Table continues on the next page...

Table 30. Thermal attributes...continued

Board type ¹	Symbol	Description	100 HLQFP	184 BGA	172 HDQFP	Unit	Notes
1s	$R_{\theta JC}$	Thermal resistance, junction to case	12.9	—	23.3	°C/W	³
2s2p	Ψ_{JT}	Junction to top of package Thermal characterization parameter	9.3	9.1	9.9	°C/W	²

1. Thermal test board meets JEDEC specification for respective package (JESD51-7 for the 100 HLQFP and 172 HDQFP; JESD51-9 for the 184 BGA)
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
3. Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers to the package bottom surface temperature in the case of the 100 HLQFP package, and to the mold surface temperature at the center of the top of the package in the case of the HDQFP package.

4 Peripheral operating requirements and behaviors

4.1 Core modules

4.1.1 Debug trace timing specifications

Table 31. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
	Frequency of operation • OD mode • SD mode • MD mode	— — —	48 36 25	MHz
T1	Clock period • OD mode • SD mode • MD mode	20.82 27.78 40	— — —	ns
T2	Low pulse width	2	—	ns
T3	High pulse width	2	—	ns
T4	Clock and data rise time	—	3	ns
T5	Clock and data fall time	—	3	ns
T6	Data setup	1.5	—	ns
T7	Data hold	1.0	—	ns

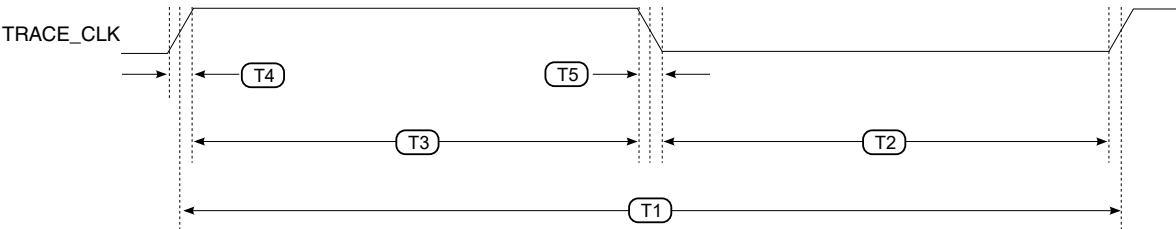


Figure 6. TRACE_CLKOUT specifications

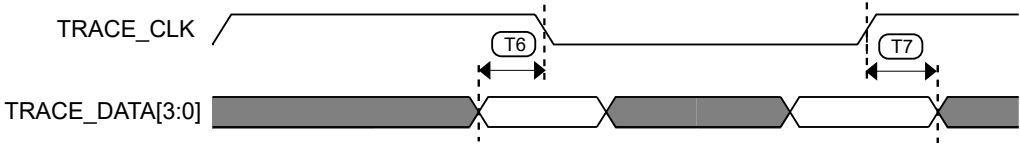


Figure 7. Trace data specifications

4.1.2 JTAG electricals

Table 32. JTAG timing (full voltage range)

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation • Boundary Scan • JTAG-DP/TAP (OD and SD mode) • JTAG-DP/TAP (MD mode)	— — —	10 25 20	MHz MHz MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width • Boundary Scan • JTAG-DP/TAP	50 25	— —	ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2	—	ns
J7	TCLK low to boundary scan output data valid	—	30	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	JTAG-DP/TAP TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	JTAG-DP/TAP TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to JTAG-DP/TAP TDO data valid	—	19	ns
J12	TCLK low to JTAG-DP/TAP TDO high-Z	—	17	ns

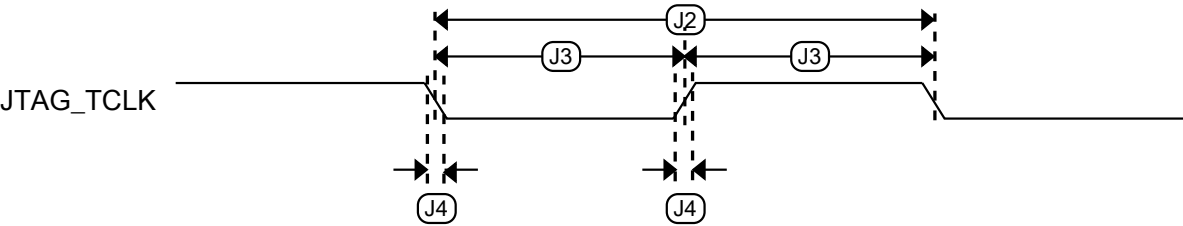


Figure 8. Test clock input timing

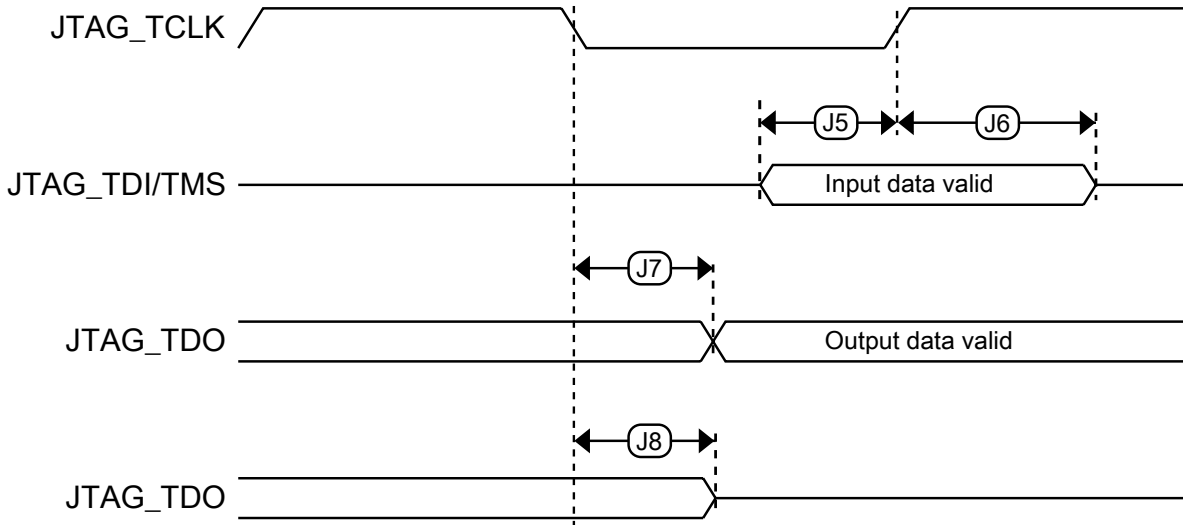


Figure 9. Boundary scan (JTAG) timing

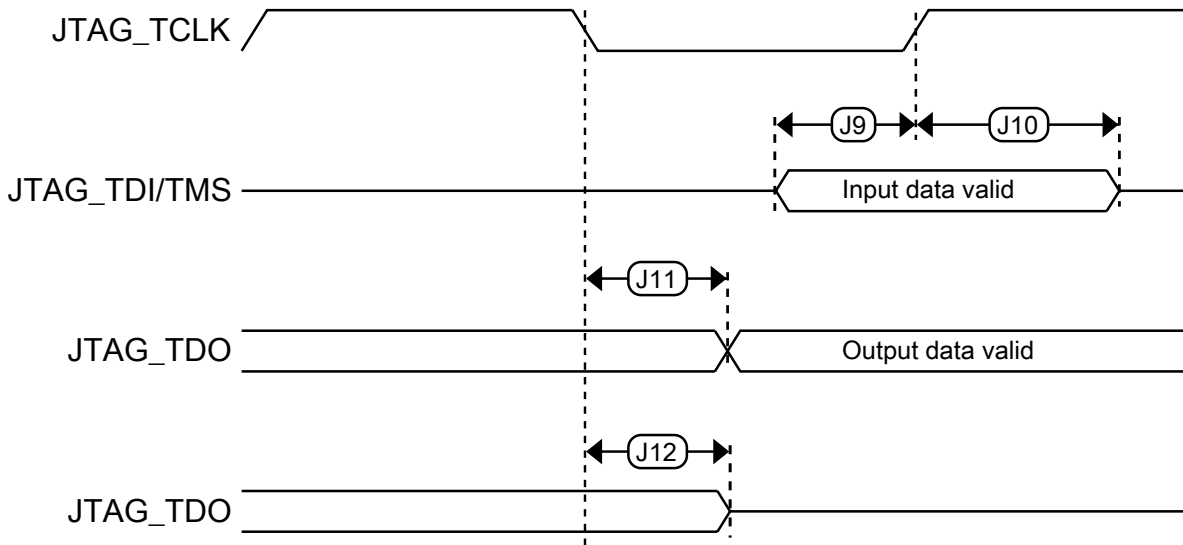


Figure 10. JTAG-DP/TAP timing

4.1.3 SWD electricals

Table 33. SWD timing

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	SWD_CLK frequency of operation	—	25	MHz
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width	20	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S5	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
S6	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
S7	SWD_CLK high to SWD_DIO data valid	—	25	ns
S8	SWD_CLK high to SWD_DIO high-Z	5	—	ns

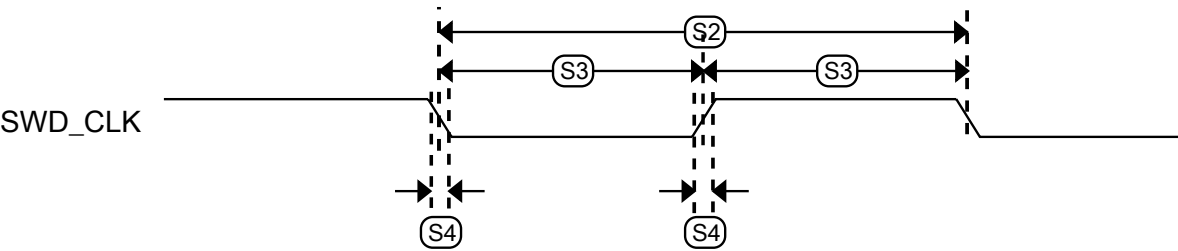


Figure 11. Serial wire clock input timing

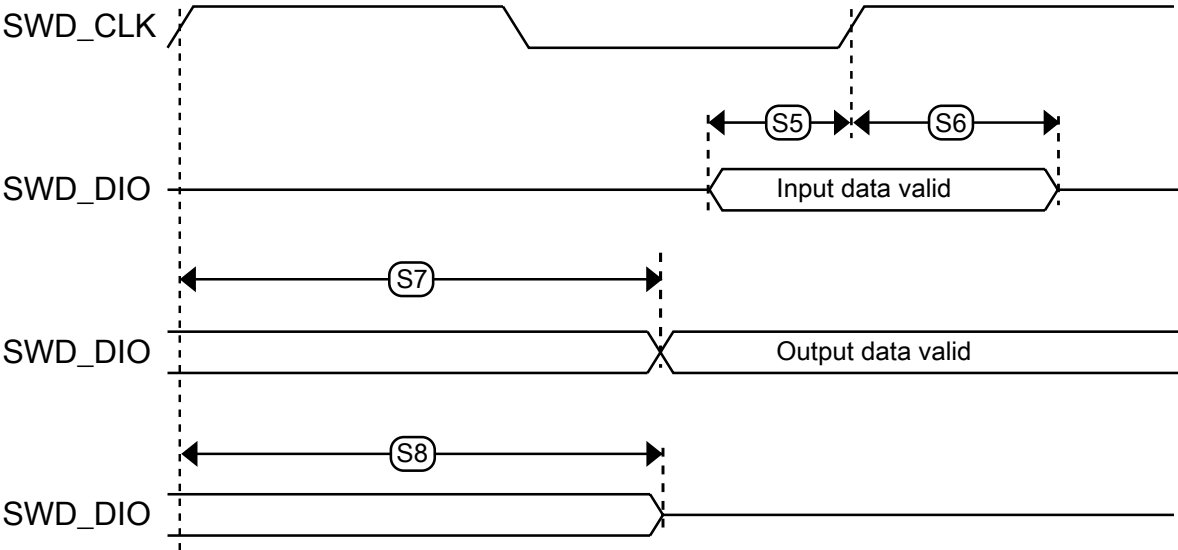


Figure 12. Serial wire data timing

4.2 Clock modules

4.2.1 Reference Oscillator Specification

This chip is designed to meet targeted specifications with a ± 40 ppm frequency error over the life of the part, which includes the temperature, mechanical, and aging excursions.

The table below shows typical specifications for the Crystal Oscillator.

Table 34. System Crystal Oscillator Specification

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{osc}	Crystal Frequency	16	—	50	MHz	
Tol	Frequency tolerance	—	± 10	± 40	ppm	
Jit_{osc}	Jitter Period jitter (RMS)	—	70	—	ps	
V_{pp}	Peak-to-peak amplitude of oscillation	—	0.6	—	V	¹
f_{ec}	Externally provided input clock frequency	0	—	50	MHz	²
t_{DC_EXTAL}	External clock duty cycle	40	50	60	%	
V_{ec}	Externally provided input clock amplitude	Refer to Table 9 for V_{IH} and V_{IL} levels				²

1. When a crystal is being used with the oscillator, the EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.
2. This specification is for an externally supplied clock driven to EXTAL and does not apply to any other clock input.

Table 35. System Oscillator Crystal Specifications. Refer to [Figure 13](#) for additional details of the crystal parameters

Freq Crystal (MHz)	R_m (ohms)	C_p (pF)	C_{load} (pF)	C_m (pF)	L_m (mH)	Typical startup (μs) ¹	Typical Current consumption (μA) ¹	Drive level (μW)	
								min	max
16	80	2.00	8.00	0.008	12.37	215	168.3	16	22
16	200	1.00	8.00	0.008	12.37	186	200.4	31	46
24	80	0.80	8.00	0.008	5.50	61.4	219.2	43	59
25	60	3.00	11.0	0.008	5.07	224	245.6	70	93
25	60	2.00	10.0	0.008	5.07	128	232.5	61	80
25	100	1.00	8.00	0.008	5.07	73.6	232.7	62	82
32	60	3.00	9.00	0.008	3.09	233	269.6	71	95
32	60	2.00	8.00	0.008	3.09	116	253.2	59	80
32	100	1.00	8.00	0.008	3.09	52.4	289.3	91	123
40	50	2.00	8.00	0.008	1.98	80.4	296.9	73	99
40	60	3.00	9.00	0.008	1.98	162	333.2	99	135
48	50	2.00	8.00	0.008	1.37	73.1	359.6	104	140
48	60	3.00	9.00	0.008	1.37	155	407.9	138	188

1. This is based on simulation

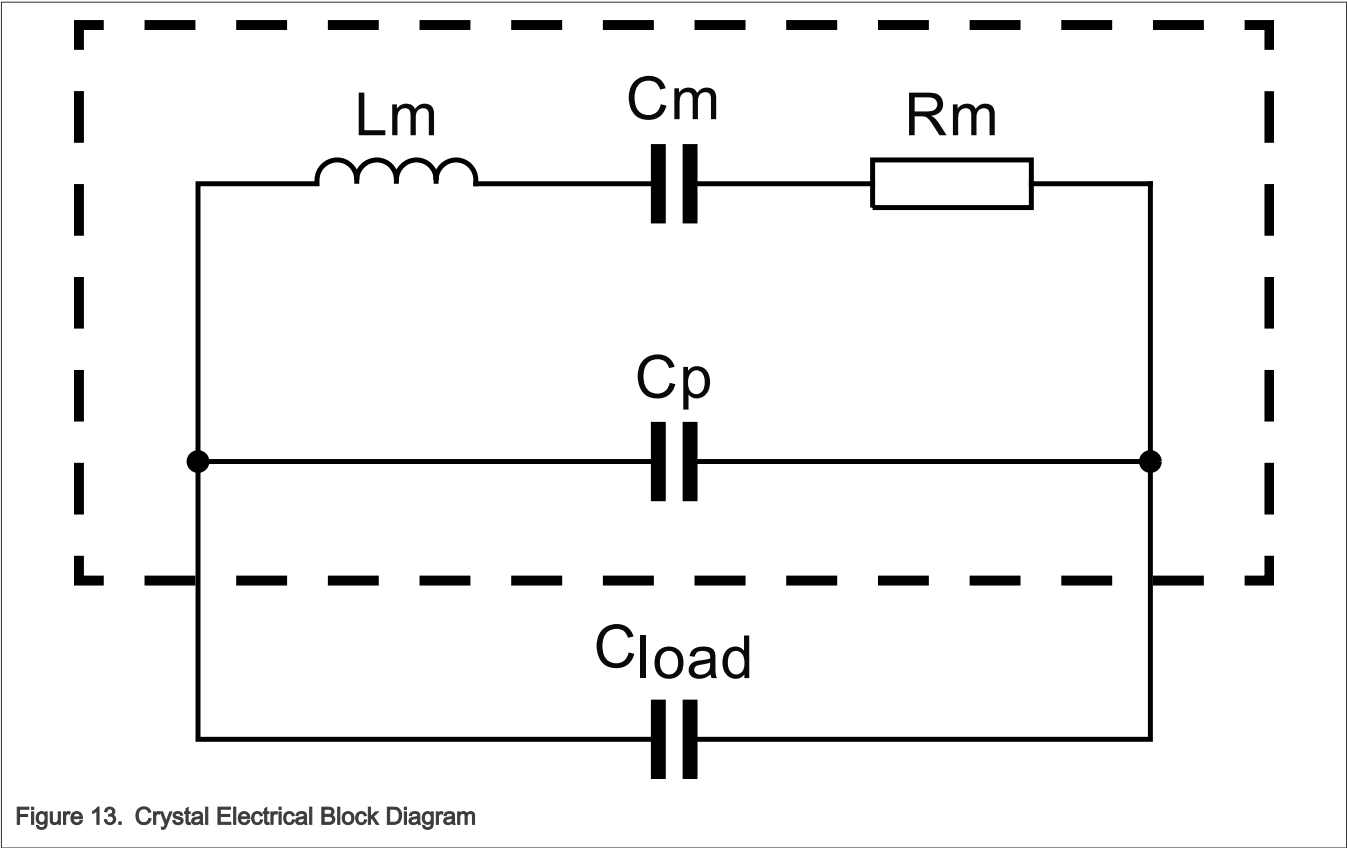


Figure 13. Crystal Electrical Block Diagram

4.2.2 32 kHz oscillator electrical specifications

Table 36. 32 kHz oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_32k}	Crystal frequency	—	32.768	—	kHz	
Tol	Frequency tolerance	—	±100	—	ppm	1
	• Normal/Start up mode	—	±150	—		
Jit _{osc}	Jitter	—	12000	—	ps	
	• Period jitter (RMS)	—	8000	—		
ESR	Crystal equivalent series resistance	—	—	100 K	kΩ	
	• Normal mode	—	—	50 K		
R _F	Internal feedback resistor	—	100	—	MΩ	
C _{para}	Parasitic capacitance of EXTAL32 and XTAL32	—	2.5	—	pF	

Table continues on the next page...

Table 36. 32 kHz oscillator electrical specifications...continued

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{start}	Crystal start-up time - Normal/Start up mode - Low power mode	— —	1000 8000		ms	2
$I_{\text{OSC_32k}}$	Current consumption - ON mode - Normal mode - Low power mode - OFF mode	— — —	220 110 0.5	— — —	nA	
V_{pp}	Peak-to-peak amplitude of oscillation - Normal mode - Low power mode	— —	0.2 0.1	— —	V	3
$f_{\text{ec_extal32}}$	Externally provided input clock frequency	—	32.768	—	kHz	4
$t_{\text{DC_EXTAL32}}$ 2	External clock duty cycle	40	50	60	kHz	
$V_{\text{ec_extal32}}$	Externally provided input clock amplitude	Refer to Voltage and current operating requirements for V_{IH} and V_{IL} levels			mV	4, 5
$C_{\text{extal/xtal}}$	On-chip EXTAL, XTAL Load Capacitance	0	—	30	pF	6,7

- For Low power mode, use crystals with load cap (CL) 7 pF or less
- Proper PC board layout procedures must be followed to achieve specifications.
- When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.
- This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
- The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to $V_{\text{DD_BAT}}$.
- These are the internally available oscillator load capacitors on each of the EXTAL32 and XTAL32 pins, selectable in 2 pF steps. The effective load capacitance is the series equivalent of the selected capacitors.
- The internally available load capacitors can be set to minimum of 0 on XTAL and 2 pF on EXTAL and external load capacitors used instead.

Table 37. 32 kHz oscillation gain setting

Coarse_Amp_Gain	Max ESR (k Ω)	Max Cx (pF) ¹	Notes
00 (default)	50	14	
01	70	22	
10	80	22	
11	100	20	

- Cx is the sum of all capacitance connected to both EXTAL32 and XTAL, including internal load capacitors, pad capacitance and PCB

NOTE

It is recommended that the oscillator margin be measured on the actual application PCB with the target crystal.

4.2.3 Free-running oscillator FRO144M specifications

Table 38. FRO144M specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
$f_{fro144m}$	FRO144M frequency (nominal)	144			MHz	
$\Delta f_{fro144m}$	Frequency deviation					
	- Open loop - Closed loop (using accurate clock source as reference)	— —	— —	± 2 ± 0.25	% %	
$t_{startup}$	Start-up time					
	- Oscillation time with initial accuracy of -20 % to +2 % of enable signal assertion - Oscillation time within +/- 2 % from enable signal assertion	— —	2 20	— —	μs μs	
f_{os}	Frequency overshoot during startup	—	—	2	%	
$j_{it_{per}}$	- Period jitter RMS ¹ - Accumulated jitter over 1 ms	—	200	—	ps	
$j_{it_{cyc}}$	Cycle to cycle jitter	—	200	—	ps	
$I_{fro144m_vdd_sys}$	Current consumption for VDD_SYS	—	70	—	μA	
$I_{fro144m_vdd_core}$	Current consumption for VDD_CORE	—	35	—	μA	

1. Reference clock = 144 MHz.

4.2.4 Free-running oscillator FRO12M specifications

Table 39. FRO12M specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{fro12m}	FRO12M frequency (nominal)	—	12	—	MHz	
Δf_{fro12m}	Frequency deviation					
	- open loop - closed loop (using accurate clock source as reference)	— —	— —	± 3 ± 0.6	% %	
$t_{startup}$	Start-up time	—	5	—	μs	
f_{os}	Frequency overshoot during startup	—	10	20	%	
I_{fro12m}	Current consumption	—	7	—	μA	

4.2.5 Free-running oscillator FRO16K specifications

Table 40. FRO16K specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{fro16k}	FRO16K frequency (nominal)	—	16.384	—	kHz	
Δf_{fro16k}	Frequency deviation over $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ open loop	—	—	± 6	%	
TRIM _{step}	Trimming step	—	1.5	—	%	
$t_{startup}$	Start-up time	—	310	—	μs	
I_{fro16k}	Current consumption	—	50	—	nA	

4.2.6 550 MHz PLL specifications

Table 41. PLL specifications

Symbol	Description	Min	Typ	Max	Units	Notes
fcco	CCO operating frequency	275	—	550	MHz	
I _{pll}	PLL operating current @ fcco = 550 MHz and f _{out} = 55 MHz	—	484	—	μA	
F _{ref}	PLL reference frequency range	5	—	150	MHz	
J _{pp_period}	Peak-Peak period jitter @ f _{ref} = 12 MHz; fcco = 550 MHz f_{vco} = 550 MHz	—	110	—	ps	
J _{rms_int}	RMS interval jitter @f _{out} = fcco = 550 MHz, f _{ref} = 12 MHz	—	14	—	ps	
t _{pon}	Start-up time	—	—	500+300/ F _{ref}	μs	

NOTE

The information in this table applies to both PLL0 (APLL) and PLL1 (SPLL).

4.3 Memories and memory interfaces

4.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

4.3.1.1 Timing specifications

The following command times assume a flash bus clock frequency of 24 MHz. Command times will be increased by up to 10 μs at 24 MHz if the module is exiting sleep mode when the command is launched. The time to abort a command is not included in the following table.

Table 42. Flash command time specifications

Symbol	Description		Typ.	Max.	Unit	Notes
t_{rd1all}	Read 1s All execution time	256 KB	—	1700	μ s	
		512 KB	—	3200		
		1024 KB	—	6200		
t_{rd1blk}	Read 1s Block execution time	256 KB	—	1500	μ s	
		512 KB	—	3050		
		1024 KB	—	6000		
t_{rd1scr}	Read 1s Sector execution time	8 KB	—	50	μ s	¹
t_{rd1pg}	Read 1s Page execution time	128 B	—	4.4	μ s	¹
$t_{rd1pglv}$	Read 1s Page at low voltage execution time	128 B	—	5.8	μ s	¹
t_{rd1phr}	Read 1s Phrase execution time	16 B	—	3.8	μ s	¹
$t_{rd1phrlv}$	Read 1s Phrase at low voltage execution time	16 B	—	4.8	μ s	¹
t_{rdmisr}	Read into MISR	8 KB	—	50	μ s	¹
		256 KB	—	1500		
		512 KB	—	3050		
		1024 KB	—	6000		
$t_{rd1iscr}$	Read 1s IFR Sector execution time	8 KB	—	50	μ s	¹
t_{rd1ipg}	Read 1s IFR Page execution time	128 B	—	4.4	μ s	¹
$t_{rd1ipglv}$	Read 1s IFR Page at low voltage execution time	128 B	—	5.8	μ s	¹
$t_{rd1iphr}$	Read 1s IFR Phrase execution time	16 B	—	3.8	μ s	¹
$t_{rd1iphrlv}$	Read 1s IFR Phrase at low voltage execution time	16 B	—	4.8	μ s	¹
$t_{rdimisr}$	Read IFR into MISR execution time	8 KB	—	50	μ s	¹
		32 KB	—	190		
$t_{pgmpg_initial}$	Program Page execution time at <1k cycles	128 B	450	600 ²	μ s	³
$t_{pgmpg_lifetime}$	Program Page execution time at >1k cycles	128 B	450	750 ²	μ s	³
$t_{pgmphr_initial}$	Program Phrase execution time at <1k cycles	16 B	135	180 ²	μ s	³
$t_{pgmphr_lifetime}$	Program Phrase execution time at >1k cycles	16 B	135	225 ²	μ s	³
t_{ersall}	Erase All execution time	256 KB	—	800	ms	

Table continues on the next page...

Table 42. Flash command time specifications...continued

Symbol	Description		Typ.	Max.	Unit	Notes
		512 KB	—	1500		
		1024 KB	—	2800		
t_{ersall}	Erase All execution time	256 KB	—	800	ms	
		512 KB	—	1500		
		1024 KB	—	2800		
t_{ersscr}	Erase Sector execution time	8 KB	2	22	ms	3
t_{masers}	Mass Erase execution time (via sideband)	256 KB	—	800	ms	
		512 KB	—	1500		
		1024 KB	—	2800		

1. Time to abort the command may significantly impact the time to execute the command.
2. Characterized but not tested in production
3. Measured from the time FSTAT[PERDY] is cleared.

4.3.1.2 Flash high voltage current behavior

Table 43. Flash high voltage current behavior

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DD_IO_PGM}$	Average current adder to VDD_Px during flash programming operation	—	—	6	mA	1
$I_{DD_IO_ERS}$	Average current adder to VDD_Px during flash erase operation	—	—	4	mA	1

1. See the Power Management chapter in the reference manual for the specific VDD_Px voltage supply powering the flash array.

4.3.1.3 Flash reliability specifications

Table 44. Flash reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
$t_{nvmp10k}$	Data retention after up to 10 K cycles	10	50	—	years	
$n_{nvmpcscr}$	Sector cycling endurance	10 K	500 K	—	cycles	2
T_{nvmp1k}	Data retention after up to 1 K cycles	20	100	—	years	
$T_{nvmp100k}$	Data retention after up to 100 K cycles	5	50	—	years	
$N_{nvmpc256k}$	Sector cycling endurance for 256 KB	100 K	500 K	—	cycles	3

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile.
2. Sector cycling endurance represents the number of Program/Erase cycles on a single sector at $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$.

3. For devices with a single flash block, sectors must be located within the last 256 KB of the flash main memory. For devices with two flash blocks, sectors must be located within the last 256 KB of each flash main memory but must not total more than 256 KB per device.

4.3.2 eFuse specifications

Table 45. Fusebox electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{SYS_PROG}	VDD_SYS Voltage for fuse programming	2.25	2.5	2.75	V	1
I _{SYS_PROG}	Fuse programming current	—	—	40	mA	2
T _{PROG}	Fuse programming time	—	10	11	μs	3

1. VDD_SYS ramp-up slew rate MUST be slower than 2.5V/100 μs to avoid unintentional program
2. This is the current required to program just the fuse and is in addition to any other current being drawn by the device.
3. The maximum total accumulated time for elevated VDD_SYS (VDD_SYS > 1.98V) is 20 seconds over the lifetime of the device.

4.4 Analog

4.4.1 ADC electrical specifications

4.4.1.1 ADC operating conditions

Table 46. ADC operating conditions

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
V_ANA	Supply voltage	1.71		3.6	V	
ΔVDD		−0.1	0	0.1	mV	2
ΔVSS		−0.1	0	0.1	mV	2
V _{REFH}	ADC reference voltage high	0.99		VDD_ANA	V	
V _{REFL}	ADC reference voltage low	VSSA		VSSA	V	3
V _{ADIN}	Input Voltage	VREFL		VREFH	V	3,4,5
f _{ADCK}	ADC Input clock frequency					
	Low-power mode (PWRSEL=00)	6		24	MHz	
	High-speed 16b mode (PWRSEL==10)	6		48	MHz	
	High-speed 12b mode (PWRSEL==10)	6		60	MHz	
C _{ADIN}	Input Capacitance		3.7	4.63	pF	
C _P	Parasitic Capacitance of pad/package		2	3	pF	
R _{AS}	Analog source resistance (external)			5	kΩ	6
R _{ADIN}	High-Speed Dedicated Input				kΩ	7,8
	VDDAD ≥ 1.71 V		0.95	1.7	kΩ	
	VDDAD ≥ 2.1 V			1.575	kΩ	

Table continues on the next page...

Table 46. ADC operating conditions...continued

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
	VDDAD ≥ 2.5 V			1.4	kΩ	
	Standard Dedicated Input				kΩ	
	VDDAD ≥ 1.71 V		1.35	3.25	kΩ	
	VDDAD ≥ 2.1 V			2.14	kΩ	
	VDDAD ≥ 2.5 V			1.75	kΩ	
	Standard Muxed Input				kΩ	
	VDDAD ≥ 1.71 V		1.65	7.25	kΩ	
	VDDAD ≥ 2.1 V			3.05	kΩ	
	VDDAD ≥ 2.5 V			2.35	kΩ	

1. Typical values assume $V_{DD_ANA} = 3.0\text{ V}$, Temp = 25 °C, $f_{ADCK} = 24\text{ MHz}$, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference
3. For devices that do not have a dedicated VREFL and VSS_ANA pins, VREFL and VSS_ANA are tied to VSS internally.
4. If V_{REFH} is less than V_{DD_ANA} , then voltage inputs greater than V_{REFH} but less than V_{DD_ANA} are allowed but result in a full-scale conversion result
5. ADC selected inputs and unselected dedicated inputs must not exceed V_{DD_ANA} during an ADC conversion. Unselected muxed inputs may exceed V_{DD_ANA} but must not exceed the IO supply associated with the inputs (V_{DD_Px}) when a conversion is in progress. If an ADC input may exceed these levels, then a minimum of 1 K series resistance must be used between the source and the ADC input pin.
6. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible.
7. There are several types of ADC inputs. To see which channels correspond to which type of ADC inputs, see ADC input connections in reference manual
8. If the input come through a mux in the IO pad, add the IO Mux Resistance Adder value to the resistance for the channel type

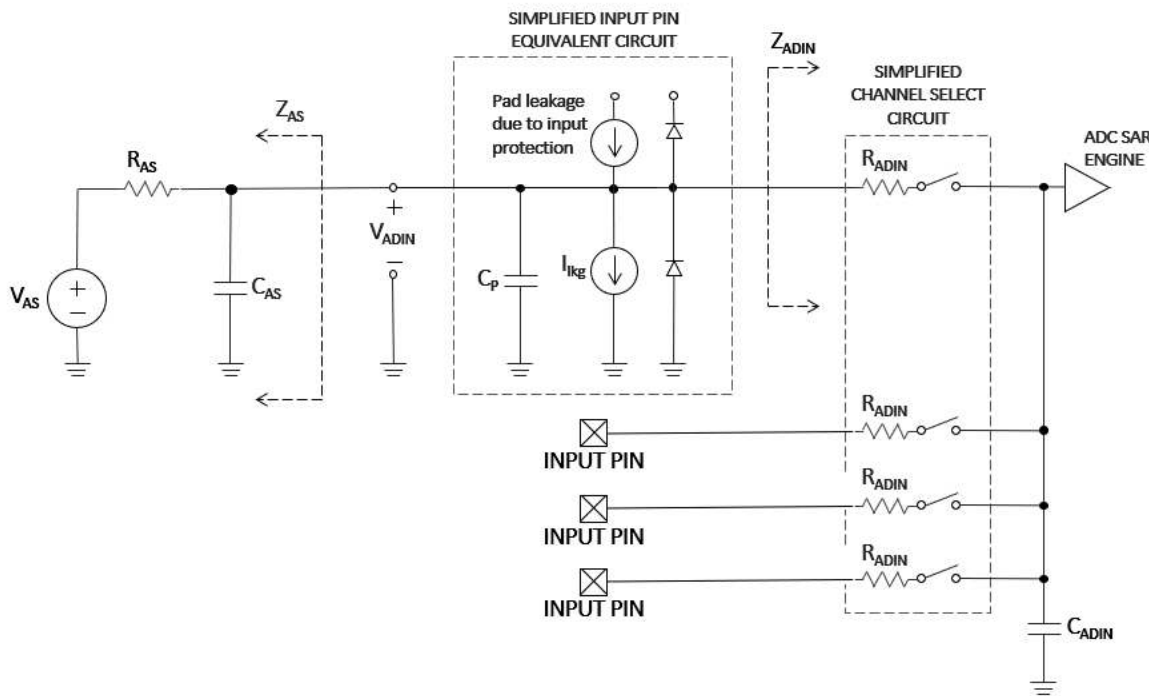


Figure 14. ADC input impedance equivalency diagram

4.4.1.2 ADC electrical characteristics

Table 47. ADC electrical specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
I _{DDA}	Supply current					²
	PWREN=0, Conversions triggered at 1 kS/s		2.2		μA	
	PWREN=1, No Conversions		160		μA	
	Low-power, single-ended mode, 6 MHz		295	390	μA	
	Low-power, differential, or dual-SE mode, 6 MHz		410	550	μA	
	Low-power, single-ended mode, 24 MHz		380	520	μA	
	Low-power, differential, or dual-SE mode, 24 MHz		500	690	μA	
	High-speed, single-ended mode, 48 MHz		730	960	μA	
	High-speed, differential, or dual-SE mode, 48 MHz		1150	1490	μA	
I _{TS}	Temp Sensor Current Adder		40	50	μA	
C _{SMP}	ADC Sample cycles	3.5		131.5	cycles	³
C _{CONV}	ADC conversion cycles					

Table continues on the next page...

Table 47. ADC electrical specifications ...continued

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
	16-bit	24		152	cycles	
	12-bit	19		147	cycles	
C_RATE	ADC conversion rate					4
	Low-power mode			0.857	MS/s	
	High-speed 12b mode			3.15	MS/s	
	High-speed 16b mode			2.0	MS/s	
T_SMP_REQ	Required Sample Time	See equation			ns	5
T_AZ_REQ	Required Auto-Zero time					5
	Low-power mode	291.7			ns	
	High-speed 12b mode	59.3			ns	
	High-speed 16b mode	72.9			ns	
T_SMP	External inputs	See equation			ns	5
T_SMP_INT	Internal inputs	1.5			μs	6
DNL	Differential non-linearity			±1	LSB ⁷	8
INL	Integral non-linearity			±3	LSB ⁷	8
Z_SE	Zero-scale error (V_ADIN = V_REFL)			±2	LSB ⁷	8
F_SE	Full-scale error (V_ADIN = V_REFH)			±5	LSB ⁷	8
TUE	Total Unadjusted Error			±7	LSB ⁷	8
ENOB	Differential Effective number of bits					8, 9
	1 MS/s (AVGS=001)		13.5		bits	
	2 MS/s		13.0		bits	
	3.15 MS/s (for 12-bit mode)		11.3		bits	
	Single-ended Effective number of bits					
	1 MS/s (AVGS=001)		13.0		bits	
	2 MS/s		12.5		bits	
	3.15 MS/s (for 12-bit mode)		11.0		bits	
SINAD	Differential Signal-to-noise plus distortion					8, 9
	1 MS/s (AVGS=001)		83		dB	
	2 MS/s		80		dB	
	3.15 MS/s (for 12-bit mode)		70		dB	
	Single-ended Signal-to-noise plus distortion					

Table continues on the next page...

Table 47. ADC electrical specifications ...continued

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
	1 MS/s (AVGS=001)		80		dB	
	2 MS/s		77		dB	
	3.15 MS/s (for 12-bit mode)		68		dB	
THD	Total Harmonic distortion		95		dB	8,9
SFDR	Spurious free dynamic range		96		dB	8,9
t _{ADCSTUP}	ADC/VREF start-up time	5			µs	10
E_IL	Input leakage error		llkg		mV	11
E_TS	Temperature sensor error					12
	T=-40 to 105 °C		1	3	°C	
	T=-40 to 125 °C		1.5	4	°C	
A	Slope Factor Constant	–	771	–		
B	Offset Constant	–	302	–		
α	Bandgap constant	–	10.06	–		

1. Typical values assume V_{DD_ANA} = 3.3 V, Temp = 25 °C, f_{ADCK} = 24 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. The ADC supply current depends on the ADC conversion clock speed, conversion rate, and power mode. Typical value show is at 6 MHz, 24 MHz, and 48 MHz. For lowest power operation, PWRSEL should be set to 00.
3. Must meet minimum TSMP requirement
4. Maximum conversion rate for high-speed mode is with F_{ADCK} = 48 MHz. Maximum conversion rate for low-power mode is F_{ADCK} = 24 MHz and 7.5 sample cycles (to meet the minimum auto-zero time requirement)
5. Required sample time is dictated by external components R_{AS}, C_{AS}, internal components R_{ADIN}, C_{ADIN}, C_P, and desired sample accuracy in bits(B). Calculate it with formula: T_{SMP_REQ} = B*0.693*[R_{AS}*(C_{AS}+C_P+C_{ADIN})+ (R_{AS} + R_{ADIN})* C_{ADIN}]. Required auto-zero time is for ADC comparator offset cancellation. The chosen sample time should be no less than maximum of the two: T_{SMP} = max(T_{SMP_REQ}, T_{AZ_REQ})
6. Internal channel inputs are those that do not come from external source (temperature sensor, bandgap).
7. 1 LSB = (V_{REFH} - V_{REFL})/2^N (N=14 bits), for 16- bit specifications, multiply by 4.
8. All accuracy numbers assume that the ADC is calibrated with V_{REFH}=V_{DD_ANA} and using a high- speed- dedicated input channel.
9. Dynamic results assume F_{in}=1 kHz sinewave, no averaging.
10. Set the power-up delay (PUDLY) according to the ADC start-up time if PWREN=0.
11. I_{lkg} = leakage current (Refer to pin leakage specification in the voltage and current operating ratings of packaged device)
12. The temperature sensor can be calibrated to a +/- 0.5 % precision after board assembly by using a 3-temperature calibration flow with accurate ± 0.15 % temperature chamber.

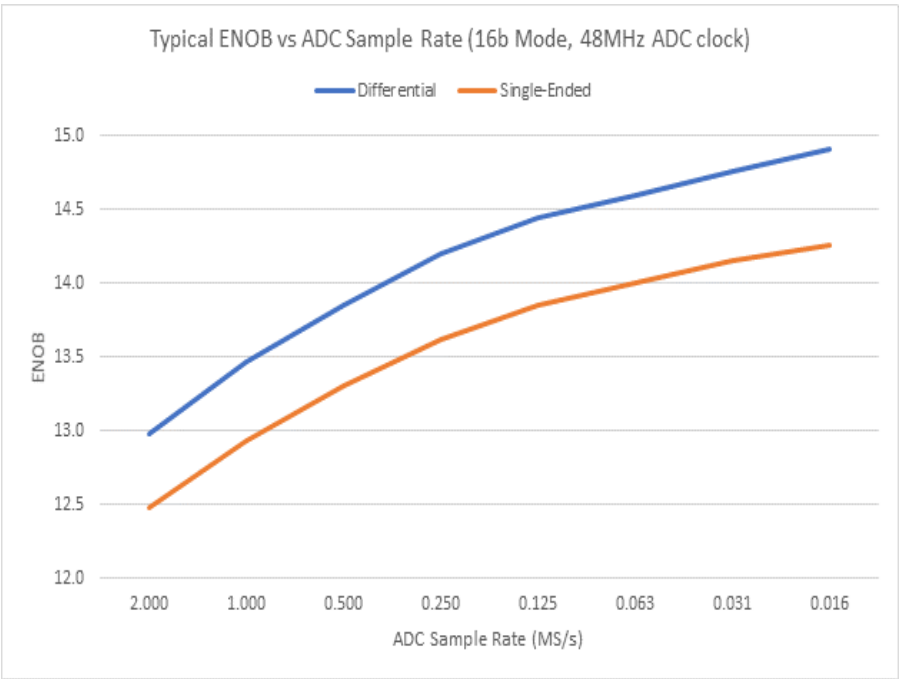


Figure 15. ENOB VS ADC clock graph

4.4.2 CMP and 8-bit DAC electrical specifications

Table 48. Comparator and 8-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD	Supply voltage	1.71	—	3.6	V	
VREFH	8-bit DAC reference voltage high	0.97	—	VDD	V	
I _{DD_CMP}	Supply current - High speed mode (EN=1, HPMD=1) - Normal mode (EN=1, HPMD=0, NPMD=0) - Low-power mode (EN=1, HPMD=0, NPMD=1)	—	200 10 400	—	μA μA nA	
V _{AIN}	Analog input voltage	VSS	—	VDD	V	
V _{AIO}	Analog input offset voltage - High speed mode - Normal mode - Low-power mode	—	—	20 20 40	mV mV mV	
V _H	Analog comparator hysteresis - CR0[HYSTCTR] = 00 - CR0[HYSTCTR] = 01	—	0 10	—	mV mV	1

Table continues on the next page...

Table 48. Comparator and 8-bit DAC electrical specifications...continued

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	- CR0[HYSTCTR] = 10 - CR0[HYSTCTR] = 11	—	20	—	mV	
		—	30	—	mV	
V _{CMPOh}	Output high	VDD - 0.2	—	—	V	
V _{CMPOl}	Output low	—	—	0.2	V	
t _D	Propagation delay - High speed mode, 100 mV overdrive, power > 1.71V - High speed mode, 30 mV overdrive, power > 1.71V - Normal mode, 30 mV overdrive, power > 1.71V - Low-power mode, 30 mV overdrive, power > 1.71V	—	—	25	ns	2
		—	—	50	ns	
		—	—	600	ns	
		—	—	5	μs	
t _{init}	Analog comparator initialization delay	—	—	40	μs	3
I _{DAC8b}	8-bit DAC current adder (enabled) - High power mode (EN=1, PMODE=1) - Low power mode (EN=1, PMODE=0)	—	10	—	μA	4
		—	1	—	μA	
INL	8-bit DAC integral non-linearity - Low/High power mode, supply power > 1.71V - Low power mode, supply power < 1.71V	-1	—	+1.0	LSB	
		-2	—	+2		
DNL	8-bit DAC differential non-linearity - Low/High power mode, power > 1.71V - Low power mode, power < 1.71V	-1	—	+1.0	LSB	4
		-1	—	+1		

1. Typical hysteresis is measured with input voltage range limited to 0.6 to VDD_ANA–0.6 V.
2. Overdrive does not include input offset voltage or hysteresis
3. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
4. 1 LSB = V_{reference}/256

Typical hysteresis

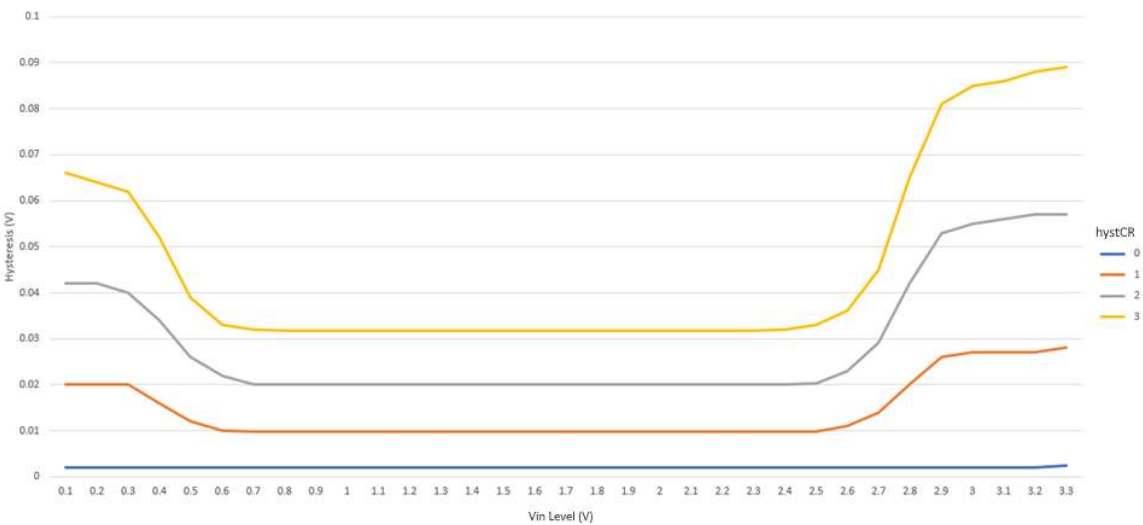


Figure 16. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 1)

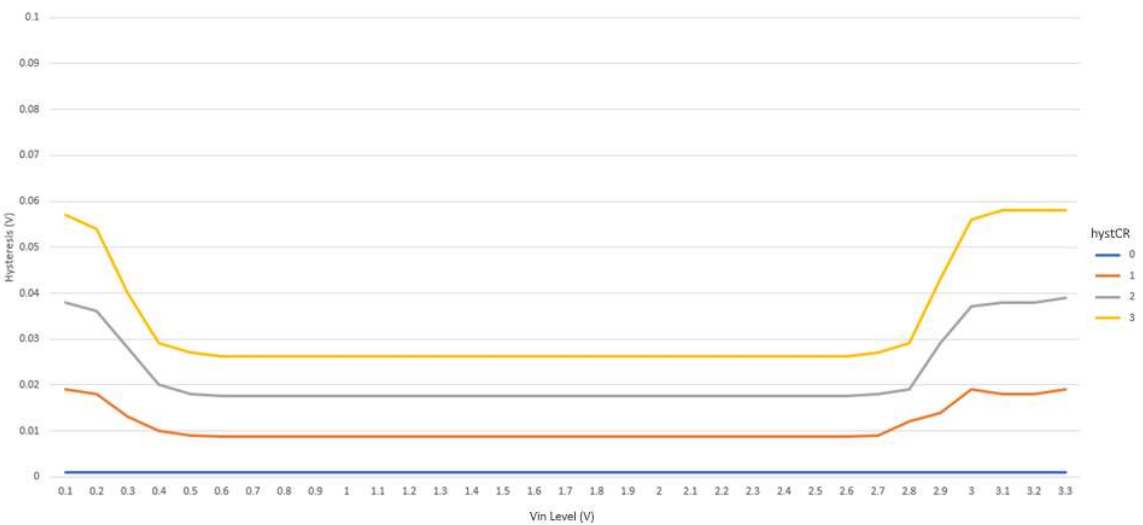


Figure 17. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 0)

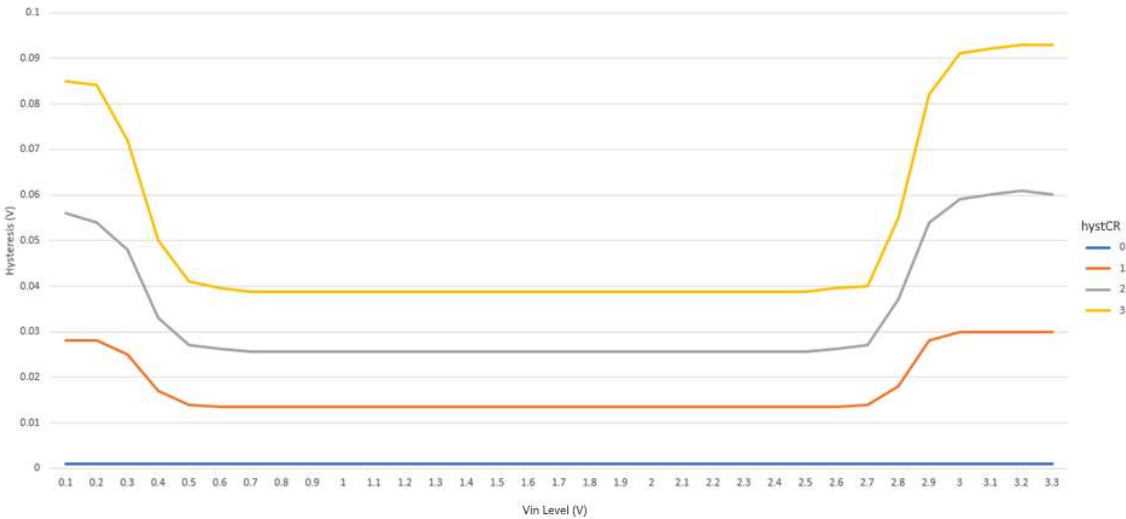


Figure 18. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 1)

4.4.3 Voltage reference electrical specifications

Table 49. VREF operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDD_ANA	Supply voltage	1.71	3.0	3.6	V	1
C _L	Output load capacitance	—	220	—	nF	2,3

1. VDD_ANA must be at least 600 mV greater than the selected VREF_O output voltage.
2. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
3. The minimum C_L capacitance must take into account the variation in capacitance of the chosen capacitor due to voltage, temperature, and aging.

Table 50. VREF operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
1.0 V low-power reference voltage						
V _{vrefo_lpbpg}	Voltage reference output 1.0 V - LP bandgap	—	1.0	—	V	1
I _{q_lpbpg}	Quiescent current - LP bandgap	—	19	—	μA	
I _{ptat}	Output current reference (PTAT) - LP bandgap (room temp)	—	1	—	μA	
I _{ztc}	Output current reference (ZTC) - LP bandgap	—	1	—	μA	
t _{st_lpbpg}	Start-up time - LP bandgap	—	—	20	μs	

Table continues on the next page...

Table 50. VREF operating behaviors...continued

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$\Delta V/V_{\text{refo_lpbg}}$	Voltage variation - LP bandgap	—	± 5	—	%	
High precision reference voltage						
V_{vrefo}	Voltage reference output 2.0 V	1.0	—	2.1	V	2,1
V_{step}	Fine trim step	—	$0.5 \times V_{\text{vrefo}}$	—	mV	
I_{q}	Quiescent current	—	750	—	μA	
I_{out}	Drive strength	± 1	—	—	mA	
$t_{\text{st_hcbg}}$	Start-up time	—	—	400	μs	
ΔV_{LOAD}	Load regulation	—	100	200	$\mu\text{V}/\text{mA}$	3
V_{acc}	Absolute voltage accuracy (room temp)	—	—	± 2	mV	4
V_{dev}	Voltage deviation over temperature	—	15	—	ppm/°C	

1. See the Reference Manual of the chip for the appropriate settings of the VREF Status and Control register.
2. V_{vrefo} max is also $\leq V_{\text{DD_ANA}} - 600 \text{ mV}$.
3. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load.
4. Under $V_{\text{vrefo}} = 1\text{V}$ configuration.

4.5 Timers

See [General switching specifications](#).

4.6 Communication interfaces

4.6.1 LPUART

See [General switching specifications](#).

4.6.2 LPSPI switching specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes.

Table 51. LPSPI master mode timing

Symbol	Description	Min.	Max.	Unit	Notes
LP1	Frequency of operation				1
	• Master TX in OD mode				
	— LPSPi0–LPSPi2	—	25	MHz	
	— LPSPi3–LPSPi5	—	50	MHz	
	— LPSPi6–LPSPi7	—	75	MHz	
	• Master RX in OD mode				

Table continues on the next page...

Table 51. LPSPI master mode timing...continued

Symbol	Description	Min.	Max.	Unit	Notes
	— LPSPi0–LPSPi2	—	25	MHz	
	— LPSPi3–LPSPi5	—	50	MHz	
	— LPSPi6–LPSPi7	—	75	MHz	
	• Master TX in SD mode				
	— LPSPi0–LPSPi2	—	21	MHz	
	— LPSPi3–LPSPi5	—	32	MHz	
	— LPSPi6–LPSPi7	—	50	MHz	
	• Master RX in SD mode				
	— LPSPi0–LPSPi2	—	21	MHz	
	— LPSPi3–LPSPi5	—	32	MHz	
	— LPSPi6–LPSPi7	—	50	MHz	
	• Master TX in MD mode				
	— LPSPi0–LPSPi2	—	12.5	MHz	
	— LPSPi3–LPSPi5	—	25	MHz	
	— LPSPi6–LPSPi7	—	25	MHz	
	• Master RX in MD mode				
	— LPSPi0–LPSPi2	—	12.5	MHz	
	— LPSPi3–LPSPi5	—	25	MHz	
	— LPSPi6–LPSPi7	—	25	MHz	
LP2	SCK period	$2 \times t_{\text{periph}}$	$2048 \times t_{\text{periph}}$	ns	
LP3	Enable lead time	1/2	—	t_{periph}	²
LP4	Enable lag time	1/2	—	t_{periph}	²
LP5	Clock (SCK) high or low time	$t_{\text{SCK}}/2 - 3$	$t_{\text{SCK}}/2$	ns	—
LP6	Data setup time (inputs)			ns	—
	• LPSPi0–LPSPi2	14.4	—		
	• LPSPi3–LPSPi5	7.2			
	• LPSPi6–LPSPi7	4.8			
LP7	Data hold time (inputs)	0	—	ns	—
LP8	Data valid (after SCK edge)			ns	—
	• LPSPi0–LPSPi2	—	14.4		
	• LPSPi3–LPSPi5		7.2		
	• LPSPi6–LPSPi7		4.8		
LP9	Data hold time (outputs)	1	—	ns	—

1. The frequency of operation is also limited to a minimum of $f_{\text{periph}}/2048$ and a max of $f_{\text{periph}}/2$, where f_{periph} is the LPSPI peripheral functional clock.

2. $t_{\text{periph}} = 1/f_{\text{periph}}$

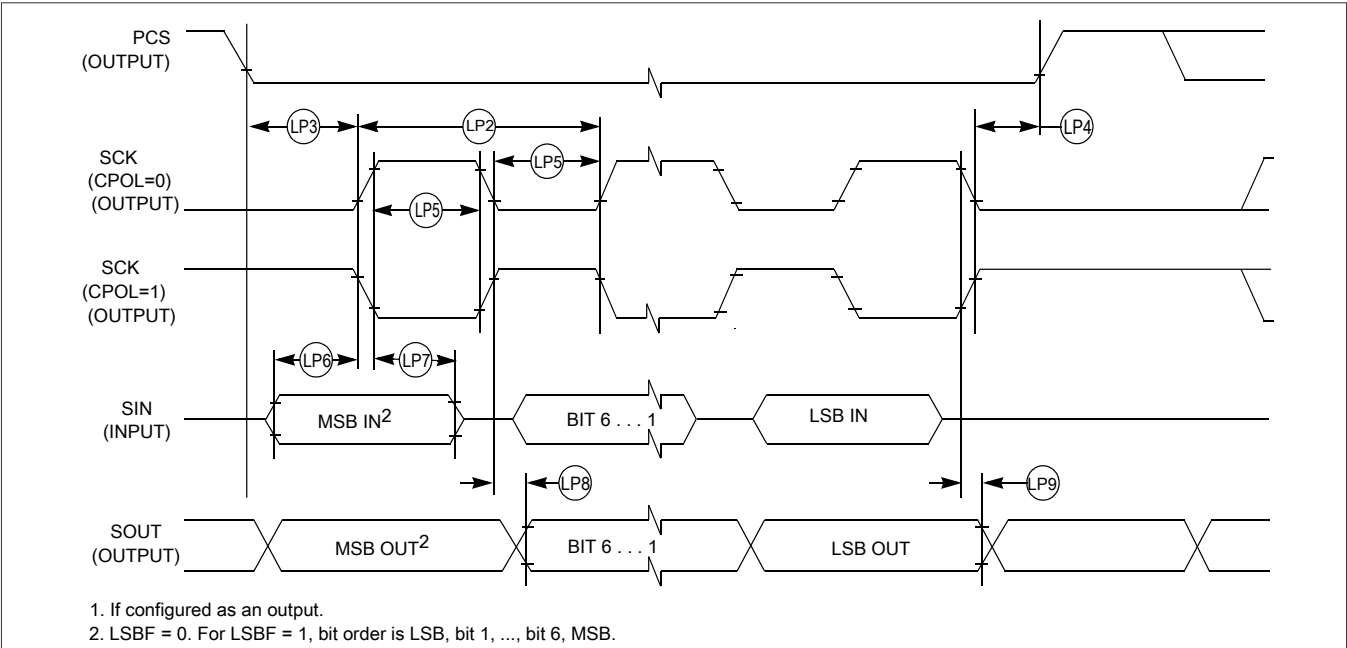


Figure 19. LPSPI master mode timing (CPHA = 0)

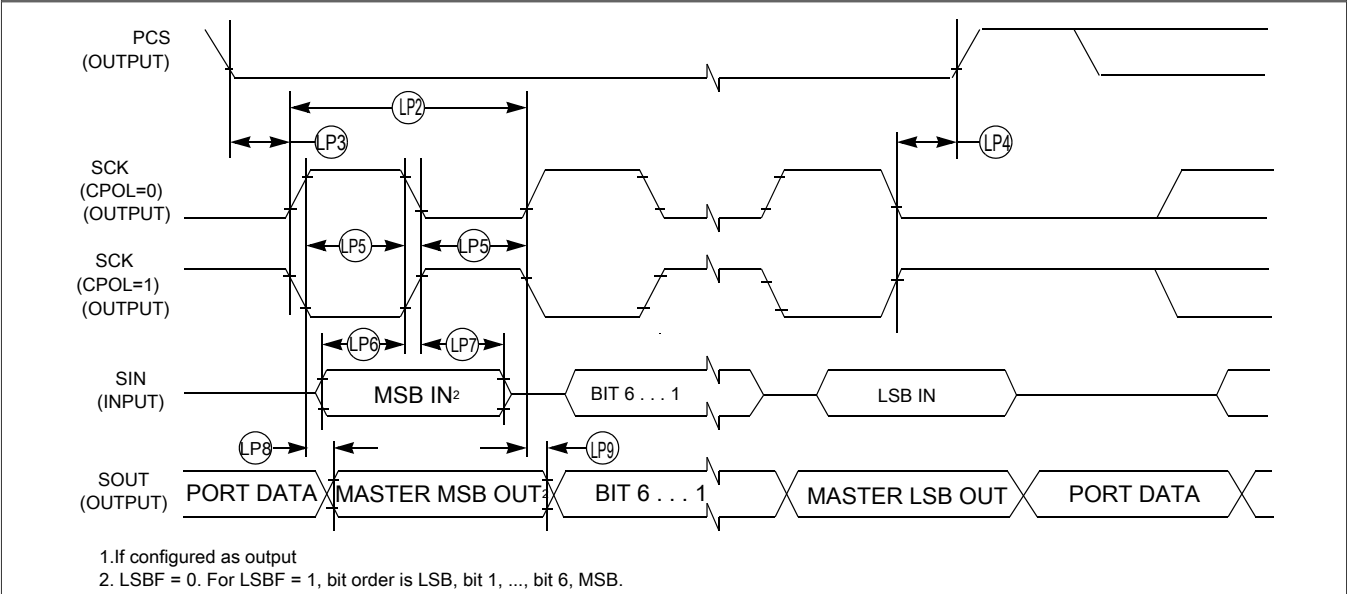


Figure 20. LPSPI master mode timing (CPHA = 1)

Table 52. LPSPI slave mode timing

Symbol	Description	Min.	Max.	Unit	Notes
LP1	Frequency of operation Slave TX in OD mode				1

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Table 52. LPSPi slave mode timing...continued

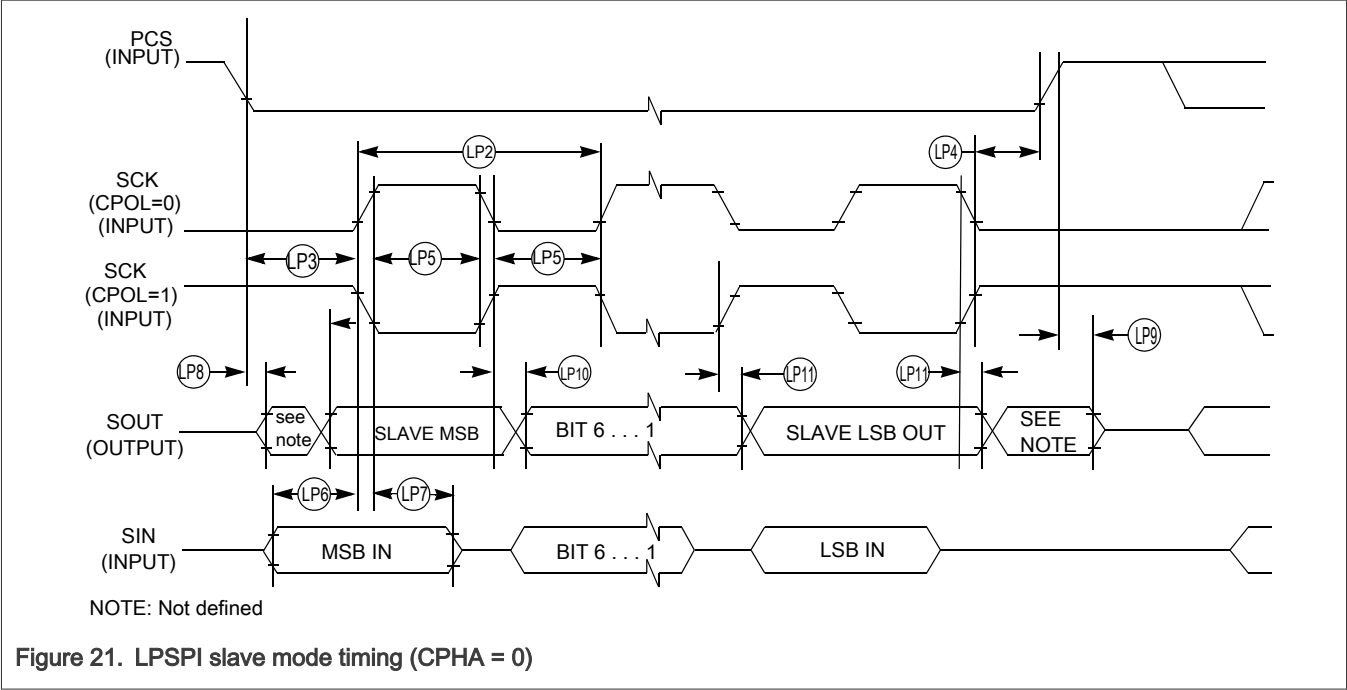
Symbol	Description	Min.	Max.	Unit	Notes
	— LPSPi0–LPSPi2	—	12.5	MHz	
	— LPSPi3–LPSPi5	—	20	MHz	
	— LPSPi6–LPSPi7	—	30	MHz	
	• Slave RX in OD mode				
	— LPSPi0–LPSPi2	—	12.5	MHz	
	— LPSPi3–LPSPi5	—	30	MHz	
	— LPSPi6–LPSPi7	—	75	MHz	
	• Slave TX in SD mode				
	— LPSPi0–LPSPi2	—	12.5	MHz	
	— LPSPi3–LPSPi5	—	16	MHz	
	— LPSPi6–LPSPi7	—	25	MHz	
	• Slave RX in SD mode				
	— LPSPi0–LPSPi2	—	12.5	MHz	
	— LPSPi3–LPSPi5	—	30	MHz	
	— LPSPi6–LPSPi7	—	50	MHz	
	• Slave TX in MD mode				
	— LPSPi0–LPSPi2	—	12.5	MHz	
	— LPSPi3–LPSPi5	—	12.5	MHz	
	— LPSPi6–LPSPi7	—	25	MHz	
	• Slave RX in MD mode				
	— LPSPi0–LPSPi2	—	12.5	MHz	
	— LPSPi3–LPSPi5	—	30	MHz	
	— LPSPi6–LPSPi7	—	30	MHz	
LP2	SCK period	$4 \times t_{\text{periph}}$	$2048 \times t_{\text{periph}}$	ns	
LP3	Enable lead time	1	—	t_{periph}	2
LP4	Enable lag time	1	—	t_{periph}	2
LP5	Clock (SCK) high or low time	$t_{\text{SCK}}/2 - 5$	$t_{\text{SCK}}/2$	ns	—
LP6	Data setup time (inputs)			ns	—
	• LPSPi0~LPSPi2	14.4	—		
	• LPSPi3~LPSPi5	6			
	• LPSPi6~LPSPi7	2.4			
LP7	Data hold time (inputs)	0	—	ns	—
LP8	Slave access time	—	t_{periph}	ns	2,3

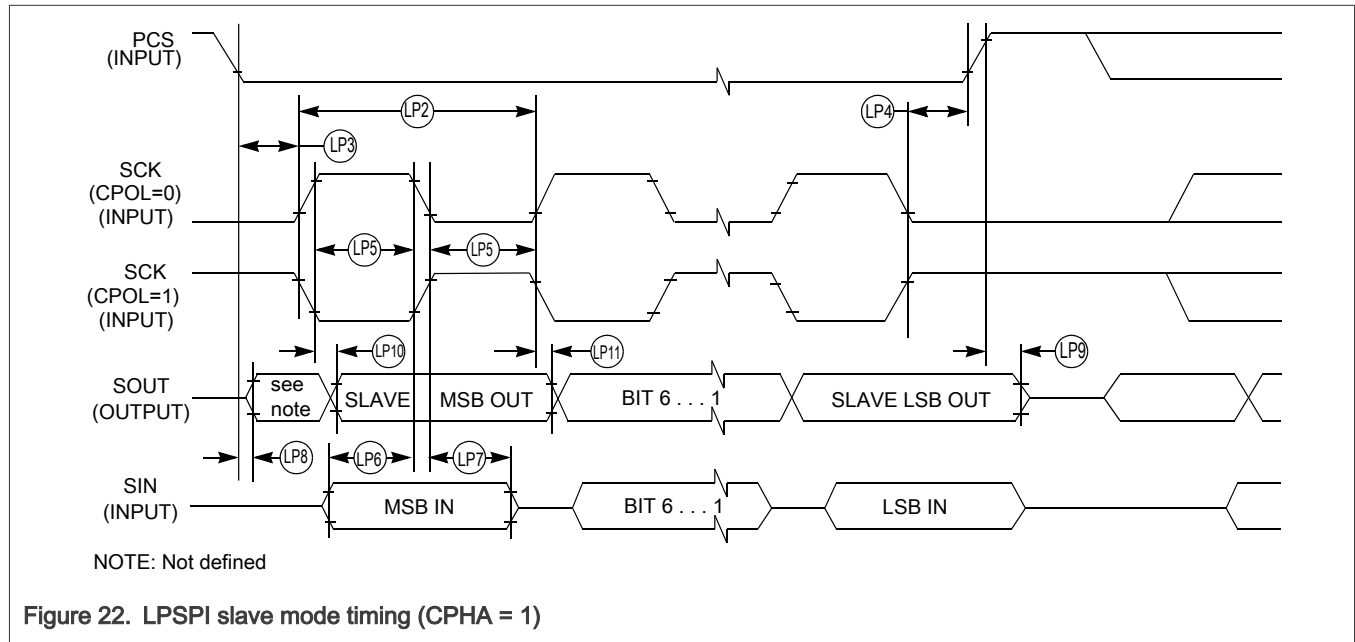
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Table 52. LPSPI slave mode timing...continued

Symbol	Description	Min.	Max.	Unit	Notes
LP9	Slave SDO disable time	—	t_{periph}	ns	2,4
LP10	Data valid (after SCK edge) • LPSPi0~LPSPi2 • LPSPi3~LPSPi5 • LPSPi6~LPSPi7	—	31.2	ns	—
			17		
			13		
LP11	Data hold time (outputs)	2	—	ns	—

1. The frequency of operation is also limited to a minimum of $f_{\text{periph}}/2048$ and a max of $f_{\text{periph}}/4$, where f_{periph} is the LPSPI peripheral functional clock.
2. $t_{\text{periph}} = 1/f_{\text{periph}}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state





4.6.3 Inter-Integrated Circuit Interface (I²C) specifications

Table 53. I²C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD; STA}$	4	—	0.6	—	μs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	μs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	$t_{SU; STA}$	4.7	—	0.6	—	μs
Data hold time for I ² C bus devices	$t_{HD; DAT}$	0 ¹	3.45 ²	0 ³	0.9 ¹	μs
Data set-up time	$t_{SU; DAT}$	250 ⁴	—	100 ^{2,5}	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	$20 + 0.1C_b$ ⁶	300	ns
Fall time of SDA and SCL signals	t_f	—	300	$20 + 0.1C_b$ ⁵	300	ns
Set-up time for STOP condition	$t_{SU; STO}$	4	—	0.6	—	μs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

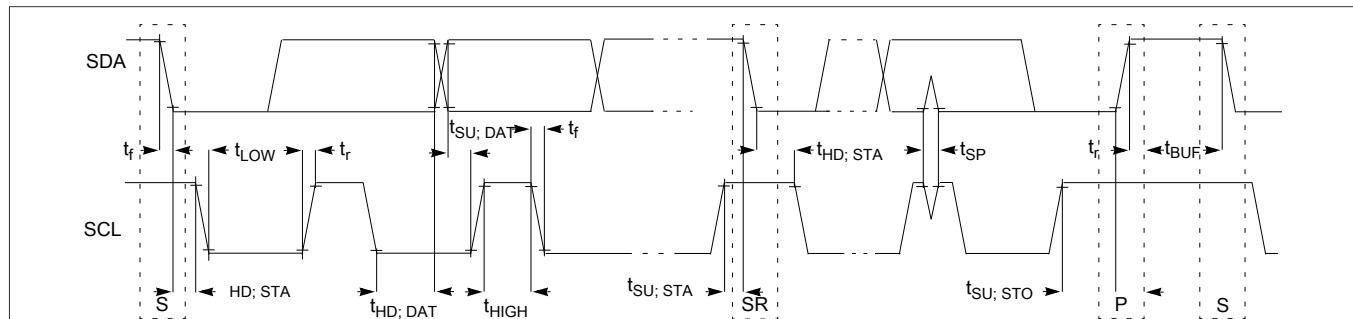
1. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum $t_{HD; DAT}$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

3. Input signal Slew = 10 ns and Output Load = 50 pF
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement $t_{\text{SU; DAT}} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{\text{rmax}} + t_{\text{SU; DAT}} = 1000 + 250 = 1250$ ns (according to the Standard mode I²C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

Table 54. I²C 1 Mbps timing

Characteristic	Symbol	Min.	Max.	Unit
SCL Clock Frequency	f_{SCL}	0	1	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{\text{HD; STA}}$	0.26	—	μs
LOW period of the SCL clock	t_{LOW}	0.5	—	μs
HIGH period of the SCL clock	t_{HIGH}	0.26	—	μs
Set-up time for a repeated START condition	$t_{\text{SU; STA}}$	0.26	—	μs
Data hold time for I ² C bus devices	$t_{\text{HD; DAT}}$	0	—	μs
Data set-up time	$t_{\text{SU; DAT}}$	50	—	ns
Rise time of SDA and SCL signals	t_r	$20 + 0.1C_b$ ¹	120	ns
Fall time of SDA and SCL signals	t_f	$20 + 0.1C_b$ ¹	120	ns
Set-up time for STOP condition	$t_{\text{SU; STO}}$	0.26	—	μs
Bus free time between STOP and START condition	t_{BUF}	0.5	—	μs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	50	ns

1. C_b = total capacitance of the one bus line in pF.

Figure 23. Timing definition for devices on the I²C bus

4.6.4 Improved Inter-Integrated Circuit Interface (MIPI-I3C) specifications

Unless otherwise specified, MIPI-I3C specifications are timed to/from the V_{IH} and/or V_{IL} signal points.

Table 55. MIPI-I3C specifications when communicating with legacy I²C devices

Symbol	Characteristic	400 kHz/Fast mode		1 MHz/ Fast+ mode		Unit
		Min.	Max.	Min.	Max.	
f _{SCL}	SCL Clock Frequency	0	0.4	0	1.0	MHz
t _{SU_STA}	Set-up time for a repeated START condition	600	—	260	—	ns
Hold time (repeated) START condition	t _{HD} ; STA	600	—	260	—	ns
t _{LOW}	LOW period of the SCL clock	1300	—	500	—	ns
t _{HIGH}	HIGH period of the SCL clock	600	—	260	—	ns
t _{SU_DAT}	Data set-up time	100	—	50	—	ns
t _{HD_DAT}	Data hold time for I ₂ C bus devices	0	—	0	—	ns
t _f	Fall time of SDA and SCL signals	20 + 0.1C _b ¹	300	20 + 0.1C _b ¹	120	ns
t _r	Rise time of SDA and SCL signals	20 + 0.1C _b ¹	300	20 + 0.1C _b ¹	120	ns
t _{SU_STO}	Set-up time for STOP condition	600	—	260	—	ns
t _{BUF}	Bus free time between STOP and START condition	1.3	—	0.5	—	μs
t _{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	0	50	ns

1. C_b = total capacitance of the one bus line in pF.

Table 56. MIPI-I3C open drain mode specifications

Symbol	Characteristic	Min.	Max.	Unit	Notes
t _{LOW_OD}	LOW period of the SCL clock	200	—	ns	
t _{DIG_OD_L}		t _{LOW_OD} + t _{rDA_OD} (min)	—	ns	
t _{HIGH}	HIGH period of the SCL clock	t _{CF}	12	ns	
t _{rDA_OD}	Fall time of SDA signal	20 + 0.1C _b	120	ns	¹
t _{SU_OD}	Data set-up time during open drain mode	3	—	ns	
t _{CAS}	Clock after START (S) Condition				
	• ENTAS0	38.4 n	1 μ	s	
	• ENTAS1	38.4 n	100 μ	s	
	• ENTAS2	38.4 n	2 m	s	
	• ENTAS3	38.4 n	50 m	s	

Table continues on the next page...

Table 56. MIPI-I3C open drain mode specifications...continued

Symbol	Characteristic	Min.	Max.	Unit	Notes
t_{CBP}	Clock before STOP (P) condition	$t_{CAS(min)}/2$	—	ns	
$t_{MMOverlap}$	Current master to secondary master overlap time during handoff	$t_{DIG_OD_L}$	—	ns	
t_{AVAL}	Bus available condition	1	—	μs	
t_{IDLE}	Bus idle condition	1	—	ms	
t_{MMLock}	Time interval where new master not driving SDA low	t_{AVAL}	—	μs	

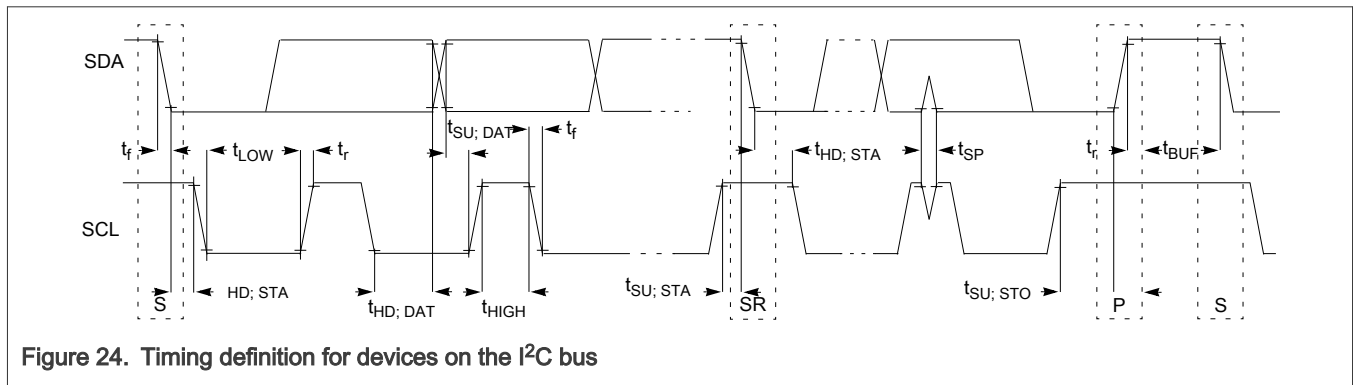
1. C_b = total capacitance of the one bus line in pF.

Table 57. MIPI-I3C push-pull specifications for SDR and HDR-DDR modes

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{SCL}	SCL Clock Frequency	0.01	12	12.5	MHz	
t_{LOW}	LOW period of the SCL clock	24	—	—	ns	
t_{DIG_L}		32	—	—	ns	
$t_{HIGH_MIXE_D}$	HIGH period of the SCL clock for a mixed bus	24	—	—	ns	
$t_{DIG_H_MIXE_D}$		32	—	45	ns	1
t_{HIGH}	HIGH period of the SCL clock	24	—	—	ns	
t_{DIG_H}		32	—	—	ns	
t_{SCO}	Clock in to data out for a slave	—	—	12 ²	ns	
t_{CR}	SCL clock rise time	—	—	150 x 1/ f_{SCL} (capped at 60)	ns	
t_{CF}	SCL clock fall time	—	—	150 x 1/ f_{SCL} (capped at 60)	ns	
t_{HD_PP}	SDA signal data hold • Master mode • Slave mode	$t_{CR} + 3$ and $t_{CF} + 3$ 0	— —	— —	ns	
t_{SU_PP}	SDA signal setup	3	—	—	ns	
t_{CASr}	Clock after repeated START (Sr)	$t_{CAS} (min)$	—	—	ns	
t_{CBSr}	Clock before repeated START (Sr)	$t_{CAS} (min)/2$	—	—	ns	
C_b	Capacitive load per bus line	—	—	50	pF	

1. When communicating with an I3C Device on a mixed Bus, the $t_{DIG_H_MIXED}$ period must be constrained in order to make sure that I²C devices do not interpret I3C signaling as valid I²C signaling.

2. It doesn't include output pad delay.



4.6.5 USB High-Speed PHY specifications

This section describes High-Speed PHY parameters. The high-speed PHY is capable of full and low-speed signaling as well. The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification with the amendments below.

- Universal Serial Bus Specification, Revision 2.0, 2000, with amendments including the ones listed below:
- Errata for “USB Revision 2.0 April 27, 2000” as of 12/7/2000
- Errata for “USB Revision 2.0 April 27, 2000” as of May 28, 2002
- Pull-up / Pull-down Resistors (USB Engineering Change Notice)
- Suspend Current Limit Changes (USB Engineering Change Notice)
- Device Capacitance (USB Engineering Change Notice)
- USB 2.0 Connect Timing Update (USB Engineering Change Notice as of April 4, 2013)
- USB 2.0 VBUS Max Limit (USB Engineering Change Notice)
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification, Revision 2.0 version 1.1a, July 27, 2012
- Maximum VBUS Voltage (USB OTGEH Engineering Change Notice)
- Universal Serial Bus Micro-USB Cables and Connectors Specification, Revision 1.01, 2007

USB1_VBUS pin is a detector function which is 5V tolerant and complies with the above specifications without needing any external voltage division components.

NOTE

The USB HS PHY does not support operation when VDD_CORE is configured to 1.0V level

4.6.6 CAN switching specifications

See [General switching specifications](#).

4.6.7 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for non-inverted serial clock polarity (TCR2[BCP] = 0 and RCR2[BCP] = 0) and a non-inverted frame sync (TCR4[FSP] = 0 and RCR4[FSP] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

All timing shown is also with respect to input signal transitions of 3 ns and a 50 pF maximum load.

Table 58. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time • OD mode • SD mode • MD mode	20 25 28.6	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	40	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	8.4	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	1	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	10	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	1	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK • P2 and P3 • P1	14 15.6	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

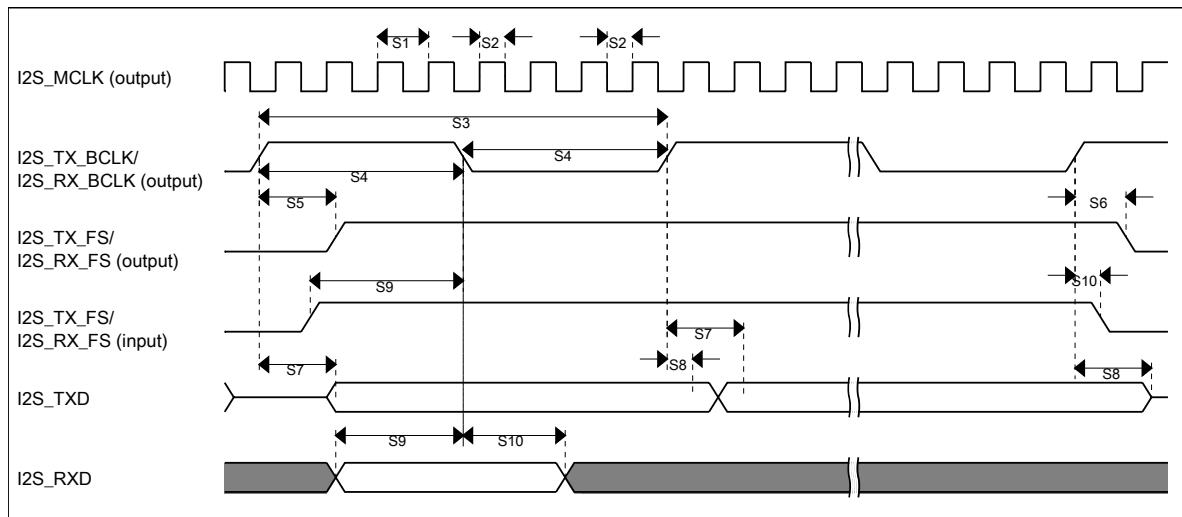


Figure 25. I2S/SAI timing — master modes

Table 59. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) • OD mode • SD mode • MD mode	40 50 50	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	6	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	20	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	-1.5	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	6	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion for I2S_TXD output valid ¹	—	25	ns

1. Applies to first in each frame and only if the TCR4[FSE] bit is clear

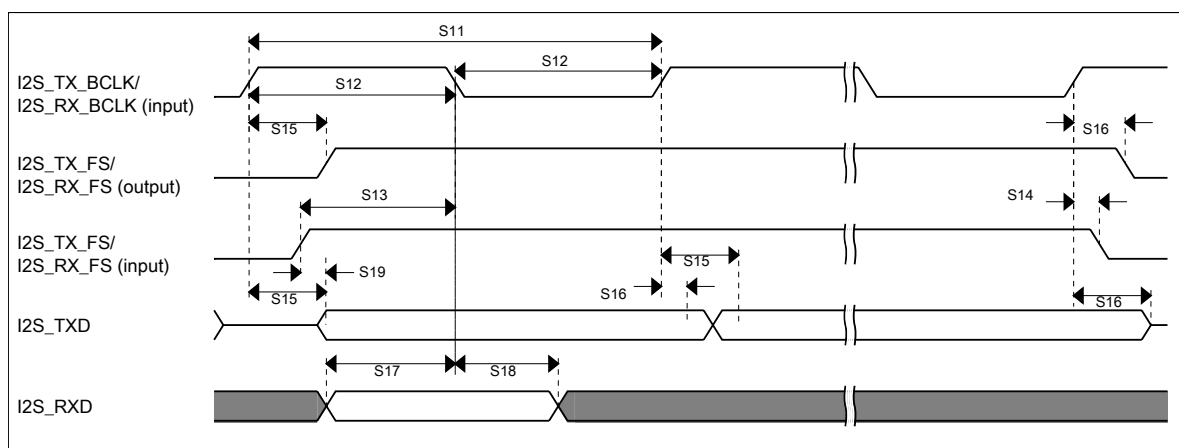


Figure 26. I2S/SAI timing — slave modes

4.6.8 Flexible IO controller (FlexIO)

Table 60. FlexIO Timing Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
t _{ODS}	Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle	0		8	ns	¹

Table continues on the next page...

Table 60. FlexIO Timing Specifications ...continued

Symbol	Description	Min	Typ	Max	Unit	Notes
t _{IDS}	Input delay skew between any two FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle	0		8	ns	¹

1. Assumes pins muxed on same VDD_Px domain with same load

4.7 Human Machine Interface (HMI) modules

4.7.1 Microphone (MIC)

The PDM microphones must meet the setup and hold timing requirements shown in Table 61 and Figure 27. The "k" factor value in Table 61 depends on the selected quality mode as shown in Table 62 .

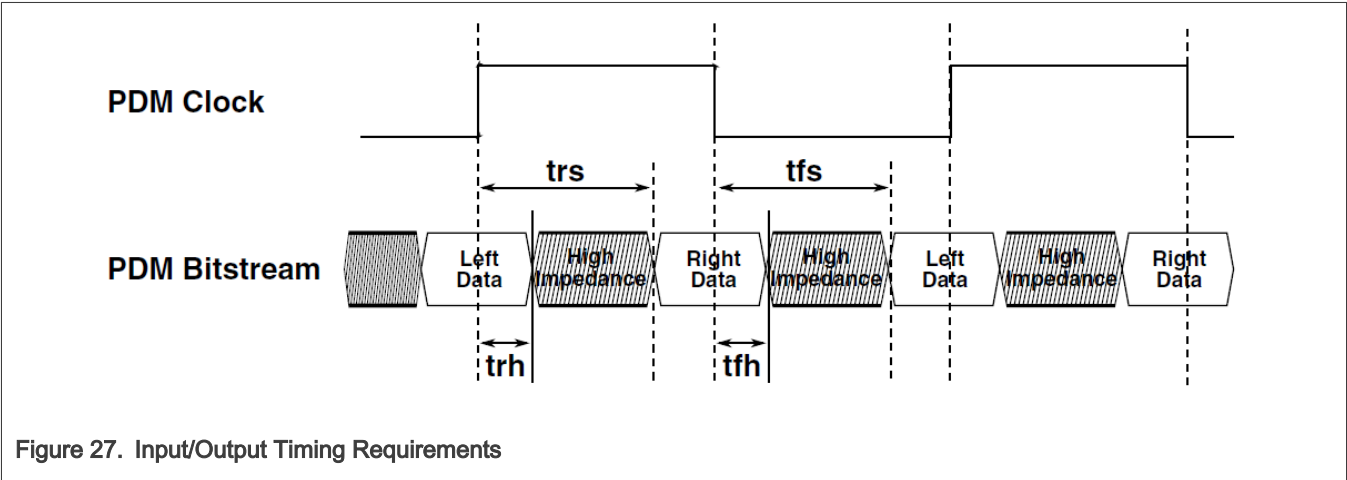
Table 61. Timing Parameters

Parameter	Value
trs, tfs	$\leq [\text{floor}(K \times \text{CLKDIV}) - 1] / [\text{functional clock rate}]^1$
trh, tfh	≥ 0

1. Depending on K value, the user must make sure $\text{floor}(K \times \text{CLKDIV}) > 1$ to avoid timing problems

Table 62. K factor value

Quality mode	K factor
High Quality	1/2
Medium Quality, Very Low Quality 0	1
Low Quality, Very Low Quality 1	2
Very Low Quality 2	4



4.7.2 General Purpose Input/Output (GPIO)

See [General switching specifications](#).

4.8 Security modules

4.8.1 Tamper

Table 63. Tamper electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
	Tamper pin VBAT operating voltage	1.613	--	3.848	V	
	Tamper pin operating temperature	-64	--	143	°C	1
	Temperature Tamper Detect assertion					1
	• low temperature detect	-64	-50	-38	°C	
	• high temperature detect	128	135	143	°C	
	Temperature Tamper No flag range	-37		125	°C	1
	Temperature tamper detect VBAT operating voltage	1.613	--	3.848	V	
	Low Voltage Detect Threshold	1.613	1.656	1.698	V	
	High Voltage Detect Threshold	3.65	3.75	3.848	V	
	Voltage Tamper Detect operational temperature					1
	• no false alarms	-38		125	°C	
	• with possible false alarms	-64		143	°C	
	Clock tamper detect assertion	Refer to VBAT chapter in SRM				
	Clock tamper detect VBAT operating voltage	1.613	--	3.848	V	
	Clock tamper detect operating temperature	-64	--	143	°C	1

1. Temperature specifications in this table are all for junction temperature.

5 Package dimensions

5.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [nxp.com](https://www.nxp.com) and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
VFBGA184	98ASA01888D
HLQFP100	98ASA02131D
HDQFP172	98ASA01107D

6 Pinout

6.1 MCXN23x Signal Multiplexing and Pin Assignments

The signal multiplexing and pin assignments are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.
2. Double-click on the Excel file to open it.
3. Select the MCXN23x_Pinmux tab.

The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

However, pinout table is also given below:

Table 64. Pinmux Assignments

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
P1_8	A1	172	1	ALT0 - P1_8 ALT1 - TRACE_DATA0 ALT2 - FC4_P0 ALT3 - FC5_P4 ALT4 - CT_INP8 ALT6 - FLEXIO0_D16 ALT7 - SmartDMA_PIO4 ALT10 - I3C1_SDA	IO Supply - VDD Pad type - MED+I2C+I3C Default - DIS	ISP - UART_RXD ANALOG - ADC1_A8 VDD SYS - WUU0_IN10/LPTMR1_ALT3
P1_9	B1	1	2	ALT0 - P1_9 ALT1 - TRACE_DATA1 ALT2 - FC4_P1 ALT3 - FC5_P5 ALT4 - CT_INP9 ALT6 - FLEXIO0_D17 ALT7 - SmartDMA_PIO5 ALT10 - I3C1_SCL	IO Supply - VDD Pad type - MED+I2C Default - DIS	ISP - UART_TXD ANALOG - ADC1_A9
P1_10	C3	2	3	ALT0 - P1_10 ALT1 - TRACE_DATA2 ALT2 - FC4_P2 ALT3 - FC5_P6 ALT4 - CT2_MAT0 ALT6 - FLEXIO0_D18 ALT7 - SmartDMA_PIO6 ALT11 - CAN0_TXD	IO Supply - VDD Pad type - MED Default - DIS	ISP - CAN_TXD ANALOG - ADC1_A10
P1_11	D3	3	4	ALT0 - P1_11 ALT1 - TRACE_DATA3 ALT2 - FC4_P3	IO Supply - VDD Pad type - MED Default - DIS	ISP - CAN_RXD ANALOG - ADC1_A11 VDD SYS - WUU0_IN11

Table continues on the next page...

Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT4 - CT2_MAT1 ALT6 - FLEXIO0_D19 ALT7 - SmartDMA_PIO7 ALT10 - I3C1_PUR ALT11 - CAN0_RXD		
P1_12	D2	4	5	ALT0 - P1_12 ALT1 - TRACE_CLK ALT2 - FC4_P4 ALT3 - FC3_P0 ALT4 - CT2_MAT2 ALT6 - FLEXIO0_D20 ALT7 - SmartDMA_PIO8 ALT11 - CAN1_RXD	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC1_A12 VDD SYS - WUU0_IN12
P1_13	D1	5	6	ALT0 - P1_13 ALT1 - TRIG_IN3 ALT2 - FC4_P5 ALT3 - FC3_P1 ALT4 - CT2_MAT3 ALT6 - FLEXIO0_D21 ALT7 - SmartDMA_PIO9 ALT11 - CAN1_TXD	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC1_A13
P1_14	D4	6	7	ALT0 - P1_14 ALT2 - FC4_P6 ALT3 - FC3_P2 ALT4 - CT_INP10 ALT6 - FLEXIO0_D22 ALT7 - SmartDMA_PIO10	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC1_A14
P1_15	E4	7	8	ALT0 - P1_15 ALT3 - FC3_P3 ALT4 - CT_INP11 ALT6 - FLEXIO0_D23 ALT7 - SmartDMA_PIO11 ALT10 - I3C1_PUR	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC1_A15 VDD SYS - WUU0_IN13
P1_16	F6	8	--	ALT0 - P1_16 ALT2 - FC5_P0 ALT3 - FC3_P4	IO Supply - VDD Pad type - MED+I2C+I3C Default - DIS	ANALOG - ADC1_A16 VDD SYS - WUU0_IN14

Table continues on the next page...

Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT4 - CT_INP12 ALT6 - FLEXIO0_D24 ALT7 - SmartDMA_PIO12 ALT10 - I3C1_SDA		
P1_17	F4	9	--	ALT0 - P1_17 ALT2 - FC5_P1 ALT3 - FC3_P5 ALT4 - CT_INP13 ALT6 - FLEXIO0_D25 ALT7 - SmartDMA_PIO13 ALT10 - I3C1_SCL	IO Supply - VDD Pad type - MED+I2C Default - DIS	ANALOG - ADC1_A17
P1_18	G4	10	--	ALT0 - P1_18 ALT1 - FREQME_CLK_IN0 ALT2 - FC5_P2 ALT3 - FC3_P6 ALT4 - CT3_MAT0 ALT6 - FLEXIO0_D26 ALT7 - SmartDMA_PIO14 ALT11 - CAN0_TXD	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC1_A18
P1_19	G5	11	--	ALT0 - P1_19 ALT1 - FREQME_CLK_IN1 ALT2 - FC5_P3 ALT4 - CT3_MAT1 ALT6 - FLEXIO0_D27 ALT7 - SmartDMA_PIO15 ALT11 - CAN0_RXD	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC1_A19 VDD SYS - WUU0_IN15
RESET_B	F3	12	9		IO Supply - VDD Pad type - RST Default - RESET_B	
P1_30	F1	13	10	ALT0 - P1_30 ALT1 - TRIG_OUT3 ALT4 - CT_INP16 ALT10 - SAI0_MCLK	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - XTAL48M
P1_31	F2	14	11	ALT0 - P1_31 ALT1 - TRIG_IN4 ALT4 - CT_INP17	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - EXTAL48M

Table continues on the next page...

Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
VSS	D6,E5,G2,H5,	15	0		IO Supply - VDD	
VDD_CORE	K10,L11	16	12		IO Supply - VDD	
VDD_LDO_CORE	K6	17	13		IO Supply - VDD	ANALOG - VDD_LDO_CORE
VDD	G7,H6,H8,	18	13		IO Supply - VDD	
VDD_P2	K8,L7	19	13		IO Supply - VDD_P2	
VSS	D6,E5,G2,H5,	--	0		IO Supply - VDD_P2	
P2_0	H2	20	14	ALT0 - P2_0 ALT1 - TRIG_IN5 ALT5 - PWM1_A3 ALT6 - FLEXIO0_D8 ALT7 - SmartDMA_PIO20 ALT10 - SAI0_RX_BCLK	IO Supply - VDD_P2 Pad type - FAST Default - DIS	
P2_1	H1	21	15	ALT0 - P2_1 ALT1 - TRACE_CLK ALT5 - PWM1_B3 ALT6 - FLEXIO0_D9 ALT7 - SmartDMA_PIO21 ALT10 - SAI0_RX_FS	IO Supply - VDD_P2 Pad type - FAST Default - DIS	
P2_2	H3	22	16	ALT0 - P2_2 ALT1 - CLKOUT ALT5 - PWM1_A2 ALT6 - FLEXIO0_D10 ALT7 - SmartDMA_PIO22 ALT10 - SAI0_TXD0	IO Supply - VDD_P2 Pad type - FAST Default - DIS	VDD SYS - WUU0_IN16
P2_3	J3	23	17	ALT0 - P2_3 ALT5 - PWM1_B2 ALT6 - FLEXIO0_D11 ALT7 - SmartDMA_PIO23 ALT10 - SAI0_RXD0	IO Supply - VDD_P2 Pad type - FAST Default - DIS	
P2_4	K3	24	18	ALT0 - P2_4 ALT5 - PWM1_A1 ALT6 - FLEXIO0_D12 ALT7 - SmartDMA_PIO24 ALT10 - SAI0_RXD1	IO Supply - VDD_P2 Pad type - FAST Default - DIS	VDD SYS - WUU0_IN17

Table continues on the next page...

Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
P2_5	K1	25	19	ALT0 - P2_5 ALT1 - TRIG_OUT3 ALT5 - PWM1_B1 ALT6 - FLEXIO0_D13 ALT7 - SmartDMA_PIO25 ALT10 - SAI0_TXD1	IO Supply - VDD_P2 Pad type - FAST Default - DIS	
NONE	--	26	--		IO Supply - VDD_P2	
NONE	--	27	--		IO Supply - VDD_P2	
P2_6	K2	28	20	ALT0 - P2_6 ALT1 - TRIG_IN4 ALT5 - PWM1_A0 ALT6 - FLEXIO0_D14 ALT7 - SmartDMA_PIO26 ALT10 - SAI0_TX_BCLK	IO Supply - VDD_P2 Pad type - FAST Default - DIS	
P2_7	L2	29	21	ALT0 - P2_7 ALT1 - TRIG_IN5 ALT5 - PWM1_B0 ALT6 - FLEXIO0_D15 ALT7 - SmartDMA_PIO27 ALT10 - SAI0_TX_FS	IO Supply - VDD_P2 Pad type - FAST Default - DIS	
P2_8	M2	30	--	ALT0 - P2_8 ALT1 - TRACE_DATA0 ALT5 - PWM1_X0 ALT6 - FLEXIO0_D16 ALT7 - SmartDMA_PIO28 ALT10 - SAI1_TXD0	IO Supply - VDD_P2 Pad type - FAST Default - DIS	
P2_9	M1	31	--	ALT0 - P2_9 ALT1 - TRACE_DATA1 ALT5 - PWM1_X1 ALT6 - FLEXIO0_D17 ALT7 - SmartDMA_PIO29 ALT10 - SAI1_RXD0	IO Supply - VDD_P2 Pad type - FAST Default - DIS	
P2_10	M3	32	--	ALT0 - P2_10 ALT1 - TRACE_DATA2 ALT5 - PWM1_X2 ALT6 - FLEXIO0_D18	IO Supply - VDD_P2 Pad type - FAST Default - DIS	

Table continues on the next page...

Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT7 - SmartDMA_PIO31 ALT10 - SAI1_RXD1		
P2_11	N4	33	--	ALT0 - P2_11 ALT1 - TRACE_DATA3 ALT5 - PWM1_X3 ALT6 - FLEXIO0_D19 ALT7 - SmartDMA_PIO30 ALT10 - SAI1_TXD1	IO Supply - VDD_P2 Pad type - FAST Default - DIS	
VSS	D6,E5,G2,H5,	34	0		IO Supply - VDD_P2	
VDD_P2	K8,L7	35	--		IO Supply - VDD_P2	
VDD_P4	N5,P4,	36	--		IO Supply - VDD_P4	
VSS_P4	P6,P7,P9,	37	--		IO Supply - VDD_P4	
P4_0	P1	38	22	ALT0 - P4_0 ALT1 - TRIG_IN6 ALT2 - FC2_P0 ALT4 - CT_INP16 ALT7 - SmartDMA_PIO24	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC0_A0 VDD SYS - WUU0_IN18
NONE	--	39	--			
NONE	--	40	--			
P4_1	P2	41	23	ALT0 - P4_1 ALT1 - TRIG_IN7 ALT2 - FC2_P1 ALT4 - CT_INP17 ALT7 - SmartDMA_PIO25	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC0_B0
P4_2	T1	42	24	ALT0 - P4_2 ALT1 - TRIG_IN6 ALT2 - FC2_P2 ALT4 - CT_INP12 ALT7 - SmartDMA_PIO26	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC0_A4/ADC1_A4/ CMP0_IN4N/CMP1_IN4N
P4_3	U1	43	25	ALT0 - P4_3 ALT1 - TRIG_IN7 ALT2 - FC2_P3 ALT4 - CT_INP13 ALT7 - SmartDMA_PIO27	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC0_B4/ADC1_B4/ CMP0_IN5N/CMP1_IN5N VDD SYS - WUU0_IN19

Table continues on the next page...

Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
P4_4	M6	44	26	ALT0 - P4_4 ALT2 - FC2_P4 ALT4 - CT_INP14 ALT7 - SmartDMA_PIO28	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC1_A0
NONE	--	45	--			
NONE	--	46	--			
P4_5	M8	47	27	ALT0 - P4_5 ALT2 - FC2_P5 ALT4 - CT_INP15 ALT7 - SmartDMA_PIO29	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC1_B0
NONE	--	48	--			
P4_6	N7	49	28	ALT0 - P4_6 ALT1 - TRIG_OUT4 ALT2 - FC2_P6 ALT4 - CT_INP18 ALT7 - SmartDMA_PIO30	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC0_A3/ADC1_A3
P4_7	T4	50	--	ALT0 - P4_7 ALT4 - CT_INP19 ALT7 - SmartDMA_PIO31	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	
ANA_7	U4	51	--		IO Supply - VDD_P4 Pad type - ANA	ANALOG - VREFI/VREFO/ ADC0_A7/ADC1_A7
P4_7/ANA_7	--	--	29	ALT0 - P4_7 ALT4 - CT_INP19 ALT7 - SmartDMA_PIO31	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - VREFI/VREFO/ ADC0_A7/ADC1_A7
VDD_ANA	R4	52	30		IO Supply - VDD_P4	
VREFH	R5	53	31		IO Supply - VDD_P4	ANALOG - VREFH
VREFL	R6	54	32		IO Supply - VDD_P4	ANALOG - VREFL
VSS_P4	P6,P7,P9,	55	33		IO Supply - VDD_P4	
VDD_P4	N5,P4,	56	34		IO Supply - VDD_P4	
P4_12	T6	57	35	ALT0 - P4_12 ALT2 - FC2_P0 ALT4 - CT4_MAT0 ALT6 - FLEXIO0_D20 ALT11 - CAN0_RXD	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC0_A5/ADC1_A5 VDD SYS - WUU0_IN20

Table continues on the next page...

Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
P4_13	T7	58	36	ALT0 - P4_13 ALT1 - TRIG_IN8 ALT2 - FC2_P1 ALT3 - USB1_OTGn_ID ALT4 - CT4_MAT1 ALT6 - FLEXIO0_D21 ALT11 - CAN0_TXD	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC0_B5/ADC1_B5
NONE	--	59	--			
P4_14	N8	60	--	ALT0 - P4_14 ALT4 - CT4_MAT2 ALT6 - FLEXIO0_D22	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	
P4_15	T8	61	37	ALT0 - P4_15 ALT1 - TRIG_OUT4 ALT3 - USB1_Vbusvalid_EXT ALT4 - CT4_MAT3 ALT6 - FLEXIO0_D23 ALT11 - CAN1_RXD	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC0_A1/CMP0_IN4P VDD SYS - WUU0_IN21
P4_16	R8	62	38	ALT0 - P4_16 ALT2 - FC2_P2 ALT3 - USB1_OTGn_PWR ALT4 - CT3_MAT0 ALT6 - FLEXIO0_D24 ALT11 - CAN1_TXD	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC0_A6
P4_17	R9	63	39	ALT0 - P4_17 ALT1 - TRIG_IN9 ALT2 - FC2_P3 ALT3 - USB1_OTGn_OC ALT4 - CT3_MAT1 ALT6 - FLEXIO0_D25	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC0_B6
NONE	--	64	--			
P4_18	N10	65	--	ALT0 - P4_18 ALT4 - CT3_MAT2 ALT6 - FLEXIO0_D26	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	
P4_19	R10	66	--	ALT0 - P4_19 ALT1 - TRIG_OUT5	IO Supply - VDD_P4 Pad type - SLOW	ANALOG - ADC0_B1/CMP1_IN4P

Table continues on the next page...

Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT4 - CT3_MAT3 ALT6 - FLEXIO0_D27	Default - DIS	
P4_20	T10	67	--	ALT0 - P4_20 ALT1 - TRIG_IN8 ALT2 - FC2_P4 ALT4 - CT2_MAT0 ALT6 - FLEXIO0_D28	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC1_A6
P4_21	T11	68	--	ALT0 - P4_21 ALT1 - TRIG_IN9 ALT2 - FC2_P5 ALT4 - CT2_MAT1 ALT6 - FLEXIO0_D29	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC1_B6
NONE	--	69	--			
P4_22	T12	70	--	ALT0 - P4_22 ALT4 - CT2_MAT2 ALT6 - FLEXIO0_D30	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	
P4_23	U12	71	--	ALT0 - P4_23 ALT1 - TRIG_OUT5 ALT2 - FC2_P6 ALT4 - CT2_MAT3 ALT6 - FLEXIO0_D31	IO Supply - VDD_P4 Pad type - SLOW Default - DIS	ANALOG - ADC0_A2/ ADC0_B2/ADC1_B3
VSS_P4	P6,P7,P9,	72	--		IO Supply - VDD_P4	
VDD_P4	N5,P4,	73	--		IO Supply - VDD_P4	
VSS	J4,J8,	--	0		IO Supply - VDD_USB	
USB1_DP	R13	74	40		IO Supply - VDD_USB Pad type - ANA	ANALOG - USB1_DP
USB1_DM	R14	75	41		IO Supply - VDD_USB Pad type - ANA	ANALOG - USB1_DM
USB1_ID	P11	--	--		IO Supply - VDD_USB Pad type - ANA	ANALOG - USB1_ID
USB1_VBUS	U14	76	42		IO Supply - VDD_USB Pad type - VDDINT_5V	ANALOG - USB1_VBUS
VSS	J4,J8,	77	43		IO Supply - VDD_USB	
VDD_USB	R12	78	44		IO Supply - VDD_USB	

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Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
NONE	--	79	45			
NONE	--	80	46			
VSS	J4,J8,	81	0		IO Supply - VDD_BAT	
VDD_BAT	T17	82	47		IO Supply - VDD_BAT	
P5_0	U16	83	48	ALT0 - P5_0 ALT1 - TRIG_IN10 ALT2 - LPTMR0_ALT2	IO Supply - VDD_BAT Pad type - AON Default - DIS	ANALOG - EXTAL32K/ADC1_B8
P5_1	U17	84	49	ALT0 - P5_1 ALT1 - TRIG_OUT6 ALT2 - LPTMR1_ALT2	IO Supply - VDD_BAT Pad type - AON Default - DIS	ANALOG - XTAL32K/ADC1_B9
P5_2	M10	85	50	ALT0 - P5_2 ALT1 - VBAT_WAKEUP_b ALT2 - SPC_LPREQ ALT3 - TAMPER0	IO Supply - VDD_BAT Pad type - RST Default - ALT1	ANALOG - ADC1_B10
P5_3	N11	86	51	ALT0 - P5_3 ALT1 - TRIG_IN11 ALT2 - RTC_CLKOUT ALT3 - TAMPER1	IO Supply - VDD_BAT Pad type - AON Default - DIS	ANALOG - ADC1_B11
P5_4	M12	87	--	ALT0 - P5_4 ALT1 - TRIG_OUT7 ALT2 - SPC_LPREQ ALT3 - TAMPER2	IO Supply - VDD_BAT Pad type - AON Default - DIS	ANALOG - ADC1_B12
P5_5	K12	88	--	ALT0 - P5_5 ALT1 - TRIG_IN10 ALT2 - LPTMR0_ALT2 ALT3 - TAMPER3	IO Supply - VDD_BAT Pad type - AON Default - DIS	ANALOG - ADC1_B13
P5_6	K13	89	--	ALT0 - P5_6 ALT1 - TRIG_OUT6 ALT2 - LPTMR1_ALT2 ALT3 - TAMPER4	IO Supply - VDD_BAT Pad type - AON Default - DIS	ANALOG - ADC1_B14
P5_7	L13	90	--	ALT0 - P5_7 ALT1 - TRIG_IN11 ALT3 - TAMPER5	IO Supply - VDD_BAT Pad type - AON Default - DIS	ANALOG - ADC1_B15
NONE	--	91	--			

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Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
NONE	--	92	--			
VSS	J10,J14,K9,N13,P12,P14,T16,	--	--		IO Supply - VDD_BAT	
VDD_BAT	T17	--	--		IO Supply - VDD_BAT	
VSS_DCDC	P16	93,94	52		IO Supply - VDD_DCDC	
DCDC_LX	P17	95,96	53		IO Supply - VDD_DCDC	ANALOG - DCDC_LX
VDD_DCDC	R15	97	54		IO Supply - VDD_DCDC	
VDD_LDO_SYS	P15	98	54		IO Supply - VDD_P3	
VDD_SYS	N14	99	55		IO Supply - VDD_P3	
VSS	J10,J14,K9,N13,P12,P14,T16,	--	0		IO Supply - VDD_P3	
P3_23	M15	100	--	ALT0 - P3_23 ALT3 - FC6_P3 ALT4 - CT_INP11 ALT5 - PWM1_X3 ALT6 - FLEXIO0_D31 ALT7 - SmartDMA_PIO23 ALT10 - SAI1_TXD1	IO Supply - VDD_P3 Pad type - FAST Default - DIS	
P3_22	M16	101	--	ALT0 - P3_22 ALT3 - FC6_P2 ALT4 - CT_INP10 ALT5 - PWM1_X2 ALT6 - FLEXIO0_D30 ALT7 - SmartDMA_PIO22 ALT10 - SAI1_RXD1	IO Supply - VDD_P3 Pad type - FAST Default - DIS	
P3_21	L16	102	56	ALT0 - P3_21 ALT1 - TRIG_OUT1 ALT3 - FC6_P1 ALT4 - CT2_MAT3 ALT5 - PWM1_B3 ALT6 - FLEXIO0_D29 ALT7 - SmartDMA_PIO21 ALT10 - SAI1_RXD0	IO Supply - VDD_P3 Pad type - FAST Default - DIS	
P3_20	M17	103	57	ALT0 - P3_20 ALT1 - TRIG_OUT0	IO Supply - VDD_P3 Pad type - FAST	VDD SYS - WUU0_IN27

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Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT3 - FC6_P0 ALT4 - CT2_MAT2 ALT5 - PWM1_A3 ALT6 - FLEXIO0_D28 ALT7 - SmartDMA_PIO20 ALT10 - SAI1_TXD0	Default - DIS	
VSS	J10,J14,K9,N13,P12,P14,T16,	104	0		IO Supply - VDD_P3	
VDD_CORE	K10,L11	105	58		IO Supply - VDD_P3	
VDD_P3	G11,H10,H12	106	59		IO Supply - VDD_P3	
P3_18	K16	--	--	ALT0 - P3_18 ALT3 - FC6_P6 ALT4 - CT2_MAT0 ALT5 - PWM1_X0 ALT6 - FLEXIO0_D26 ALT7 - SmartDMA_PIO18 ALT10 - SAI1_RX_BCLK	IO Supply - VDD_P3 Pad type - FAST Default - DIS	
P3_17	K15	107	60	ALT0 - P3_17 ALT4 - CT_INP9 ALT5 - PWM1_B2 ALT6 - FLEXIO0_D25 ALT7 - SmartDMA_PIO17 ALT10 - SAI1_TX_FS	IO Supply - VDD_P3 Pad type - FAST Default - DIS	VDD SYS - WUU0_IN26
P3_16	J15	108	61	ALT0 - P3_16 ALT4 - CT_INP8 ALT5 - PWM1_A2 ALT6 - FLEXIO0_D24 ALT7 - SmartDMA_PIO16 ALT10 - SAI1_TX_BCLK	IO Supply - VDD_P3 Pad type - FAST Default - DIS	
P3_15	H15	109	62	ALT0 - P3_15 ALT4 - CT_INP7 ALT5 - PWM1_B1 ALT6 - FLEXIO0_D23 ALT7 - SmartDMA_PIO15 ALT10 - SAI0_RX_FS	IO Supply - VDD_P3 Pad type - FAST Default - DIS	
P3_14	H17	110	63	ALT0 - P3_14	IO Supply - VDD_P3	VDD SYS - WUU0_IN25

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Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT4 - CT_INP6 ALT5 - PWM1_A1 ALT6 - FLEXIO0_D22 ALT7 - SmartDMA_PIO14 ALT10 - SAI0_RX_BCLK	Pad type - FAST Default - DIS	
P3_13	H16	111	64	ALT0 - P3_13 ALT2 - FC7_P5 ALT3 - FC6_P5 ALT4 - CT1_MAT3 ALT5 - PWM1_B0 ALT6 - FLEXIO0_D21 ALT7 - SmartDMA_PIO13 ALT10 - SAI0_TXD1	IO Supply - VDD_P3 Pad type - FAST Default - DIS	
P3_12	G16	112	65	ALT0 - P3_12 ALT2 - FC7_P4 ALT3 - FC6_P4 ALT4 - CT1_MAT2 ALT5 - PWM1_A0 ALT6 - FLEXIO0_D20 ALT7 - SmartDMA_PIO12 ALT10 - SAI0_RXD1	IO Supply - VDD_P3 Pad type - FAST Default - DIS	
VSS	J10,J14,K9,N13,P12,P14,T16,	113	0		IO Supply - VDD_P3	
VDD_P3	G11,H10,H12	114	66		IO Supply - VDD_P3	
P3_11	F16	115	67	ALT0 - P3_11 ALT2 - FC6_P3 ALT3 - FC7_P5 ALT4 - CT1_MAT1 ALT5 - PWM0_B3 ALT6 - FLEXIO0_D19 ALT7 - SmartDMA_PIO11 ALT10 - SAI0_RXD0	IO Supply - VDD_P3 Pad type - FAST Default - DIS	VDD SYS - WUU0_IN24
P3_10	F17	116	68	ALT0 - P3_10 ALT2 - FC6_P2 ALT3 - FC7_P4 ALT4 - CT1_MAT0	IO Supply - VDD_P3 Pad type - FAST Default - DIS	

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Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT5 - PWM0_A3 ALT6 - FLEXIO0_D18 ALT7 - SmartDMA_PIO10 ALT10 - SAI0_TXD0		
P3_9	F15	117	69	ALT0 - P3_9 ALT2 - FC6_P5 ALT3 - FC7_P2 ALT4 - CT_INP5 ALT5 - PWM0_B2 ALT6 - FLEXIO0_D17 ALT7 - SmartDMA_PIO9 ALT10 - SAI0_TX_FS	IO Supply - VDD_P3 Pad type - FAST Default - DIS	
P3_8	E14	118	70	ALT0 - P3_8 ALT2 - FC6_P4 ALT3 - FC7_P0 ALT4 - CT_INP4 ALT5 - PWM0_A2 ALT6 - FLEXIO0_D16 ALT7 - SmartDMA_PIO8 ALT10 - SAI0_TX_BCLK	IO Supply - VDD_P3 Pad type - FAST Default - DIS	VDD SYS - WUU0_IN23
P3_7	D14	119	71	ALT0 - P3_7 ALT2 - FC6_P6 ALT3 - FC7_P1 ALT4 - CT4_MAT3 ALT5 - PWM0_B1 ALT6 - FLEXIO0_D15 ALT7 - SmartDMA_PIO7 ALT10 - SAI0_MCLK	IO Supply - VDD_P3 Pad type - FAST Default - DIS	
P3_6	D17	120	72	ALT0 - P3_6 ALT1 - CLKOUT ALT2 - FC6_P1 ALT4 - CT4_MAT2 ALT5 - PWM0_A1 ALT6 - FLEXIO0_D14 ALT7 - SmartDMA_PIO6 ALT10 - SAI1_MCLK	IO Supply - VDD_P3 Pad type - FAST Default - DIS	

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Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
VSS	J10,J14,K9,N13,P12,P14,T16,	121	0		IO Supply - VDD_P3	
VDD_P3	G11,H10,H12	122	73		IO Supply - VDD_P3	
NONE	--	123	--			
NONE	--	124	--			
NONE	--	125	--			
P3_2	D15	126	--	ALT0 - P3_2 ALT2 - FC7_P0 ALT4 - CT4_MAT0 ALT5 - PWM0_X0 ALT6 - FLEXIO0_D10 ALT7 - SmartDMA_PIO2	IO Supply - VDD_P3 Pad type - FAST Default - DIS	
P3_1	C15	127	74	ALT0 - P3_1 ALT1 - TRIG_IN1 ALT2 - FC6_P0 ALT3 - FC7_P6 ALT4 - CT_INP17 ALT5 - PWM0_B0 ALT6 - FLEXIO0_D9 ALT7 - SmartDMA_PIO1	IO Supply - VDD_P3 Pad type - FAST Default - DIS	
P3_0	B17	128	75	ALT0 - P3_0 ALT1 - TRIG_IN0 ALT3 - FC7_P3 ALT4 - CT_INP16 ALT5 - PWM0_A0 ALT6 - FLEXIO0_D8 ALT7 - SmartDMA_PIO0	IO Supply - VDD_P3 Pad type - FAST Default - DIS	VDD SYS - WUU0_IN22
VSS	J10,J14,K9,N13,P12,P14,T16,	--	--		IO Supply - VDD_P3	
VDD_P3	G11,H10,H12	129	--		IO Supply - VDD_P3	
VDD	G7,H6,H8,	130	--		IO Supply - VDD	
VSS	D9,D12,E13,H9,H13,	131	--		IO Supply - VDD	
P0_0	A17	132	76	ALT0 - P0_0 ALT1 - TMS/SWDIO	IO Supply - VDD Pad type - MED	

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Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT2 - FC1_P0 ALT4 - CT_INP0	Default - ALT1	
P0_1	A16	133	77	ALT0 - P0_1 ALT1 - TCLK/SWCLK ALT2 - FC1_P1 ALT4 - CT_INP1	IO Supply - VDD Pad type - MED Default - ALT1	
P0_2	B16	134	78	ALT0 - P0_2 ALT1 - TDO/SWO ALT2 - FC1_P2 ALT4 - CT0_MAT0 ALT5 - UTICK_CAP0 ALT10 - I3C0_PUR	IO Supply - VDD Pad type - MED Default - ALT1	
P0_3	B15	135	79	ALT0 - P0_3 ALT1 - TDI ALT2 - FC1_P3 ALT4 - CT0_MAT1 ALT5 - UTICK_CAP1 ALT8 - HSCMP0_OUT	IO Supply - VDD Pad type - MED Default - ALT1	ANALOG - CMP1_IN1
P0_4	B14	136	80	ALT0 - P0_4 ALT1 - EWM0_IN ALT2 - FC0_P0 ALT3 - FC1_P4 ALT4 - CT0_MAT2 ALT5 - UTICK_CAP2 ALT8 - HSCMP1_OUT ALT9 - PDM0_CLK	IO Supply - VDD Pad type - MED+I2C Default - DIS	VDD SYS - WUU0_IN0
P0_5	A14	137	81	ALT0 - P0_5 ALT1 - EWM0_OUT_b ALT2 - FC0_P1 ALT3 - FC1_P5 ALT4 - CT0_MAT3 ALT5 - UTICK_CAP3 ALT9 - PDM0_DATA0	IO Supply - VDD Pad type - MED+I2C Default - DIS	
P0_6	C14	138	82	ALT0 - P0_6 ALT1 - ISPMODE_N ALT2 - FC0_P2	IO Supply - VDD Pad type - MED Default - ALT1	ISP - ISPMODE_N

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Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT3 - FC1_P6 ALT4 - CT_INP2 ALT9 - PDM0_DATA1		
P0_7	C13	139	--	ALT0 - P0_7 ALT2 - FC0_P3 ALT4 - CT_INP3	IO Supply - VDD Pad type - MED Default - DIS	VDD SYS - WUU0_IN1
NONE	--	140	--			
NONE	--	141	--			
NONE	--	142	--			
NONE	--	143	--			
VDD	G7,H6,H8,	144	83		IO Supply - VDD	
VSS	D9,D12,E13,H9,H13,	145	0		IO Supply - VDD	
NONE	--	146	--		IO Supply - VDD	
NONE	--	147	--		IO Supply - VDD	
P0_14	E11	148	--	ALT0 - P0_14 ALT2 - FC1_P6 ALT3 - FC0_P2 ALT4 - CT_INP2 ALT5 - UTICK_CAP0 ALT6 - FLEXIO0_D6	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_B14
P0_15	G13	149	--	ALT0 - P0_15 ALT3 - FC0_P3 ALT4 - CT_INP3 ALT5 - UTICK_CAP1 ALT6 - FLEXIO0_D7	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_B15
P0_16	B10	150	84	ALT0 - P0_16 ALT2 - FC0_P0 ALT4 - CT0_MAT0 ALT5 - UTICK_CAP2 ALT6 - FLEXIO0_D0 ALT9 - PDM0_CLK ALT10 - I3C0_SDA	IO Supply - VDD Pad type - MED+I2C+I3C Default - DIS	ISP - I2C_SDA ANALOG - ADC0_A8 VDD SYS - WUU0_IN2
P0_17	A10	151	85	ALT0 - P0_17 ALT2 - FC0_P1	IO Supply - VDD Pad type - MED+I2C	ISP - I2C_SCL

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Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT4 - CT0_MAT1 ALT5 - UTICK_CAP3 ALT6 - FLEXIO0_D1 ALT9 - PDM0_DATA0 ALT10 - I3C0_SCL	Default - DIS	ANALOG - ADC0_A9
P0_18	C10	152	86	ALT0 - P0_18 ALT1 - EWM0_IN ALT2 - FC0_P2 ALT4 - CT0_MAT2 ALT6 - FLEXIO0_D2 ALT8 - HSCMP0_OUT ALT9 - PDM0_DATA1	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_A10
P0_19	C9	153	87	ALT0 - P0_19 ALT1 - EWM0_OUT_b ALT2 - FC0_P3 ALT4 - CT0_MAT3 ALT6 - FLEXIO0_D3 ALT8 - HSCMP1_OUT	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_A11 VDD SYS - WUU0_IN3
P0_20	C8	154	88	ALT0 - P0_20 ALT2 - FC0_P4 ALT3 - FC1_P0 ALT4 - CT_INP0 ALT6 - FLEXIO0_D4 ALT10 - I3C0_SDA	IO Supply - VDD Pad type - MED+I2C+I3C Default - DIS	ANALOG - ADC0_A12 VDD SYS - WUU0_IN4
P0_21	A8	155	89	ALT0 - P0_21 ALT2 - FC0_P5 ALT3 - FC1_P1 ALT4 - CT_INP1 ALT6 - FLEXIO0_D5 ALT10 - I3C0_SCL	IO Supply - VDD Pad type - MED+I2C Default - DIS	ANALOG - ADC0_A13
P0_22	B8	156	90	ALT0 - P0_22 ALT1 - EWM0_IN ALT2 - FC0_P6 ALT3 - FC1_P2 ALT4 - CT_INP2 ALT6 - FLEXIO0_D6	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_A14/CMP1_IN2

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Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT10 - I3C0_PUR		
P0_23	B7	157	91	ALT0 - P0_23 ALT1 - EWM0_OUT_b ALT3 - FC1_P3 ALT4 - CT_INP3 ALT6 - FLEXIO0_D7	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_A15 VDD SYS - WUU0_IN5
VSS	D9,D12,E13,H9,H13,	--	--		IO Supply - VDD	
P0_24	B6	158	--	ALT0 - P0_24 ALT2 - FC1_P0 ALT4 - CT0_MAT0	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_B16
P0_25	A6	159	--	ALT0 - P0_25 ALT2 - FC1_P1 ALT4 - CT0_MAT1	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_B17
P0_26	F10	160	--	ALT0 - P0_26 ALT2 - FC1_P2 ALT4 - CT0_MAT2	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_B18
P0_27	E10	161	--	ALT0 - P0_27 ALT2 - FC1_P3 ALT4 - CT0_MAT3	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_B19
P0_28	E8	--	--	ALT0 - P0_28 ALT2 - FC1_P4 ALT3 - FC0_P4 ALT4 - CT_INP0	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_B20
P0_29	F8	--	--	ALT0 - P0_29 ALT2 - FC1_P5 ALT3 - FC0_P5 ALT4 - CT_INP1	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_B21
P1_0	C6	162	92	ALT0 - P1_0 ALT1 - TRIG_IN0 ALT2 - FC3_P0 ALT3 - FC4_P4 ALT4 - CT_INP4 ALT6 - FLEXIO0_D8 ALT10 - SAI1_TX_BCLK	IO Supply - VDD Pad type - MED+I2C Default - DIS	ISP - SPI_SDO ANALOG - ADC0_A16/CMP0_IN0 VDD SYS - WUU0_IN6/LPTMR0_ALT3

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Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
P1_1	C5	163	93	ALT0 - P1_1 ALT1 - TRIG_IN1 ALT2 - FC3_P1 ALT3 - FC4_P5 ALT4 - CT_INP5 ALT6 - FLEXIO0_D9 ALT10 - SAI1_TX_FS	IO Supply - VDD Pad type - MED+I2C Default - DIS	ISP - SPI_SCK ANALOG - ADC0_A17/CMP1_IN0
P1_2	C4	164	94	ALT0 - P1_2 ALT1 - TRIG_OUT0 ALT2 - FC3_P2 ALT3 - FC4_P6 ALT4 - CT1_MAT0 ALT6 - FLEXIO0_D10 ALT10 - SAI1_TXD0 ALT11 - CAN0_TXD	IO Supply - VDD Pad type - MED Default - DIS	ISP - SPI_SDI ANALOG - ADC0_A18
P1_3	B4	165	95	ALT0 - P1_3 ALT1 - TRIG_OUT1 ALT2 - FC3_P3 ALT4 - CT1_MAT1 ALT6 - FLEXIO0_D11 ALT10 - SAI1_RXD0 ALT11 - CAN0_RXD	IO Supply - VDD Pad type - MED Default - DIS	ISP - SPI_PCS ANALOG - ADC0_A19/CMP0_IN1 VDD SYS - WUU0_IN7
VDD	G7,H6,H8,	166	96		IO Supply - VDD	
VSS	D9,D12,E13,H9,H13,	167	0		IO Supply - VDD	
P1_4	A4	168	97	ALT0 - P1_4 ALT1 - FREQME_CLK_IN0 ALT2 - FC3_P4 ALT3 - FC5_P0 ALT4 - CT1_MAT2 ALT6 - FLEXIO0_D12 ALT7 - SmartDMA_PIO0 ALT10 - SAI0_TXD1	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_A20/CMP0_IN2 VDD SYS - WUU0_IN8
P1_5	B3	169	98	ALT0 - P1_5 ALT1 - FREQME_CLK_IN1 ALT2 - FC3_P5	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_A21/CMP0_IN3

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Table 64. Pinmux Assignments...continued

Pin Name	184BGA Ball	172HDQFP ALL	100HLQFP	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT3 - FC5_P1 ALT4 - CT1_MAT3 ALT6 - FLEXIO0_D13 ALT7 - SmartDMA_PIO1 ALT10 - SAI0_RXD1		
P1_6	B2	170	99	ALT0 - P1_6 ALT1 - TRIG_IN2 ALT2 - FC3_P6 ALT3 - FC5_P2 ALT4 - CT_INP6 ALT6 - FLEXIO0_D14 ALT7 - SmartDMA_PIO2 ALT10 - SAI1_RX_BCLK ALT11 - CAN1_TXD	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_A22
P1_7	A2	171	100	ALT0 - P1_7 ALT1 - TRIG_OUT2 ALT3 - FC5_P3 ALT4 - CT_INP7 ALT6 - FLEXIO0_D15 ALT7 - SmartDMA_PIO3 ALT10 - SAI1_RX_FS ALT11 - CAN1_RXD	IO Supply - VDD Pad type - MED Default - DIS	ANALOG - ADC0_A23 VDD SYS - WUU0_IN9

Note: Pin 54 is double bonded with VDD_DCDC/VDD_LDO_SYS on HLQFP100 package, when VDD_CORE is generated by LDO_CORE and DCDC_CORE is disabled, Pin 54 still needs to be powered to supply VDD_LDO_SYS to generate VDD_SYS.

Note: HLQFP pin 0 is the thermal pad on the bottom of the package and must be connected to GND.

Note:

1. For BGA package, all balls with same name are shorted together on BGA package.
2. VSS_ANA and VSS_P4 are shorted together on package.
3. +I3C in Pad Type represents strong pull up resistor is implemented on the pin. PV bit is implemented in the Pin Control register of the pin.
4. +I2C in Pad Type represents I2C filter is implemented on the pin. PFE bit is implemented in the Pin Control register of the pin
5. DIS in default column means the pin's input buffer is disabled by default
6. AON and RST pads support passive filter. PFE bit is implemented in the Pin Control register of the pin
7. PE, PS, SRE, ODE and DSE are supported in the Pin Control register of all types of IO.

6.2 MCXN23x Pinout Diagrams

The pinout diagrams are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.
2. Double-click on the Excel file to open it.
3. Select the respective package tab.

Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, refer to the MCXN23x_Pinmux tab in the Excel file.

6.3 Recommended connection for unused analog and digital pins

Table 65 shows the recommended connections for pins if those pins are not used in the customer's application

Table 65. Recommended connection for unused interfaces

Pin Type	Pin Function	Recommendation	Comments
Power	VDD_LDO_CORE	Connect to VDD_CORE	When the LDO_CORE is bypassed, the input VDD_LDO_CORE and output VOUT_CORE/ VDD_CORE should be connected together, and tied to the output from DCDC_CORE. The regulator should also be disabled in software.
Power	VDD_CORE	Connect to VDD_LDO_CORE	When the LDO_CORE is bypassed, the input VDD_LDO_CORE and output VOUT_CORE/ VDD_CORE should be connected together, and tied to the output from DCDC_CORE. The regulator should also be disabled in software.
Power	VDD_LDO_SYS	Connect to VDD_SYS	When the LDO_SYS is bypassed, the input VDD_LDO_SYS and output VDD_SYS should be connected together and tied to an external supply. The regulator should also be disabled in software.
Power	VDD_DCDC	Ground	When the DCDC is not used, the input VDD_DCDC should be tied to VSS through a 10 kΩ resistor.
Power	DCDC_LX	Float/Ground	For package where VDD_DCDC has an independent pin, connect VDD_DCDC and DCDC_LX to VSS with a 10 kΩ resistor. For package where VDD_DCDC and VDD_LDO_SYS share a package pin, DCDC_LX must be floating. The DCDC should be disabled in software.
Power	VDD_SYS/VOUT_SYS	Must be powered	VDD_SYS is used to power parts of the system power controller (SPC) and must be powered to use the chip. If LDO_SYS is not being used, then tie VDD_LDO_SYS to VDD_SYS/VOUT_SYS and supply power from an external source. The regulator should also be disabled in software.
Power	VDD	Must be powered	VDD powers the mux logic for PORT 0, PORT 1, and PORT 2. It must be powered during POR. The recommendation is to keep it powered, but it can be connected to the output of the Smart

Table continues on the next page...

Table 65. Recommended connection for unused interfaces...continued

Pin Type	Pin Function	Recommendation	Comments
			Power Switch and be left floating in shelf storage mode.
Power	VDD_ANA	Float	
Power	VDD_USB	Tie to ground through a 10 kΩ resistor if VDD_USB is an independent pin in the package version used	
Power	VREFH	Always connect to VDD_ANA potential	Always connect to VDD_ANA potential
Power	VREFL	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_ANA	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_DCDC	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_USB	Always connect to VSS potential	Always connect to VSS potential
Analog/non-GPIO	ADC _n _x	Float	
Analog/non-GPIO	VREF_OUT	Float	Analog output - Float
Analog/non-GPIO	TAMPERx	Float	
Analog/non-GPIO	VBAT_WAKEUP_b	Float	
Analog/non-GPIO	RTC_CLKOUT	Float	
Analog/non-GPIO	EXTAL32K	Float	
Analog/non-GPIO	XTAL32K	Float	Analog output - Float
Analog/non-GPIO	EXTAL_32M	Float	
Analog/non-GPIO	XTAL_32M	Float	Analog output - Float
Analog/non-GPIO	USB1_DP	Float	Float
Analog/non-GPIO	USB1_DM	Float	Float
Analog/non-GPIO	USB1_VBUS	Float	
Analog/non-GPIO	USB1_ID	Float	
GPIO/Analog	Px/ADC _n _x	Float	Float (default is analog input)
GPIO/Analog	Px/CMP _n _IN _x	Float	Float (default is analog input)
GPIO/Digital	P0_1/JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	P0_3/JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	P0_2/JTAG_TDO	Float	Float (default is JTAG with pullup)

Table continues on the next page...

Table 65. Recommended connection for unused interfaces...continued

Pin Type	Pin Function	Recommendation	Comments
GPIO/Digital	P0_0/JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	Px	Float	Float (default is disabled)

7 Ordering parts

7.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [nxp.com](https://www.nxp.com) and perform a part number search for the following device numbers:MCXN236VDFT

NOTE

For complete list of Orderable part numbers, please refer [Table 1](#)

8 Part identification

Part numbers for the device have fields that identify the specific part. Use the values of these fields to determine the specific part.

8.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

8.2 Part number format

Part numbers for this device have the following format:

Q B PS F T PG PT

Table 66. Part number fields descriptions

Field	Description	Values
Q	Qualification Status	- P = Prequalification - Blank = Fully qualified, general market flow
B	Brand	MCX
PS	Product series name	N
F	Family	23x
T	Junction Temperature range (°C)	V = -40 to 125
PG	Package	- KL = 100 HLQFP (14 x 14 x 1 mm, 0.5 mm pitch) - DF = 184 VFBGA (9 x 9 x 0.85 mm, 0.5 mm pitch)

Table continues on the next page...

Table 66. Part number fields descriptions...continued

Field	Description	Values
		PB = 172 HDQFP (16 x 16 x 1.65 mm, 0.65 mm pitch)
PT	Package Type	- R = Tape and Reel - T = Tray

8.3 Example

This is an example part number:

MCXN236VDFT

8.4 Package marking

8.4.1 Package marking information

VFBGA and HLQFP packages have the following top-side marking:

- First line: NXP logo
- Second line: Part number, minus the package extension info (ex. part# = PMCXN236VDFT, marking = PMCXN236V)
- Third line: Lot Information: (assembly site + wafer/diffusion lot + assembly lot)
- Fourth line: Trace Code: (year + work week)
- Fifth line: Mask set

Table 67. VFBGA and HLQFP Package marking

Identifier
(O)
PMCXNxxxV
AWLZ
YYWW
MMMMM

HDQFP package has the following top-side marking:

- First line: NXP logo
- Second line: Part number, minus the package extension info (ex. part# = PMCXN236VPBT, marking = PMCXN236V)
- Third line: Mask set
- Fourth line: assembly site + wafer/diffusion lot + Trace Code (year + work week) + assembly lot

Table 68. Package marking HDQFP

Identifier
(O)
PMCXNxxxV

Table continues on the next page...

Table 68. Package marking HDQFP ...continued

Identifier
MMMMM
AAWLYYWWZZ

9 Terminology and guidelines

9.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • <i>Operating ratings</i> apply during operation of the chip. • <i>Handling ratings</i> apply when the chip is not powered. NOTE The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions NOTE Typical values are provided as design guidelines and are neither tested nor guaranteed.

9.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	−0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a typical value:

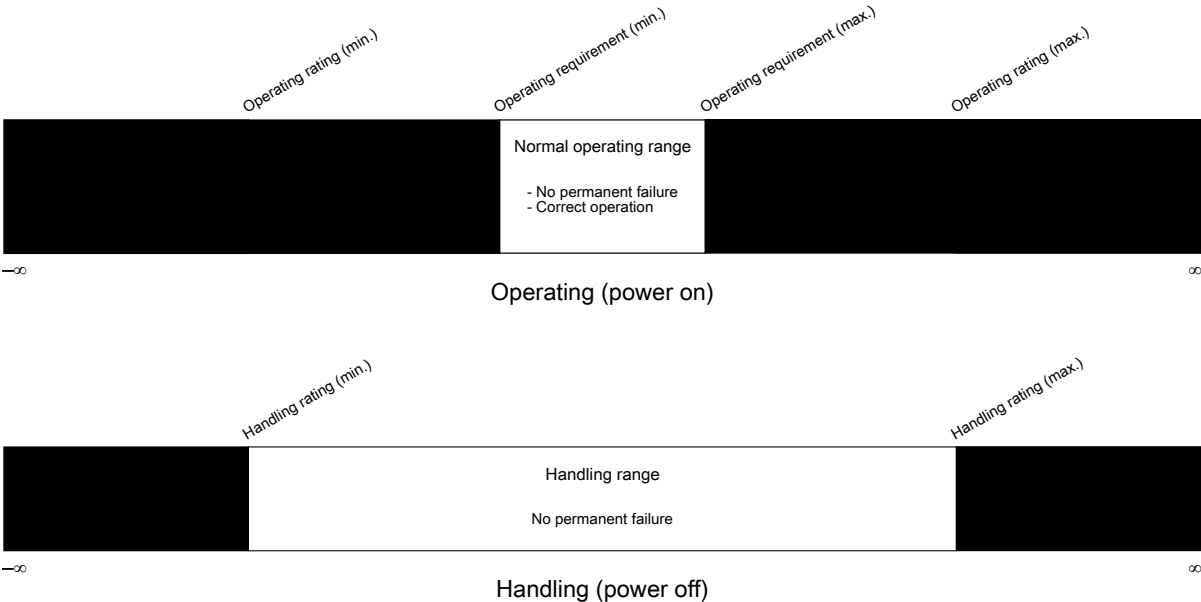
Symbol	Description	Min.	Typ.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

9.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	°C
V _{DD}	Supply voltage	3.3	V

9.4 Relationship between ratings and operating requirements



9.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

10 Revision History

The following table provides a revision history for this document.

Table 69. Revision History

Document ID.	Release Date	Substantial Changes
MCXN23x v.3.0	21 Jan 2025	• Added HDQFP172 package details. • Updated notes in Feature Comparison • Updated Table 66. • Updated Table 64. • Updated Power Consumption Operating Behaviors . • Added table VBAT supply POR operating requirements in HVD, LVD, and POR operating requirements. • Updated clock names "FRO-144M" to "FRO144M", "FRO-12M" to "FRO12M", "FRO-16K" to "FRO16K". • Updated Feature Comparison .

Table continues on the next page...

Table 69. Revision History

Rev. No.	Date	Substantial Changes
		• Removed "IDD_VBAT_TAMPER" from Power Consumption Operating Behaviors . • Added a footnote in ordering Information table "Devices with prefix "P"...". • Added V_REFH and V_REFL entries in Voltage and current maximum ratings • Updated Table 63 in Tamper. • Updated Package marking information. • Updated Thermal attributes. • Updated Pinout table. Added note to pin 54
MCXN23x v.2.0		Initial Release

Legal information

Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

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Date of release: 21 January 2025
Document identifier: MCXN23x