ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	BT1308-400D,412
Manufacturer:	NXP USA Inc.
Package:	TO-92-3
Availability:	Please confirm with sales

Product Page:

https://antrexco.com/product/details/nxp-usa-inc/bt1308-400d-412.html

Request a Quote:

Submit RFQ for this part

Scan for product page

Contact Information

Email: info@antrexco.com

WhatsApp: +86-186-8066-5326

Website: https://antrexco.com

Quality & Trust

New & Original Components

Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

Secure sourcing support for OEM / EMS projects

Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

BT1308 series D

Triacs logic level

Rev. 01 — 26 February 2008 Product data sheet

1. Product profile

1.1 General description

Passivated sensitive gate triacs in a SOT54 plastic package

1.2 Features

- Sensitive gate
- Direct interfacing to logic level ICs
- Gate triggering in four quadrants
- Direct interfacing to low-power gate drive circuits

1.3 Applications

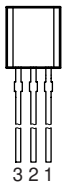
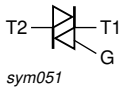
- General purpose switching and phase control
- Low-power AC fan speed control

1.4 Quick reference data

- $V_{DRM} \leq 400$ V (BT1308-400D)
- $V_{DRM} \leq 600$ V (BT1308-600D)
- $I_{TSM} \leq 9$ A (t = 20 ms)
- $I_{GT} \leq 5$ mA
- $I_{GT} \leq 7$ mA (T2– G+)
- $I_{T(RMS)} \leq 0.8$ A

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	main terminal 2 (T2)	 SOT54 (TO-92)	 sym051
2	gate (G)		
3	main terminal 1 (T1)		

3. Ordering information

Table 2. Ordering information

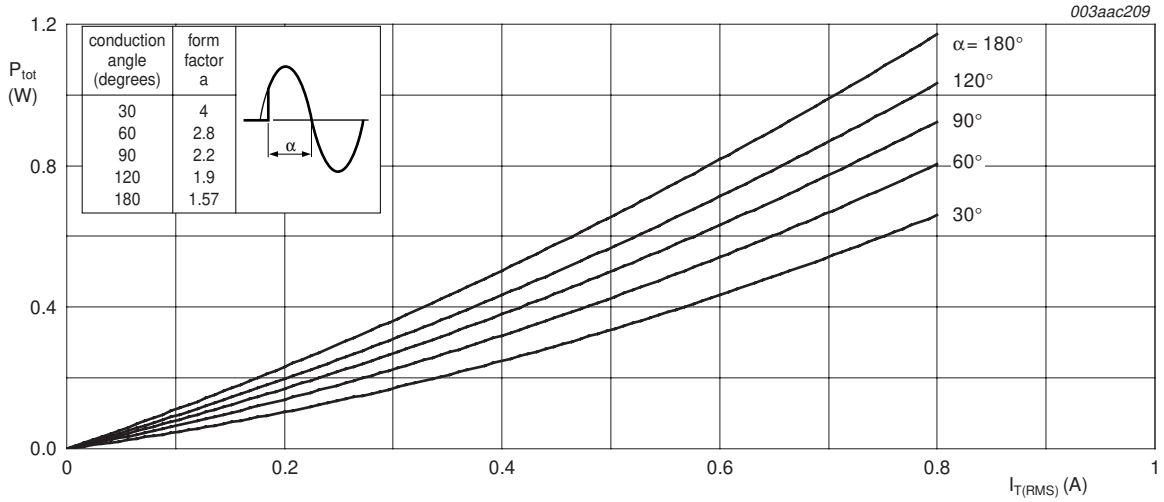
Type number	Package		
	Name	Description	Version
BT1308-400D	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54
BT1308-600D			

4. Limiting values

Table 3. Limiting values

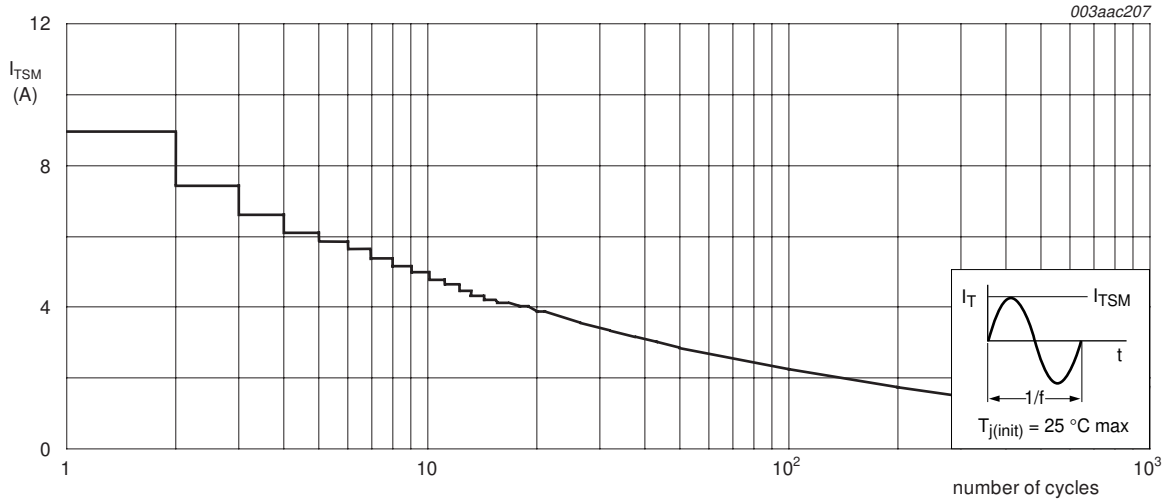
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage	BT1308-400D	-	400	V
		BT1308-600D	-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 55$ °C; see Figure 4 and 5	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_j = 25$ °C prior to surge; see Figure 2 and 3			
		t = 20 ms	-	9	A
		t = 16.7 ms	-	10	A
I^2t	I^2t for fusing	$t_p = 10$ ms	-	0.32	A^2s
dI_T/dt	rate of rise of on-state current	$I_{TM} = 1$ A; $I_G = 20$ mA; $dI_G/dt = 0.2$ A/µs			
		T2+ G+	-	50	A/µs
		T2+ G–	-	50	A/µs
		T2– G–	-	50	A/µs
		T2– G+	-	10	A/µs
I_{GM}	peak gate current		-	1	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		–40	+150	°C
T_j	junction temperature		-	125	°C



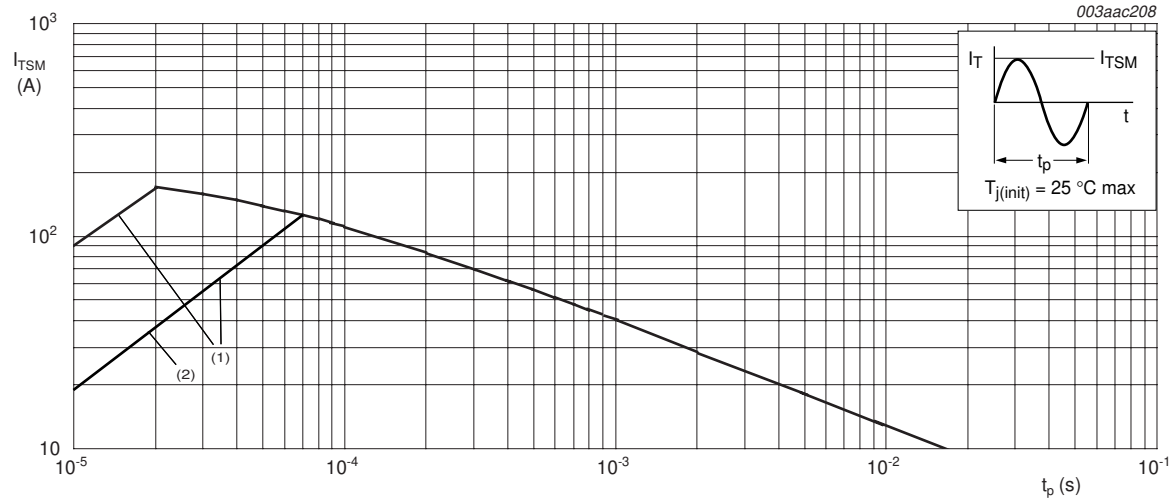
α = conduction angle

Fig 1. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

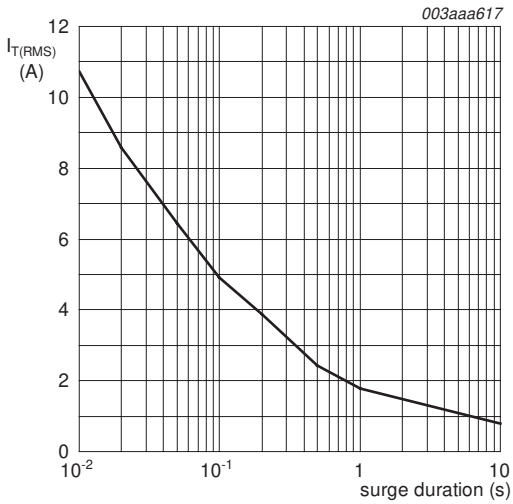


$t_p \leq 20$ ms

(1) dI_T/dt limit

(2) T2– G+ quadrant limit

Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values



f = 50 Hz

T_{lead} = 55 °C

Fig 4. RMS on-state current as a function of surge duration; maximum values

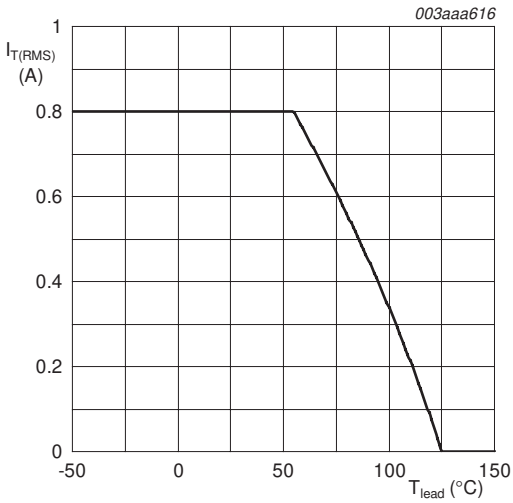


Fig 5. RMS on-state current as a function of lead temperature; maximum values

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}lead)}$	thermal resistance from junction to lead	full cycle	-	-	60	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	full cycle; printed-circuit board mounted; lead length 4 mm; see Figure 6	-	150	-	K/W

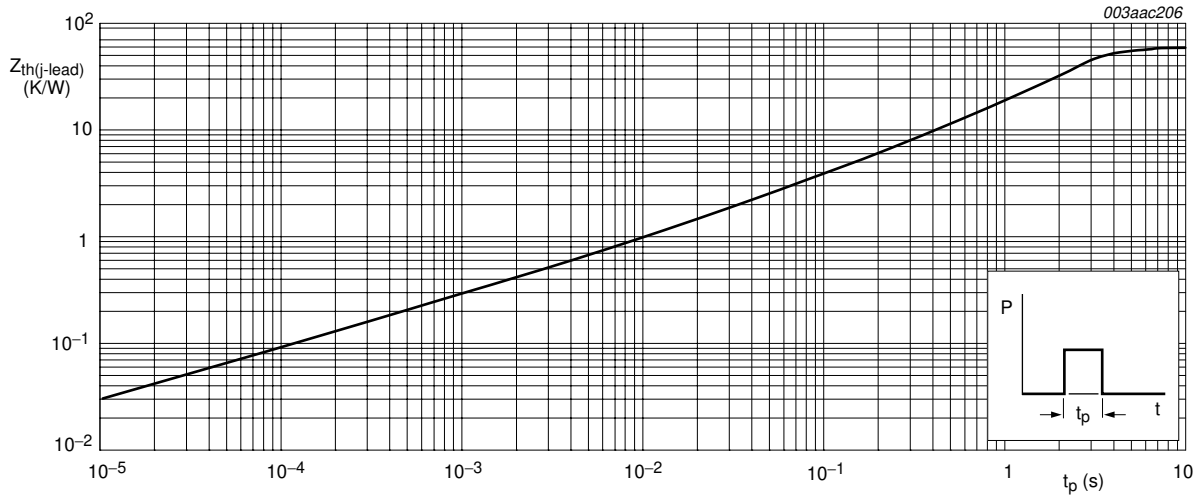


Fig 6. Transient thermal impedance from junction to solder point as a function of pulse width

6. Characteristics

Table 5. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; see Figure 8				
		T2+ G+	-	1	5	mA
		T2+ G–	-	2	5	mA
		T2– G–	-	2	5	mA
		T2– G+	-	4	7	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; see Figure 10				
		T2+ G+	-	1	10	mA
		T2+ G–	-	5	10	mA
		T2– G–	-	1	10	mA
		T2– G+	-	2	10	mA
I_H	holding current	V_D = 12 V; I_G = 0.1 A; see Figure 11	-	1	10	mA
V_T	on-state voltage	I_T = 0.85 A; see Figure 9	-	1.35	1.6	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; see Figure 7	-	0.9	2	V
		$V_D = V_{DRM}$; I_T = 0.1 A; T_j = 110 °C	0.1	0.7	-	V
I_D	off-state current	$V_D = V_{DRM(max)}$; T_j = 125 °C	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 0.67 \times V_{DRM(max)}$; T_j = 110 °C; exponential waveform; gate open circuit	30	45	-	V/µs
dV_{com}/dt	rate of change of commutating voltage	$V_{DM} = V_{DRM(max)}$; T_j = 50 °C; I_{TM} = 0.84 A; dI_{com}/dt = 0.3 A/ms	-	5	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 1 A; $V_D = V_{DRM(max)}$; I_G = 25 mA; dI_G/dt = 5 A/µs	-	2	-	µs

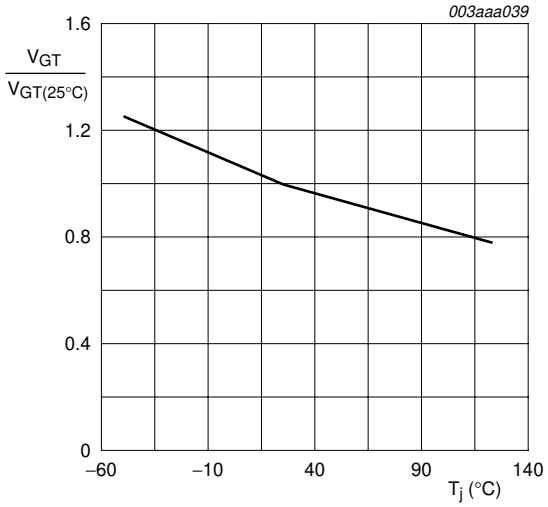
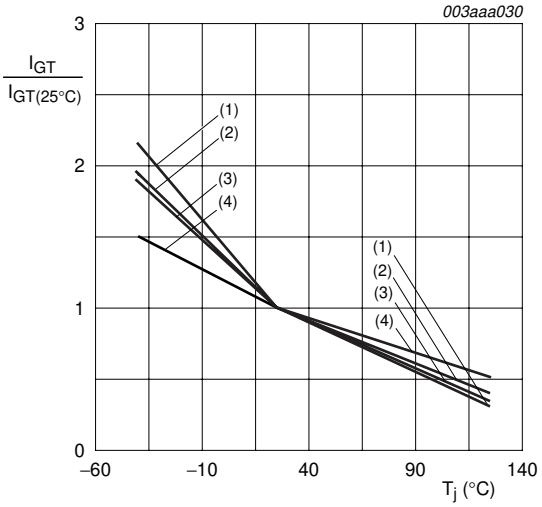
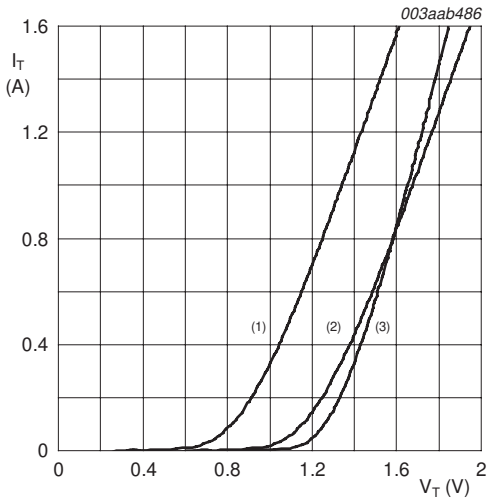


Fig 7. Normalized gate trigger voltage as a function of junction temperature



(1) T2+ G+
(2) T2− G+
(3) T2− G−
(4) T2+ G−

Fig 8. Normalized gate trigger current as a function of junction temperature



V_o = 1.171 V

R_s = 0.5125 Ω

(1) T_j = 125 °C; typical values

(2) T_j = 125 °C; maximum values

(3) T_j = 25 °C; maximum values

Fig 9. On-state current as a function of on-state voltage

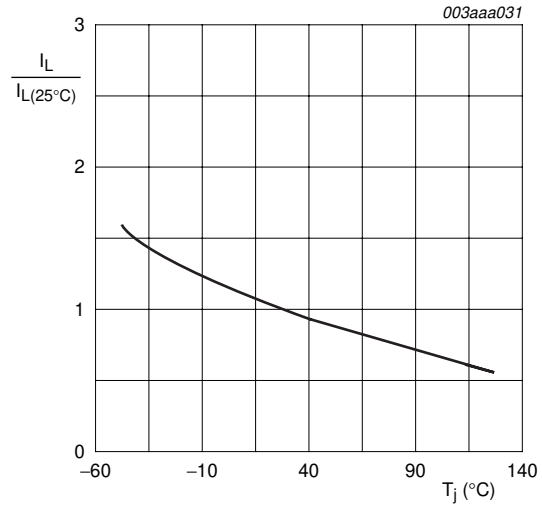


Fig 10. Normalized latching current as a function of junction temperature

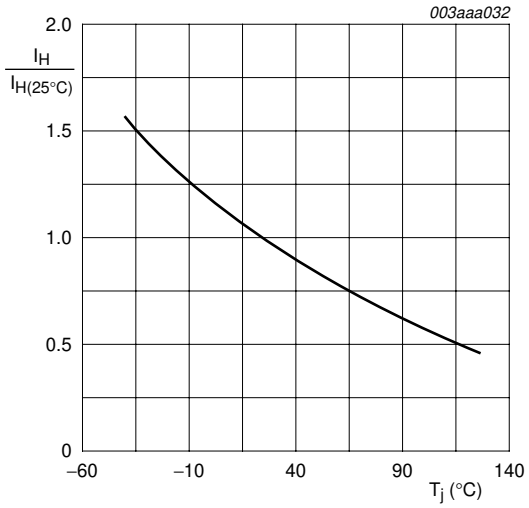
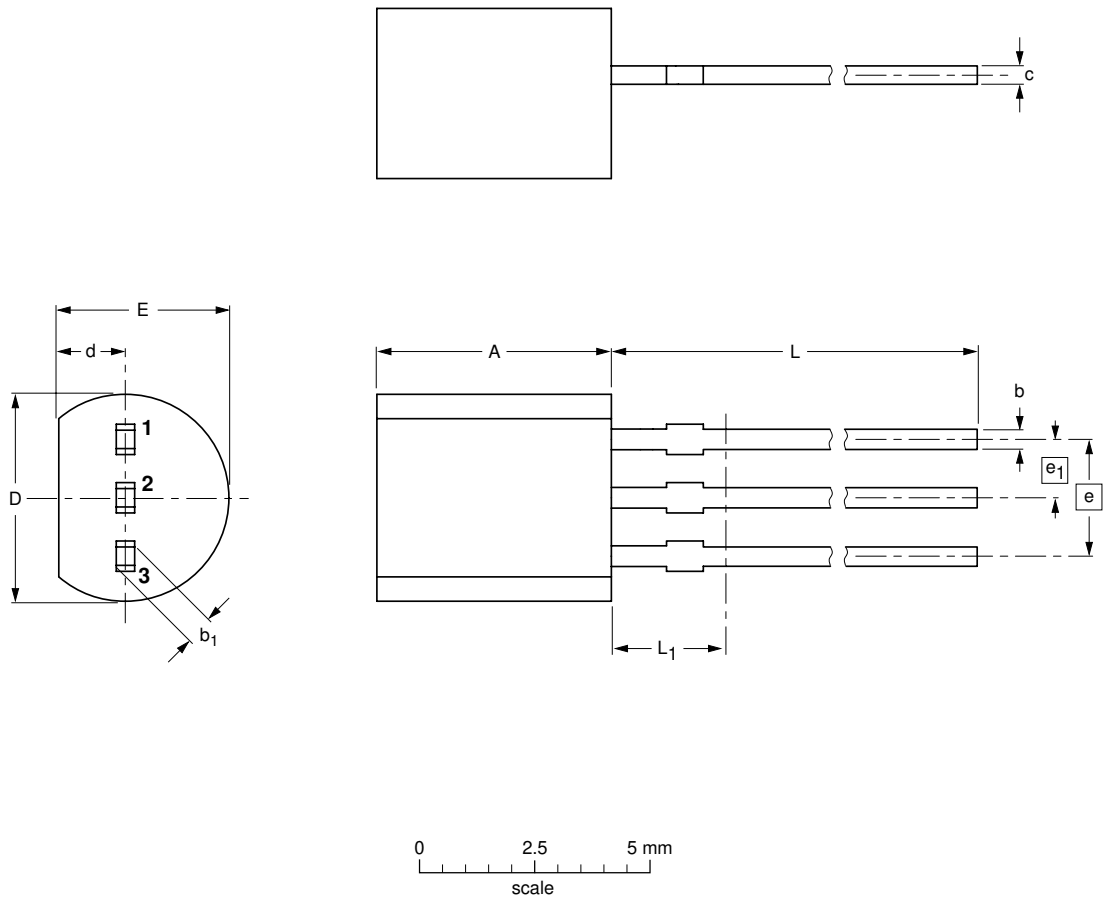


Fig 11. Normalized holding current as a function of junction temperature

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~04-06-28~~ 04-11-16

Fig 12. Package outline SOT54 (TO-92)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BT1308_SER_D_1	20080226	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

9.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

9.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

10. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

11. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 26 February 2008

Document identifier: BT1308_SER_D_1