

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	BF1201R,215
Manufacturer:	NXP USA Inc.
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nxp-usa-inc/bf1201r-215.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

DATA SHEET

BF1201; BF1201R; BF1201WR N-channel dual-gate PoLo MOS-FETs

Product specification
Supersedes data of 1999 Dec 01

2000 Mar 29



N-channel dual-gate PoLo MOS-FETs

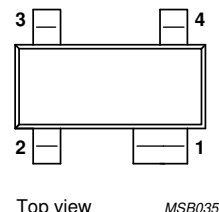
BF1201; BF1201R; BF1201WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier
- Partly internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



BF1201R marking code: LBp

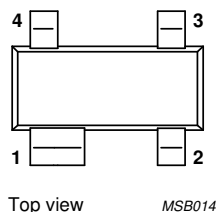
Fig.2 Simplified outline (SOT143R).

APPLICATIONS

- VHF and UHF applications with 3 to 9 V supply voltage, such as digital and analogue television tuners and professional communications equipment.

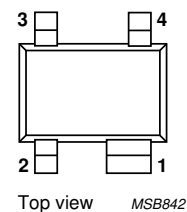
DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1201, BF1201R and BF1201WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.



BF1201 marking code: LAp.

Fig.1 Simplified outline (SOT143B).



BF1201WR marking code: LA

Fig.3 Simplified outline (SOT343R).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	10	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	200	mW
$ y_{fs} $	forward transfer admittance		23	28	35	mS
C_{ig1-ss}	input capacitance at gate 1		–	2.6	3.1	pF
C_{rss}	reverse transfer capacitance	$f = 1 \text{ MHz}$	–	15	30	fF
F	noise figure	$f = 400 \text{ MHz}$	–	1	1.8	dB
X_{mod}	cross-modulation	input level for $k = 1\%$ at 40 dB AGC	105	–	–	dB μ V
T_j	operating junction temperature		–	–	150	°C

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling.

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

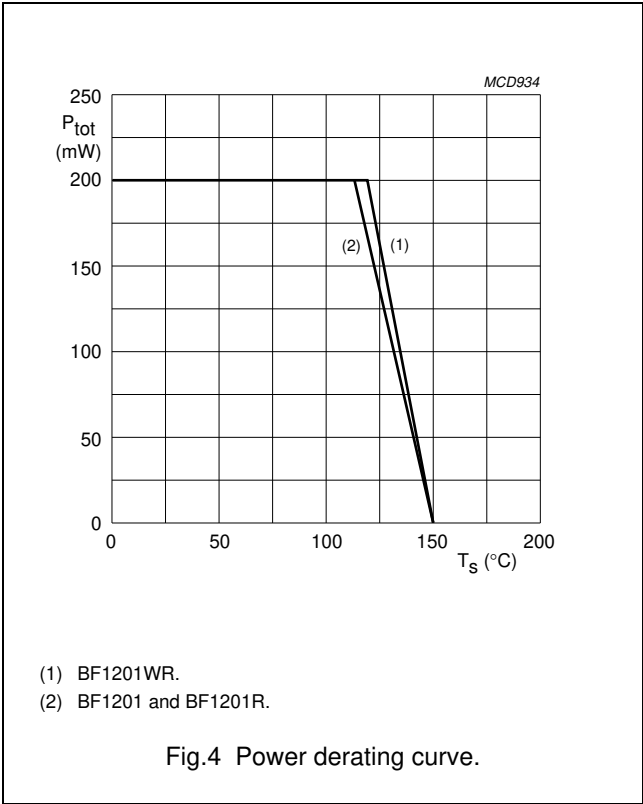
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage		–	10	V
I _D	drain current (DC)		–	30	mA
I _{G1}	gate 1 current		–	±10	mA
I _{G2}	gate 2 current		–	±10	mA
P _{tot}	total power dissipation				
	BF1201; BF1201R	T _s ≤ 113 °C; note 1	–	200	mW
	BF1201WR	T _s ≤ 109 °C; note 1	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	150	°C

Note

1. T_s is the temperature of the soldering point of the source lead.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-s}	thermal resistance from junction to soldering point		
	BF1201; BF1201R	185	K/W
	BF1201WR	155	K/W



N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

STATIC CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$; $I_D = 10\text{ }\mu\text{A}$	10	–	V
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; $I_{G1-S} = 10\text{ mA}$	6	–	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10\text{ mA}$	6	–	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10\text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10\text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 100\text{ }\mu\text{A}$	0.3	1.0	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = V_{DS} = 5\text{ V}$; $I_D = 100\text{ }\mu\text{A}$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $R_{G1} = 62\text{ k}\Omega$; note 1	11	19	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$; $V_{G1-S} = 5\text{ V}$	–	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = 4\text{ V}$	–	20	nA

Note

1. R_{G1} connects G_1 to $V_{GG} = 5\text{ V}$.

DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 15\text{ mA}$; unless otherwise specified.

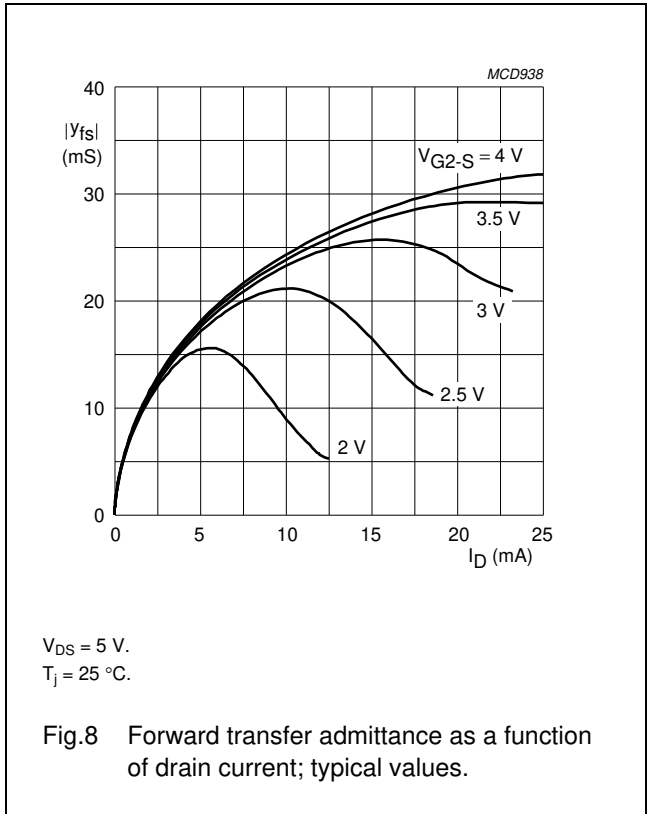
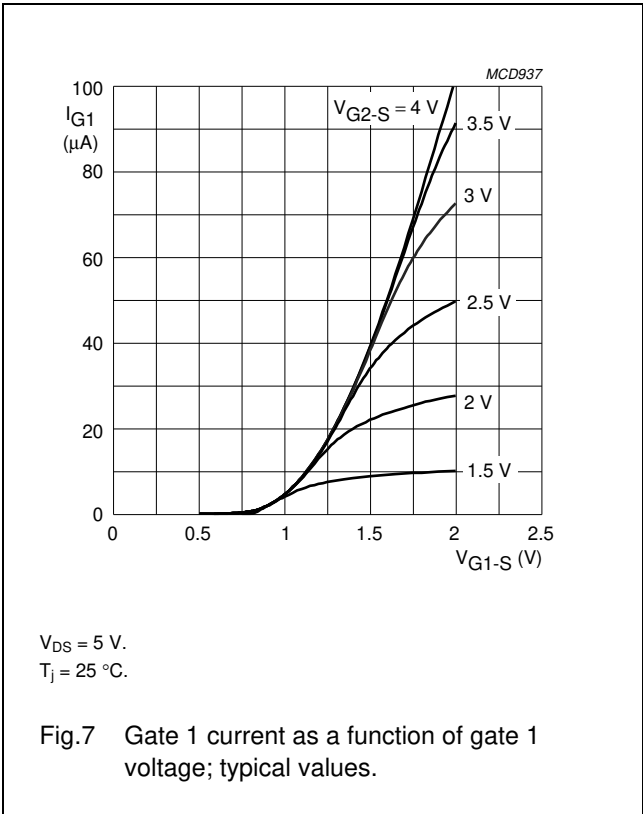
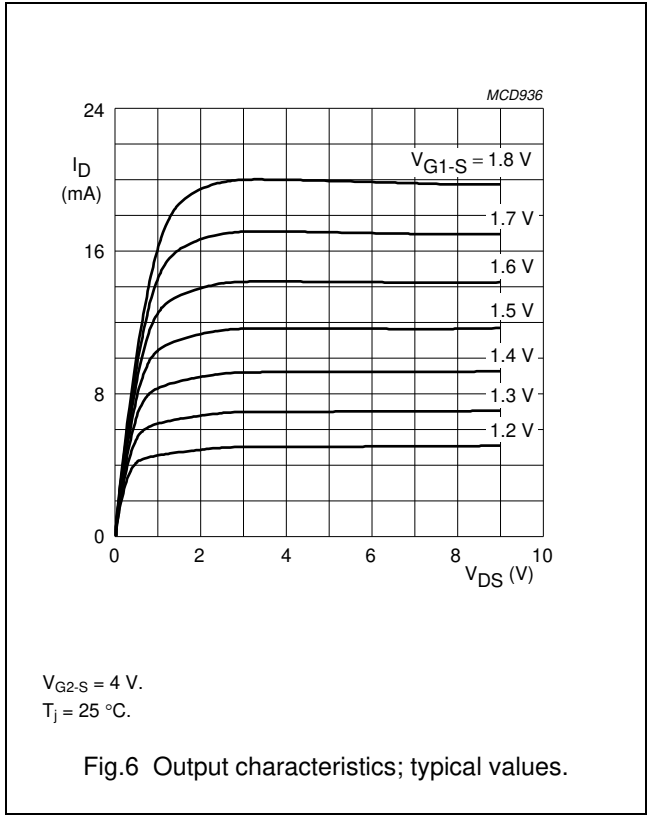
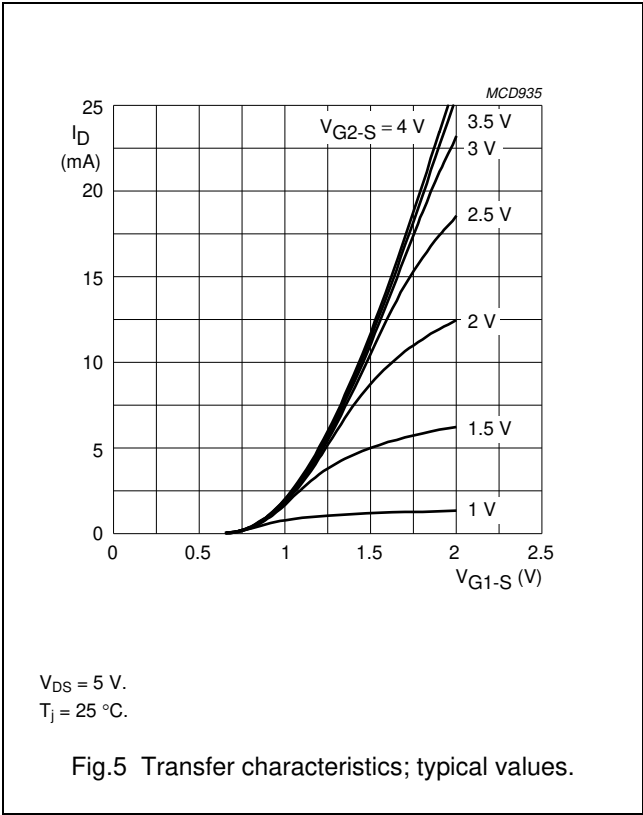
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ }^{\circ}\text{C}$	23	28	35	mS
C_{ig1-ss}	input capacitance at gate 1	$f = 1\text{ MHz}$	–	2.6	3.1	pF
C_{ig2-ss}	input capacitance at gate 2	$f = 1\text{ MHz}$	–	1.1	–	pF
C_{oss}	output capacitance	$f = 1\text{ MHz}$	–	0.9	–	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	15	30	fF
F	noise figure	$f = 10.7\text{ MHz}$; $G_S = 20\text{ mS}$; $B_S = 0$	–	5	7	dB
		$f = 400\text{ MHz}$; $Y_S = Y_{S\text{ opt}}$	–	1	1.8	dB
		$f = 800\text{ MHz}$; $Y_S = Y_{S\text{ opt}}$	–	1.9	2.5	dB
G_{tr}	power gain	$f = 200\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 0.5\text{ mS}$; $B_L = B_{L\text{ opt}}$	–	33.5	–	dB
		$f = 400\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 1\text{ mS}$; $B_L = B_{L\text{ opt}}$	–	29	–	dB
		$f = 800\text{ MHz}$; $G_S = 3.3\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 1\text{ mS}$; $B_L = B_{L\text{ opt}}$	–	24	–	dB
X_{mod}	cross-modulation	input level for $k = 1\%$; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; note 1				
		at 0 dB AGC	90	–	–	dB μ V
		at 10 dB AGC	–	95	–	dB μ V
		at 40 dB AGC	105	–	–	dB μ V

Note

1. Measured in Fig.21 test circuit.

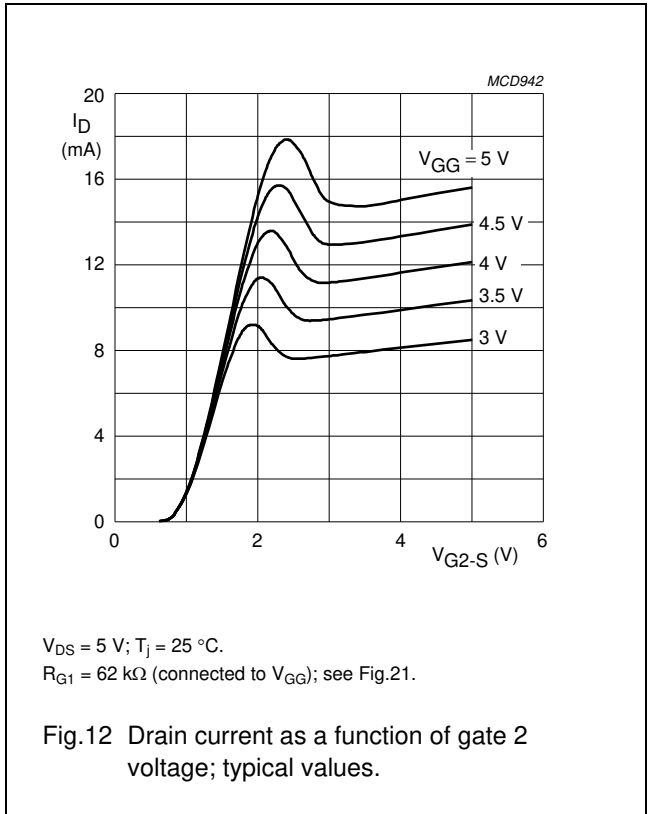
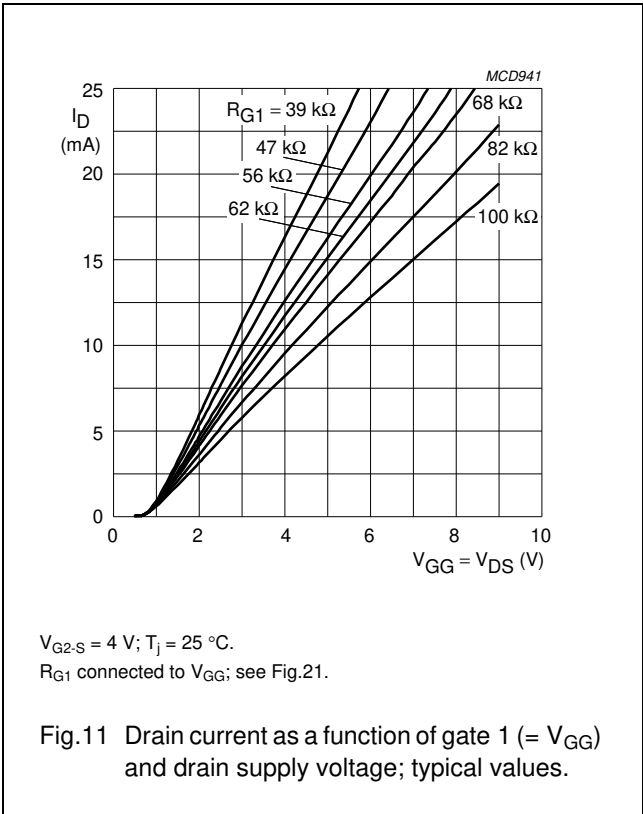
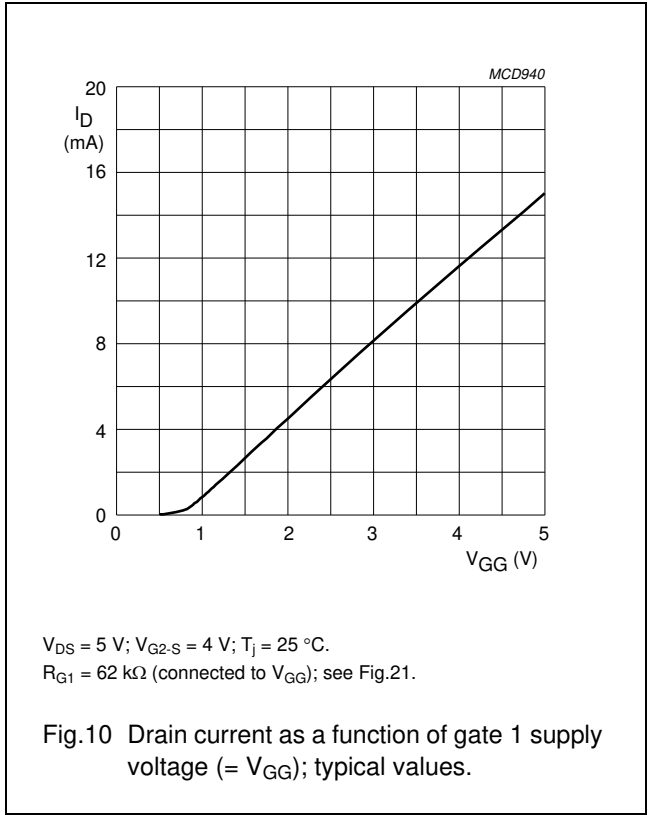
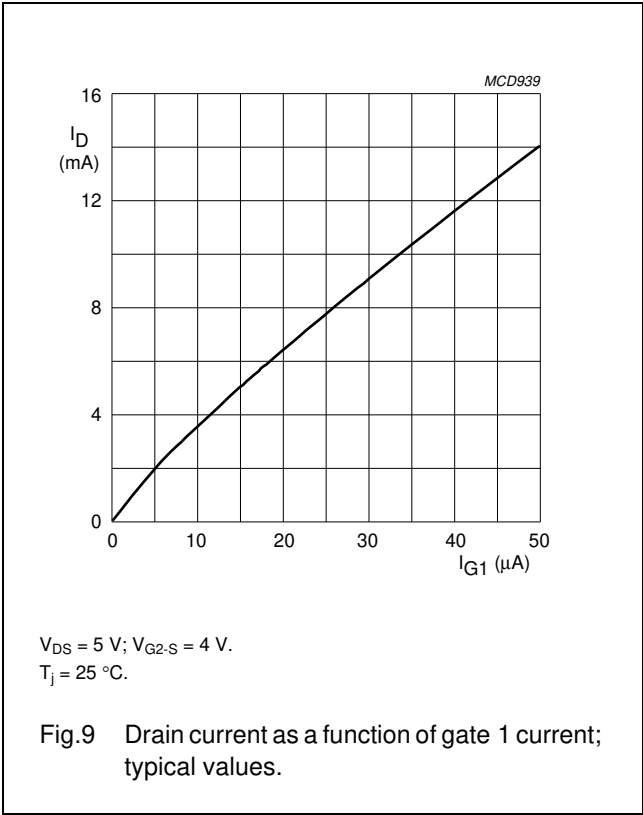
N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR



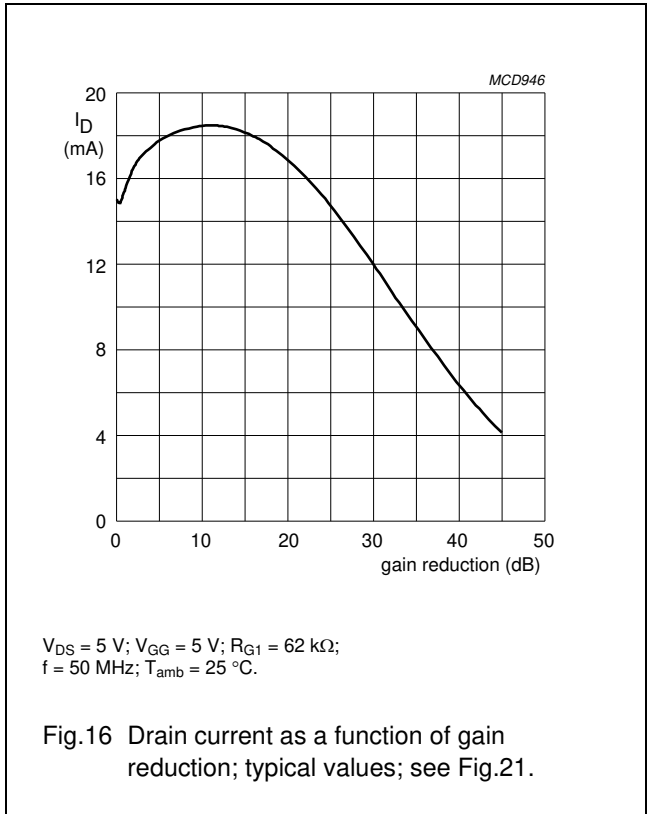
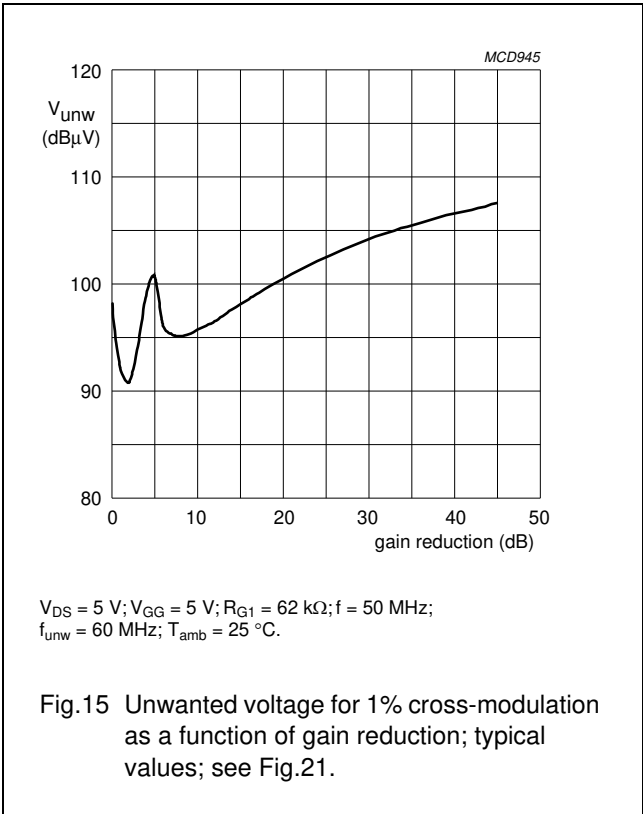
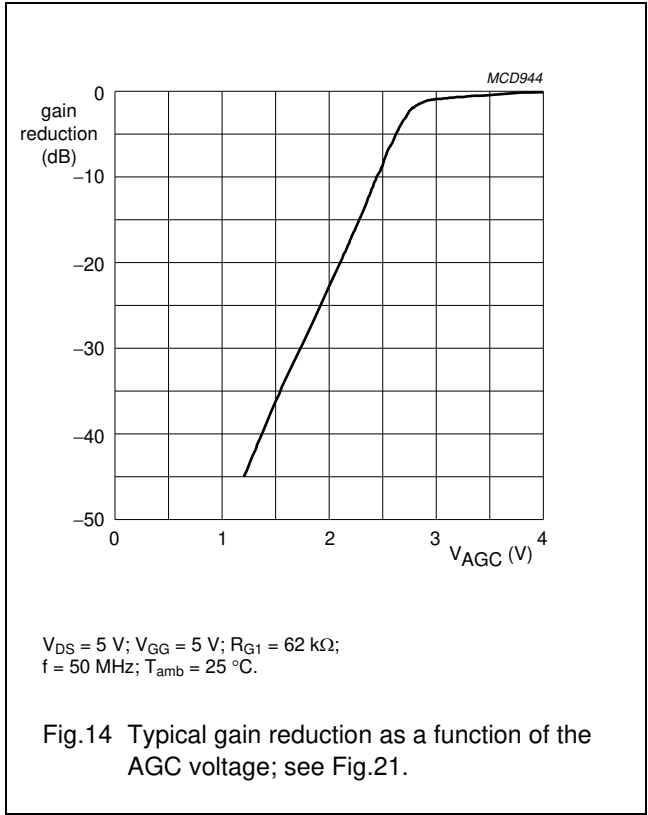
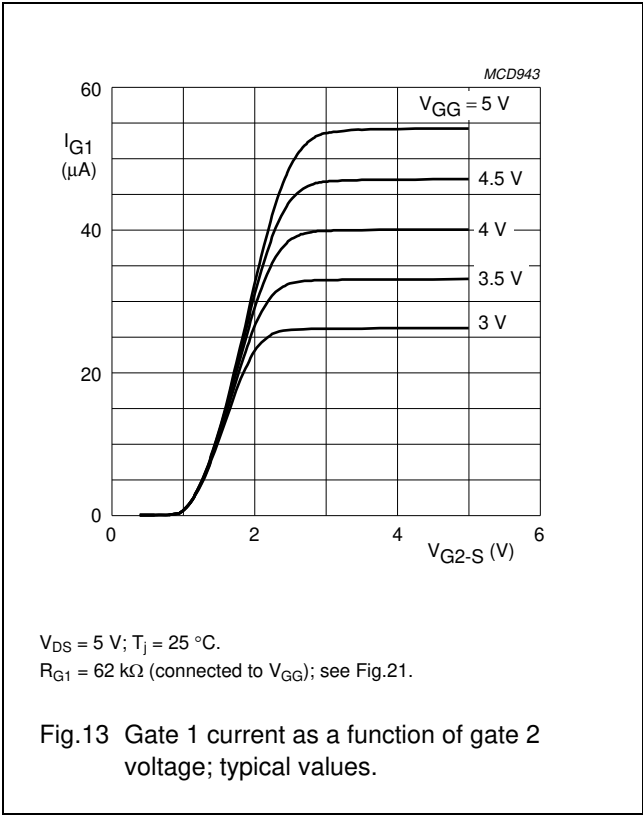
N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR



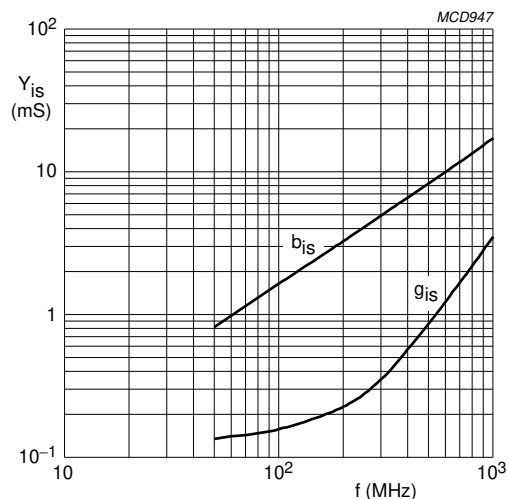
N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR



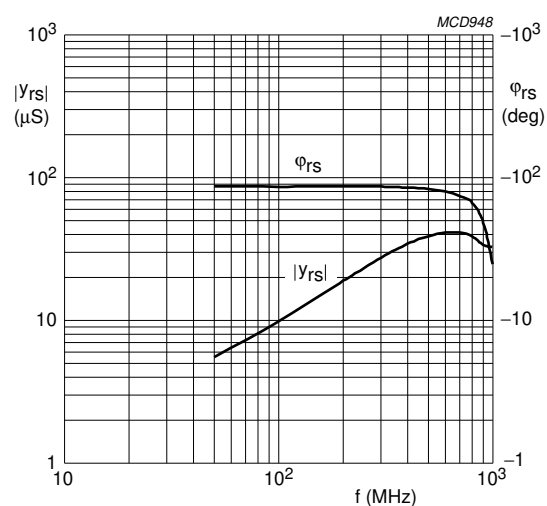
N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR



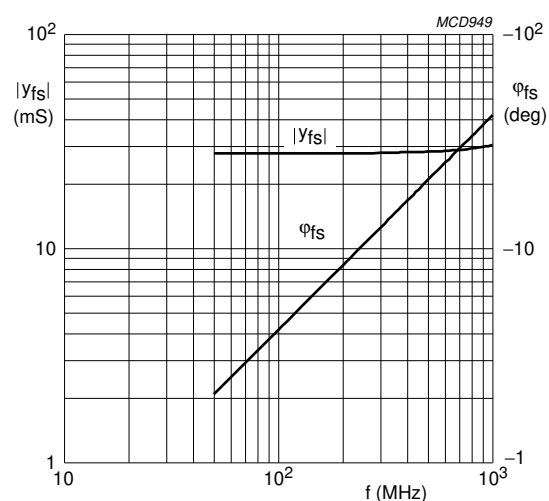
$V_{DS} = 5 \text{ V}$; $V_{G2} = 4 \text{ V}$.
 $I_D = 15 \text{ mA}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

Fig.17 Input admittance as a function of frequency; typical values.



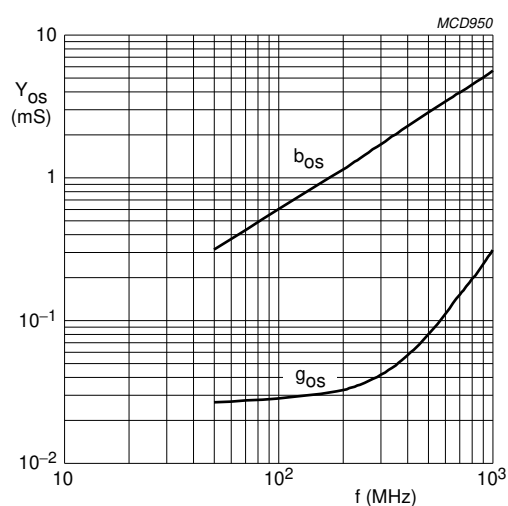
$V_{DS} = 5 \text{ V}$; $V_{G2} = 4 \text{ V}$.
 $I_D = 15 \text{ mA}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

Fig.18 Reverse transfer admittance and phase as a function of frequency; typical values.



$V_{DS} = 5 \text{ V}$; $V_{G2} = 4 \text{ V}$.
 $I_D = 15 \text{ mA}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

Fig.19 Forward transfer admittance and phase as a function of frequency; typical values.



$V_{DS} = 5 \text{ V}$; $V_{G2} = 4 \text{ V}$.
 $I_D = 15 \text{ mA}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

Fig.20 Output admittance as a function of frequency; typical values.

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

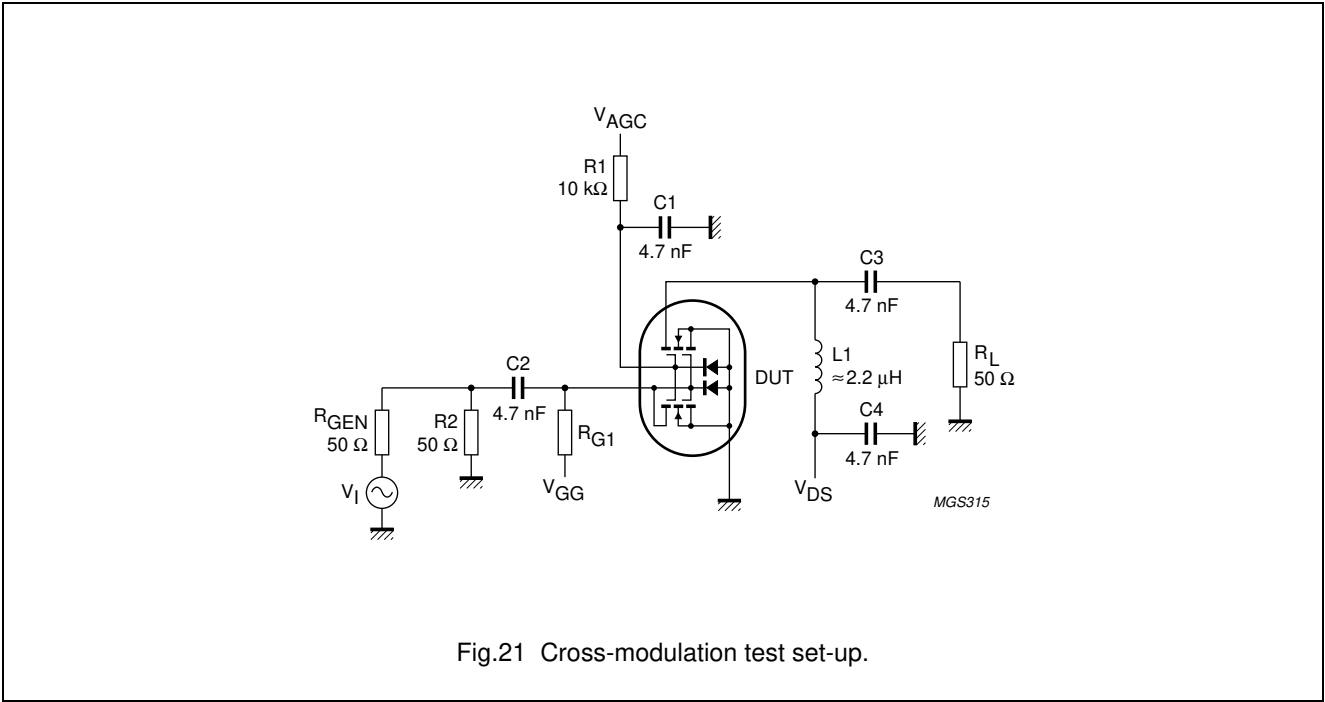


Table 1 Scattering parameters: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.987	−4.72	2.775	174.6	0.0006	88.8	0.997	−1.84
100	0.985	−9.39	2.774	169.5	0.0010	86.7	0.997	−3.37
200	0.978	−18.59	2.731	159.1	0.0019	79.7	0.996	−6.72
300	0.976	−27.74	2.671	148.8	0.0026	74.2	0.994	−10.02
400	0.949	−36.59	2.599	138.8	0.0032	69.9	0.992	−13.33
500	0.928	−45.08	2.501	129.1	0.0035	65.9	0.989	−16.55
600	0.905	−53.26	2.400	119.8	0.0035	64.6	0.986	−19.64
700	0.882	−61.07	2.297	110.9	0.0033	65.7	0.982	−22.63
800	0.860	−68.48	2.199	102.4	0.0029	69.1	0.979	−25.54
900	0.838	−75.55	2.096	94.2	0.0024	83.3	0.975	−28.44
1000	0.818	−82.23	1.997	86.3	0.0021	103.8	0.971	−31.42

Table 2 Noise data: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

f (MHz)	F _{min} (dB)	Γ _{opt}		R _n (Ω)
		(ratio)	(deg)	
400	1	0.825	38.93	50
800	1.9	0.753	70.65	38.75

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

PACKAGE OUTLINES

Plastic surface-mounted package; 4 leads

SOT143B

The technical drawing illustrates the SOT143B package in three views: top, side, and a detailed view of the lead (labeled 'detail X'). The top view shows a rectangular body with four leads labeled 1, 2, 3, and 4. Dimensions include D (body length), B (body width), e (lead pitch), e₁ (lead width), b_p (lead width at base), b₁ (lead width at tip), and w (lead width at base). The side view shows the package height H_E, lead height A, and lead width E. The detailed view of the lead shows dimensions A₁, Q, L_p, and c. A scale bar indicates 0 to 2 mm.

DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

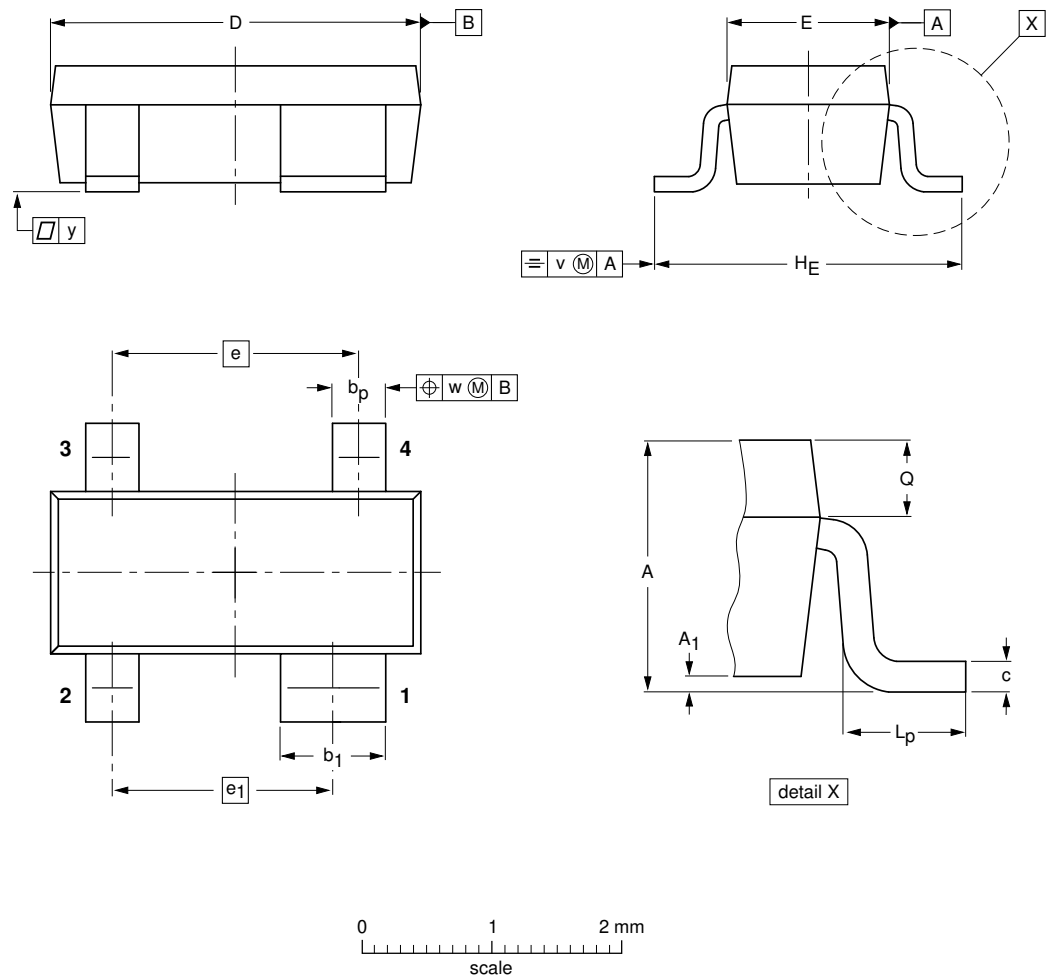
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143B						04-11-16 06-03-16

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

Plastic surface-mounted package; reverse pinning; 4 leads

SOT143R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

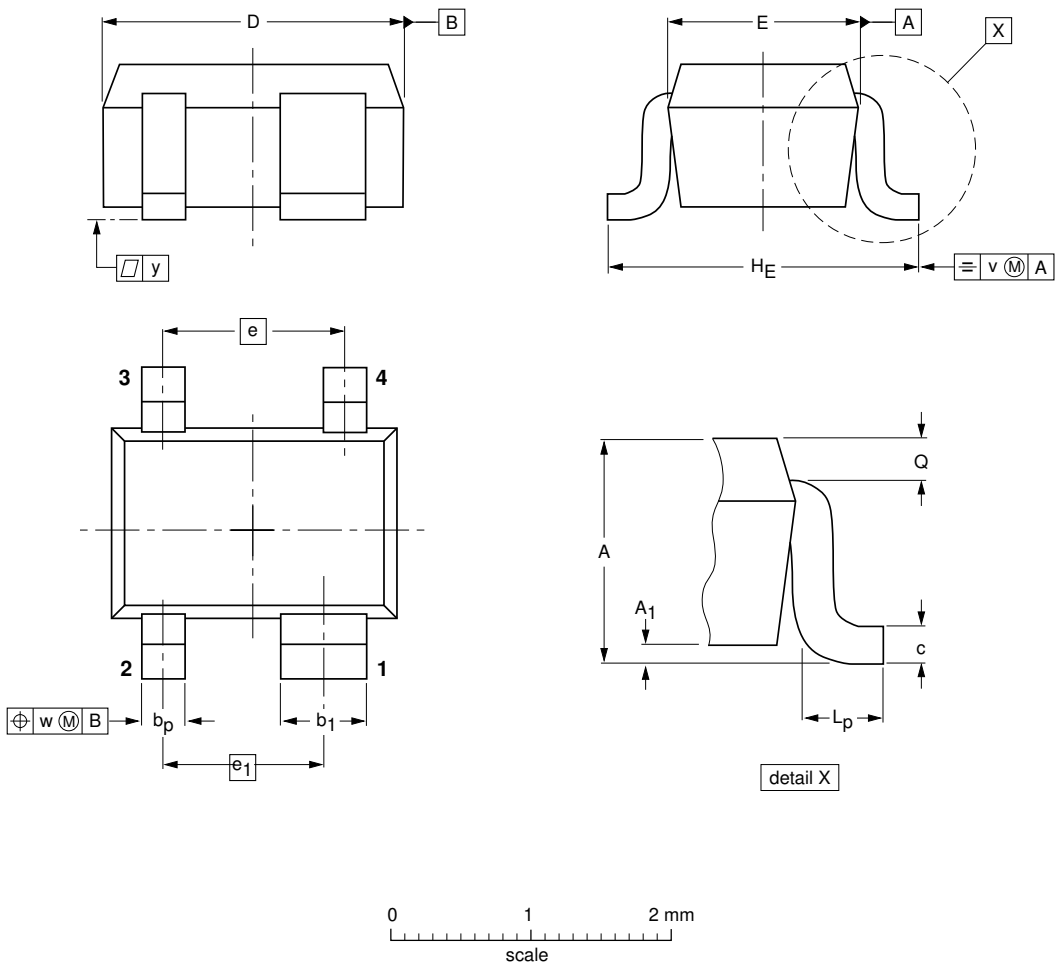
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143R			SC-61AA			04-11-16 06-03-16

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

Plastic surface-mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21 06-03-16

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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N-channel dual-gate PoLo MOS-FETsBF1201; BF1201R; BF1201WR

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This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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