

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: NJU72322V-TE1

Manufacturer: Nisshinbo Micro Devices Inc.

Package: 32-LSSOP (0.220", 5.60mm Width)

Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nisshinbo-micro-devices-inc/nju72322v-te1.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

±18V OPERATION HIGH QUALITY AUDIO VOLUME

■FEATURES

- Operating Voltage Analog ±10 to ±18V
 Digital +3.0 to +5.5V
- 3-Wired Serial Control
- Selectable Chip Address
Available for using two chips on same serial bus line.
- Low Output Noise *
- Low Distortion *
- Volume 0 to -111.5dB / 0.5dB step, Mute
 +21 to 0dB / 3dB step
- Zero Cross Detection
- Package Outline SSOP32

* It conforms to the characteristics of an external operational amplifier.

■GENERAL DESCRIPTION

The NJU72322 is a ±18V operation high quality audio volume. It provides low output noise and low distortion characteristics. In addition, employing external op-amps as output signal buffers, it offers designer's variety of circuit design.

All of functions are controlled via three-wired serial bus. Selectable chip address is available for using two chips on same serial bus line.

The NJU72322 is suitable for High-end audio equipment and professional audio equipment.

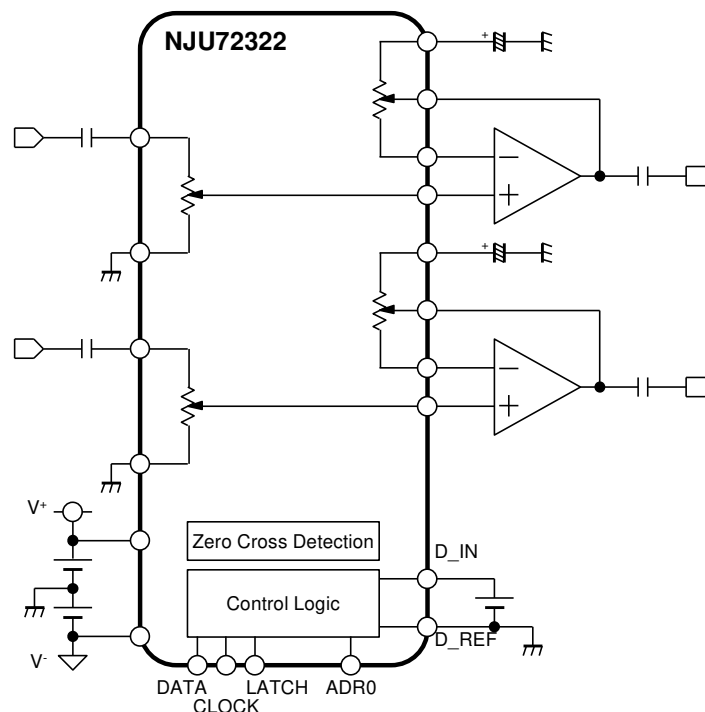
■APPLICATION

- Hi-Fi Audio Application
- Professional Audio Application

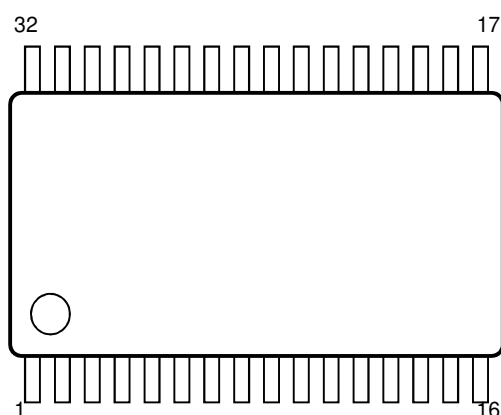
■AUDIO VOLUME VARIATION

OPERATING VOLTAGE	PRODUCT NAME
±8.5 to ±18V	MUSES72320
±10 to ±18V	MUSES72323

■APPLICATION CIRCUIT

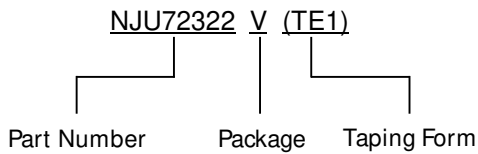


■PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION	PIN NO.	SYMBOL	DESCRIPTION
1	NC	No connection	17	NC	No connection
2	L_CAP	Lch switching noise rejection capacitor connection terminal	18	DATA	Control data signal input
3	OUTL	Lch output	19	CLOCK	Clock signal input
4	L-	Lch Op-amp inverting input connection terminal	20	LATCH	Latch signal input
5	L_REF	Lch reference voltage	21	D_V+	Power supply (+) [digital block] (+10V to +18V)
6	L+	Lch Op-amp non-inverting input connection terminal	22	INR	Rch input
7	L_REF	Lch reference voltage	23	AR_V+	Power supply (+) [Rch] (+10V to +18V)
8	L_REF	Lch reference voltage	24	AL_V+	Power supply (+) [Lch] (+10V to +18V)
9	R_REF	Rch reference voltage	25	AR_V-	Power supply (-) [Rch] (-10V to -18V)
10	R_REF	Rch reference voltage	26	AL_V-	Power supply (-) [Lch] (-10V to -18V)
11	R+	Rch Op-amp non-inverting input connection terminal	27	INL	Lch Input
12	R_REF	Rch reference voltage	28	D_V-	Power supply (-) [digital block] (-10V to -18V)
13	R-	Rch Op-amp inverting input connection terminal	29	D_CAP	Digital block noise rejection capacitor connection terminal
14	OUTR	Rch output	30	ADR0	Chip address setting terminal
15	R_CAP	Rch switching noise rejection capacitor connection terminal	31	NC	No connection
16	D_IN	Digital block power supply (+3.0V to +5.5V)	32	D_REF	Digital block reference voltage

■ MARK INFORMATION



■ ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJU72322V (TE1)	SSOP32	YES	YES	Sn2Bi	NJU72322	185	2,000

■ ABSOLUTE MAXIMUM RATINGS

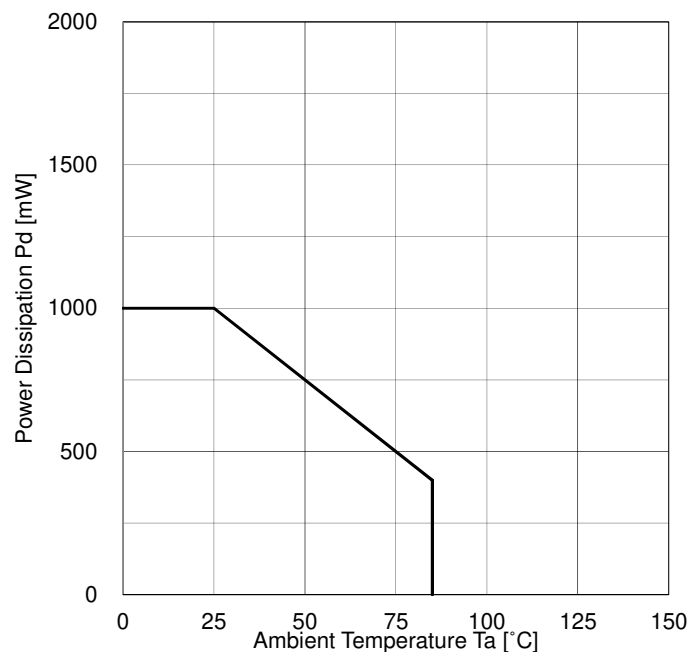
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+/V^-	+20/-20	V
Digital Block Voltage	V_{D_CAP}	$V^- + 6^{(1)}$	V
Digital Input Voltage	V_{ID}	$6^{(2)}$	V
Analog Input Voltage	V_{IA}	V^+/V^-	V
Power Dissipation	P_D	1000 ⁽³⁾	mW
Junction Temperature	T_{jmax}	+125	°C
Storage Temperature Range	T_{stg}	-40 to +125	°C

(1): D_CAP terminal.

(2): CLOCK, DATA, LATCH, D_IN terminal.

(3): Mounted on glass epoxy board. (76.2x114.3x1.6mm:based on EIA/JEDEC standard, 2layers FR-4)

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Operating Voltage	V^+/V^-	± 10 to ± 18	V
Digital Block Control Voltage	D_IN	+3.0 to +5.5 ⁽⁴⁾	V
Operating Temperature Range	T _{opr}	-40 to +85	°C

(4): D_REF(32pin)=0V

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(Ta=25°C, $V^+/V^- = \pm 15$ V, V_{IN}=5V, D_REF=0V, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current 1	I _{CC}	No Signal, No Load	-	2	10	mA
Supply Current 2	I _{EE}	No Signal, No Load	-	2	10	mA
Input Impedance	R _{IN}	INR(22pin), INL(27pin) terminals	14	20	-	kΩ

AC CHARACTERISTICS

(Ta=25°C, $V^+/V^- = \pm 15$ V, f=1kHz, V_{IN}=2Vrms, Volume=0dB, Gain=0dB, V_{OUT} with MUSES8920, R_L=47kΩ, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Input Voltage	V _{IM}	THD=1%, Volume=-20dB	11	-	-	Vrms
Maximum Output Voltage	V _{OM}	THD=1%	-	10.3	-	Vrms
Voltage Gain 1	G _{V1}	-	-0.5	0	+0.5	dB
Voltage Gain 2	G _{V2}	V _{IN} =0.5Vrms, Gain=+12dB	+11	+12	+13	dB
Voltage Gain Error 1	ΔG _{V1}	-	-0.5	0	+0.5	dB
Voltage Gain Error 2	ΔG _{V2}	Volume=-60dB	-1.0	0	+1.0	dB
Maximum Attenuation	A _{TT}	Volume=-111.5dB, A-weight	-	-111.5	-	dB
Mute Level	Mute	Volume=Mute, A-weight	-	-120	-	dB
Total Harmonic Distortion1	THD1	V _{IN} =1.6Vrms BW=400 to 22kHz	-	0.00024	-	%
Total Harmonic Distortion2	THD2	F=10kHz, V _{IN} =1Vrms BW=400 to 30kHz	-	0.0007	-	%
Output Noise	V _{NO}	R _g =0Ω, A-weight, R _L =100kΩ V _{OUT} without MUSES8920	-	-118 (1.26μ)	-	dBV (Vrms)
Channel Separation 1	CS1	R _g =0Ω	-	-110	-90	dB
Channel Separation 2	CS2	F=20kHz, R _g =0Ω	-	-90	-	dB

LOGIC CONTROL CHARACTERISTICS

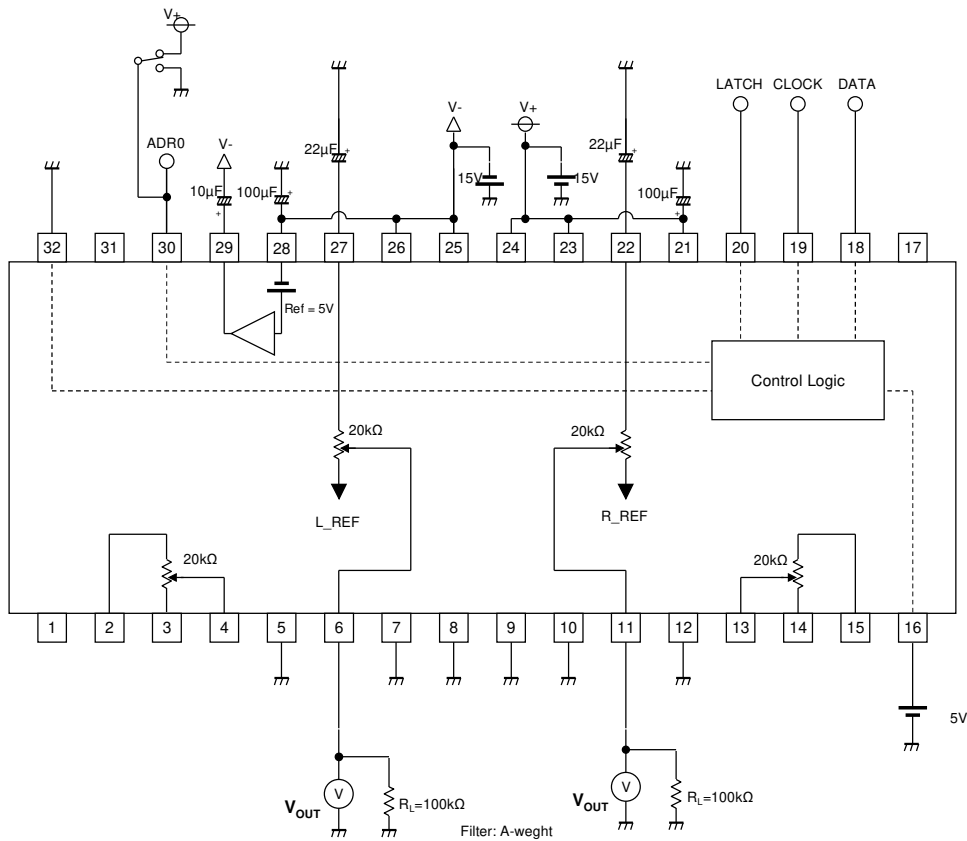
(Ta=25°C, V_{+/-}=±15V, D_{VDD}=“D_IN”-“D_REF” unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Input Voltage 1	V _{IH1}	DATA, CLOCK, LATCH terminal	0.7*D _{VDD}	-	5.5	V
Low Level Input Voltage 1	V _{IL1}		0	-	0.3*D _{VDD}	V
High Level Input Voltage 2	V _{IH2}	ADR0 terminal	0.7*D _{VDD}	-	V ⁺	V
Low Level Input Voltage 2	V _{IL2}		0	-	0.3*D _{VDD}	V

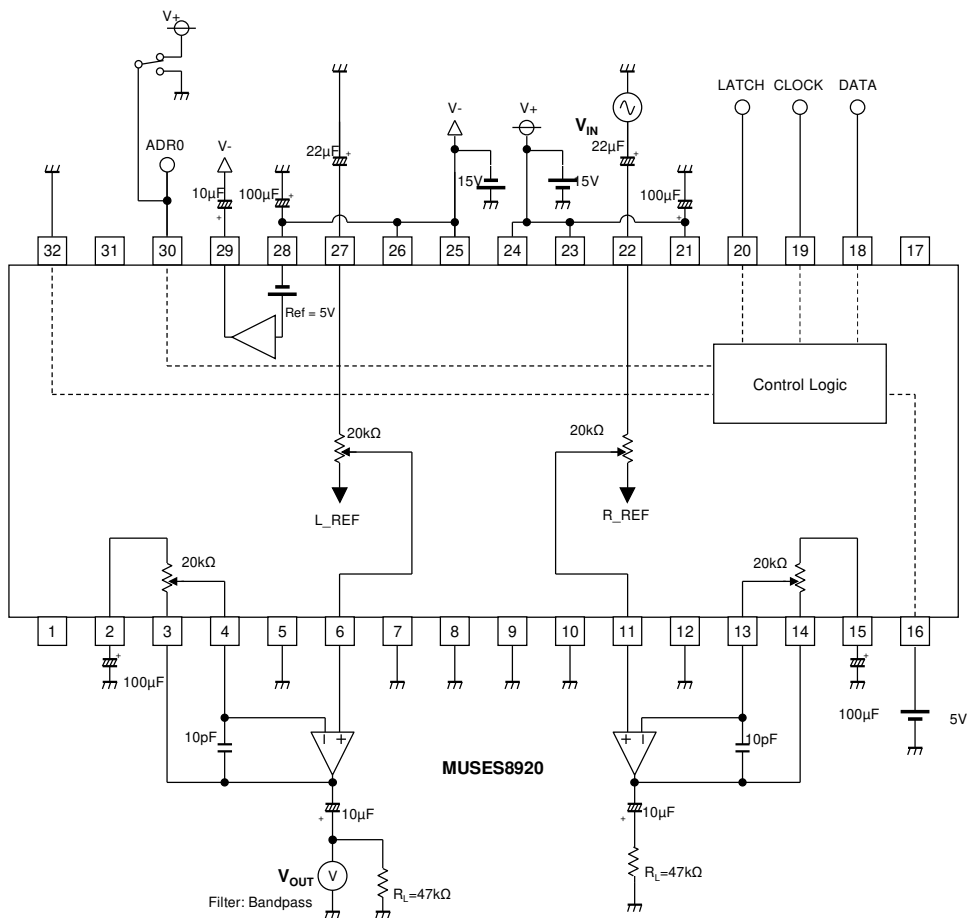
◆ I_{CC}, I_{EE}



◆V_{NO}



◆CS1, CS2



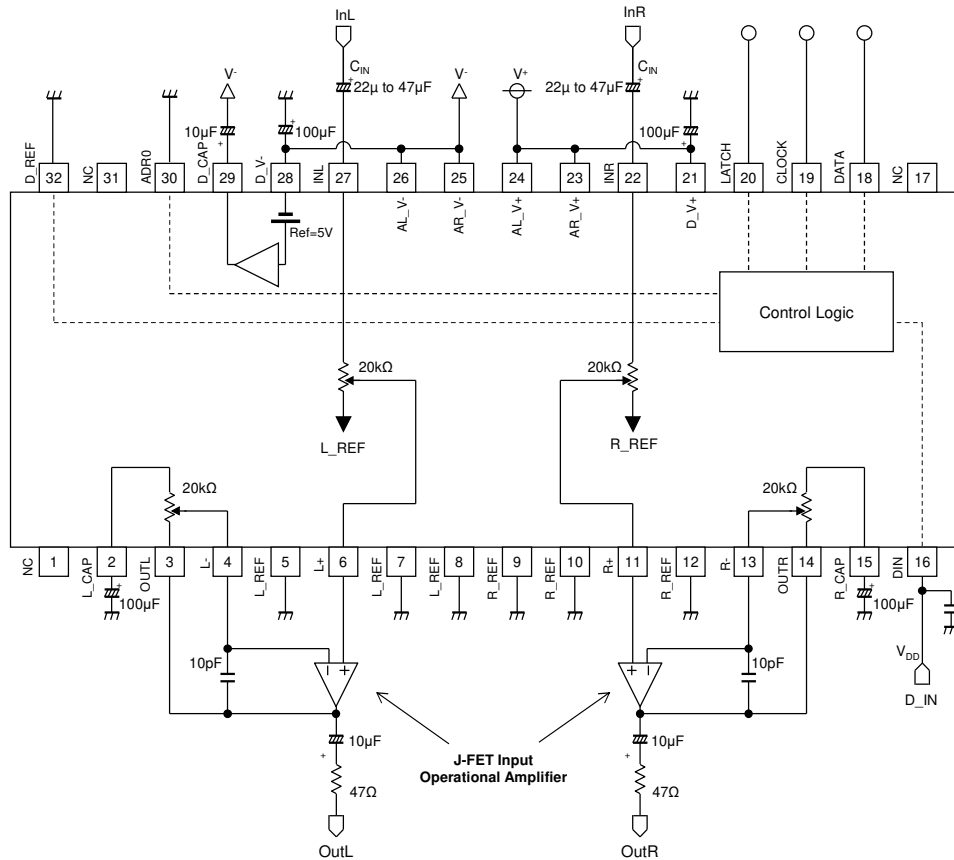
■TERMINAL DESCRIPTION

TERMINAL	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
2	L_CAP	Lch switching noise rejection capacitor connection terminal		0V
15	R_CAP	Rch switching noise rejection capacitor connection terminal		
3	OUTL	Lch output		0V
5	L_REF	Lch reference voltage		
7	L_REF	Lch reference voltage		
8	L_REF	Lch reference voltage		
9	R_REF	Rch reference voltage		
10	R_REF	Rch reference voltage		
12	R_REF	Rch reference voltage		
14	OUTR	Rch output		
4	L-	Lch Op-amp inverting input connection terminal		0V
6	L+	Lch Op-amp non-inverting input connection terminal		
11	R+	Rch Op-amp non-inverting input connection terminal		
13	R-	Rch Op-amp inverting input connection terminal		
16	D_IN	Digital block power supply		0V
32	D_REF	Digital block Reference voltage		

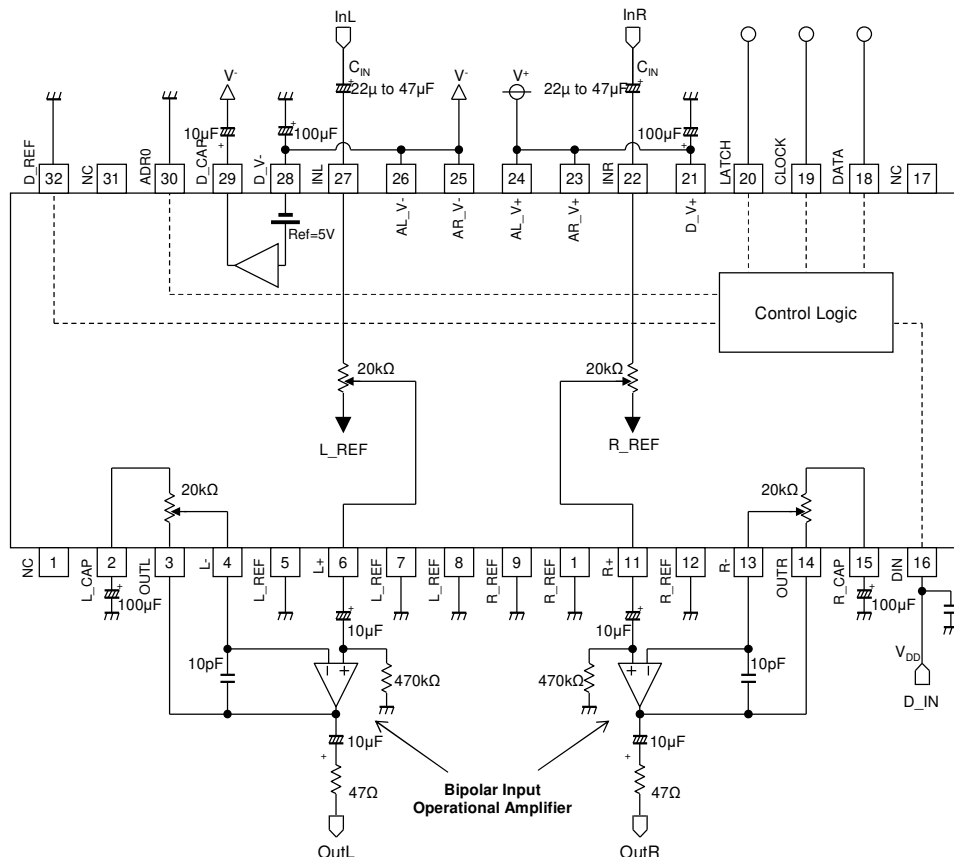
TERMINAL	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
18 19 20	DATA CLOCK LATCH	Control data signal input Clock signal input Latch signal input		-
22 27	INR INL	Rch input Lch input		0V
29	D_CAP	Digital block noise rejection capacitor connection terminal		V + 5V
30	ADR0	Chip address setting terminal		-

■ APPLICATION CIRCUIT

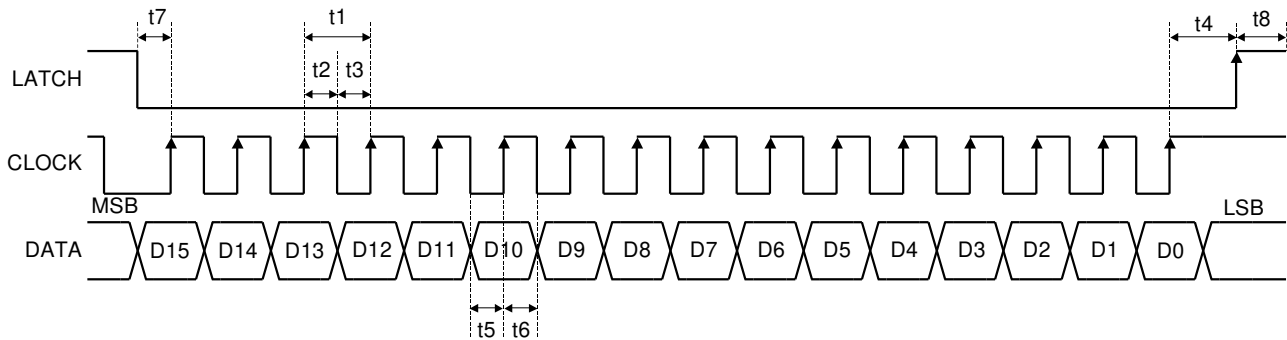
◆ Application circuit with J-FET input type Op-Amp.



◆ Application circuit with Bipolar input type Op-Amp.



■TIMING ON 3-wired BUS (DATA, CLOCK, LATCH)



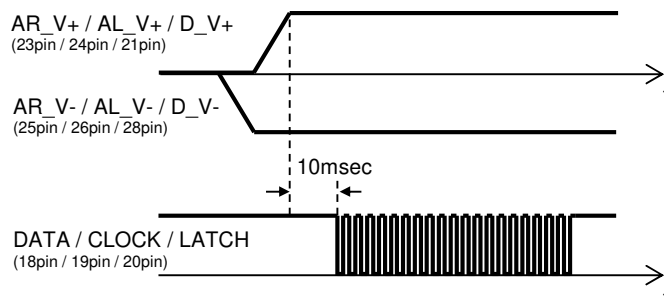
*) MSB First

■CHARACTERISTICS OF BUS LINES (DATA, CLOCK, LATCH) FOR 3-wired BUS DEVICES

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t1	CLOCK Clock Width	1	-	-	μsec
t2	CLOCK Pulse Width(High)	0.4	-	-	μsec
t3	CLOCK Pulse Width(Low)	0.4	-	-	μsec
t4	LATCH Rise Hold Time	1	-	-	μsec
t5	DATA Setup Time	0.4	-	-	μsec
t6	DATA Hold Time	0.4	-	-	μsec
t7	CLOCK Setup Time	0.4	-	-	μsec
t8	LATCH Pulse Width(High)	0.4	-	-	μsec

■RECOMMENDED POWER-UP SEQUENCE

The NJU72322 should be used under the condition that potential V^- terminals are always the lowest potential. It is recommended that V^- power supply turns on before or just same time that V^+ power supply turns on.



■DEFINITION OF 3-wired REGISTER

Note) Please don't send except specified data for avoiding an incorrect operation.

◆3-wired BUS FORMAT / CONTROL RESISTER TABLE

The NJU72322 control data is constructed with 16bits.

MSB								LSB							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data								0	0	0	0	Select Address		Chip Address	

MSB														LSB	
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L channel Volume								0	0	0	0	0	0	1	*
R channel Volume								0	0	0	0	0	1	1	*
L/R Cont	L channel Gain					R channel Gain		Z/C	0	0	0	0	1	0	*

◆CHIP ADDRESS

Chip address is set by the ADR0 (chip address setting terminal) status.

Chip address setting terminal	Chip Address	
ADR0 (30pin)	D1	D0
Low	1	0
High	1	1

◆CONTROL REGISTER DEFAULT VALUE

MSB														LSB	
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	*
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	*
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	*

Note) This product starts up by MUTE setting in power "ON". Use it after removing MUTE of each setting.

If any audio signal is inputted in input signal terminal before power "ON", it may cause initial condition abnormality. In conditions of using such as the above, it prevents that abnormality by setting MUTE before power "OFF".

■DEFINITION OF RESISTOR

◆Volume : 0 to -111.5dB / 0.5dB step.

Each volume is controlled independently when L/RCont="0".

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L channel Volume								0	0	0	0	0	0	1	*
R channel Volume								0	0	0	0	0	1	1	*

< L channel Volume / R channel Volume Setting >

Data								Setting
D15	D14	D13	D12	D11	D10	D9	D8	
0	0	0	0	0	0	0	0	Mute ^(*)
0	0	0	1	0	0	0	0	0dB
0	0	0	1	0	0	0	1	-0.5dB
0	0	0	1	0	0	1	0	-1.0dB
0	0	0	1	0	0	1	1	-1.5dB
0	0	0	1	0	1	0	0	-2.0dB
0	0	0	1	0	1	0	1	-2.5dB
0	0	0	1	0	1	1	0	-3.0dB
0	0	0	1	0	1	1	1	-3.5dB
0	0	0	1	1	0	0	0	-4.0dB
0	0	0	1	1	0	0	1	-4.5dB
0	0	0	1	1	0	1	0	-5.0dB
0	0	0	1	1	0	1	1	-5.5dB
0	0	0	1	1	1	0	0	-6.0dB
0	0	0	1	1	1	0	1	-6.5dB
0	0	0	1	1	1	1	0	-7.0dB
0	0	0	1	1	1	1	1	-7.5dB
0	0	1	0	0	0	0	0	-8.0dB

⋮

1	1	1	0	0	0	0	0	-104.0dB
1	1	1	0	0	0	0	1	-104.5dB
1	1	1	0	0	0	1	0	-105.0dB
1	1	1	0	0	0	1	1	-105.5dB
1	1	1	0	0	1	0	0	-106.0dB
1	1	1	0	0	1	0	1	-106.5dB
1	1	1	0	0	1	1	0	-107.0dB
1	1	1	0	0	1	1	1	-107.5dB
1	1	1	0	1	0	0	0	-108.0dB
1	1	1	0	1	0	0	1	-108.5dB
1	1	1	0	1	0	1	0	-109.0dB
1	1	1	0	1	0	1	1	-109.5dB
1	1	1	0	1	1	0	0	-110.0dB
1	1	1	0	1	1	0	1	-110.5dB
1	1	1	0	1	1	1	0	-111.0dB
1	1	1	0	1	1	1	1	-111.5dB
1	1	1	1	1	1	1	1	Mute

(*)Default Setting

- ◆**L/R Cont :** Select “L channel Volume, R channel Volume independent control” or “L channel Volume, R channel Volume link control” of method of volume control.
- ◆**Gain :** 0 to +21dB / 3dB step.
Each gain is controlled independently.
- ◆**Z/C :** Zero Cross Detection circuit ON/OFF setting.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L/R Cont	L channel Gain			R channel Gain			Z/C	0	0	0	0	1	0	1	*

<L/R Cont Setting>

Data	Setting
D15	
0	L channel Volume, R channel Volume independent control ^(*)
1	L channel Volume, R channel Volume link control

^(*)Default Setting

Command table when L channel Volume and R channel Volume are linked

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L /R channel Volume								0	0	0	0	0	0	1	*
No Acceptable								0	0	0	0	0	1	1	*

<L channel Gain / R channel Gain Setting>

Data			Setting
D14	D13	D12	
D11	D10	D9	
D11	D10	D9	
0	0	0	0dB ^(*)
0	0	1	+3dB
0	1	0	+6dB
0	1	1	+9dB
1	0	0	+12dB
1	0	1	+15dB
1	1	0	+18dB
1	1	1	+21dB

^(*)Default Setting

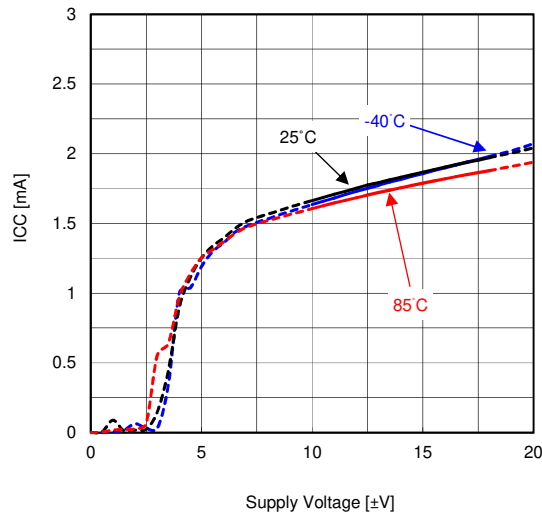
<Z/C Setting>

Data	Setting
D8	
0	Zero Cross Detection Circuit ON ^(*)
1	Zero Cross Detection Circuit OFF

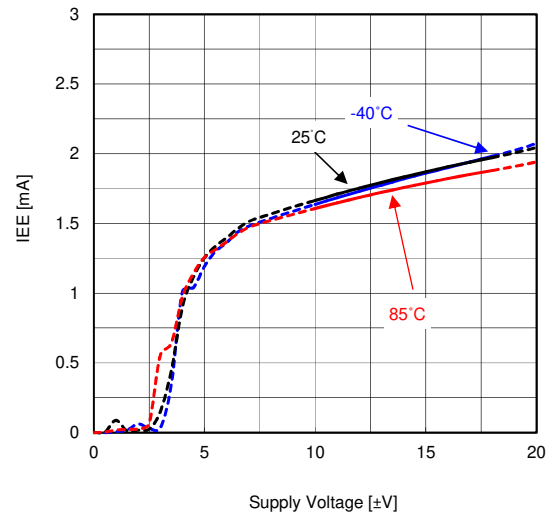
^(*)Default Setting

■ TYPICAL CHARACTERISTICS

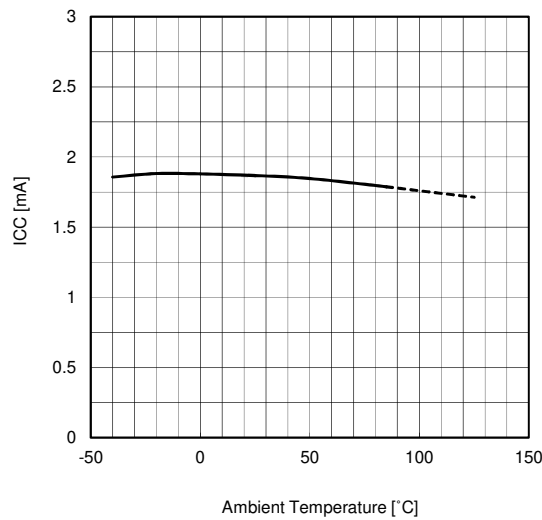
ICC vs Supply Voltage
No Signal



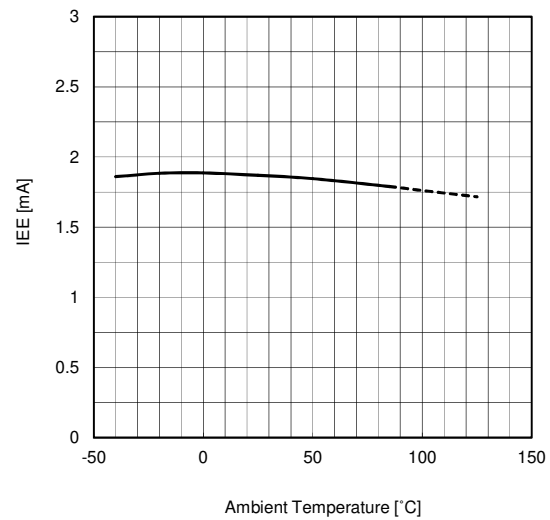
IEE vs Supply Voltage
No Signal



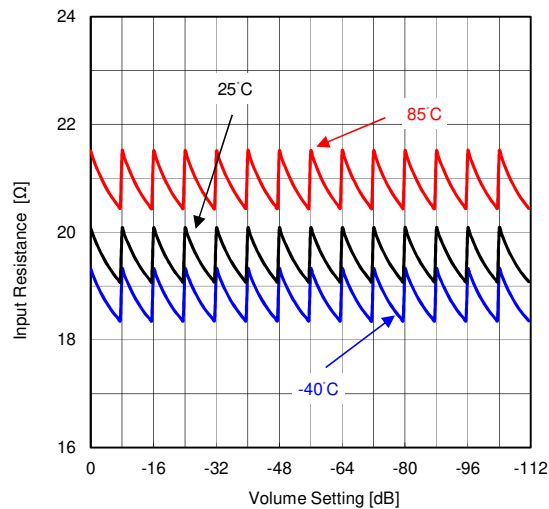
ICC vs Ambient Temperature
V=±15V, No Signal



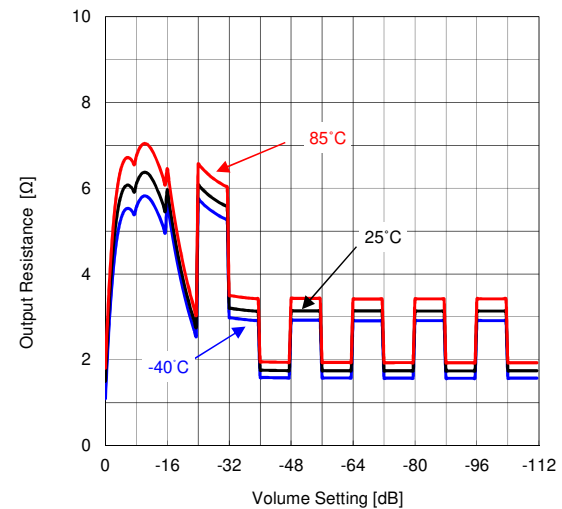
IEE vs Ambient Temperature
V=±15V, No Signal



Input Resistance vs Volume Setting
V=±15V, No signal



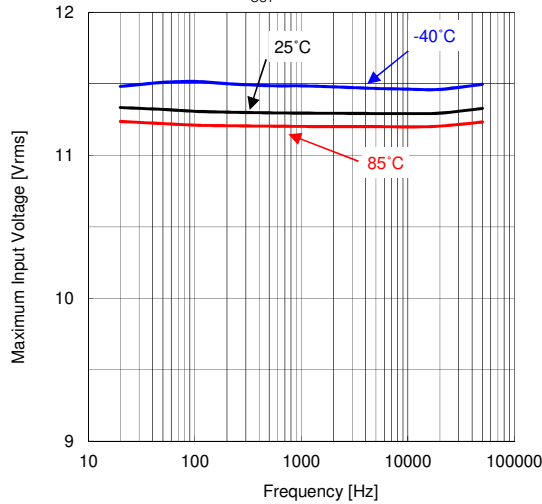
Output Resistance vs Volume Setting
V=±15V, No signal



■TYPICAL CHARACTERISTICS

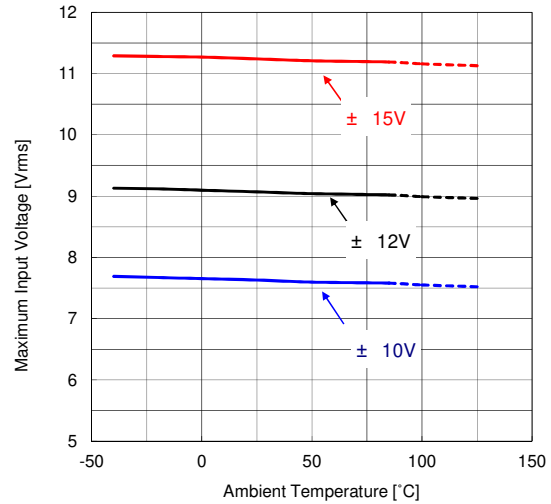
Maximum Input Voltage vs Frequency

$V=\pm 15V$, THD=1%, Volume=-20dB, Gain=0dB,
 V_{OUT} with MUSES8920



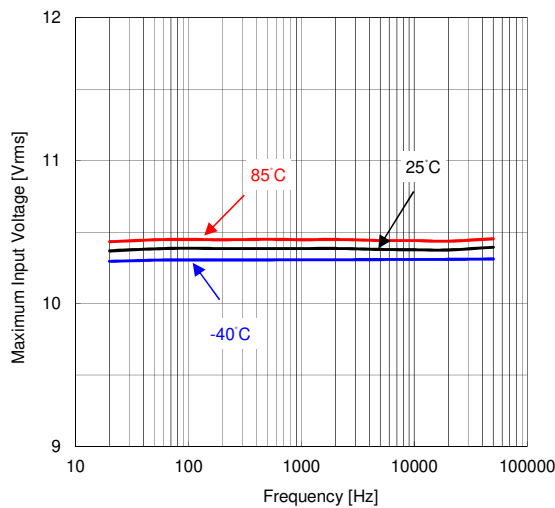
Maximum Input Voltage vs Ambient Temperature

$f=1kHz$, THD=1%, Volume=-20dB, Gain=0dB,
 V_{OUT} with MUSES8920



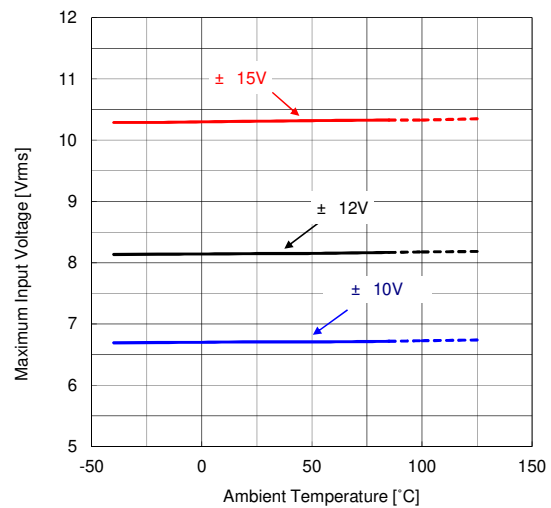
Maximum Output Voltage vs Frequency

$V=\pm 15V$, THD=1%, V_{OUT} with MUSES8920



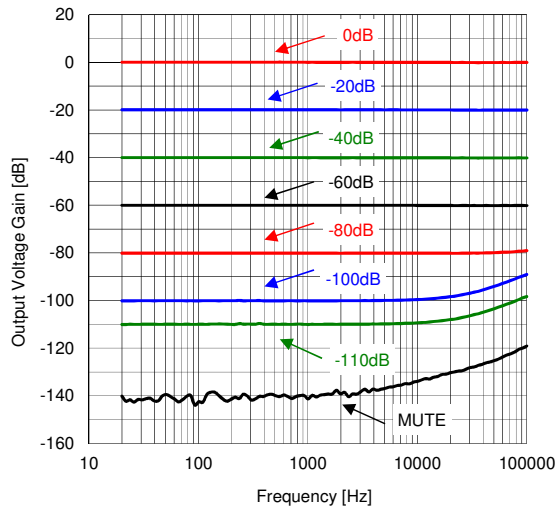
Maximum Output Voltage vs Ambient Temperature

$f=1kHz$, THD=1%, V_{OUT} with MUSES8920



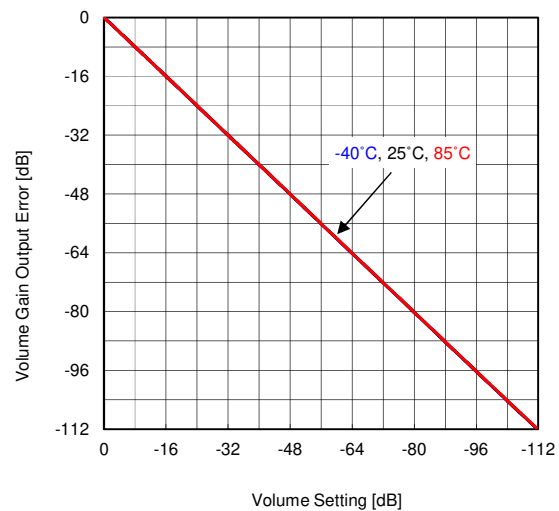
Output Voltage Gain vs Frequency

$V=\pm 15V$, $V_{in}=4V_{rms}$, Bandpass



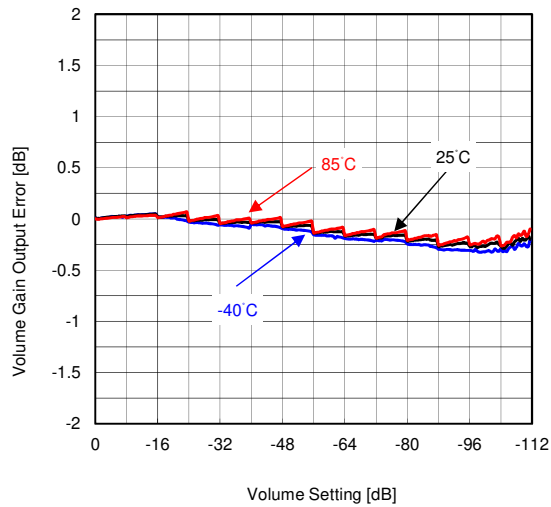
Volume Gain Output vs Volume Setting

$V=\pm 15V$, $f=1kHz$, $V_{in}=4V_{rms}$, Gain=0dB, Bandpass

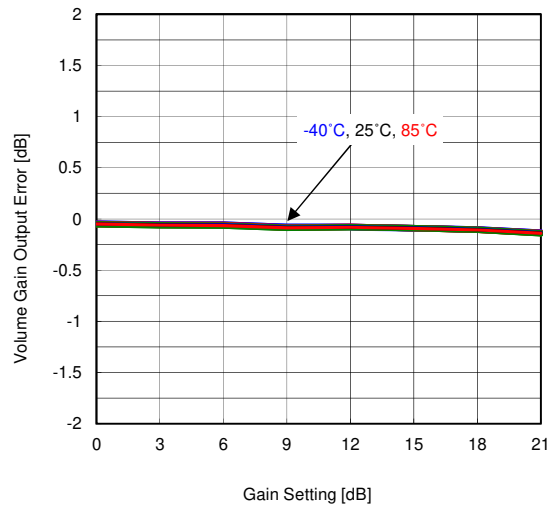


■TYPICAL CHARACTERISTICS

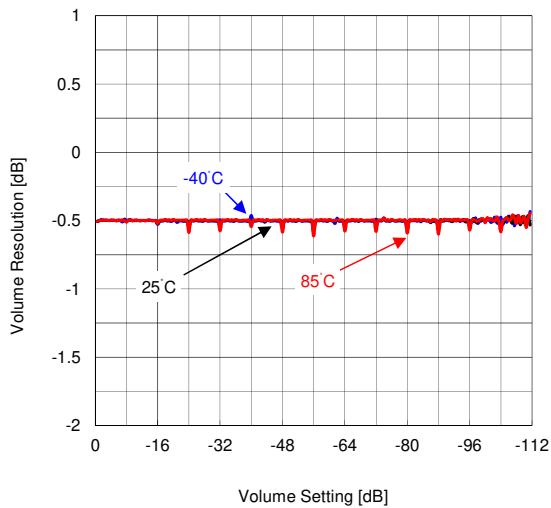
Volume Gain Output Error vs Volume Setting
 $V=\pm 15V$, $f=1kHz$, $V_{in}=4V_{rms}$, $Gain=0dB$, Bandpass



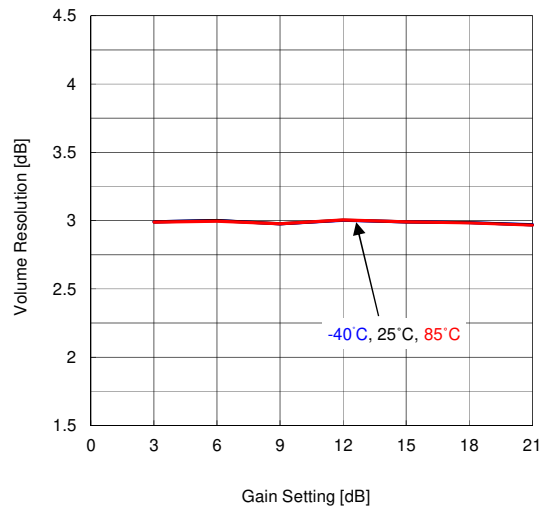
Volume Gain Output Error vs Volume Setting
 $V=\pm 15V$, $f=1kHz$, $V_{in}=200mV_{rms}$, $Volume=0dB$, Bandpass



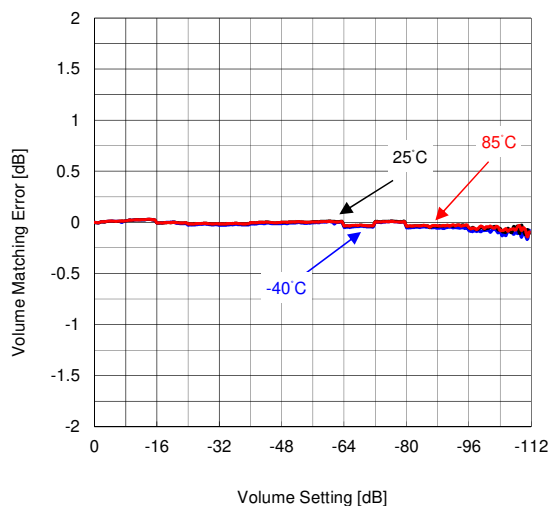
Volume Resolution vs Volume Setting
 $V=\pm 15V$, $f=1kHz$, $V_{in}=4V_{rms}$, $Gain=0dB$, Bandpass



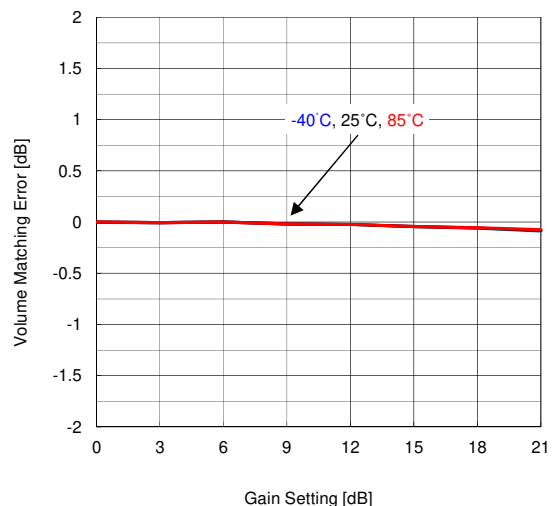
Volume Resolution vs Volume Setting
 $V=\pm 15V$, $f=1kHz$, $V_{in}=200mV_{rms}$, $Volume=0dB$, Bandpass



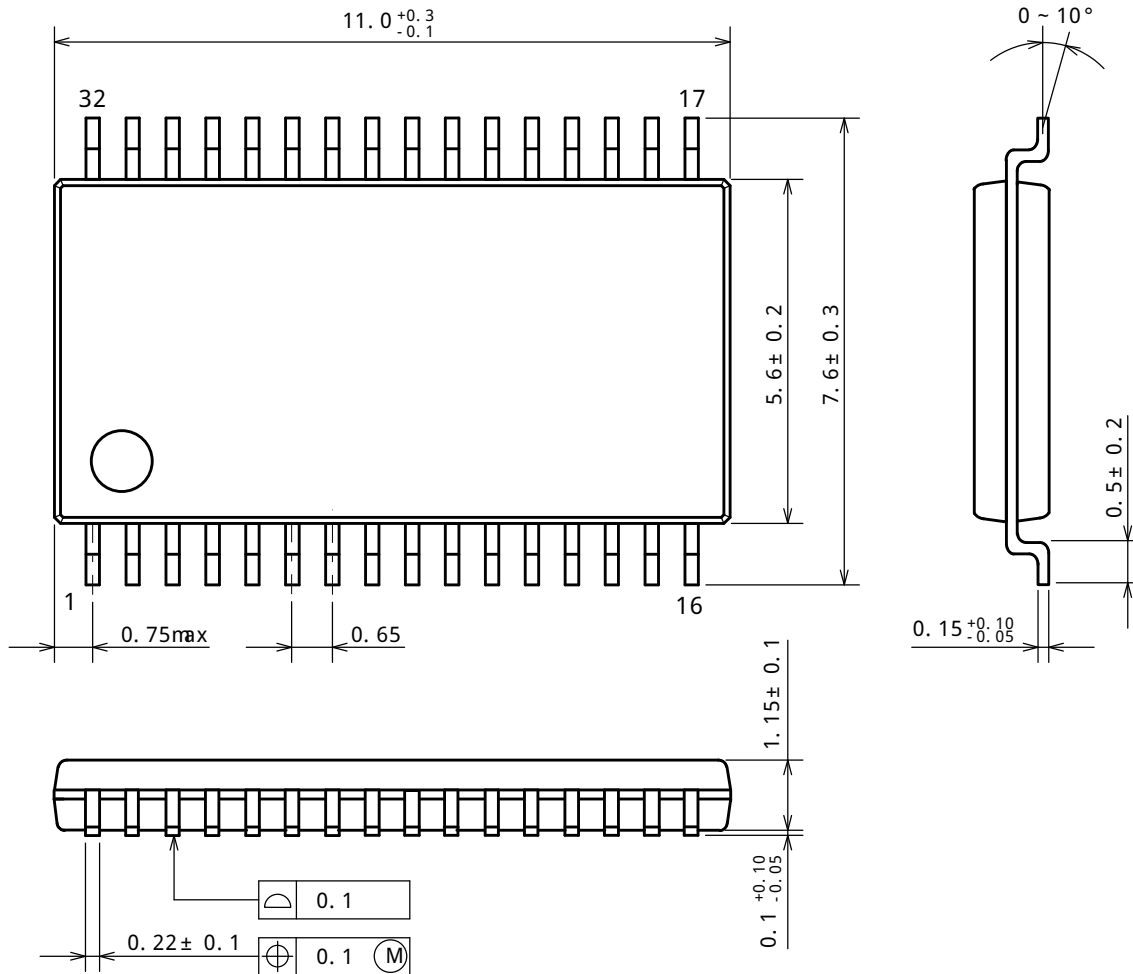
Volume Matching Error vs Volume Setting
 $V=\pm 15V$, $f=1kHz$, $V_{in}=4V_{rms}$, $Gain=0dB$, Bandpass



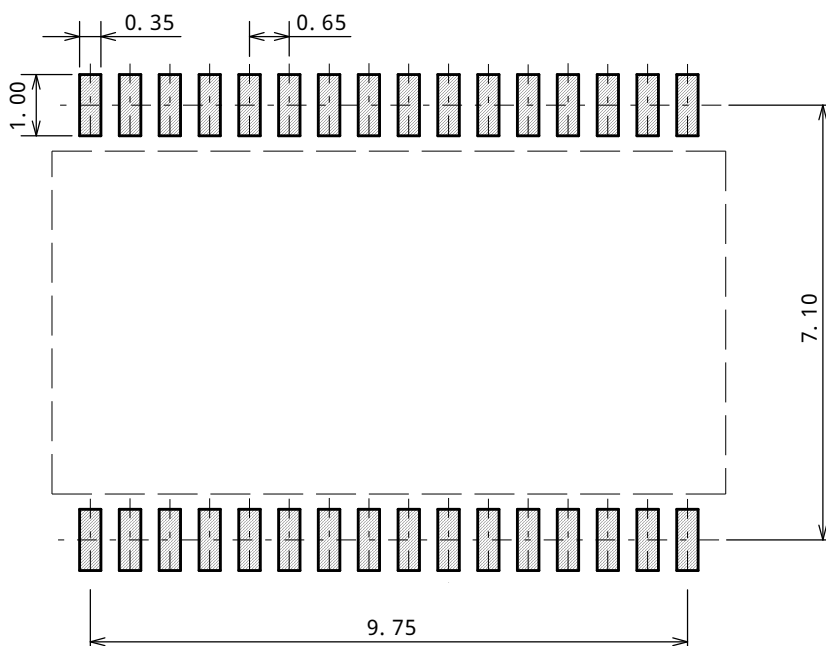
Volume Matching Error vs Volume Setting
 $V=\pm 15V$, $f=1kHz$, $V_{in}=200mV_{rms}$, $Volume=0dB$, Bandpass



■PACKAGE DIMENSIONS



■EXAMPLE OF SOLDER PADS DIMENSIONS

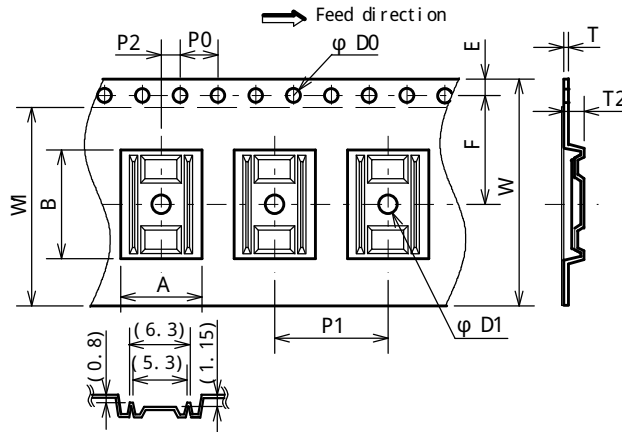


SSOP32

Unit: mm

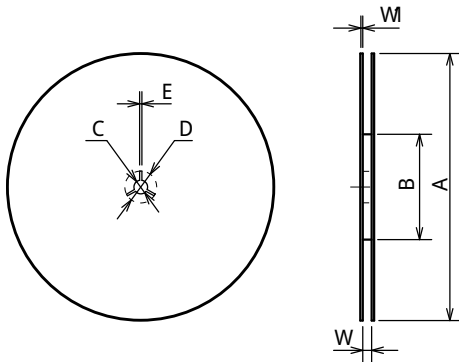
PACKING SPEC

TAPING DIMENSIONS



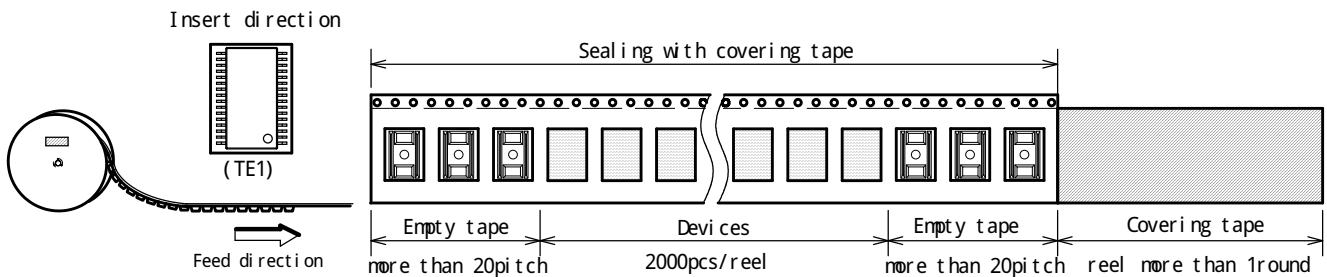
SYMBOL	DI MENSION	REMARKS
A	8.6± 0.1	BOTTOM DI MENSION
B	11.5± 0.1	BOTTOM DI MENSION
D0	1.5 ^{+0.1} ₀	
D1	2.0 ^{+0.1} ₀	
E	1.75± 0.1	
F	11.5± 0.01	
P0	4.0± 0.1	
P1	12.0± 0.1	
P2	2.0± 0.1	
T	0.3± 0.05	
T2	2.1± 0.1	
W	24.0± 0.3	
W1	21.0± 0.1	THICKNESS 0.1max

REEL DIMENSIONS

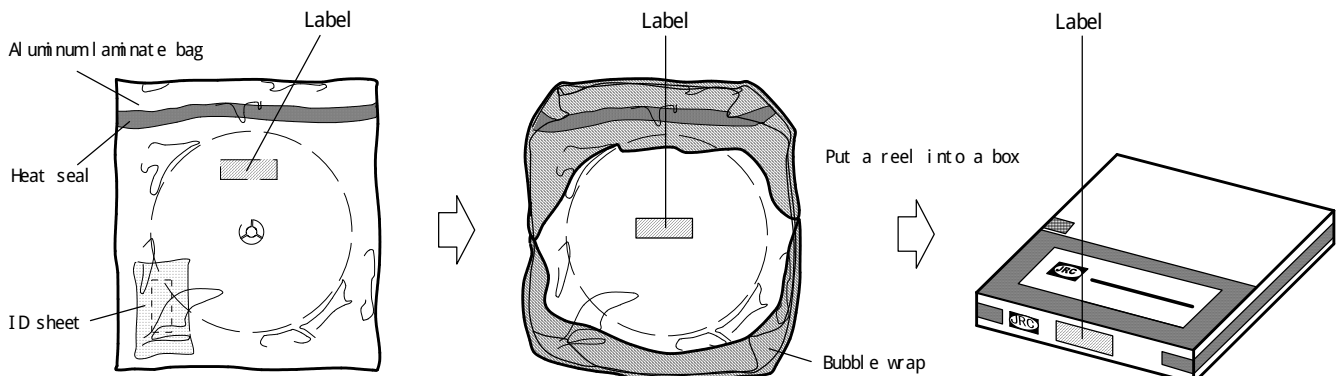


SYMBOL	DI MENSION
A	φ 330± 2
B	φ 80± 1
C	φ 13± 0.5
D	φ 21± 0.8
E	2± 0.5
W	25.5± 1.0
W1	2

TAPING STATE

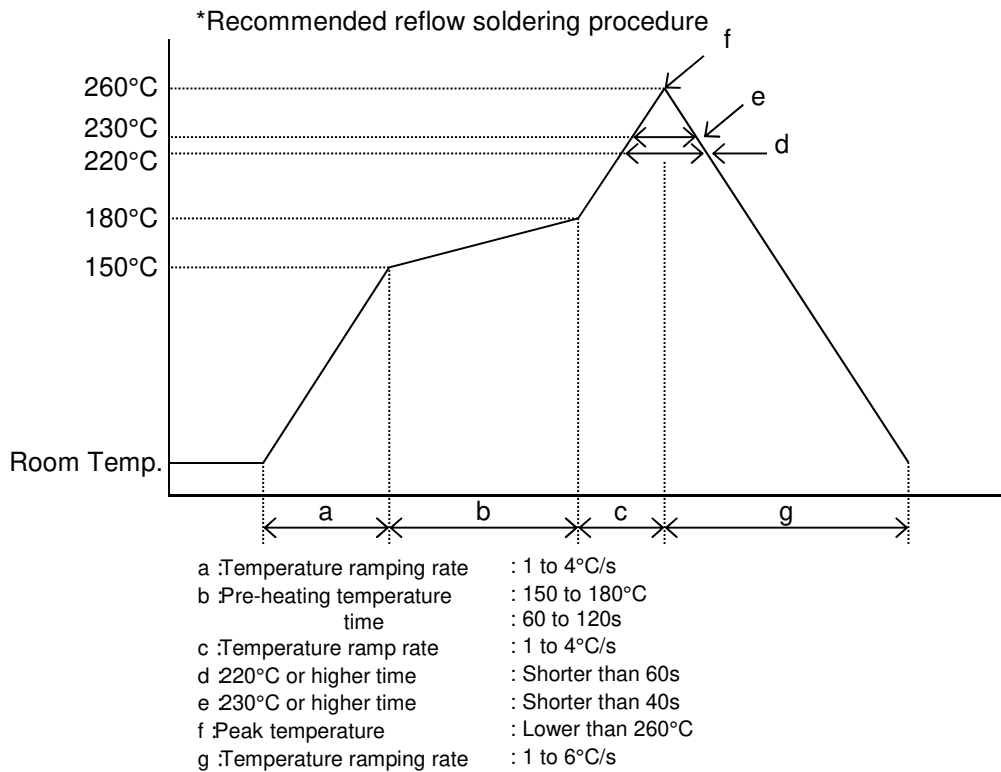


PACKING STATE



■RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING METHOD



The temperature indicates at the surface of mold package.

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Various Safety devices
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