

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	PUMH11F
Manufacturer:	Nexperia USA Inc.
Package:	6-TSSOP, SC-88, SOT-363
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nexperia-usa-inc/pumh11f.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



PUMH11

50 V, 100 mA NPN/NPN resistor-equipped double transistor;
R1 = 10 k Ω , R2 = 10 k Ω

15 July 2026

Product data sheet

1. General description

NPN/NPN double Resistor-Equipped Transistor (RET) in a very small SOT363-3 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PUMD3

PNP/PNP complement: PUMB11

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

3. Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

4. Quick reference data

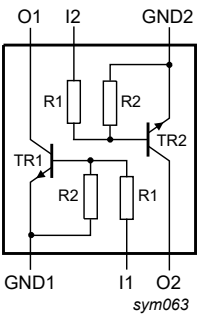
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	100	mA
R1	bias resistor 1 (input)	[1]	7	10	13	k Ω
R2/R1	bias resistor ratio	[1]	0.8	1	1.2	

[1] See "Section 11: Test information" for resistor calculation and test conditions.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 Transparent top view TSSOP6 (SOT363-3)	 <i>sym063</i>
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMH11	TSSOP6	Plastic surface-mounted package; 6 leads	SOT363-3

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMH11	H%1

[1] % = placeholder for manufacturing site code

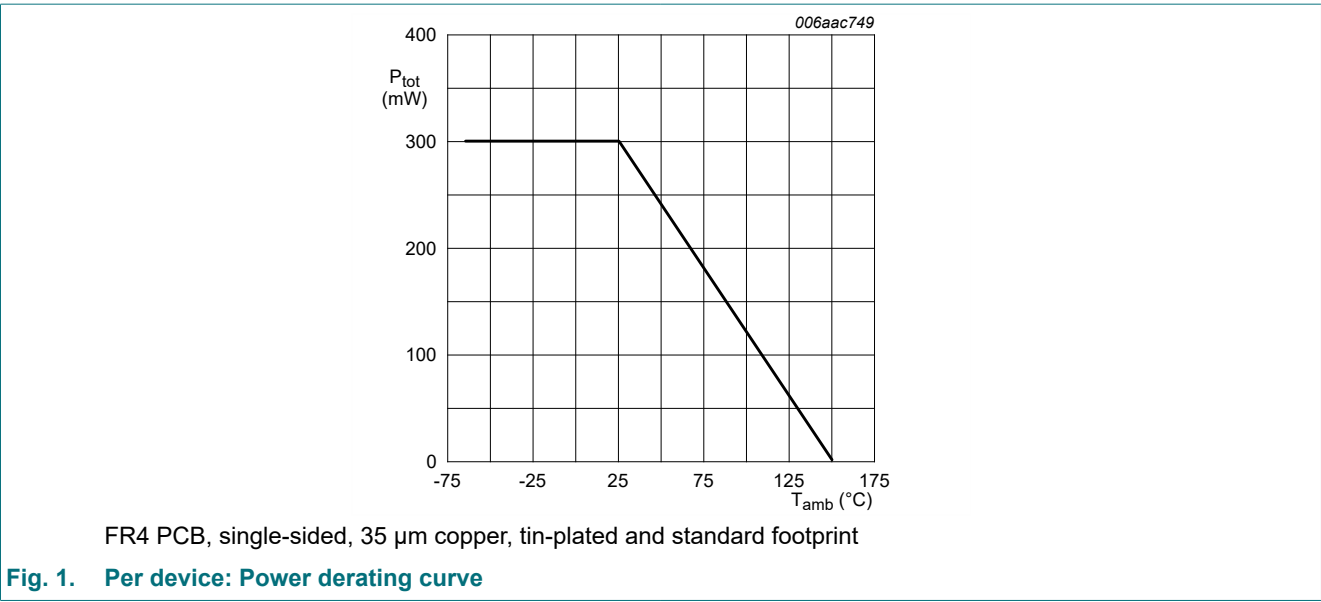
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	10	V
V _I	input voltage	positive		-	40	V
		negative		-	-10	V
I _O	output current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	200	mW
Per device						
P _{tot}	total power dissipation	T _{amb} = 25 °C	[1]	-	300	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.

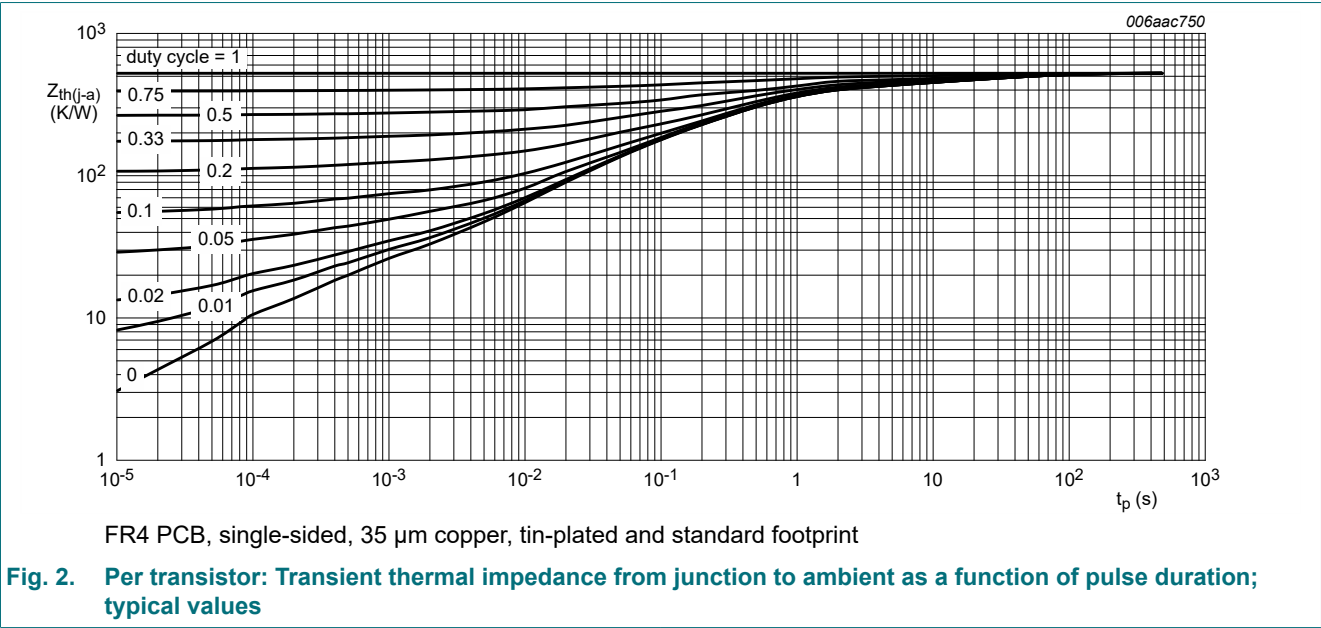


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.



10. Characteristics

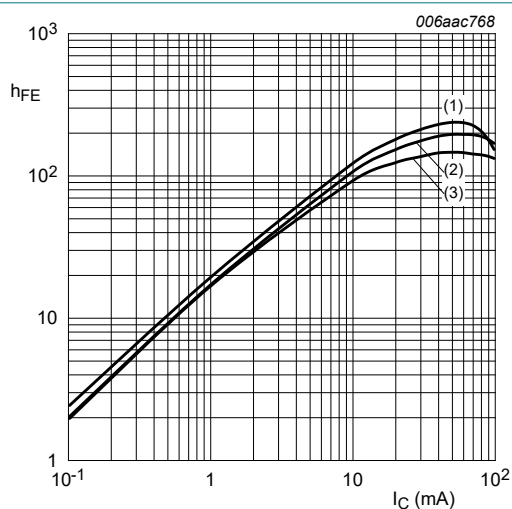
Table 7. Characteristics

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100\text{ }\mu\text{A}$; $I_E = 0\text{ A}$; $T_{amb} = 25\text{ °C}$	50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2\text{ mA}$; $I_B = 0\text{ A}$; $T_{amb} = 25\text{ °C}$	50	-	-	V
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}$; $I_E = 0\text{ A}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$	-	-	1	μA
		$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$; $T_J = 150\text{ °C}$	-	-	5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}$; $I_C = 0\text{ A}$	-	-	400	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}$; $I_C = 5\text{ mA}$	30	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}$; $I_B = 0.5\text{ mA}$	-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}$; $I_C = 100\text{ }\mu\text{A}$	-	1.1	0.8	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}$; $I_C = 10\text{ mA}$	2.5	1.8	-	V
R1	bias resistor 1 (input)	[1]	7	10	13	kΩ
R2/R1	bias resistor ratio	[1]	0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = 10\text{ V}$; $I_E = 0\text{ A}$; $i_e = 0\text{ A}$; $f = 1\text{ MHz}$	-	-	2.5	pF
f_T	transition frequency	$V_{CE} = 5\text{ V}$; $I_C = 10\text{ mA}$; $f = 100\text{ MHz}$	[2]	230	-	MHz

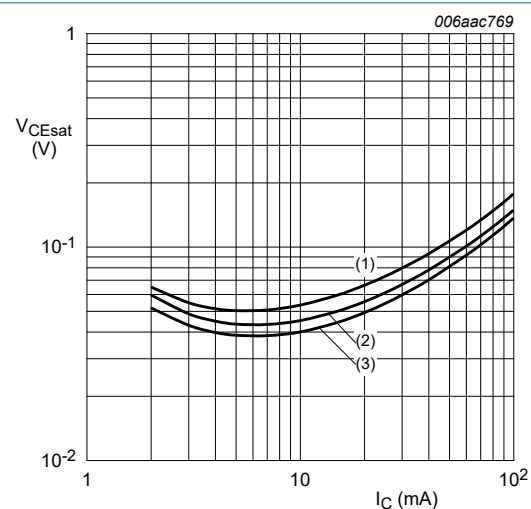
[1] See "Section 11: Test information" for resistor calculation and test conditions.

[2] Characteristics of built-in transistor



$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig. 3. DC current gain as a function of collector current; typical values



$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig. 4. Collector-emitter saturation voltage as a function of collector current; typical values

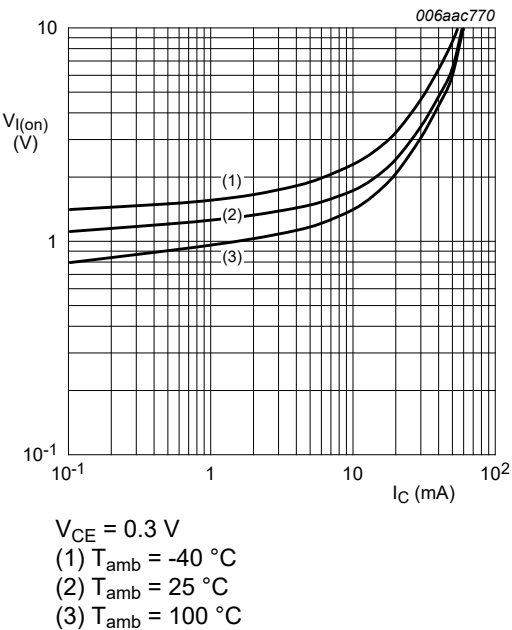


Fig. 5. On-state input voltage as a function of collector current; typical values

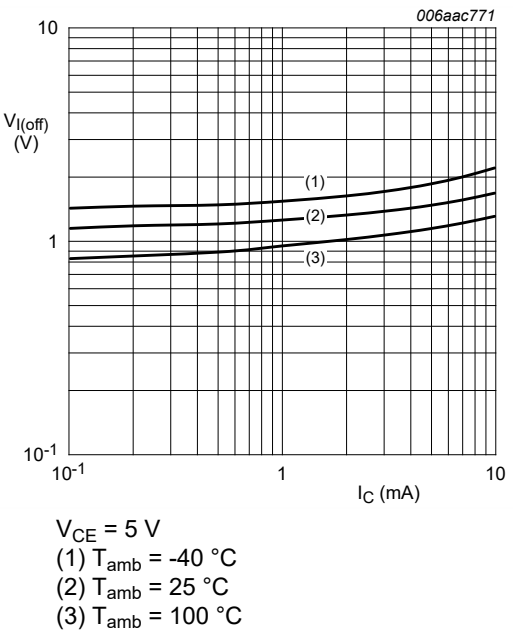


Fig. 6. Off-state input voltage as a function of collector current; typical values

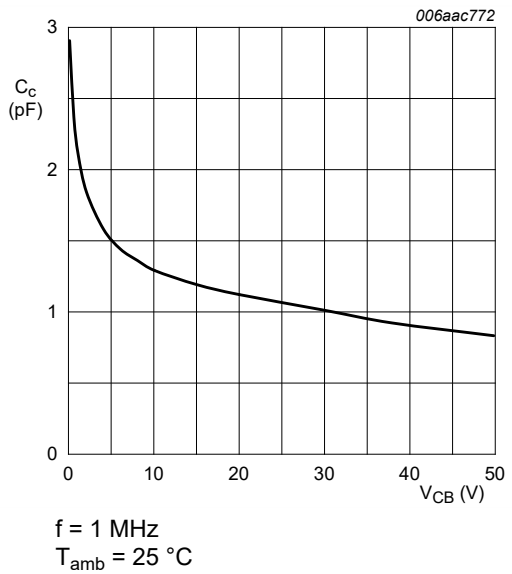


Fig. 7. Collector capacitance as a function of collector-base voltage; typical values

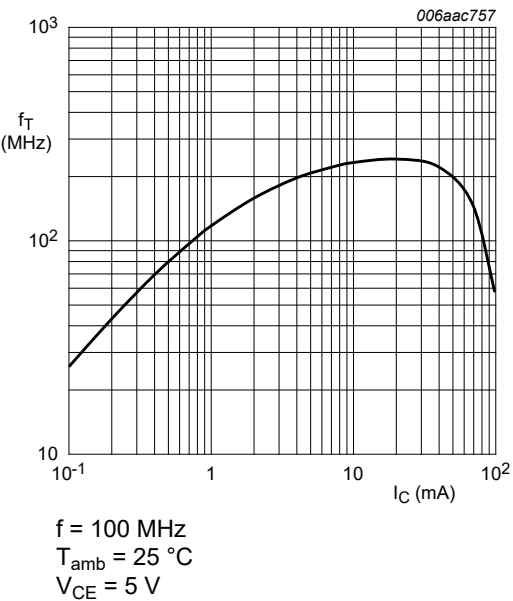


Fig. 8. Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

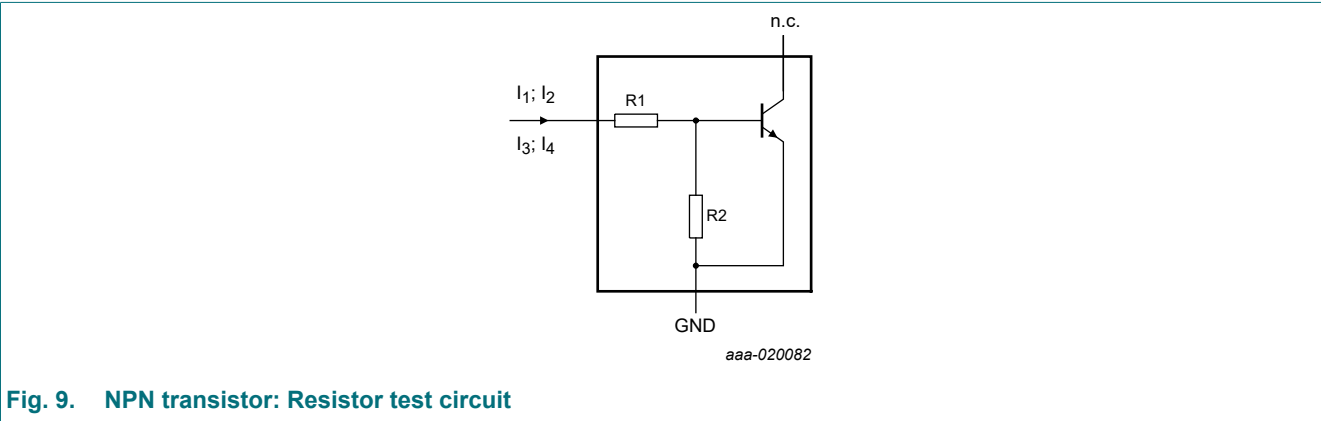


Fig. 9. NPN transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

PUMH11	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I1	I2	I3	I4
TR1 (NPN)	10	10	350 μA	450 μA	-350 μA	-450 μA
TR2 (NPN)	10	10	350 μA	450 μA	-350 μA	-450 μA

12. Package outline

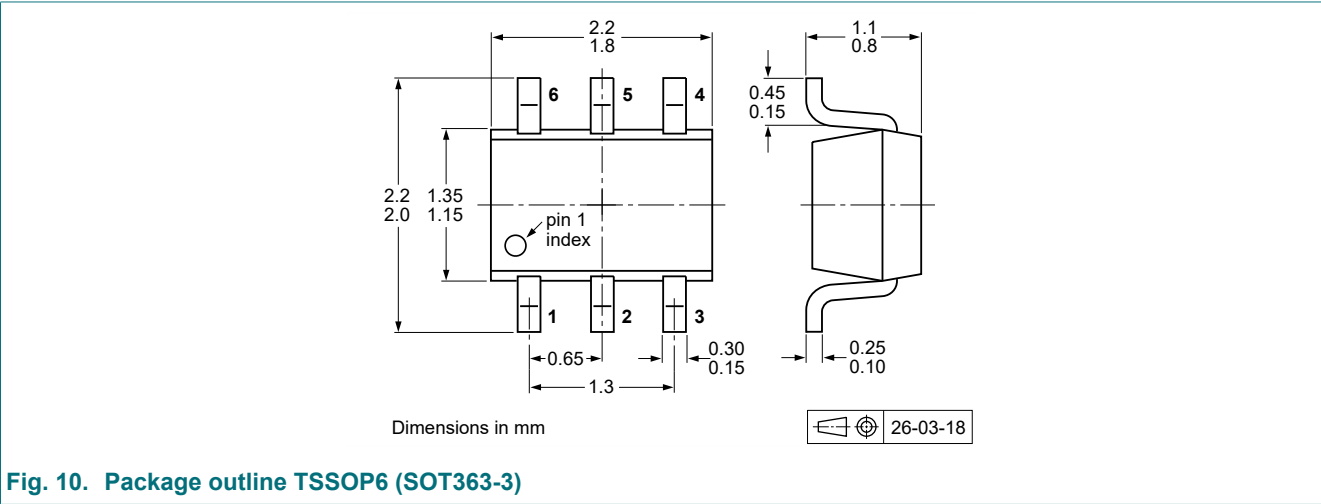


Fig. 10. Package outline TSSOP6 (SOT363-3)

13. Soldering

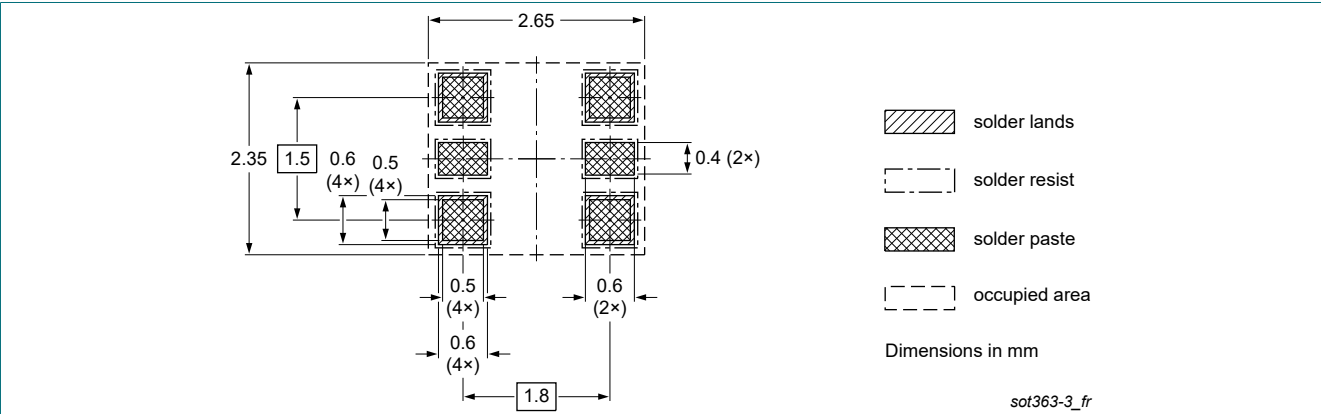


Fig. 11. Reflow soldering footprint for TSSOP6 (SOT363-3)

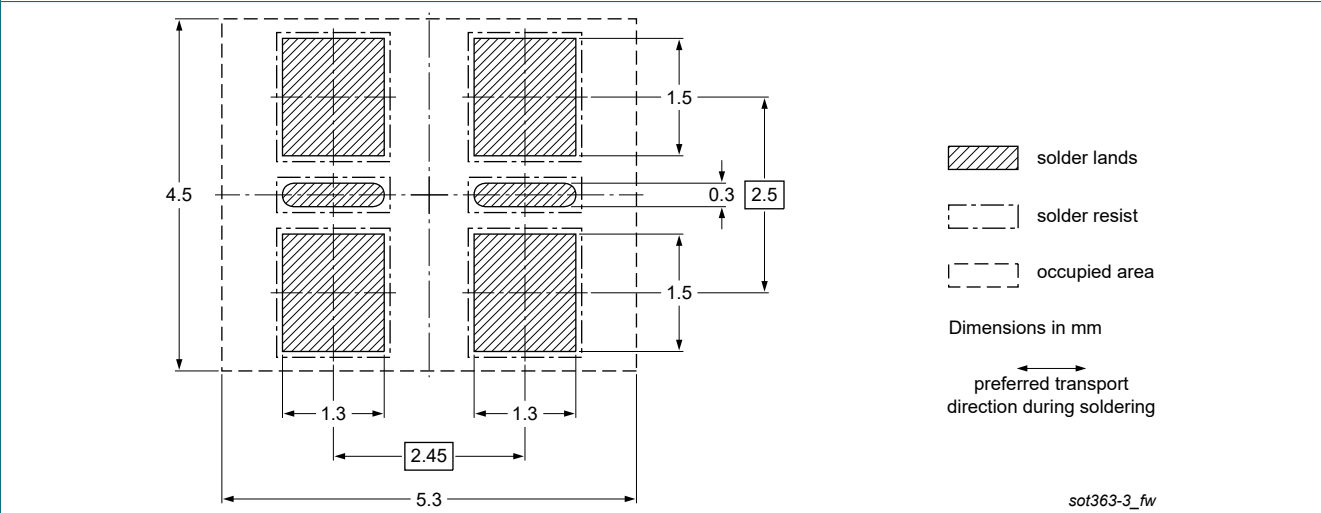


Fig. 12. Wave soldering footprint for TSSOP6 (SOT363-3)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMH11 v.8	20260715	Product data sheet	-	PUMH11 v.7
Modifications:	• Package changed from SOT363 to SOT363-3			
PUMH11 v.7	20221001	Product data sheet	-	PEMH11_PUMH11 v.6
PEMH11_PUMH11 v.6	20111129	Product data sheet	-	PEMH11_PUMH11 v.5
PEMH11_PUMH11 v.5	20031020	Product data sheet	-	PUMH11 v.4 PEMH11 v.1
PUMH11 v.4	19990413	Product specification	-	-
PEMH11 v.1	20011022	Preliminary specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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