ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	PUMD16,115
Manufacturer:	Nexperia USA Inc.
Package:	6-TSSOP, SC-88, SOT-363
Availability:	Please confirm with sales

Product Page:

https://antrexco.com/product/details/nexperia-usa-inc/pumd16-115.html

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

PUMD16

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 22 kΩ, R2 = 47 kΩ

27 July 2026 Product data sheet

1. General description

NPN/PNP double Resistor-Equipped Transistor (RET) in a very small SOT363-3 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PUMH16

PNP/PNP complement: PUMB16

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplified circuit design
- Reduces component count
- Reduces pick and place costs

3. Applications

- Low current peripheral driver
- Controlling IC inputs
- Replacement of general purpose transistors in digital applications

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{CEO}	collector-emitter voltage	open base	[1]	-	-	50	V
I_O	output current		[1]	-	-	100	mA
R1	bias resistor 1 (input)		[2]	15.4	22	28.6	kΩ
R2/R1	bias resistor ratio		[2]	1.7	2.1	2.6	

[1] For the PNP transistor with negative polarity.
[2] See section "Test information" for resistor calculation and test conditions.

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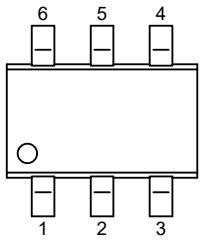
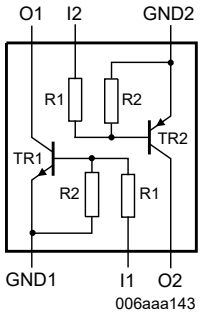
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 Transparent top view **TSSOP6 (SOT363-3)**	
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMD16	TSSOP6	Plastic surface-mounted package; 6 leads	SOT363-3

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMD16	D1%

[1] % = placeholder for manufacturing site code

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{CBO}	collector-base voltage	open emitter	[1]	-	50	V
V_{CEO}	collector-emitter voltage	open base	[1]	-	50	V
V_{EBO}	emitter-base voltage	open collector	[1]	-	5	V
V_I	input voltage	TR1 (NPN)		-7	40	V
		TR2 (PNP)		-40	7	V
I_O	output current		[1]	-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[2]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[2]	-	300	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] For the PNP transistor with negative polarity.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 100 µA; I_E = 0 A; T_{amb} = 25 °C	[1]	50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 2 mA; I_B = 0 A; T_{amb} = 25 °C	[1]	50	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A; T_{amb} = 25 °C	[1]	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A; T_{amb} = 25 °C	[1]	-	-	100	nA
		V_{CE} = 30 V; I_B = 0 A; T_j = 150 °C	[1]	-	-	5	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A; T_{amb} = 25 °C	[1]	-	-	120	µA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 5 mA; T_{amb} = 25 °C	[1]	80	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA; T_{amb} = 25 °C	[1]	-	-	150	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 µA; T_{amb} = 25 °C	[1]	-	0.8	0.5	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 2 mA; T_{amb} = 25 °C	[1]	2	1.1	-	V
R1	bias resistor 1 (input)		[2]	15.4	22	28.6	kΩ
R2/R1	bias resistor ratio		[2]	1.7	2.1	2.6	
TR1 (NPN)							
C_c	collector capacitance	V_{CB} = 10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	2.5	pF
TR2 (PNP)							
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	3	pF

[1] For the PNP transistor with negative polarity.
[2] See section "Test information" for resistor calculation and test conditions.

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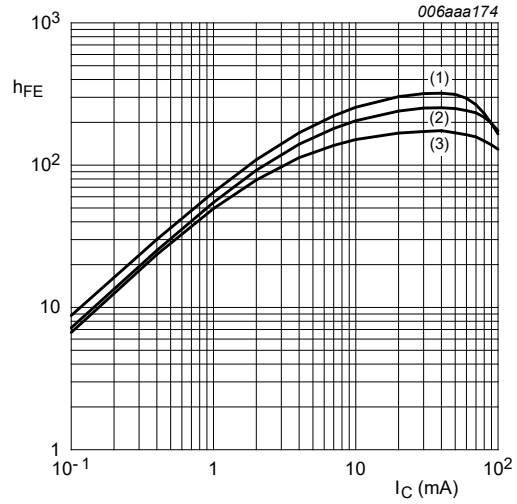
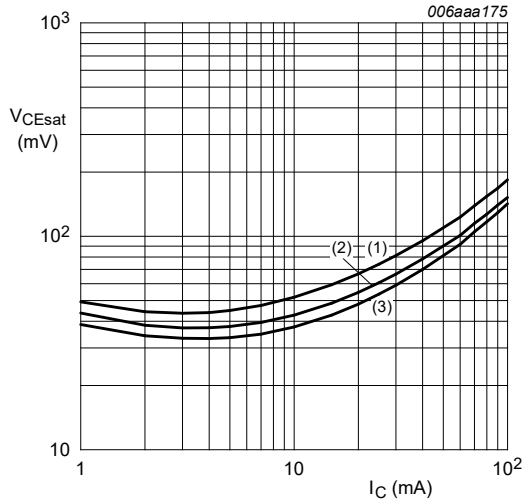


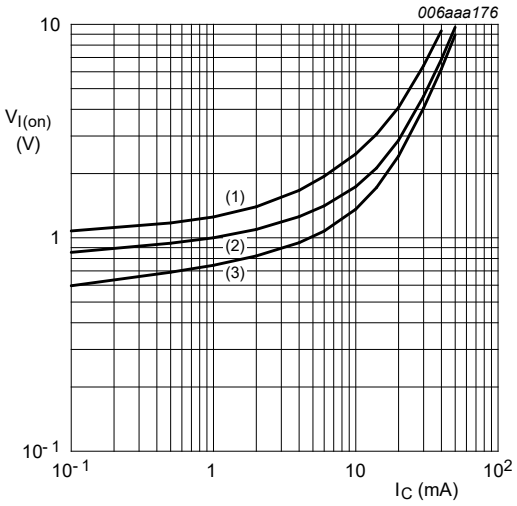
V_{CE} = 5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 1. TR1 (NPN): DC current gain as a function of collector current; typical values



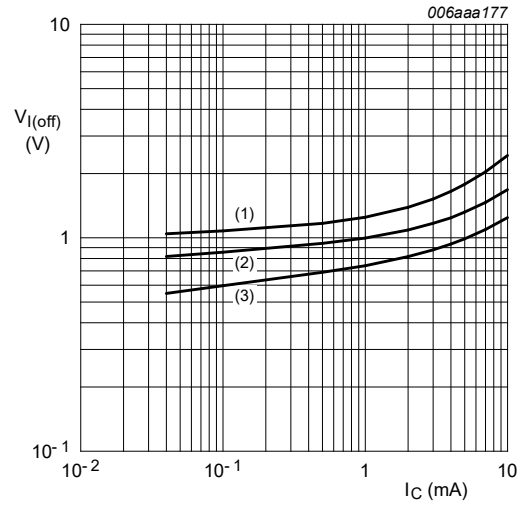
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 2. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



V_{CE} = 0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 3. TR1 (NPN): On-state input voltage as a function of collector current; typical values



V_{CE} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 4. TR1 (NPN): Off-state input voltage as a function of collector current; typical values

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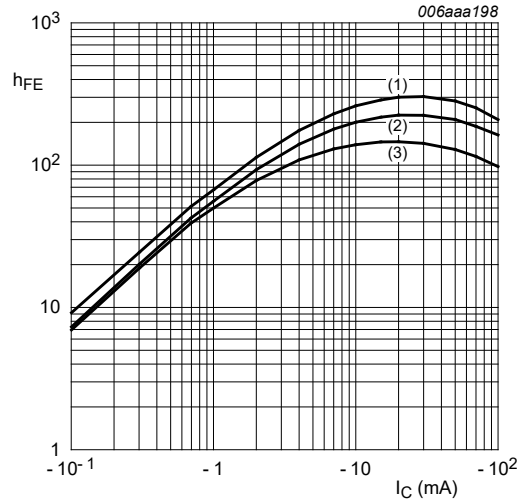
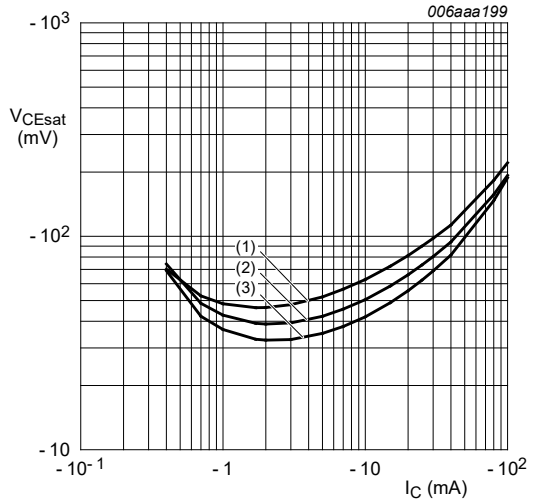


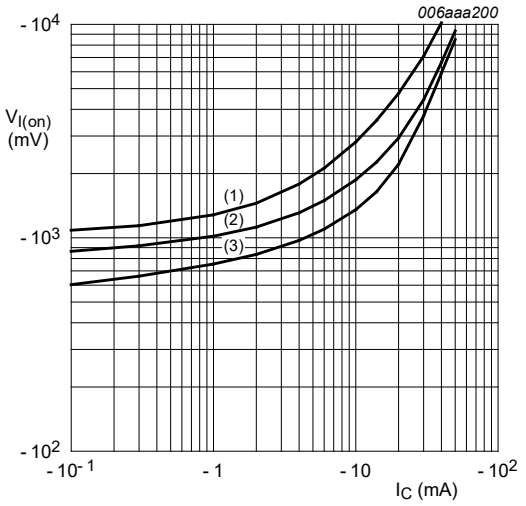
V_{CE} = -5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 5. TR2 (PNP): DC current gain as a function of collector current; typical values



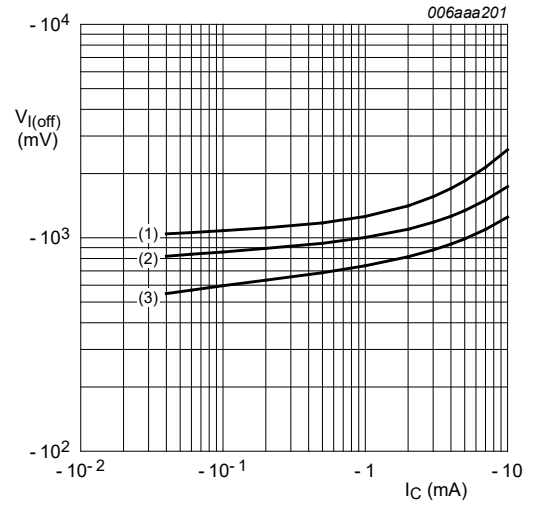
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 6. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



V_{CE} = -0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 7. TR2 (PNP): On-state input voltage as a function of collector current; typical values



V_{CE} = -5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 8. TR2 (PNP): Off-state input voltage as a function of collector current; typical values

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11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I_4) - V(I_3)}{R1 \cdot (I_4 - I_3)} - 1$$

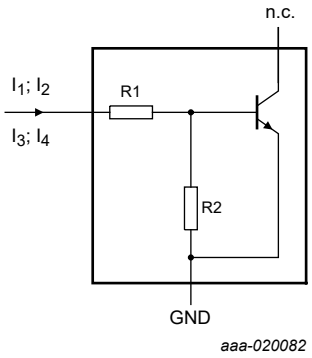

Fig. 9. NPN transistor: Resistor test circuit

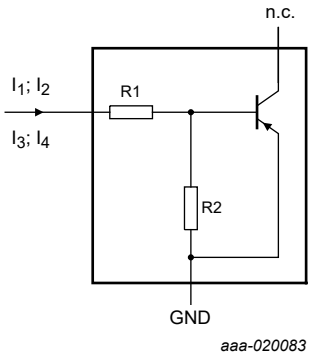

Fig. 10. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

PUMD16	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I_1	I_2	I_3	I_4
TR1 (NPN)	22	47	55 µA	105 µA	-55 µA	-105 µA
TR2 (PNP)	22	47	-55 µA	-105 µA	55 µA	105 µA

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12. Package outline

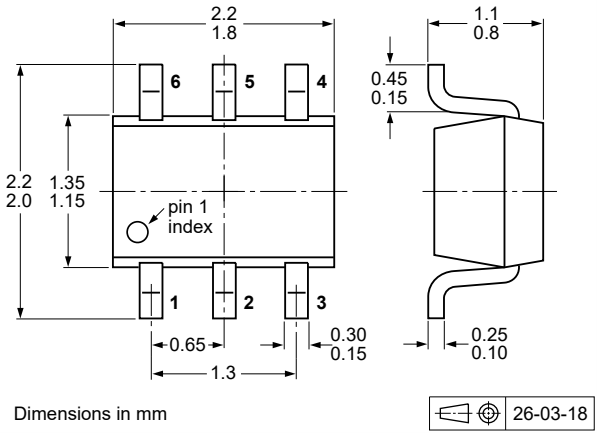

Fig. 11. Package outline TSSOP6 (SOT363-3)

13. Soldering

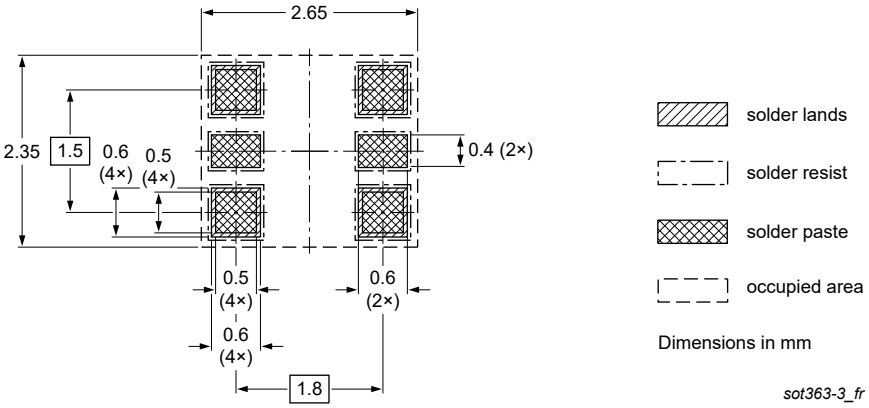

Fig. 12. Reflow soldering footprint for TSSOP6 (SOT363-3)

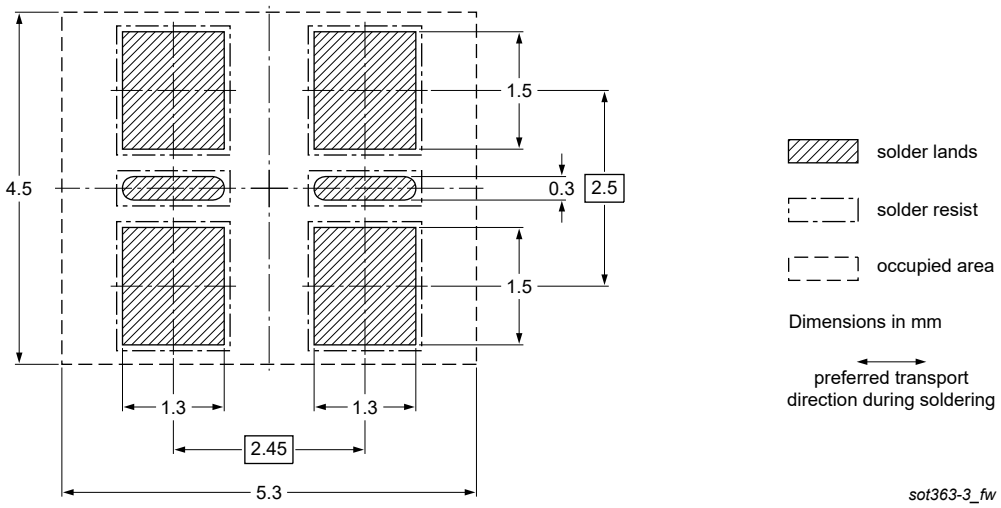

Fig. 13. Wave soldering footprint for TSSOP6 (SOT363-3)

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14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMD16 v.6	20260727	Product data sheet	-	PUMD16 v.5
Modifications:	• Package changed from SOT363 to SOT363-3			
PUMD16 v.5	20250507	Product data sheet	-	PUMD16 v.4
PUMD16 v.4	20230331	Product data sheet	-	PEMD16_PUMD16 v.3
PEMD16_PUMD16 v.3	20110628	Product data sheet	-	PEMD16_PUMD16 v.2
PEMD16_PUMD16 v.2	20050607	Product data sheet	-	PUMD16 v.1
PUMD16 v.1	20031022	Product specification	-	-

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 27 July 2026