

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	PUMB2,115
Manufacturer:	Nexperia USA Inc.
Package:	6-TSSOP, SC-88, SOT-363
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nexperia-usa-inc/pumb2-115.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



PUMB2

50 V, 100 mA PNP/PNP resistor-equipped double transistor;
R1 = 47 k Ω , R2 = 47 k Ω

22 July 2026

Product data sheet

1. General description

PNP/PNP double Resistor-Equipped Transistor (RET) in a very small SOT363-3 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PUMD12

NPN/NPN complement: PUMH2

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

3. Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

4. Quick reference data

Table 1. Quick reference data

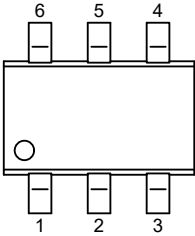
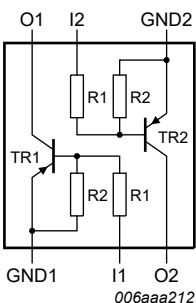
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V _{CEO}	collector-emitter voltage	open base	-	-	-50	V
I _O	output current		-	-	-100	mA
R1	bias resistor 1 (input)	[1]	33	47	61	k Ω
R2/R1	bias resistor ratio	[1]	0.8	1	1.2	

[1] See "Test information" for resistor calculation and test conditions.

50 V, 100 mA PNP/PNP resistor-equipped double transistor; R1 = 47 kΩ, R2 = 47 kΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 Transparent top view TSSOP6 (SOT363-3)	 006aaa212
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMB2	TSSOP6	Plastic surface-mounted package; 6 leads	SOT363-3

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMB2	B%2

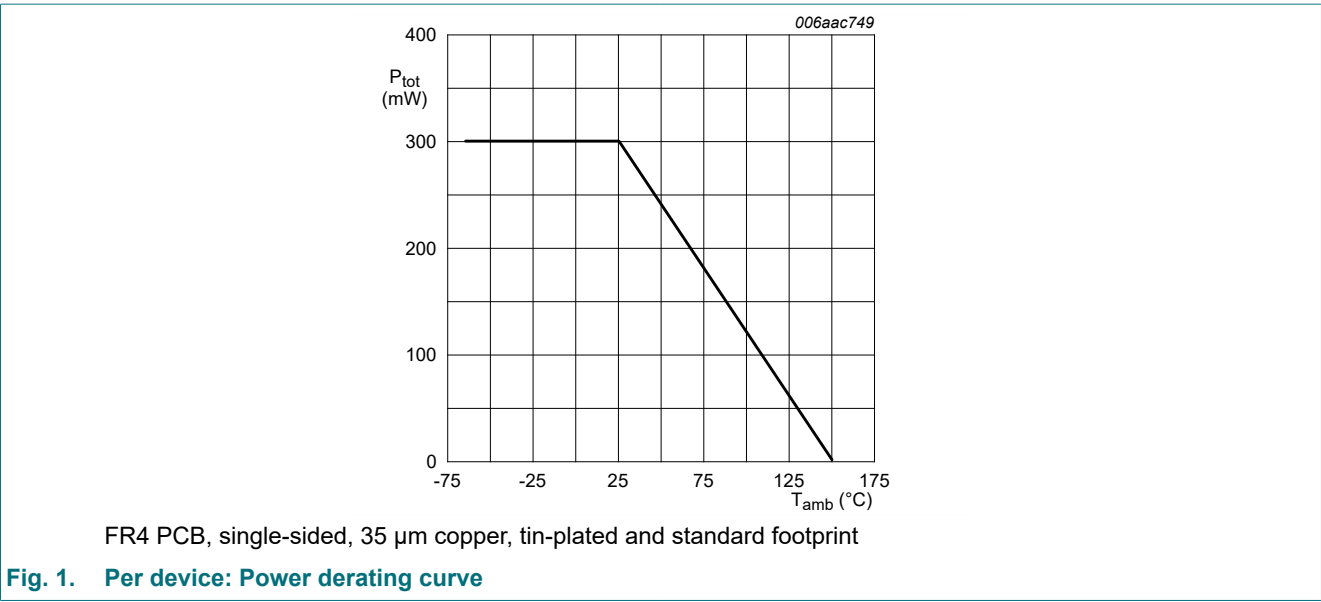
[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{CBO}	collector-base voltage	open emitter		-	-50	V
V _{CEO}	collector-emitter voltage	open base		-	-50	V
V _{EBO}	emitter-base voltage	open collector		-	-10	V
V _I	input voltage	positive		-	10	V
		negative		-	-40	V
I _O	output current			-	-100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	200	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	300	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.

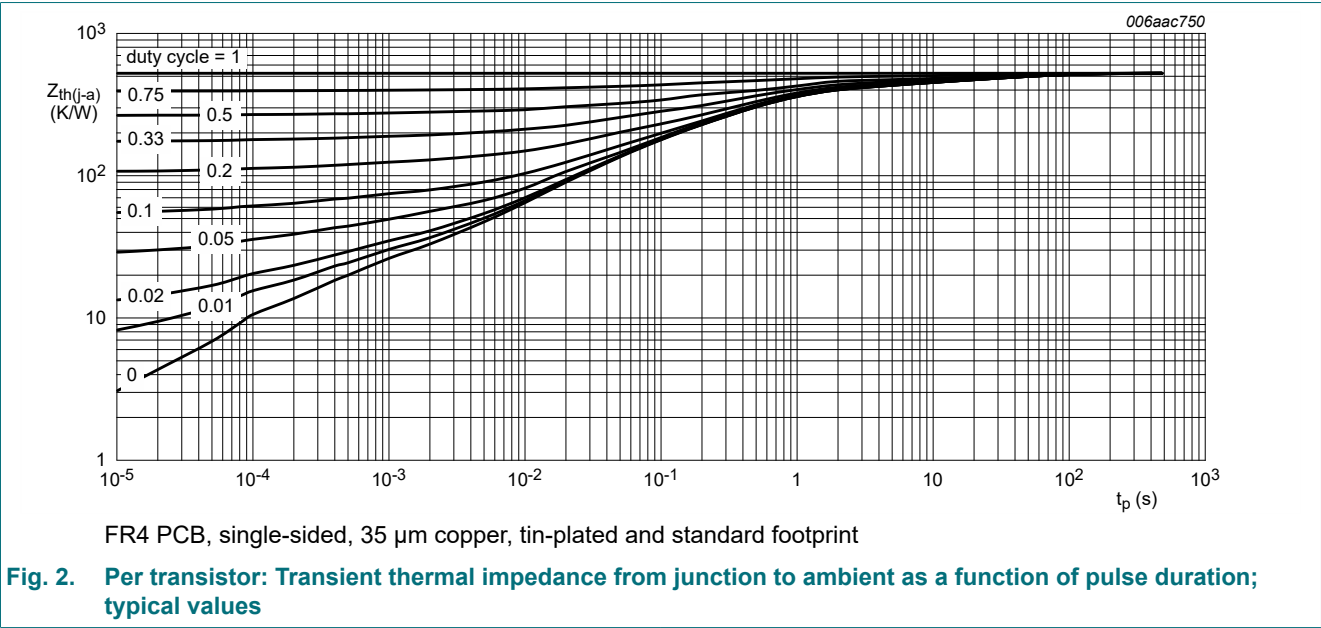


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.

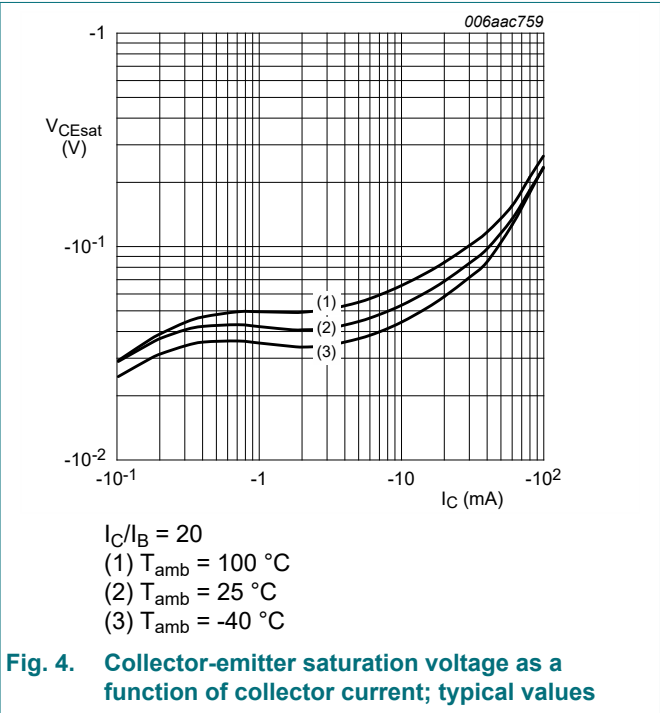
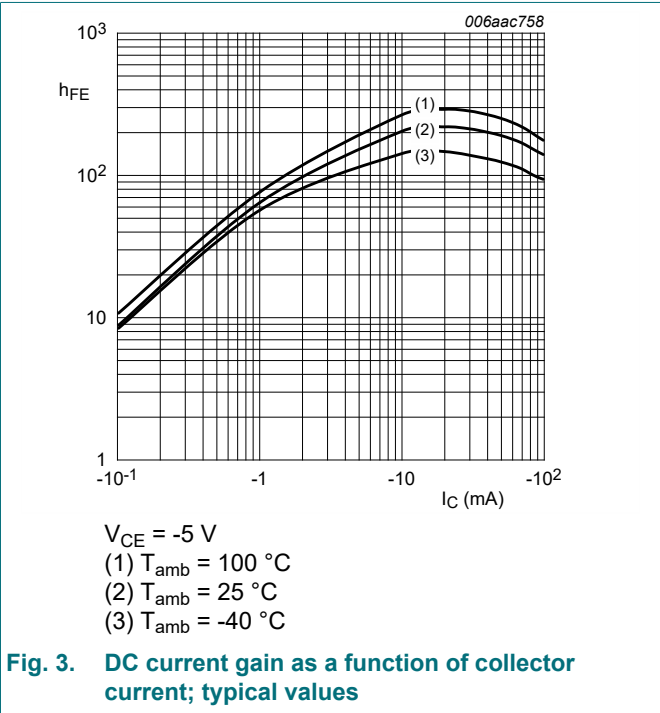


10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = -100 \mu A$; $I_E = 0 A$; $T_{amb} = 25 \text{ }^{\circ}C$	-50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = -2 \text{ mA}$; $I_B = 0 A$; $T_{amb} = 25 \text{ }^{\circ}C$	-50	-	-	V
I_{CBO}	collector-base cut-off current	$V_{CB} = -50 \text{ V}$; $I_E = 0 A$; $T_{amb} = 25 \text{ }^{\circ}C$	-	-	-100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = -30 \text{ V}$; $I_B = 0 A$; $T_{amb} = 25 \text{ }^{\circ}C$	-	-	-100	nA
		$V_{CE} = -30 \text{ V}$; $I_B = 0 A$; $T_j = 150 \text{ }^{\circ}C$	-	-	-5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5 \text{ V}$; $I_C = 0 A$; $T_{amb} = 25 \text{ }^{\circ}C$	-	-	-90	μA
h_{FE}	DC current gain	$V_{CE} = -5 \text{ V}$; $I_C = -5 \text{ mA}$; $T_{amb} = 25 \text{ }^{\circ}C$	80	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10 \text{ mA}$; $I_B = -0.5 \text{ mA}$; $T_{amb} = 25 \text{ }^{\circ}C$	-	-	-150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5 \text{ V}$; $I_C = -100 \mu A$; $T_{amb} = 25 \text{ }^{\circ}C$	-	-1.2	-0.8	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3 \text{ V}$; $I_C = -2 \text{ mA}$; $T_{amb} = 25 \text{ }^{\circ}C$	-3	-1.6	-	V
R1	bias resistor 1 (input)	[1]	33	47	61	kΩ
R2/R1	bias resistor ratio	[1]	0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = -10 \text{ V}$; $I_E = 0 A$; $i_e = 0 A$; $f = 1 \text{ MHz}$; $T_{amb} = 25 \text{ }^{\circ}C$	-	-	3	pF
f_T	transition frequency	$V_{CE} = -5 \text{ V}$; $I_C = -10 \text{ mA}$; $f = 100 \text{ MHz}$; $T_{amb} = 25 \text{ }^{\circ}C$	[2]	180	-	MHz

- [1] See "Test information" for resistor calculation and test conditions.
 [2] Characteristics of built-in transistor



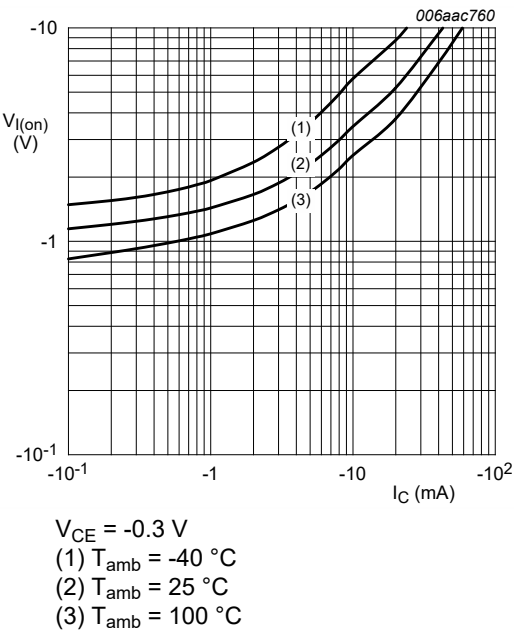


Fig. 5. On-state input voltage as a function of collector current; typical values

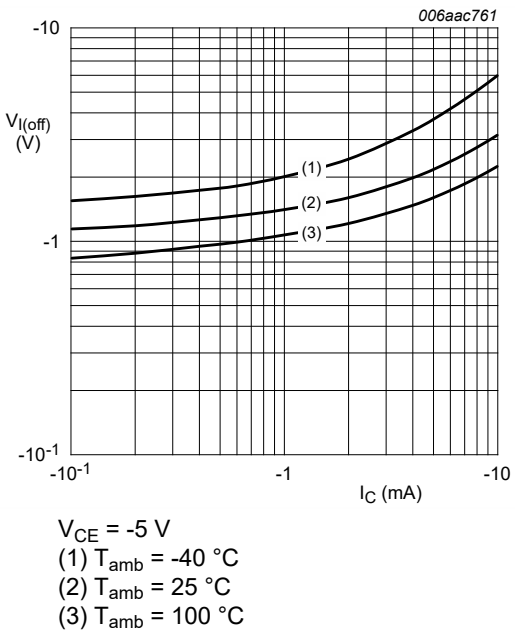


Fig. 6. Off-state input voltage as a function of collector current; typical values

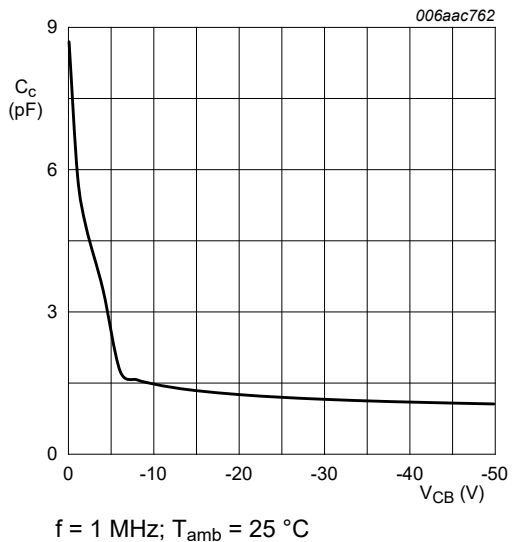


Fig. 7. Collector capacitance as a function of collector-base voltage; typical values

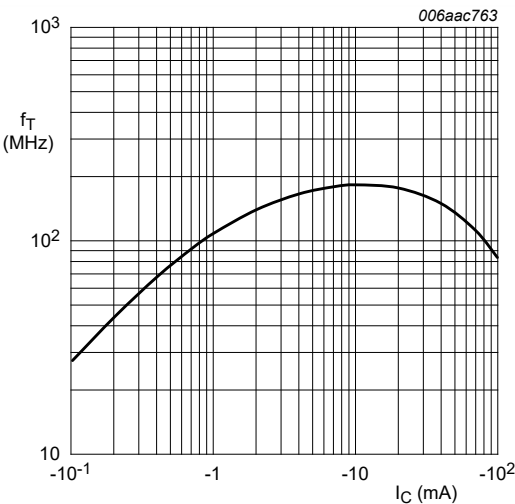


Fig. 8. Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

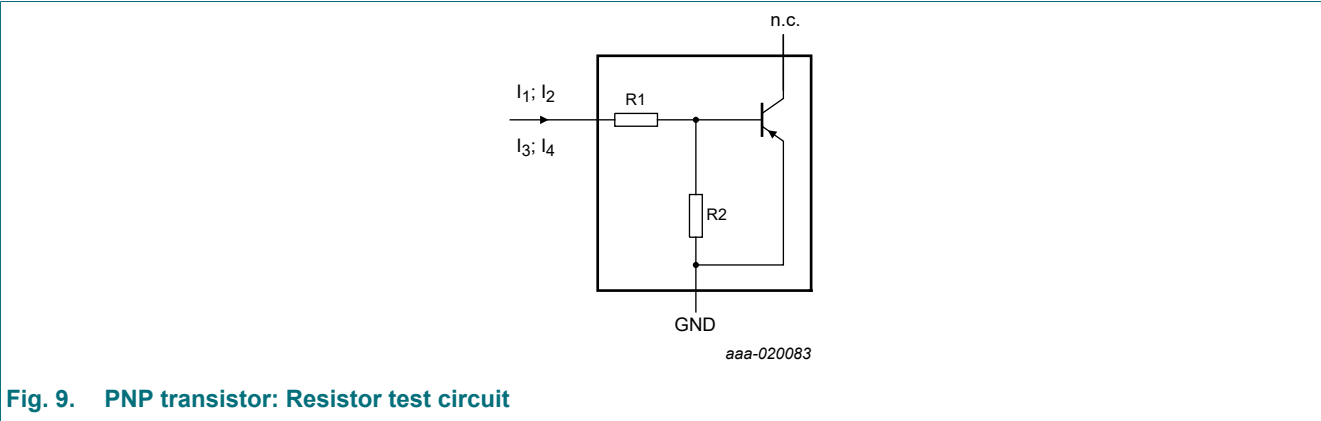


Fig. 9. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Per transistor

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I1	I2	I3	I4
PUMB2	47	47	-55 μA	-105 μA	55 μA	105 μA

12. Package outline

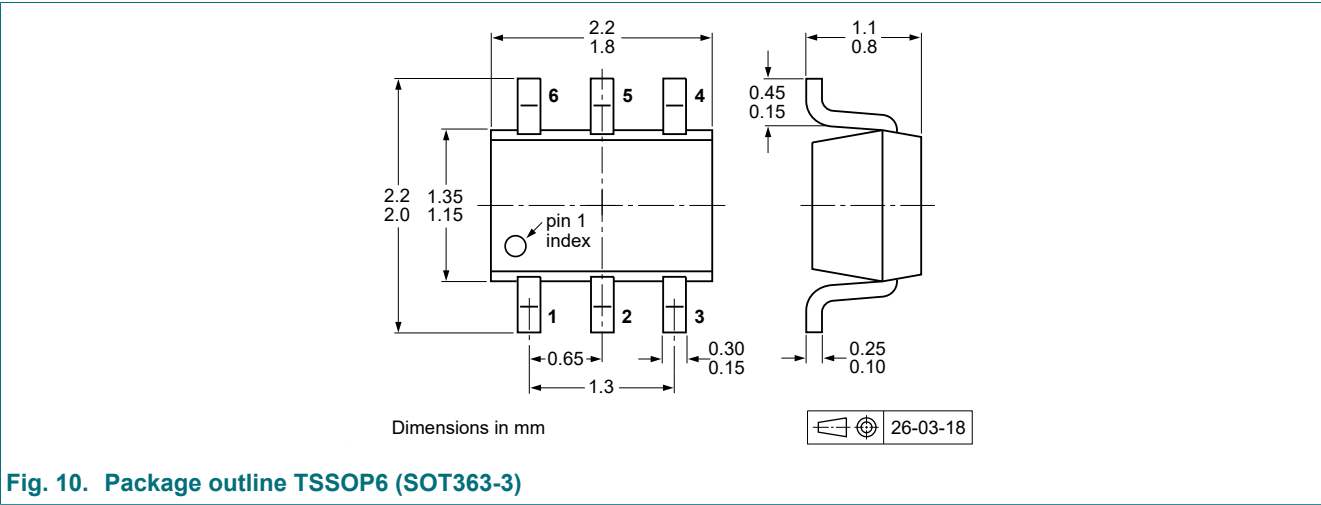


Fig. 10. Package outline TSSOP6 (SOT363-3)

13. Soldering

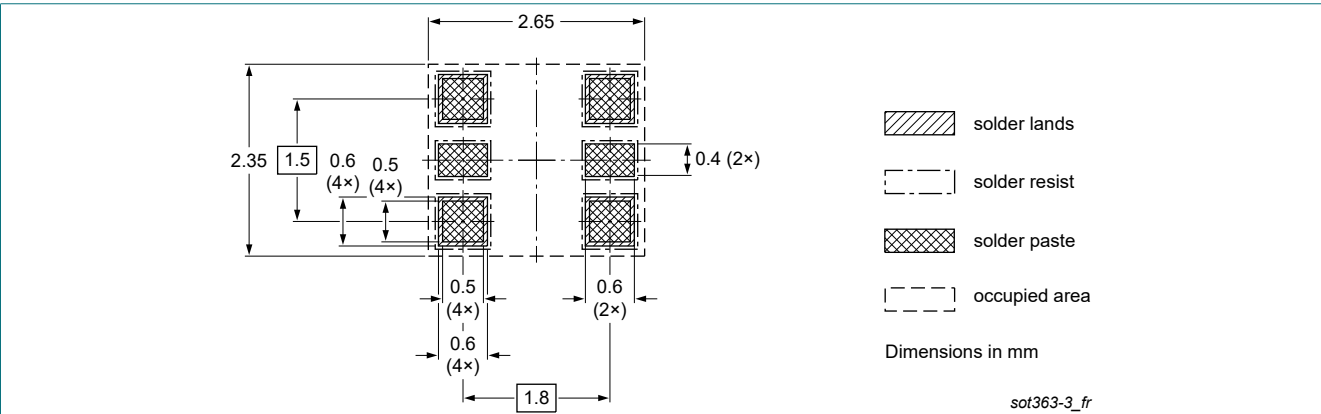


Fig. 11. Reflow soldering footprint for TSSOP6 (SOT363-3)

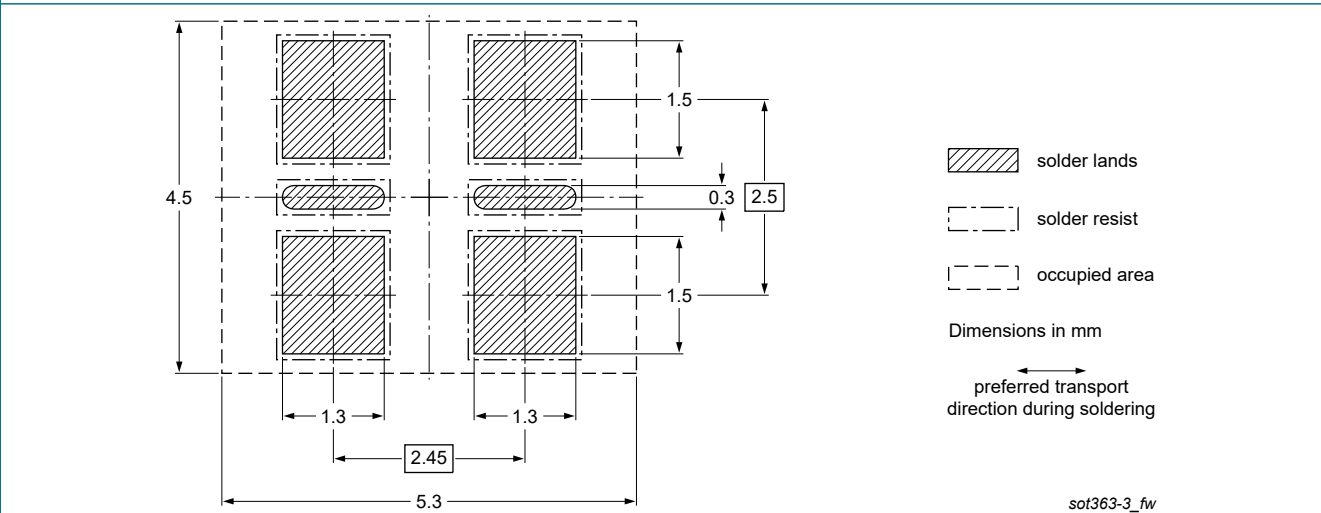


Fig. 12. Wave soldering footprint for TSSOP6 (SOT363-3)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMB2 v.6	20260722	Product data sheet	-	PUMB2 v.5
Modifications:	• Package changed from SOT363 to SOT363-3			
PUMB2 v.5	20230719	Product data sheet	-	PUMB2 v.4
PUMB2 v.4	20230104	Product data sheet	-	PEMB2_PUMB2 v.3
PEMB2_PUMB2 v.3	20111117	Product data sheet	-	PEMB2_PUMB2 v.2
PEMB2_PUMB2 v.2	20031015	Product data sheet	-	PUMB2 v.1 PEMB2 v.1
PEMB2 v.1	20010914	Product specification	-	-
PUMB2 v.1	19910803	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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