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Electronic Components Sourcing Information

Product Reference Information

Part Number:	PSMP033-60YEX
Manufacturer:	Nexperia USA Inc.
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nexperia-usa-inc/psmp033-60yex.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



PSMP033-60YE

60 V, P-channel Trench MOSFET

13 January 2021

Product data sheet

1. General description

P-channel enhancement mode MOSFET in an LFPAK56 (Power SO8) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- High thermal power dissipation capability
- Suitable for thermally demanding environments due to 175 °C rating
- Trench MOSFET technology

3. Applications

- Reverse battery protection
- Power management
- High-side load switch
- Motor drive

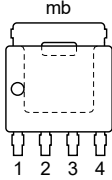
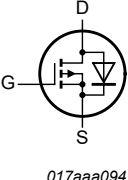
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = -10\text{ V}; T_{mb} = 25\text{ °C}$	-	-	-30	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	-	-	110	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -7\text{ A}; T_j = 25\text{ °C}$	-	26	33	mΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56; Power-SO8 (SOT669)	 017aaa094
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMP033-60YE	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMP033-60YE	03360YE

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-60	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = -10 V; T _{mb} = 25 °C		-	-30	A
		V _{GS} = -10 V; T _{mb} = 100 °C		-	-21	A
I _{DM}	peak drain current	single pulse; t _p ≤ 10 μs; T _{mb} = 25 °C		-	-120	A
P _{tot}	total power dissipation	T _{mb} = 25 °C		-	110	W
T _j	junction temperature			-55	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-65	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	-30	A
I _{SM}	peak source current	single pulse; t _p ≤ 10 μs; T _{mb} = 25 °C		-	-120	A
ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM	[1]	-	1000	V
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	T _{j(initial)} = 25 °C; I _D = -2.8 A; DUT in avalanche (unclamped)		-	85	mJ

[1] Measured between all pins.

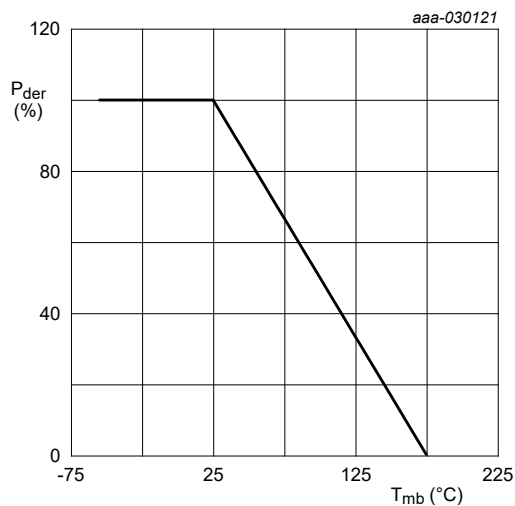


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

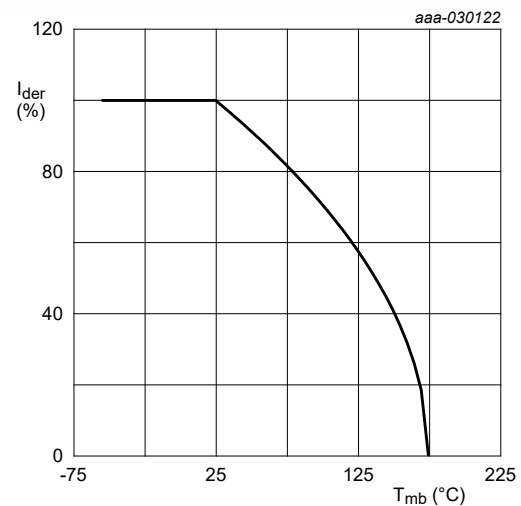
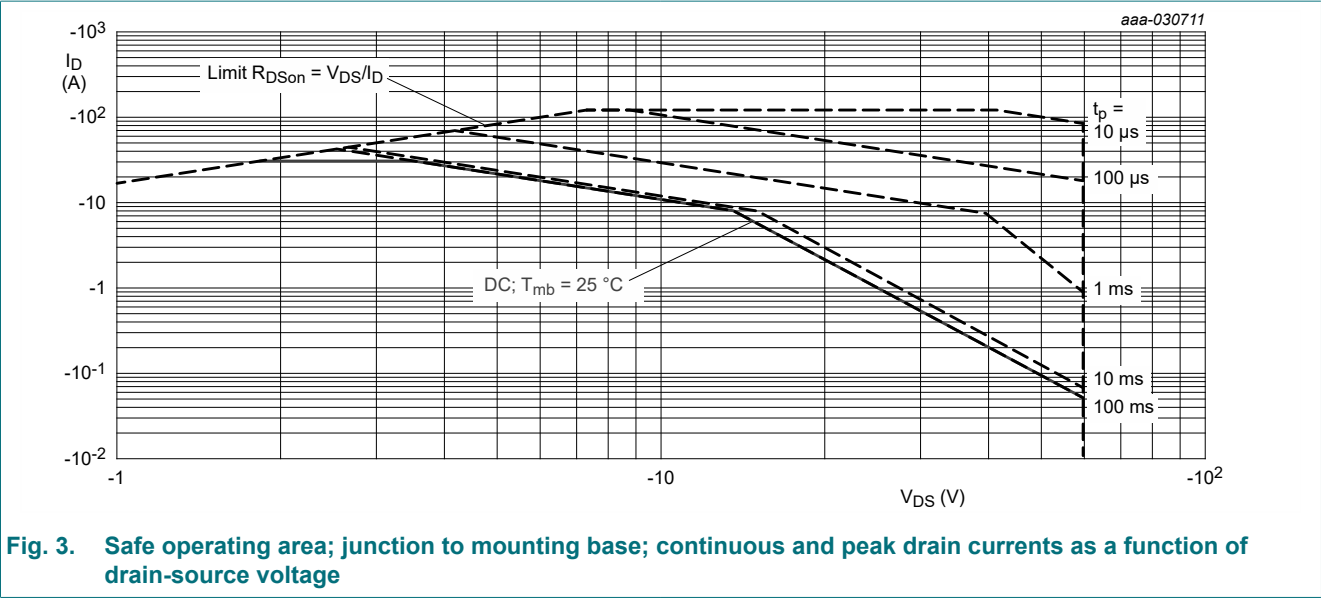


Fig. 2. Normalized continuous drain current as a function of mounting base temperature



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	83	91	K/W
			[2]	-	46	51	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	1.1	1.4	K/W

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-60	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} =V _{GS} ; T _j = 25 °C		-1.5	-2	-3	V
I _{DSS}	drain leakage current	V _{DS} = -60 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
		V _{DS} = -60 V; V _{GS} = 0 V; T _j = 125 °C		-	-	-10	μA
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -10 V; I _D = -7 A; T _j = 25 °C		-	26	33	mΩ
		V _{GS} = -10 V; I _D = -7 A; T _j = 175 °C		-	55	69	mΩ
		V _{GS} = -4.5 V; I _D = -6.7 A; T _j = 25 °C		-	30	36	mΩ
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -4.8 A; T _j = 25 °C		-	99	-	S
R _G	gate resistance	f = 1 MHz		-	6.1	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -30 V; I _D = -7 A; V _{GS} = -10 V; T _j = 25 °C		-	46	69	nC
Q _{GS}	gate-source charge			-	7.3	-	nC
Q _{GD}	gate-drain charge			-	9.4	-	nC
C _{iss}	input capacitance	V _{DS} = -30 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	2590	-	pF
C _{oss}	output capacitance			-	202	-	pF
C _{rss}	reverse transfer capacitance			-	118	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -30 V; I _D = -7 A; V _{GS} = -10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	9	-	ns
t _r	rise time			-	16	-	ns
t _{d(off)}	turn-off delay time			-	81	-	ns
t _f	fall time			-	310	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -30 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.7	-1.2	V
t _{rr}	reverse recovery time	I _S = -30 A; dI _S /dt = 100 A/μs;		-	32	-	ns
Q _r	recovered charge	V _{GS} = -10 V; V _{DS} = -30 V; T _j = 25 °C		-	18	-	nC

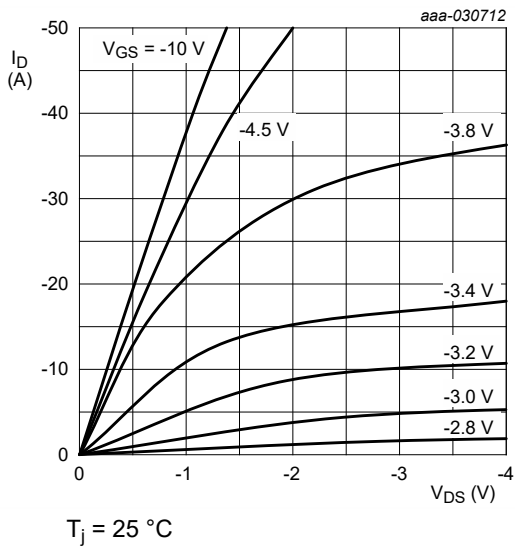


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

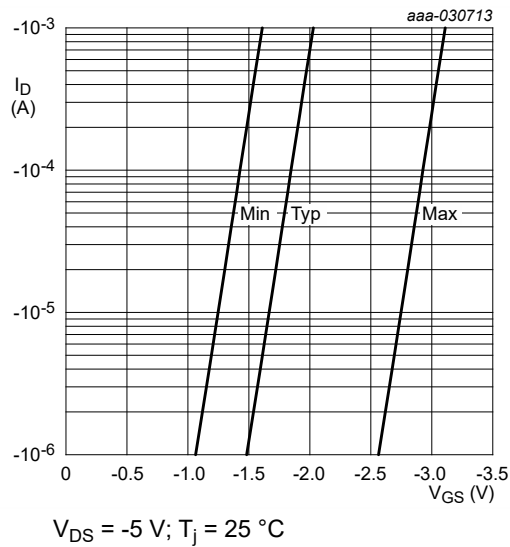


Fig. 6. Sub-threshold drain current as a function of gate-source voltage

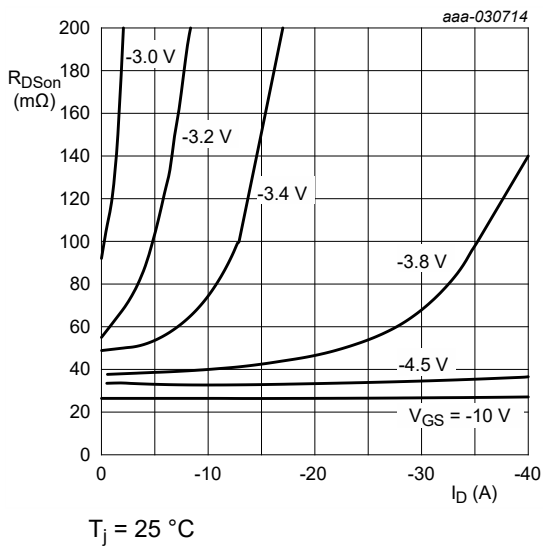


Fig. 7. Drain-source on-state resistance as a function of drain current; typical values

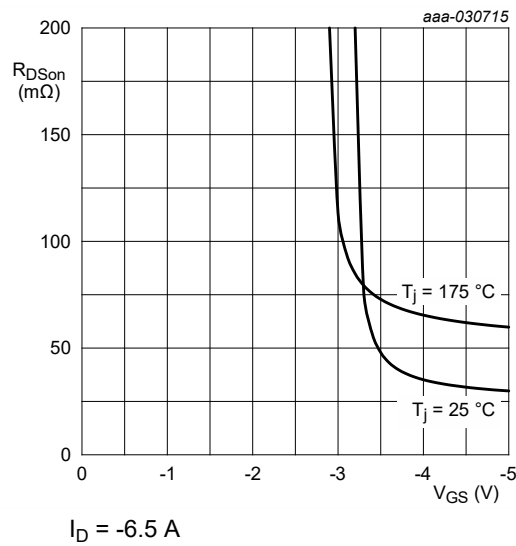
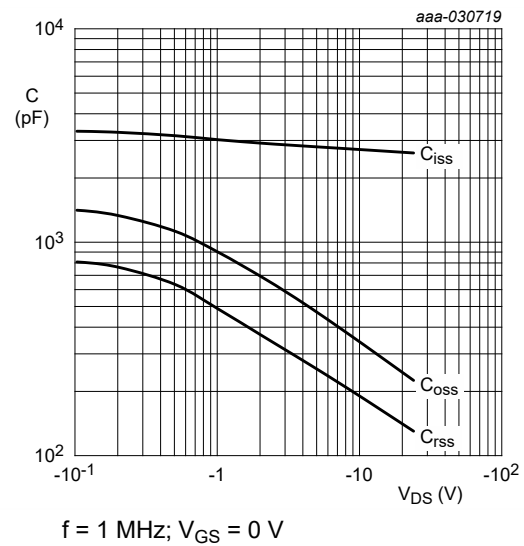
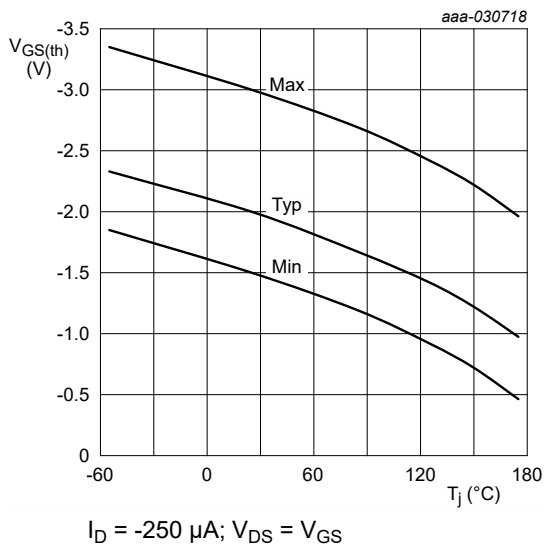
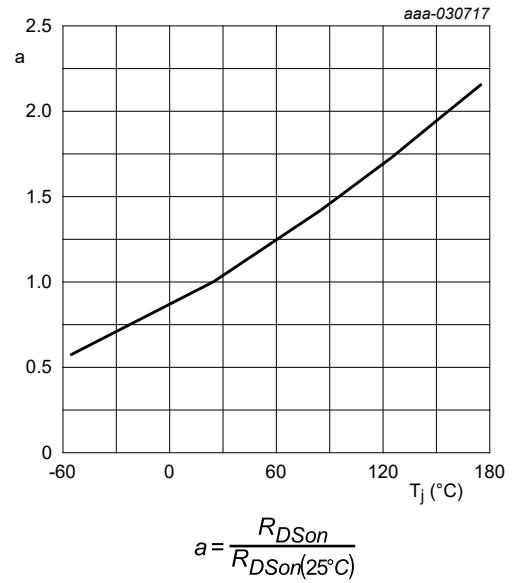
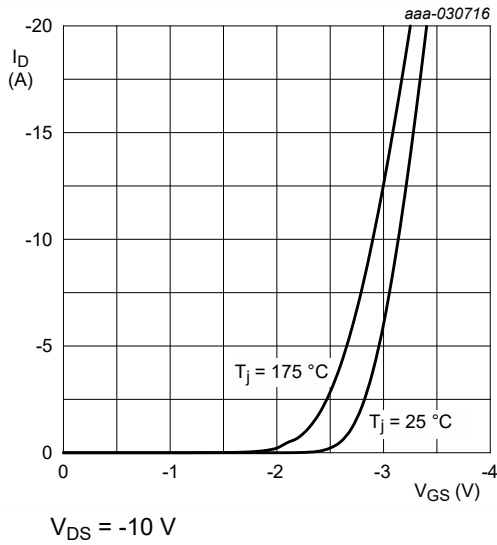


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



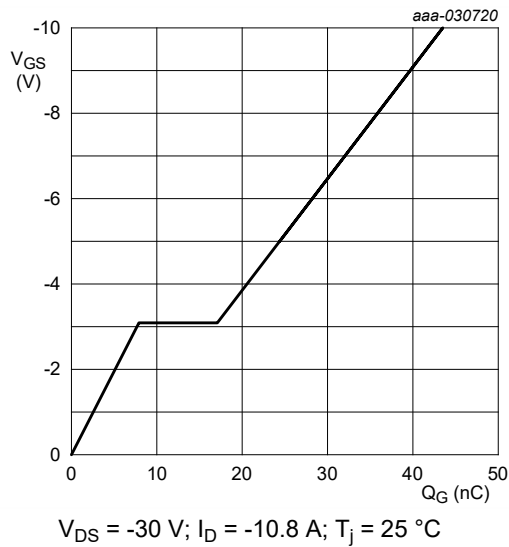


Fig. 13. Gate-source voltage as a function of gate charge; typical values

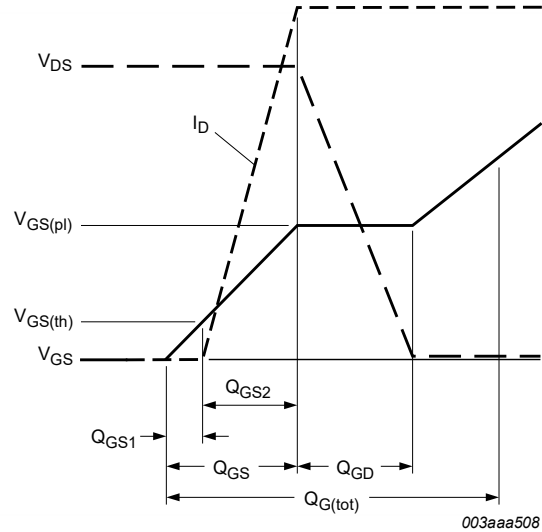


Fig. 14. Gate charge waveform definitions

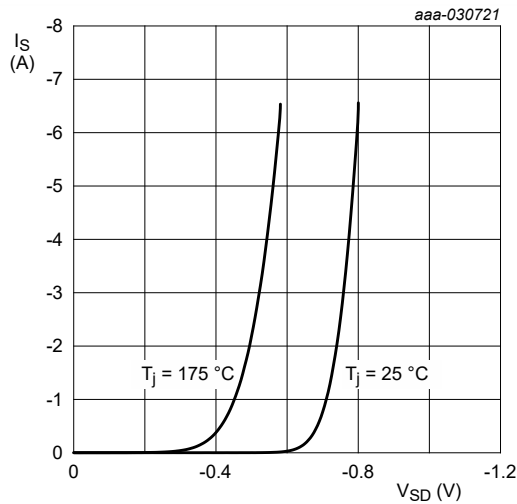
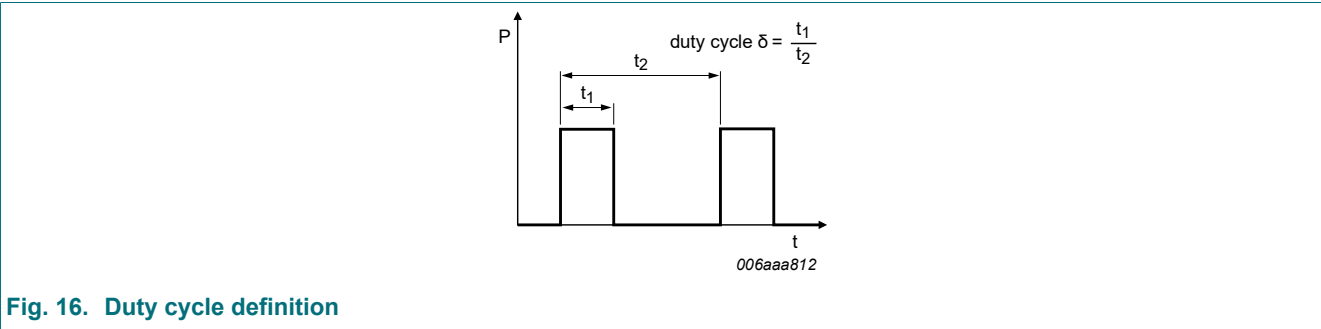


Fig. 15. Source current as a function of source-drain voltage; typical values

11. Test information



12. Package outline

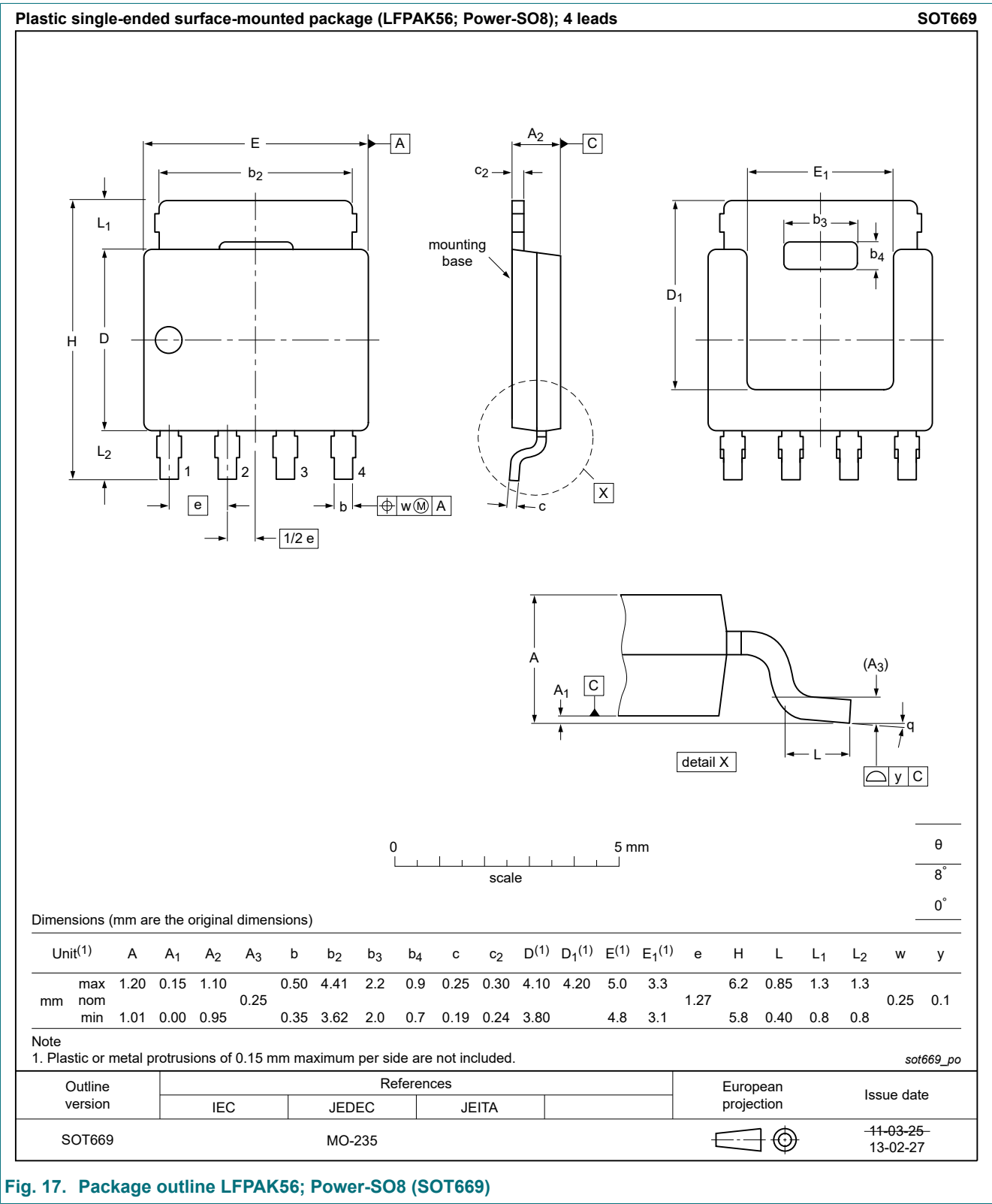


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

13. Soldering

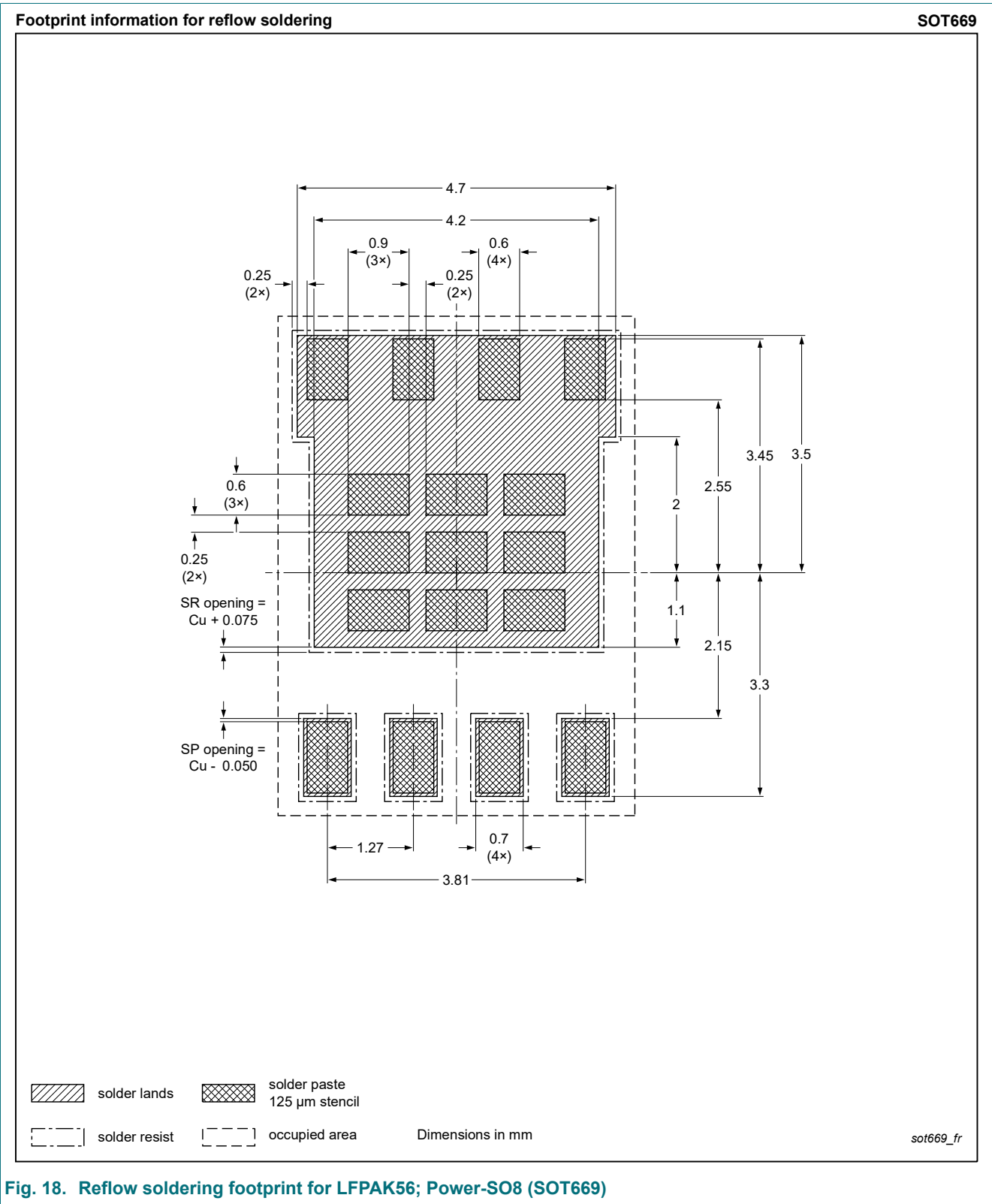
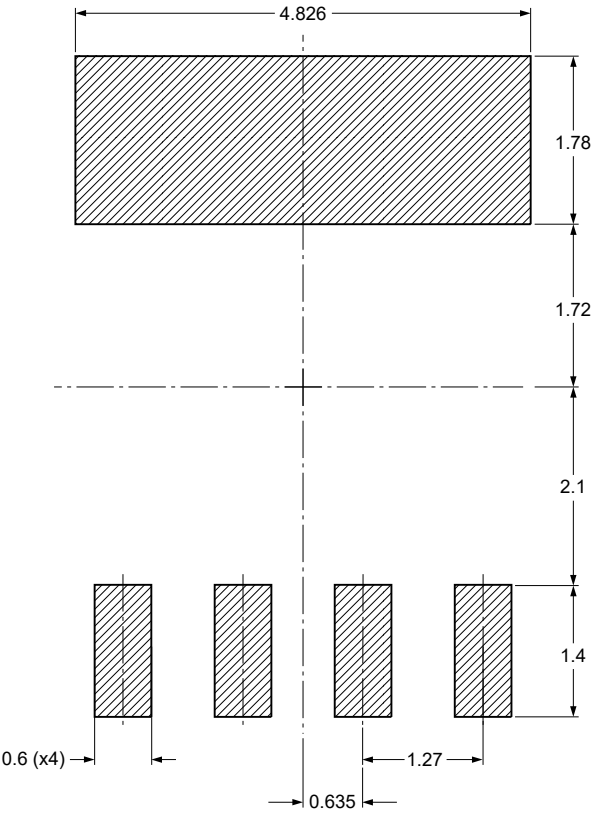


Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

Wave soldering footprint information for LFPAK56 package

SOT669



 solder lands

Dimensions in mm

Issue date ~~15-04-13~~
15-04-16

sot669_fw

Fig. 19. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PSMP033-60YE v.1	20210113	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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