

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	PMT200EPEAX
Manufacturer:	Nexperia USA Inc.
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nexperia-usa-inc/pmt200epeax.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



PMT200EPEA

70 V, P-channel Trench MOSFET

26 October 2016

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a medium power SOT223 (SC-73) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic level compatible
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

4. Quick reference data

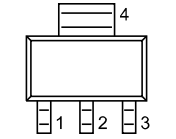
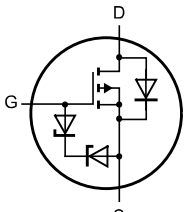
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-	-70	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-	-2.4	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -2.4\text{ A}; T_j = 25\text{ °C}$		-	130	167	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SC-73 (SOT223)	 017aaa259
2	D	drain		
3	S	source		
4	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMT200EPEA	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Marking

Table 4. Marking codes

Type number	Marking code
PMT200EPEA	T2EPEA

8. Limiting values

Table 5. Limiting values

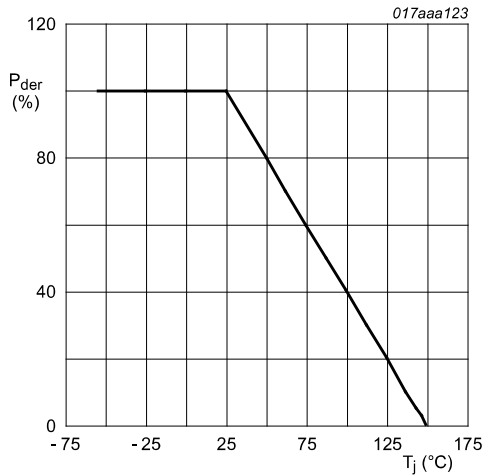
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	-70	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = -10\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-2.4	A
		$V_{GS} = -10\text{ V}$; $T_{amb} = 100\text{ }^{\circ}\text{C}$	[1]	-	-1.5	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	-9.7	A
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $I_D = -1.3\text{ A}$; DUT in avalanche (unclamped)		-	19.5	mJ
P_{tot}	total power dissipation	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	-	800	mW
			[1]	-	1.75	W
		$T_{sp} = 25\text{ }^{\circ}\text{C}$		-	8.3	W
T_j	junction temperature			-55	150	$^{\circ}\text{C}$
T_{amb}	ambient temperature			-55	150	$^{\circ}\text{C}$
T_{stg}	storage temperature			-65	150	$^{\circ}\text{C}$
Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-1.8	A
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

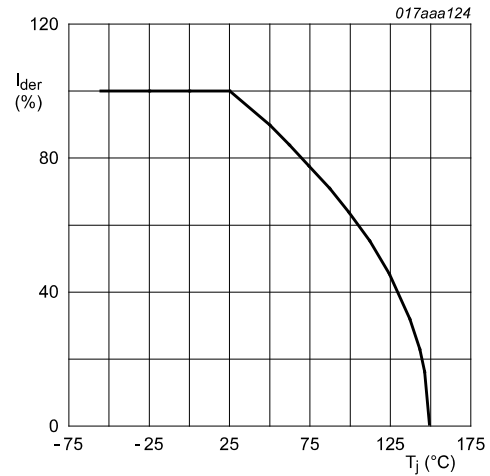
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



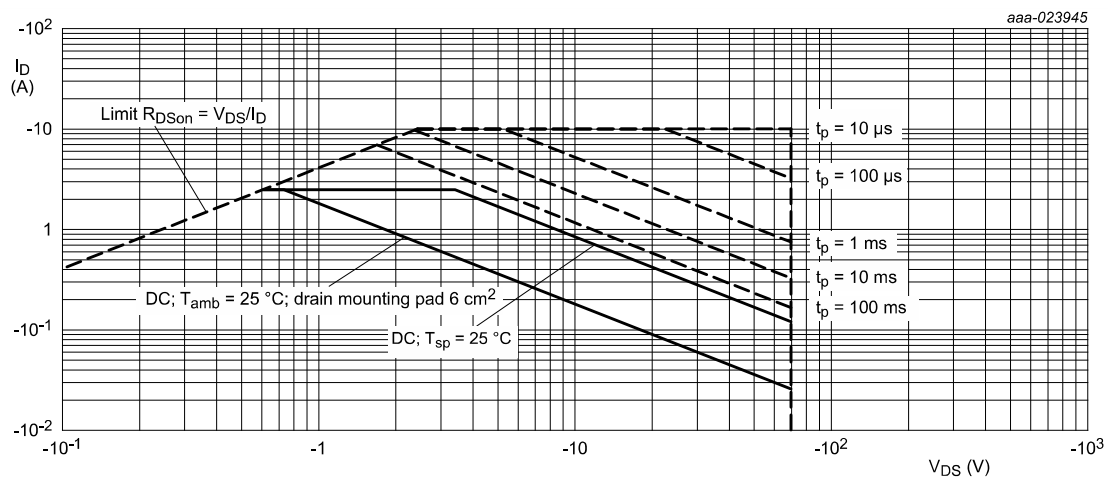
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$

Fig. 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

Fig. 2. Normalized continuous drain current as a function of junction temperature



I_{DM} = single pulse

Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	135	155	K/W
			[2]	-	54	70	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	7	15	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

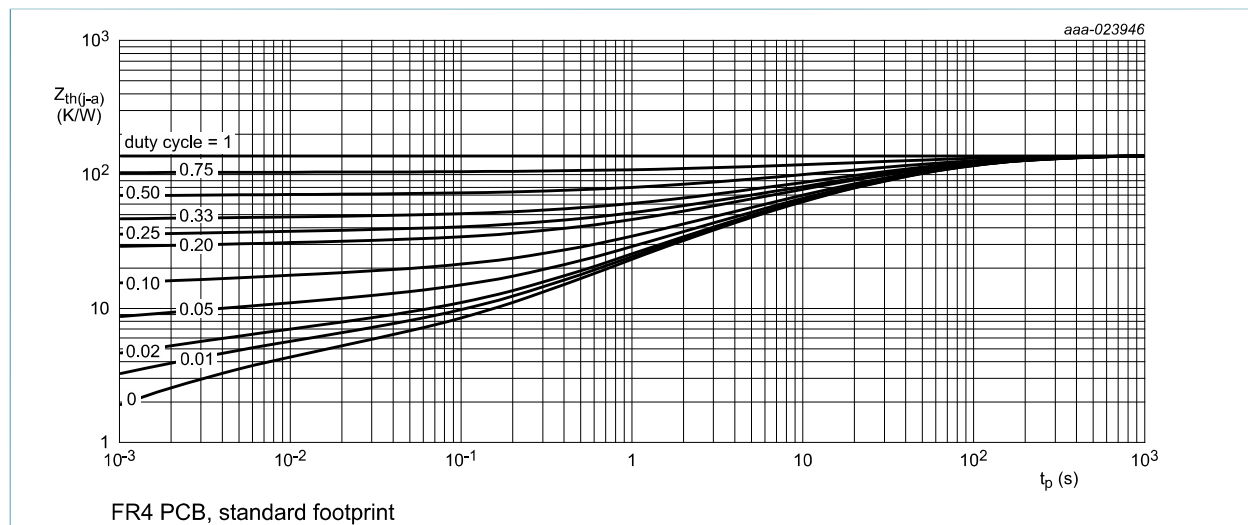


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

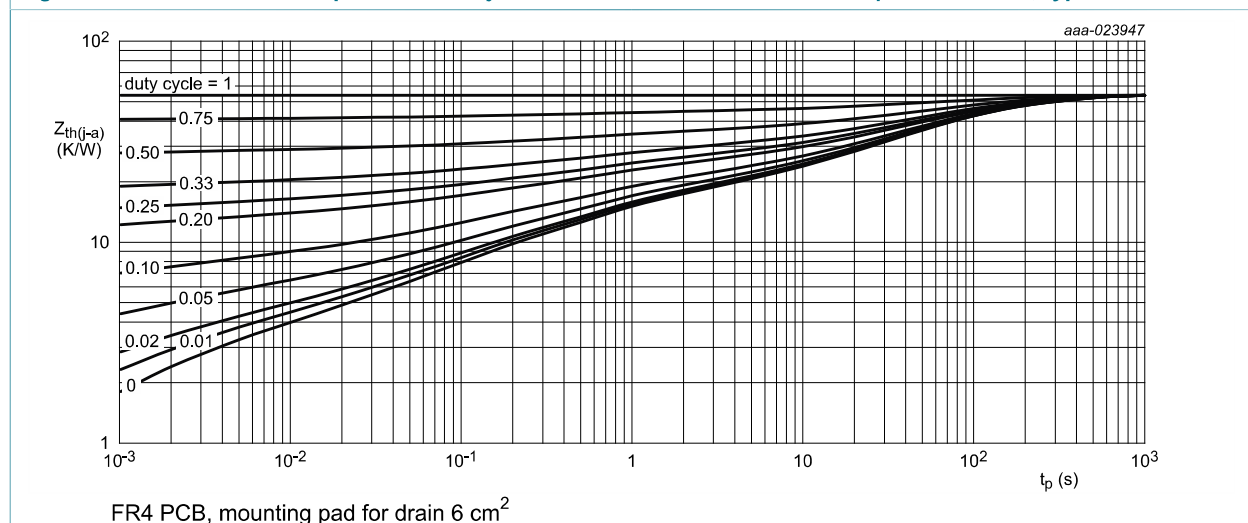


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-70	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} =V _{GS} ; T _j = 25 °C		-1	-2	-3	V
I _{DSS}	drain leakage current	V _{DS} = -70 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-10	μA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	2	μA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-2	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = -10 V; I _D = -2.4 A; T _j = 25 °C		-	130	167	mΩ
		V _{GS} = -10 V; I _D = -2.4 A; T _j = 150 °C		-	234	250	mΩ
		V _{GS} = -4.5 V; I _D = -2.1 A; T _j = 25 °C		-	150	225	mΩ
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -2.4 A; T _j = 25 °C		-	13.5	-	S
R _G	gate resistance	f = 1 MHz		-	12	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -35 V; I _D = -2.4 A; V _{GS} = -10 V; T _j = 25 °C		-	10.6	15.9	nC
Q _{GS}	gate-source charge			-	2.2	-	nC
Q _{GD}	gate-drain charge			-	1.05	-	nC
C _{iss}	input capacitance	V _{DS} = -35 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	822	-	pF
C _{oss}	output capacitance			-	47	-	pF
C _{rss}	reverse transfer capacitance			-	31.5	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -35 V; I _D = -2.4 A; V _{GS} = -10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	6	-	ns
t _r	rise time			-	8	-	ns
t _{d(off)}	turn-off delay time			-	42	-	ns
t _f	fall time			-	20	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -2.4 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.8	-1.2	V

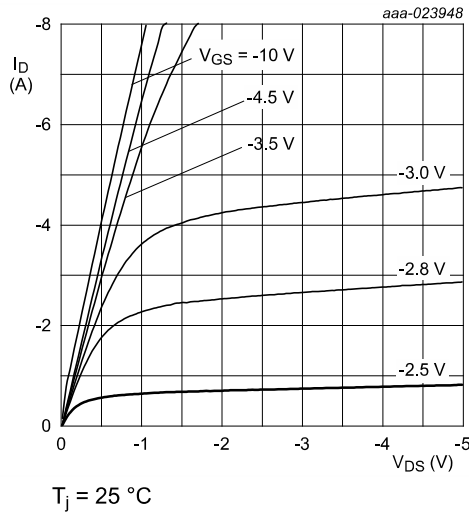


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

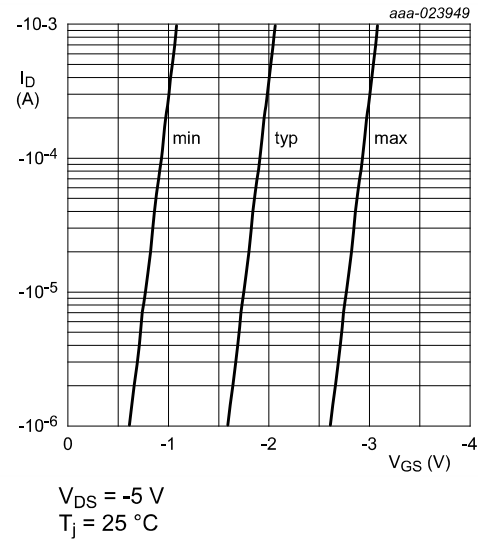


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

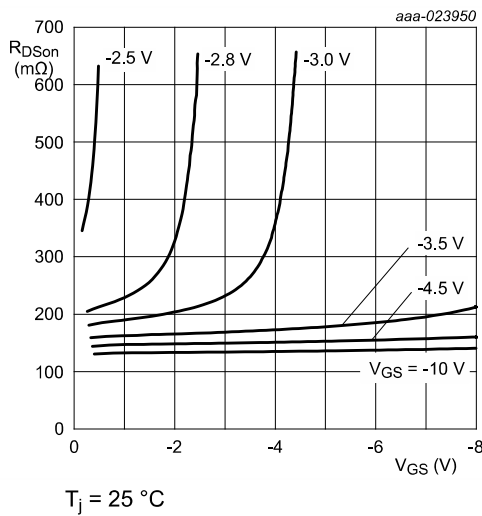


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

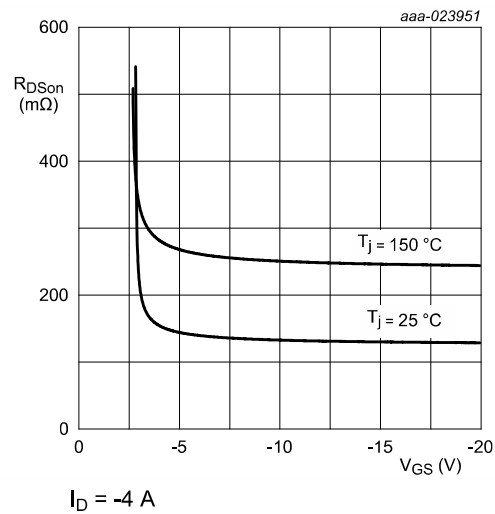


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

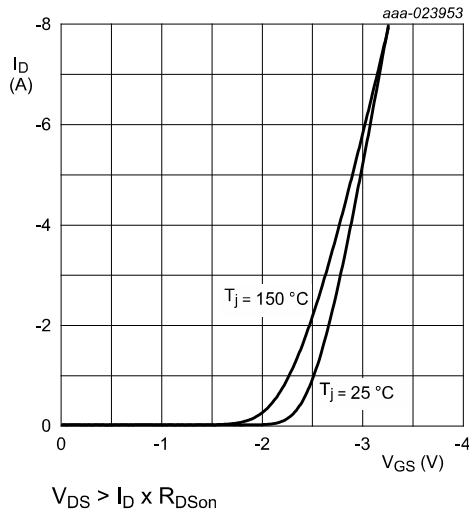


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

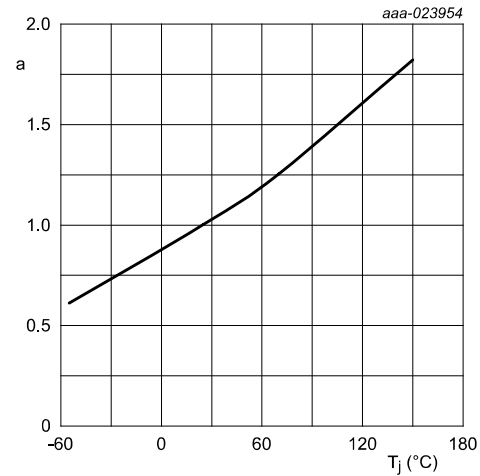


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

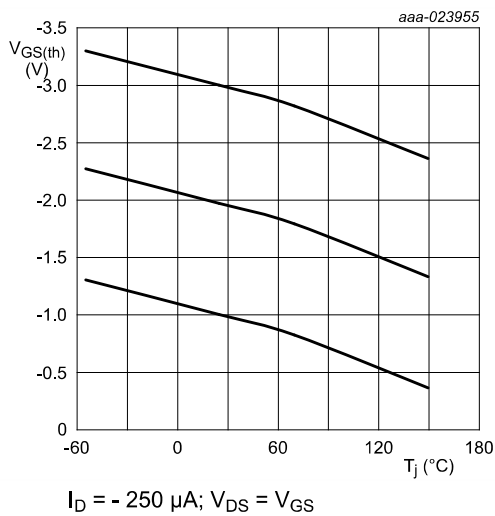


Fig. 12. Gate-source threshold voltage as a function of junction temperature

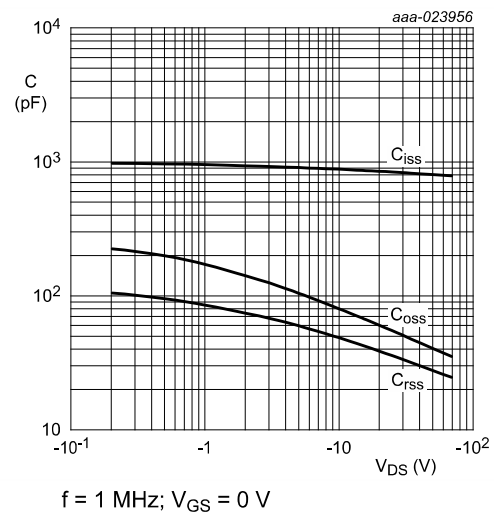


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

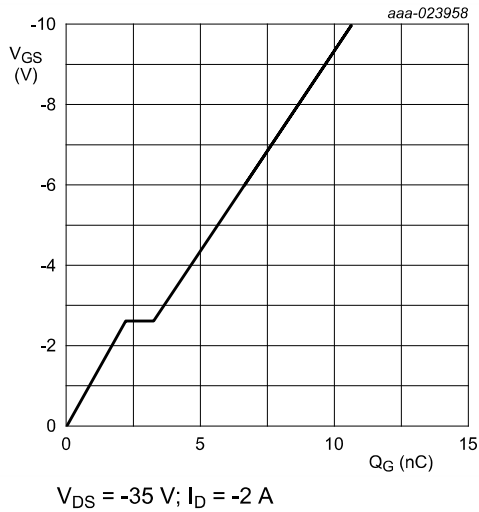


Fig. 14. Gate-source voltage as a function of gate charge; typical values

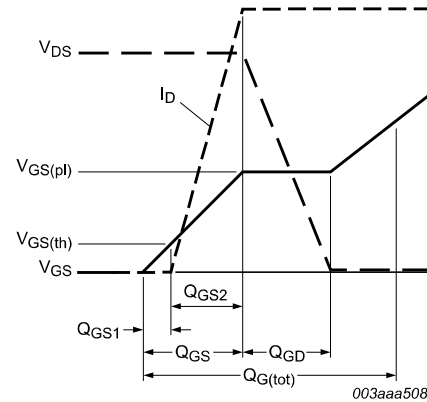


Fig. 15. Gate charge waveform definitions

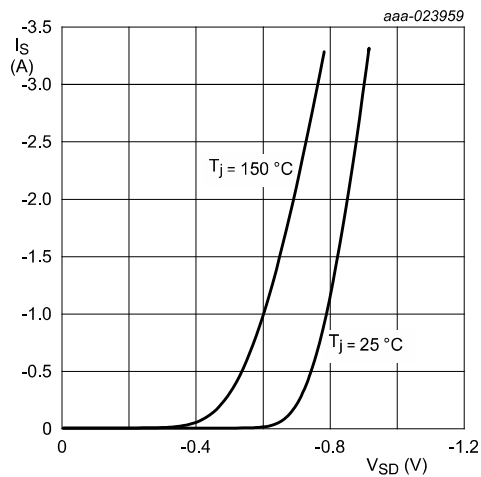


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

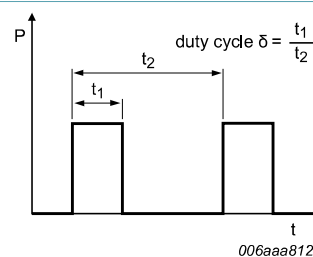


Fig. 17. Duty cycle definition

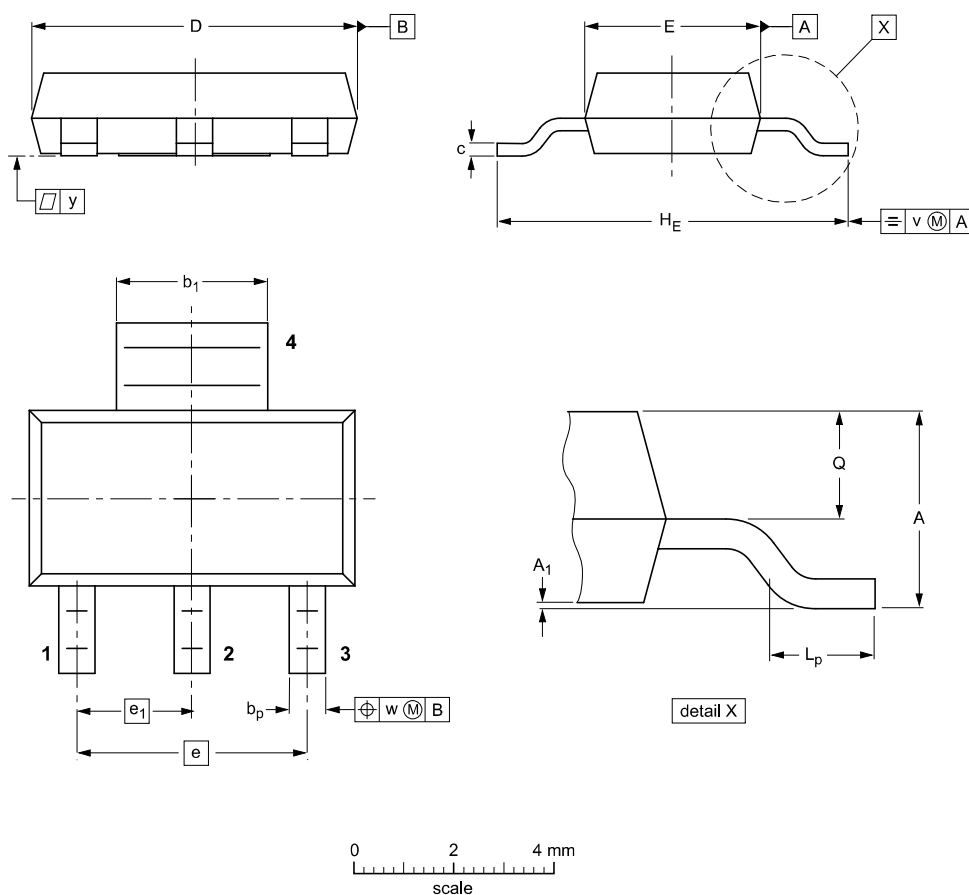
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			04-11-10 06-03-16

Fig. 18. Package outline SC-73 (SOT223)

13. Soldering

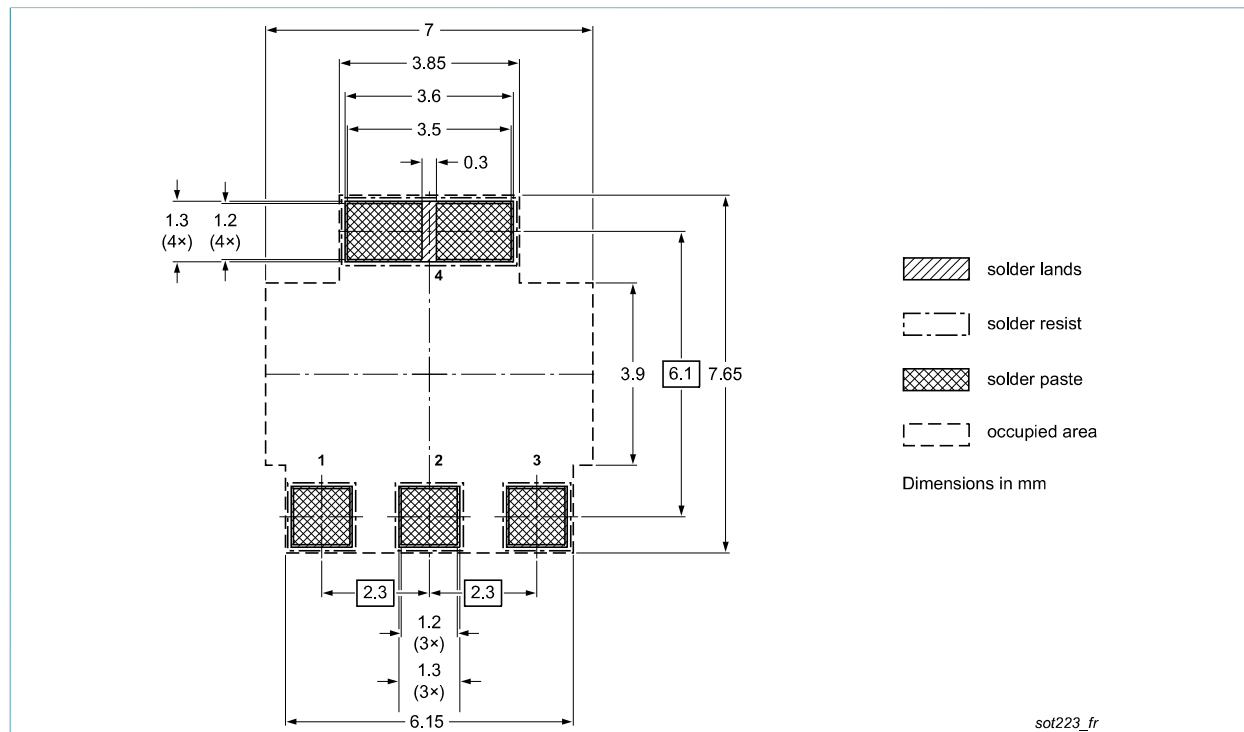


Fig. 19. Reflow soldering footprint for SC-73 (SOT223)

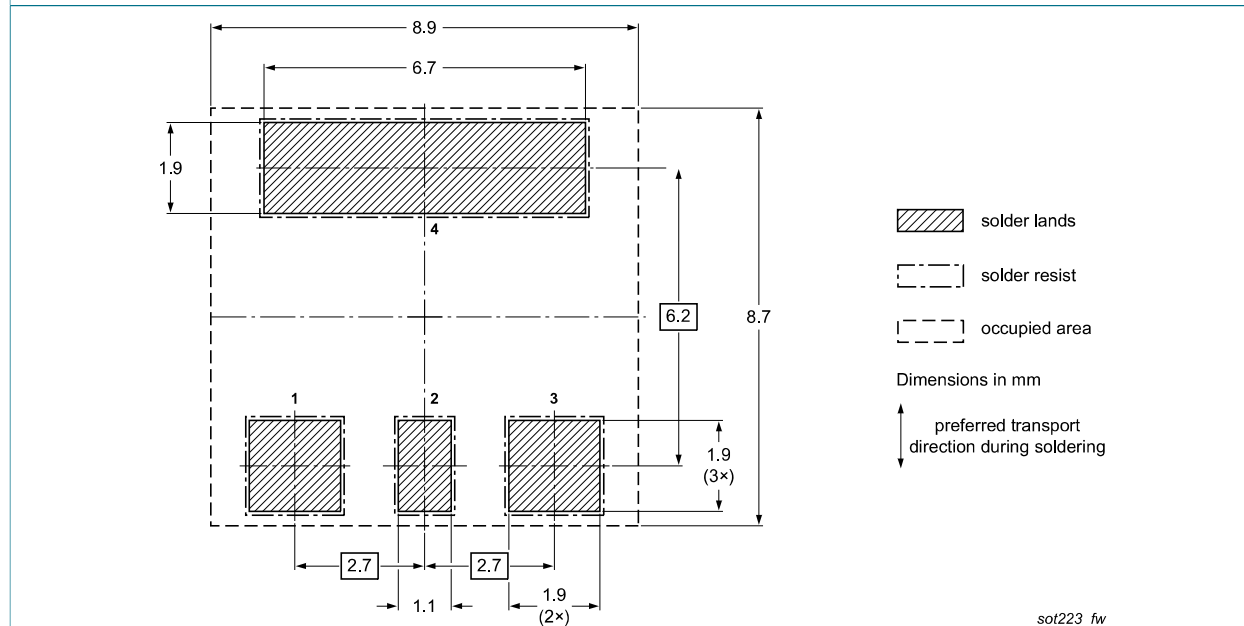


Fig. 20. Wave soldering footprint for SC-73 (SOT223)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMT200EPEA v.2	20161026	Product data sheet	-	20160707
Modification:	- Product status changed - Value of I_S = source current corrected (section 8 Limiting values)			
PMT200EPEA v.1	20160707	Preliminary data sheet	-	-

15. Legal information

Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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