

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	PMN80XP,115
Manufacturer:	Nexperia USA Inc.
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nexperia-usa-inc/pmn80xp-115.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



PMN80XP

20 V, single P-channel Trench MOSFET

Rev. 1 — 8 May 2012

Product data sheet

1. Product profile

1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- R_{DSon} specified at 1.8 V operation
- Fast switching
- Trench MOSFET technology

1.3 Applications

- Relay driver
- High-side loadswitch
- High-speed line driver
- Switching circuits

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_{amb} = 25\text{ °C}$	-	-	-20	V
V_{GS}	gate-source voltage		-12	-	12	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-3.2	A
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -2.5\text{ A}; T_j = 25\text{ °C}$	-	80	102	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	SOT457 (TSOP6)	017aaa257
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PMN80XP	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code
PMN80XP	WA

5. Limiting values

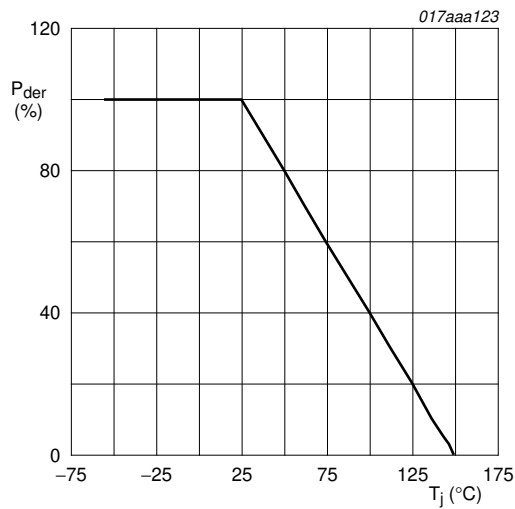
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_{amb} = 25\text{ °C}$		-	-20	V
V_{GS}	gate-source voltage			-12	12	V
I_D	drain current	$V_{GS} = -4.5\text{ V}$; $T_{amb} = 25\text{ °C}$; $t \leq 5\text{ s}$	[1]	-	-3.2	A
		$V_{GS} = -4.5\text{ V}$; $T_{amb} = 25\text{ °C}$	[1]	-	-2.5	A
		$V_{GS} = -4.5\text{ V}$; $T_{amb} = 100\text{ °C}$	[1]	-	-1.6	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	-10	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	385	mW
			[1]	-	925	mW
		$T_{sp} = 25\text{ °C}$		-	4000	mW
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-1	A

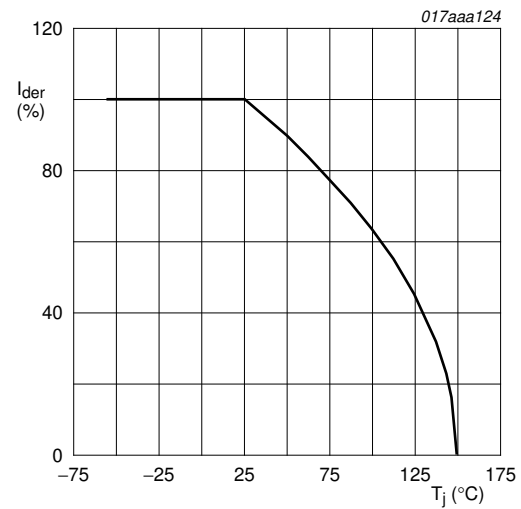
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



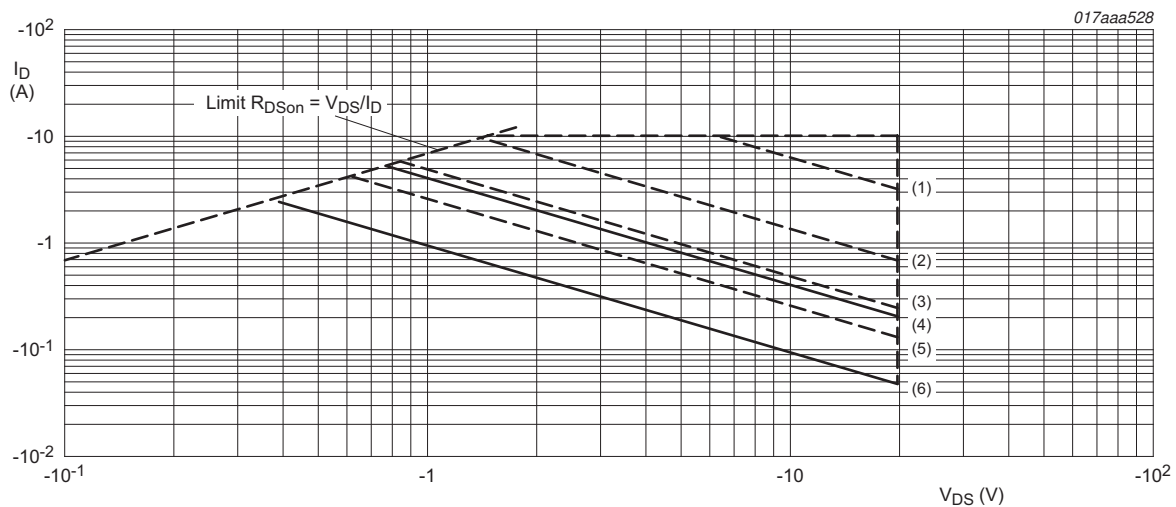
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} = single pulse

(1) $t_p = 100 \mu\text{s}$

(2) $t_p = 1 \text{ ms}$

(3) $t_p = 10 \text{ ms}$

(4) DC; $T_{sp} = 25^{\circ}\text{C}$

(5) $t_p = 100 \text{ ms}$

(6) DC; $T_{amb} = 25^{\circ}\text{C}$; drain mounting pad 6 cm^2

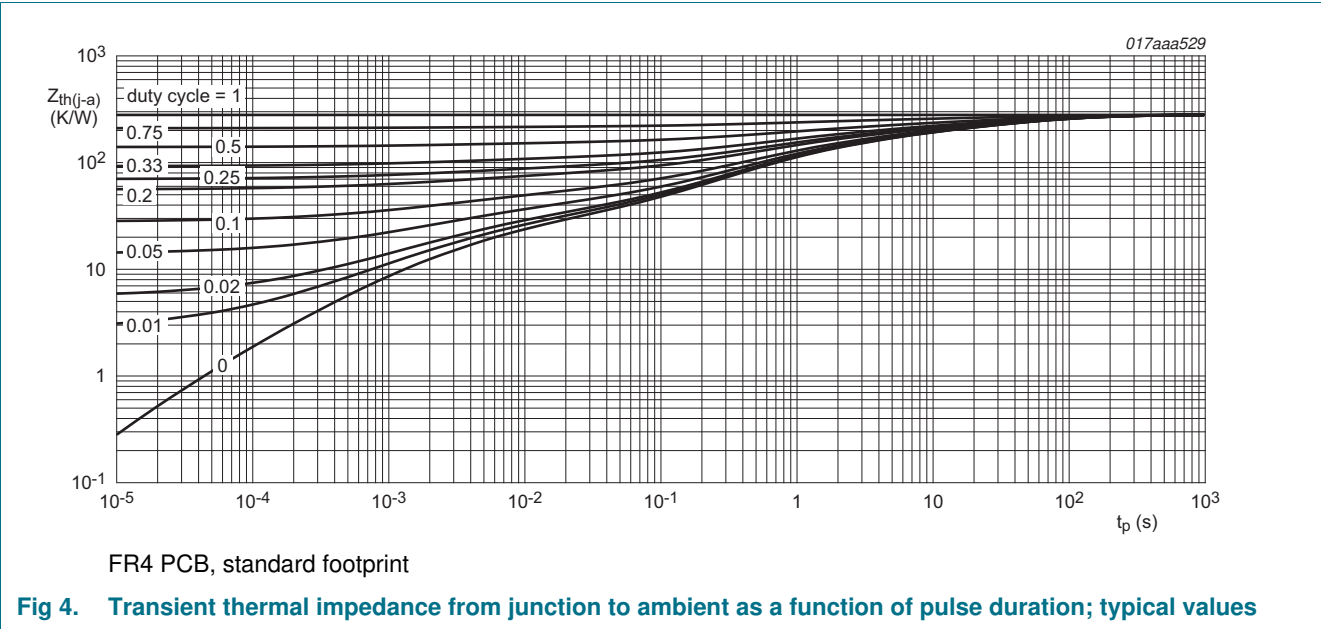
Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	281	325 K/W
			[2]	-	116	135 K/W
			[3]	-	73	85 K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	27	31	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm²
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm², t ≤ 5 s



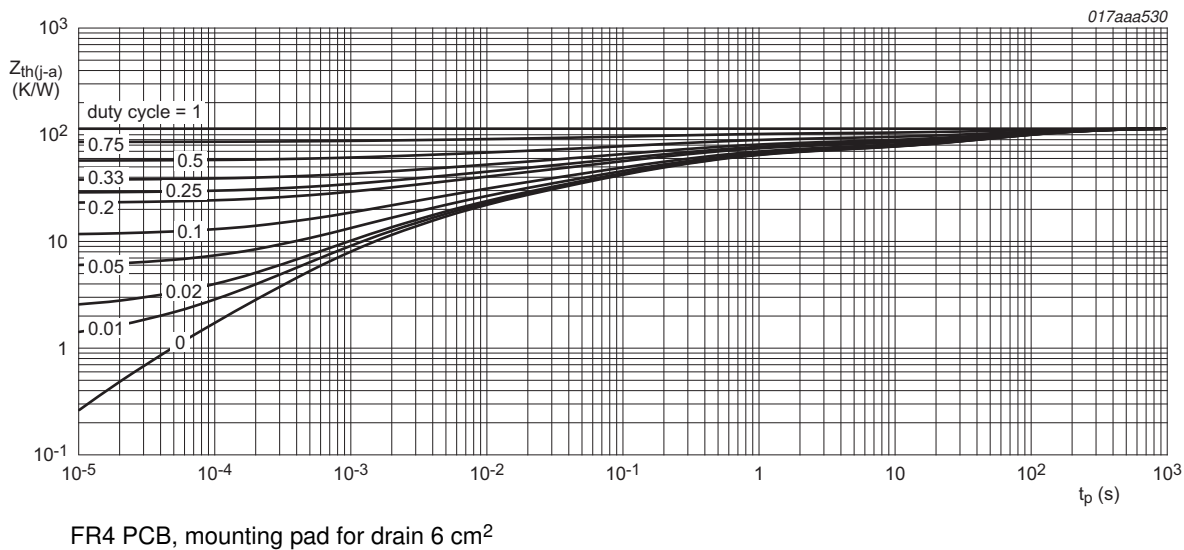


Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250\ \mu\text{A}$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ\text{C}$	-0.45	-0.75	-1	V
I_{DSS}	drain leakage current	$V_{DS} = -20\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	-1	μA
		$V_{DS} = -20\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_{amb} = 150\ ^\circ\text{C}$	-	-	-10	μA
I_{GSS}	gate leakage current	$V_{GS} = 12\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	-100	nA
		$V_{GS} = -12\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	-100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\ \text{V}$; $I_D = -2.5\ \text{A}$; $T_j = 25\ ^\circ\text{C}$	-	80	102	m Ω
		$V_{GS} = -4.5\ \text{V}$; $I_D = -2.5\ \text{A}$; $T_j = 150\ ^\circ\text{C}$	-	116	148	m Ω
		$V_{GS} = -2.5\ \text{V}$; $I_D = -2.3\ \text{A}$; $T_j = 25\ ^\circ\text{C}$	-	95	125	m Ω
		$V_{GS} = -1.8\ \text{V}$; $I_D = -1.1\ \text{A}$; $T_j = 25\ ^\circ\text{C}$	-	120	156	m Ω
g_{fs}	forward transconductance	$V_{DS} = -10\ \text{V}$; $I_D = -2.5\ \text{A}$; $T_j = 25\ ^\circ\text{C}$	-	15	-	S
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10\ \text{V}$; $I_D = -2.5\ \text{A}$; $V_{GS} = -4.5\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	5	7.5	nC
Q_{GS}	gate-source charge		-	0.7	-	nC
Q_{GD}	gate-drain charge		-	0.9	-	nC
C_{iss}	input capacitance	$V_{DS} = -10\ \text{V}$; $f = 1\ \text{MHz}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	550	-	pF
C_{oss}	output capacitance		-	63	-	pF
C_{rss}	reverse transfer capacitance		-	53	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10\ \text{V}$; $I_D = -2.5\ \text{A}$; $V_{GS} = -4.5\ \text{V}$; $R_{G(ext)} = 6\ \Omega$; $T_j = 25\ ^\circ\text{C}$	-	6	-	ns
t_r	rise time		-	14	-	ns
$t_{d(off)}$	turn-off delay time		-	120	-	ns
t_f	fall time		-	50	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = -1.0\ \text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-0.8	-1.2	V

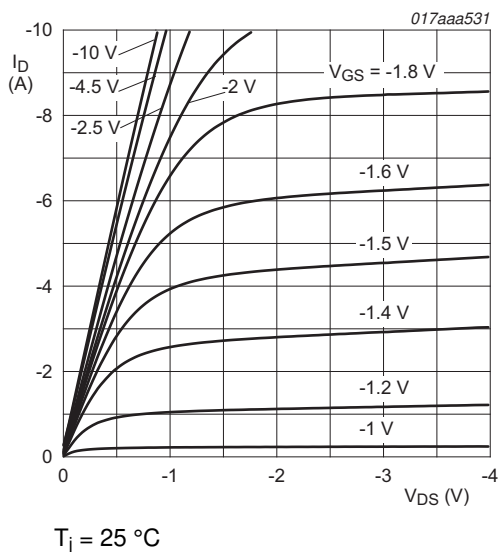


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

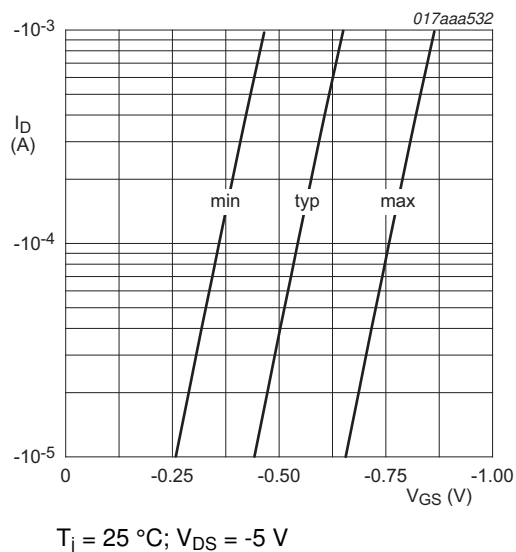


Fig 7. Sub-threshold drain current as a function of gate-source voltage

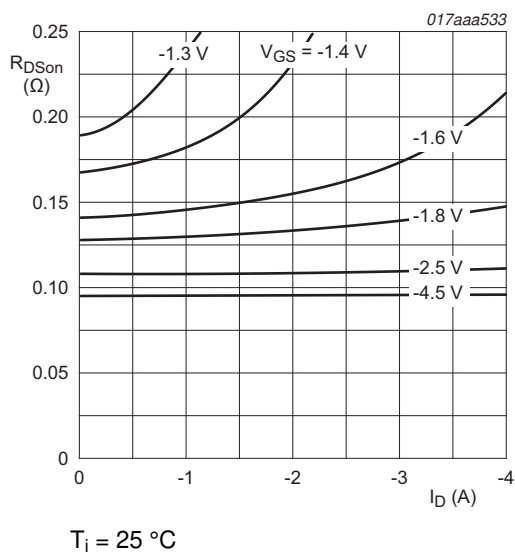


Fig 8. Drain-source on-state resistance as a function of drain current; typical values

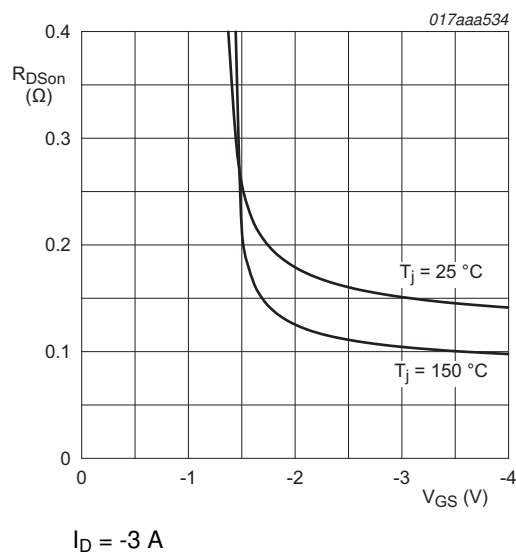


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

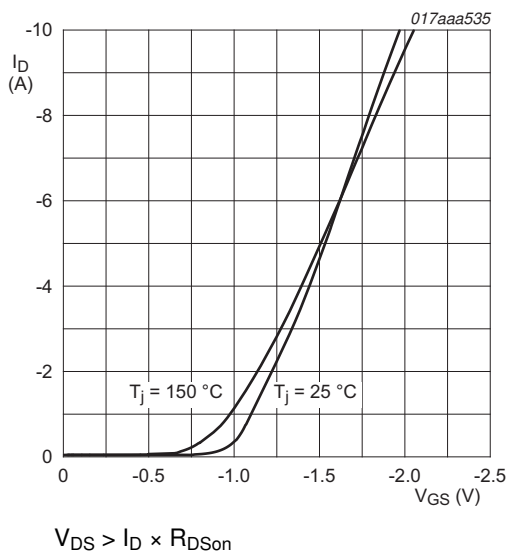


Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

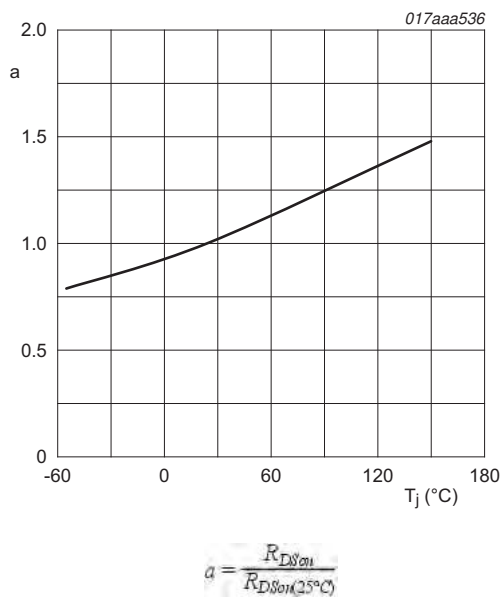


Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

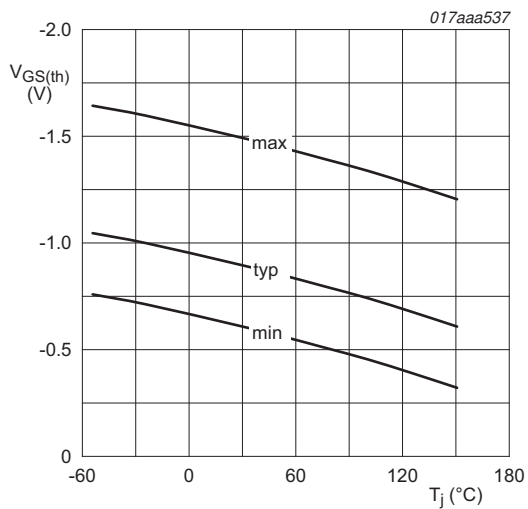


Fig 12. Gate-source threshold voltage as a function of junction temperature

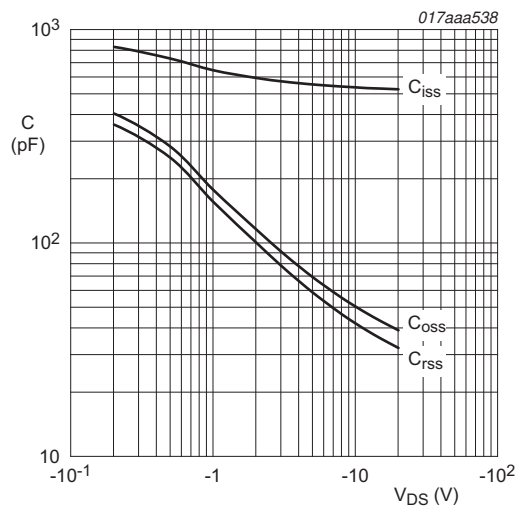


Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

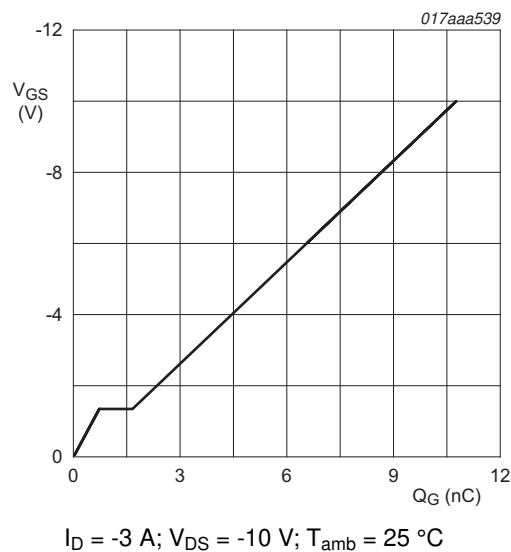


Fig 14. Gate charge waveform definitions

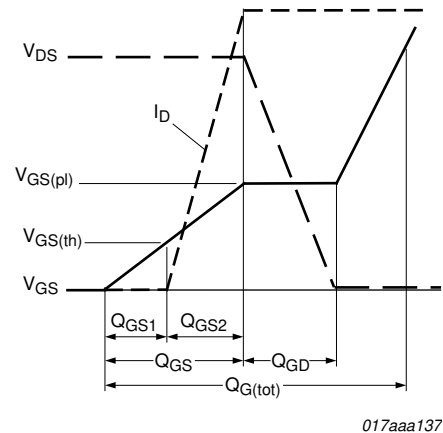
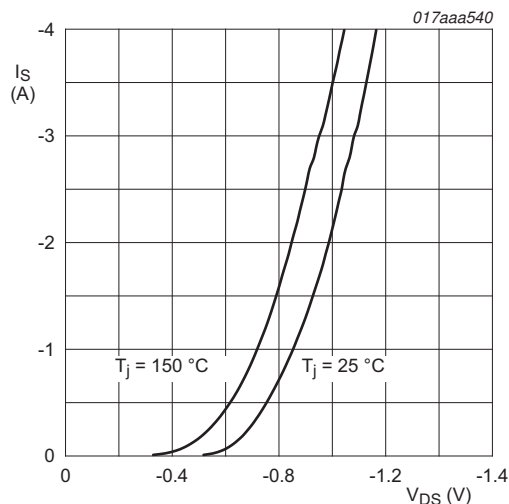


Fig 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig 16. Source current as a function of source-drain voltage; typical values

8. Test information

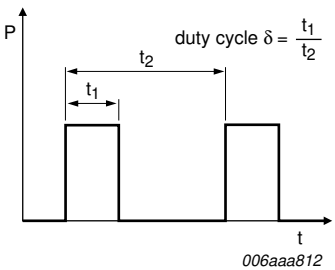


Fig 17. Duty cycle definition

9. Package outline

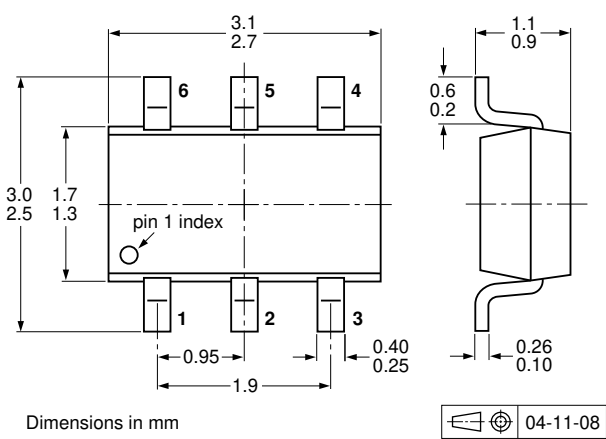


Fig 18. Package outline SOT457 (TSOP6)

10. Soldering

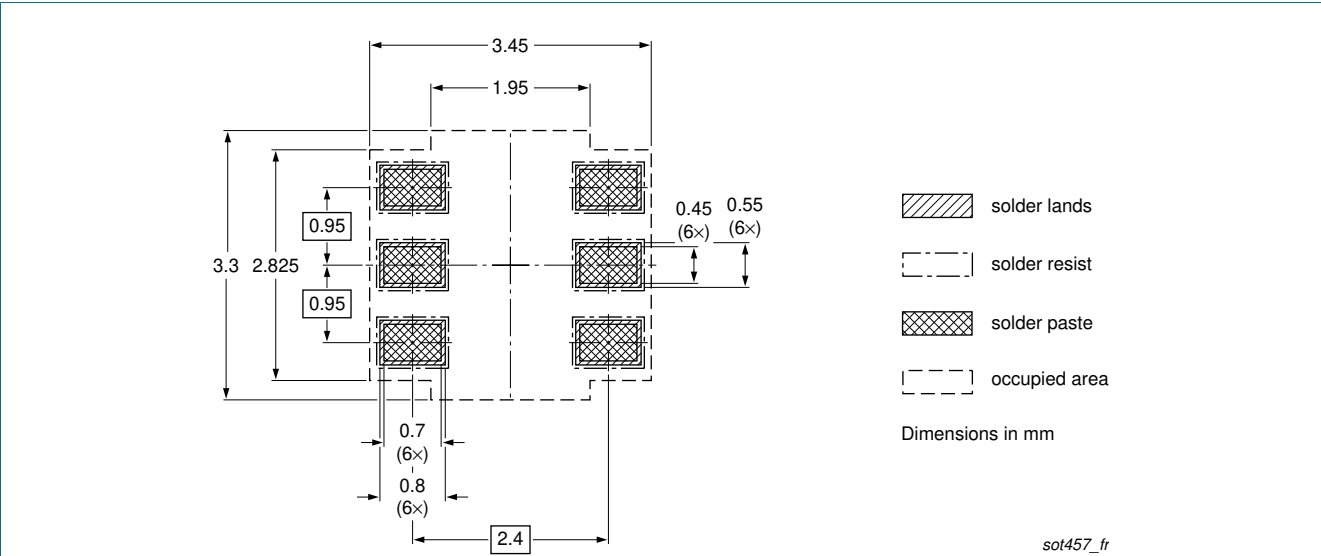


Fig 19. Reflow soldering footprint for SOT457 (TSOP6)

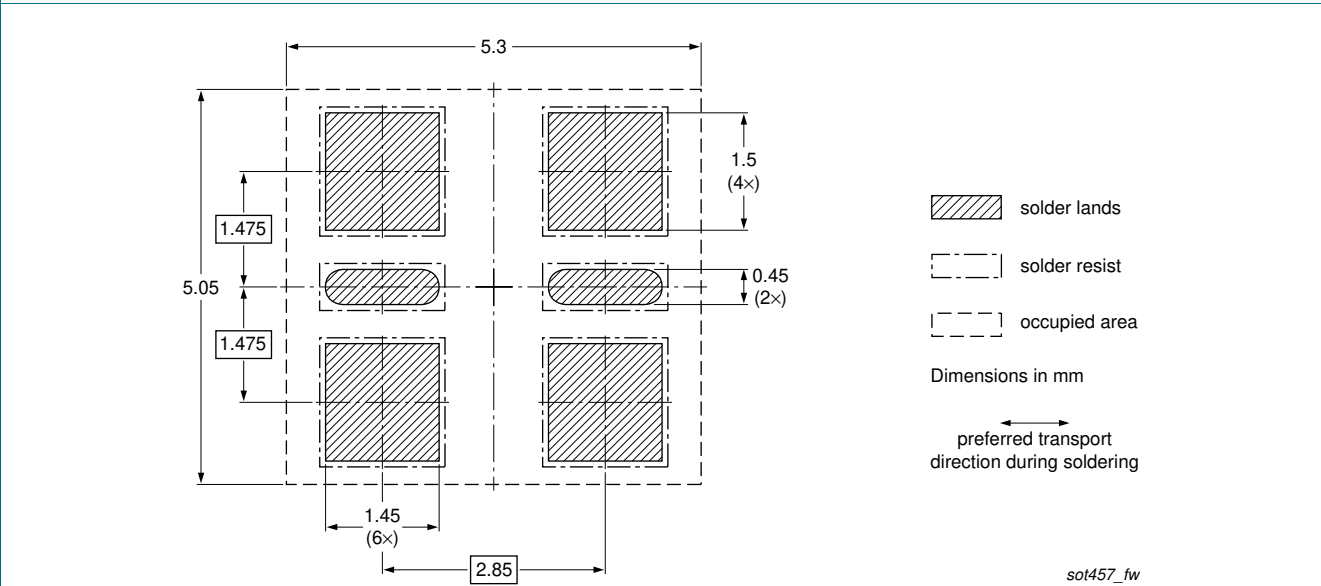


Fig 20. Wave soldering footprint for SOT457 (TSOP6)

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMN80XP v.1	20120508	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	1
3	Ordering information	2
4	Marking	2
5	Limiting values	2
6	Thermal characteristics	4
7	Characteristics	6
8	Test information	10
9	Package outline	10
10	Soldering	11
11	Revision history	12
12	Legal information	13
12.1	Data sheet status	13
12.2	Definitions	13
12.3	Disclaimers	13
12.4	Trademarks	14
13	Contact information	14