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Product Reference Information

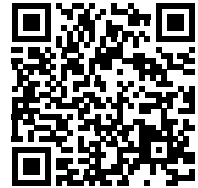
Part Number:	PH955L,115
Manufacturer:	Nexperia USA Inc.
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nexperia-usa-inc/ph955l-115.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



PH955L

N-channel TrenchMOS logic level FET

Rev. 02 — 19 February 2009

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC convertors
- Motors, lamps and solenoids
- General purpose power switching
- Portable equipment

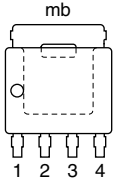
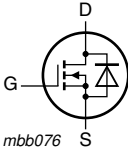
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	55	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 1 ; see Figure 3	-	-	62.5	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	62.5	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 44\text{ V}$; $T_j = 25\text{ °C}$; see Figure 11 ; see Figure 12	-	16.4	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 10	-	6.2	8.3	mΩ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		
			SOT669 (LFAK)	

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PH955L	LFAK	plastic single-ended surface-mounted package (LFAK); 4 leads	SOT669

4. Limiting values

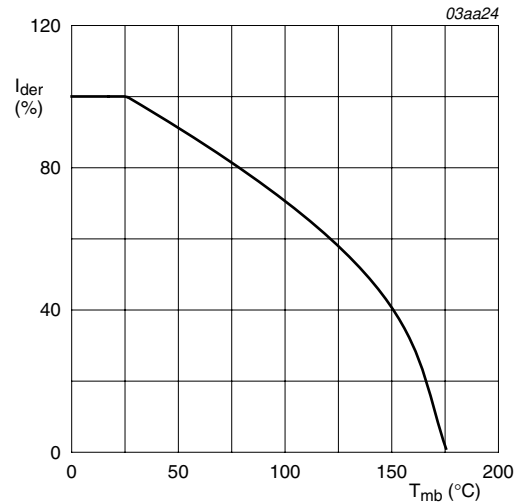
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C	-	55	V	
V _{DGR}	drain-gate voltage	T _j ≥ 25 °C; T _j ≤ 150 °C; R _{GS} = 20 kΩ	-	55	V	
V _{GS}	gate-source voltage		-20	20	V	
I _D	drain current	V _{GS} = 5 V; T _{mb} = 100 °C; see Figure 1	-	43.7	A	
		V _{GS} = 5 V; T _{mb} = 25 °C; see Figure 1 ; see Figure 3	-	62.5	A	
I _{DM}	peak drain current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C; see Figure 3	-	187	A	
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	62.5	W	
T _{stg}	storage temperature		-55	150	°C	
T _j	junction temperature		-55	150	°C	
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	-	52	A	
I _{SM}	peak source current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C	-	156	A	
Avalanche ruggedness						
E _{DS(AL)R}	repetitive drain-source avalanche energy	V _{GS} = 5 V; I _D = 4.4 A; V _{sup} ≤ 55 V; unclamped; t _p = 0.1 ms; R _{GS} = 50 Ω	[1] [2]	-	2	mJ
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 5 V; T _{j(init)} = 25 °C; I _D = 44 A; V _{sup} ≤ 55 V; unclamped; t _p = 0.1 ms; R _{GS} = 50 Ω	-	195	mJ	

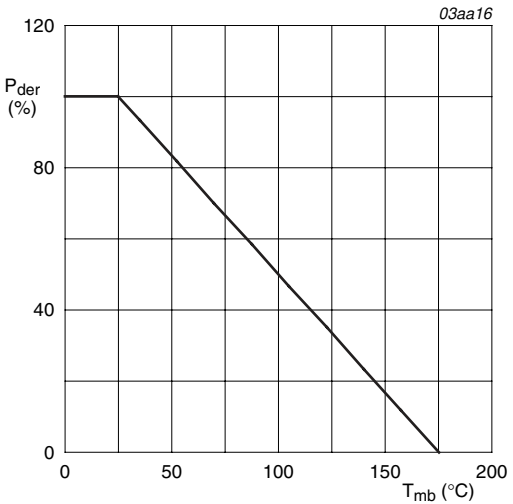
[1] Duty cycle is limited by the maximum junction temperature.

[2] Repetitive avalanche failure is not determined simply by thermal effects. Repetitive avalanche transients should only be applied for short bursts, not every switching cycle.



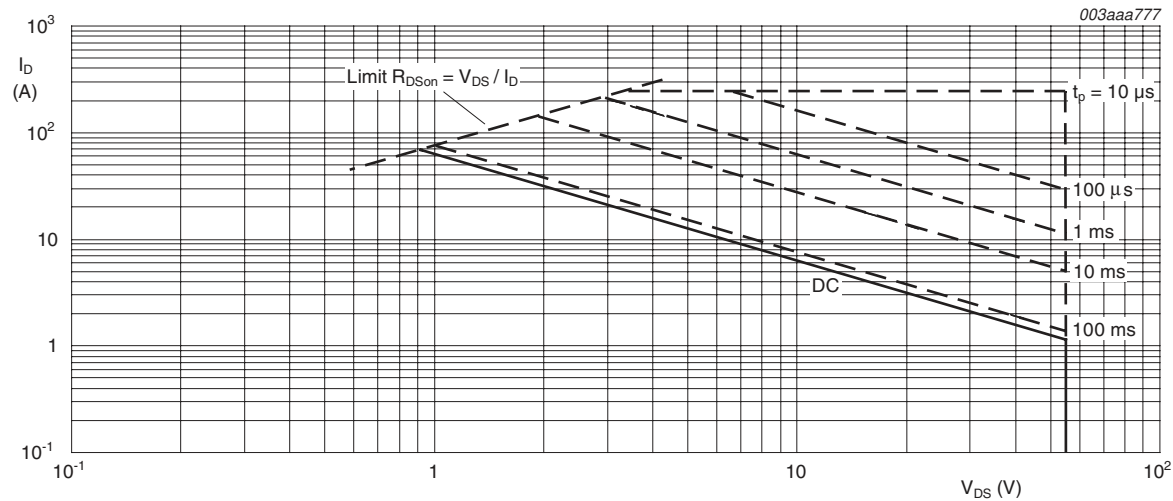
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25^{\circ}\text{C}; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2	K/W

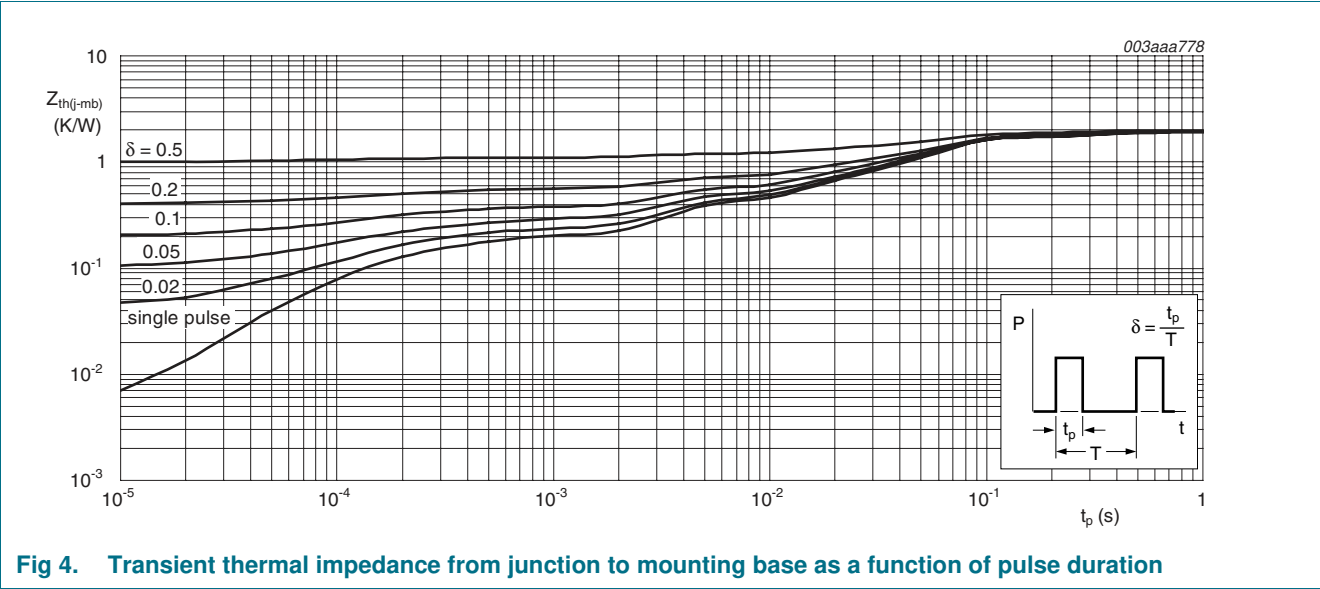
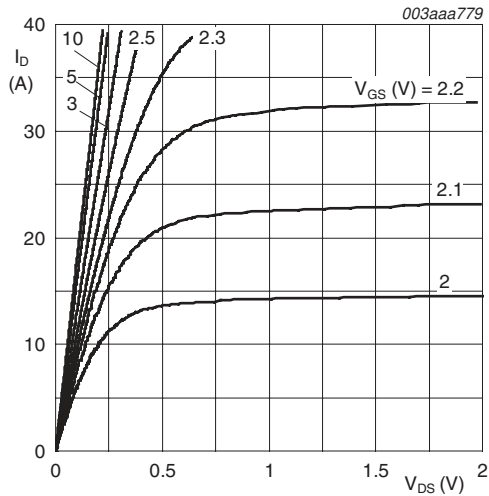


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

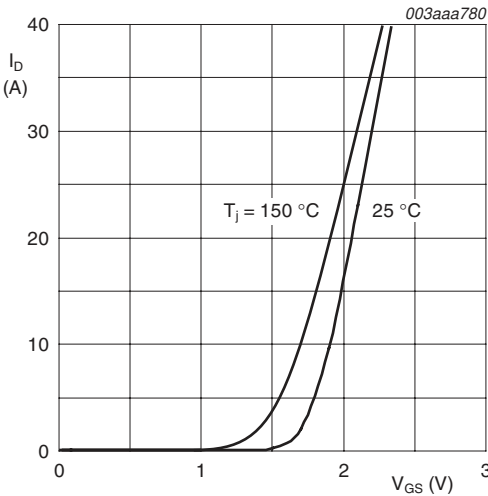
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	50	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	55	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 7 ; see Figure 8	-	-	2.3	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 150 °C; see Figure 7 ; see Figure 8	0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 7 ; see Figure 8	1	1.5	2	V
I _{DSS}	drain leakage current	V _{DS} = 55 V; V _{GS} = 0 V; T _j = 25 °C	-	0.02	1	μA
		V _{DS} = 55 V; V _{GS} = 0 V; T _j = 150 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 15 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -15 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C	-	7.1	9.9	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 150 °C; see Figure 9	-	-	16	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 10	-	6.2	8.3	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 44 V; V _{GS} = 5 V; T _j = 25 °C; see Figure 11 ; see Figure 12	-	42	-	nC
Q _{GS}	gate-source charge		-	5.7	-	nC
Q _{GS1}	pre-threshold gate-source charge		-	4.3	-	nC
Q _{GS2}	post-threshold gate-source charge		-	1.4	-	nC
Q _{GD}	gate-drain charge		-	16.4	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 44 V; T _j = 25 °C; see Figure 11 ; see Figure 12	-	2	-	V
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 13	-	2836	-	pF
C _{oss}	output capacitance		-	441	-	pF
C _{rss}	reverse transfer capacitance		-	210	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 25 V; R _L = 1 Ω; V _{GS} = 5 V; R _{G(ext)} = 4.7 Ω; T _j = 25 °C	-	18	-	ns
t _r	rise time		-	71	-	ns
t _{d(off)}	turn-off delay time		-	105	-	ns
t _f	fall time		-	25	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 14	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 30 V; T _j = 25 °C	-	62	-	ns
Q _r	recovered charge		-	48	-	nC



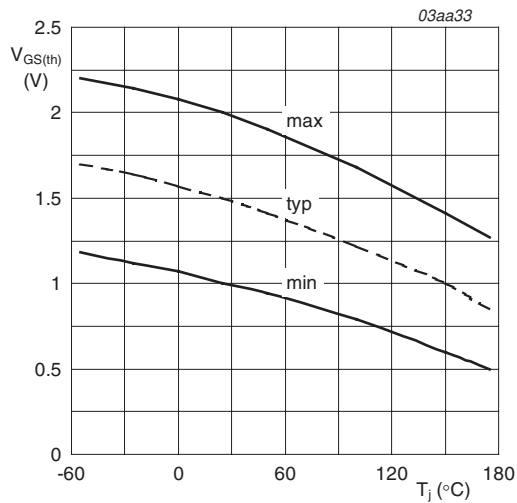
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



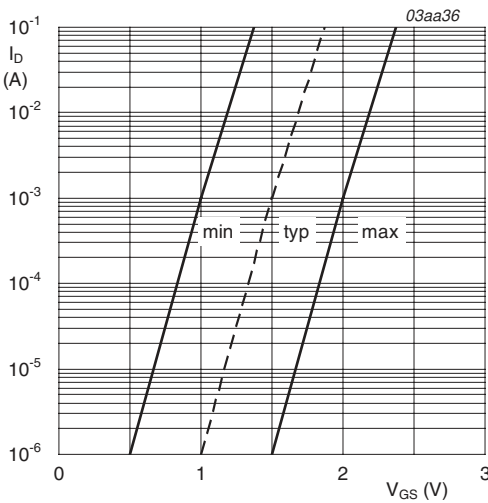
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DS(on)}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



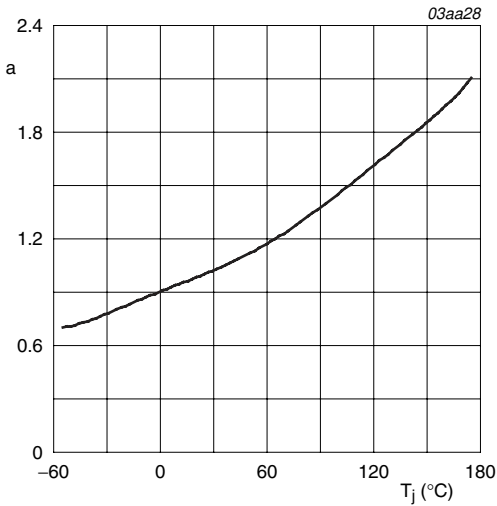
$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

Fig 7. Gate-source threshold voltage as a function of junction temperature



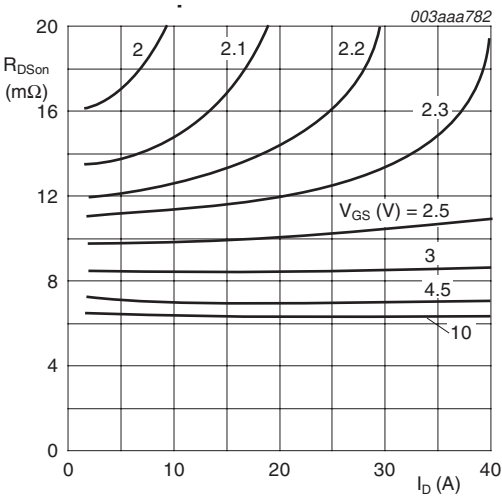
$T_j = 25^\circ\text{C}$; $V_{DS} = V_{GS}$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



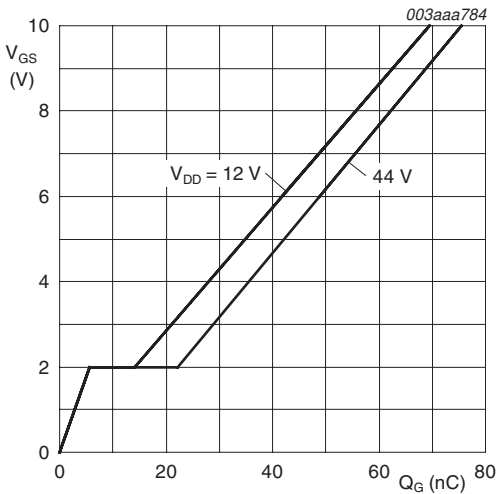
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^{\circ}\text{C}$

Fig 10. Drain-source on-state resistance as a function of drain current; typical values



$I_D = 25\text{ A}; V_{DS} = 12\text{ V and } 44\text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

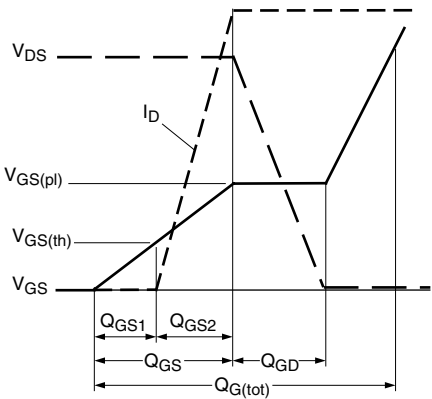


Fig 12. Gate charge waveform definitions

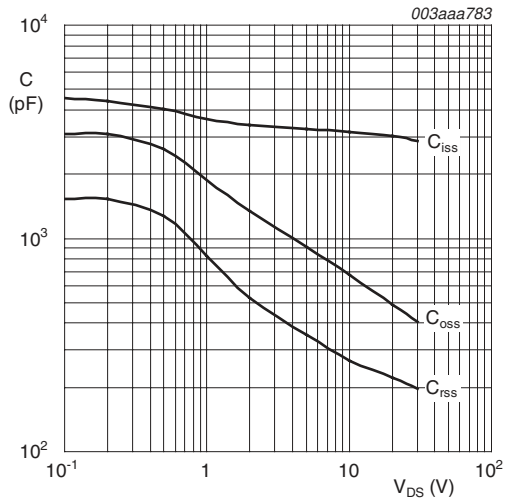


Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

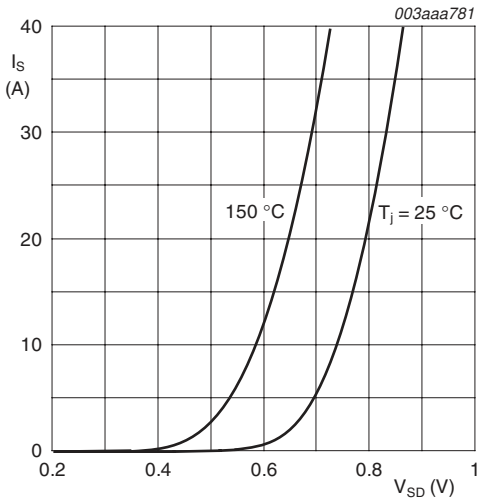


Fig 14. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

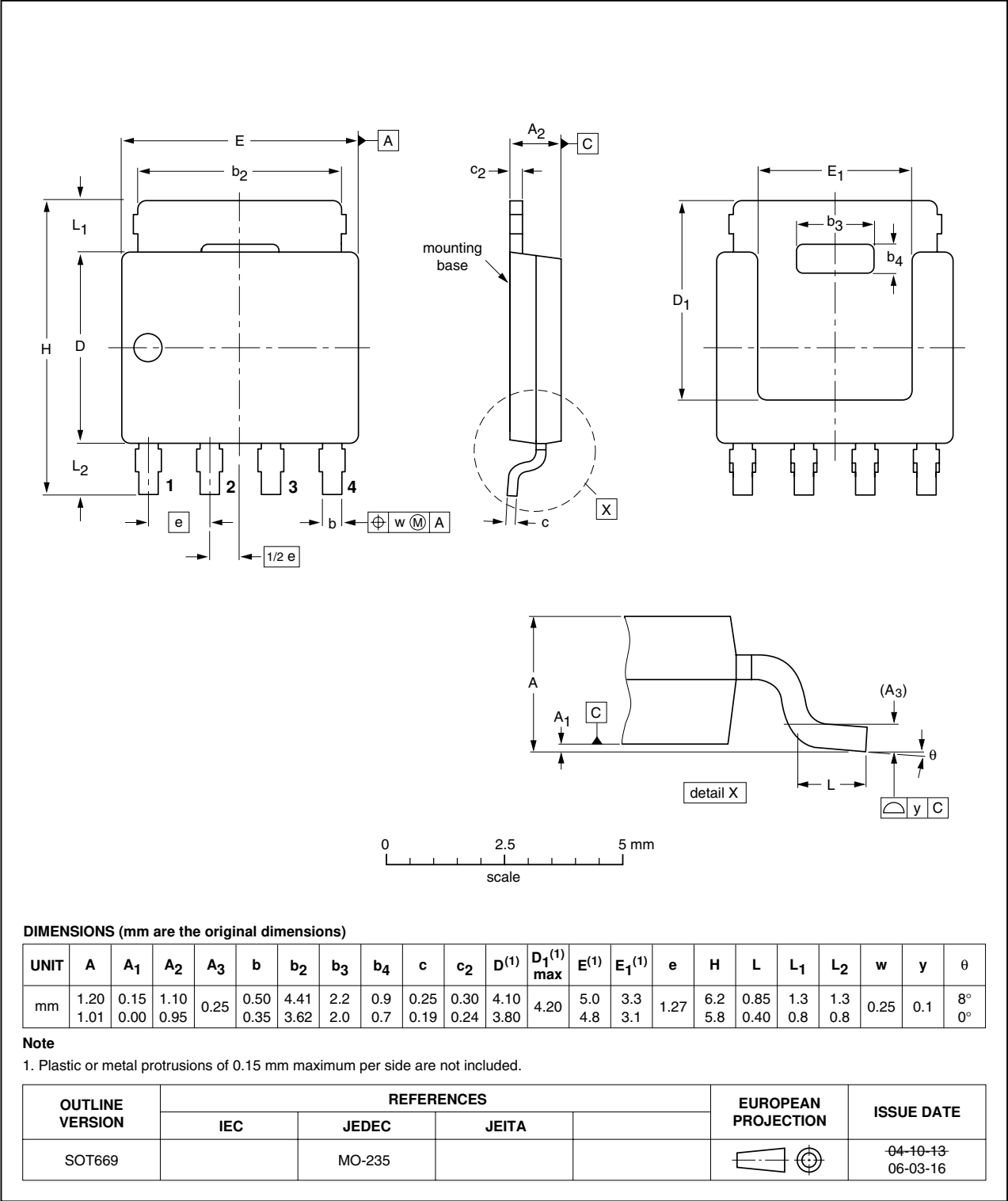


Fig 15. Package outline SOT669 (LPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH955L_2	20090219	Product data sheet	-	PH955L_1
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate.			
PH955L_1 (9397 750 14557)	20050301	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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