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Electronic Components Sourcing Information

Product Reference Information

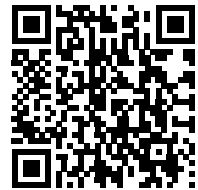
Part Number: PEMD14,115
Manufacturer: Nexperia USA Inc.
Package: SOT-563, SOT-666
Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nexperia-usa-inc/pemd14-115.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



PEMD14

50 V, 100 mA NPN/PNP resistor-equipped transistor;
R1 = 47 k Ω , R2 = open

27 April 2023

Product data sheet

1. General description

NPN/PNP Resistor-Equipped Transistor (RET) in a SOT666 ultra small and flat lead Surface-Mounted Device (SMD) plastic package.

PNP/PNP complement: PEMB14

NPN/NPN complement: PEMH14

2. Features and benefits

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place cost

3. Applications

- Low current peripheral driver
- Control of IC inputs
- Replacement of general-purpose transistors in digital applications

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V _{CEO}	collector-emitter voltage	open base	[1]	-	-	50	V
I _O	output current		[1]	-	-	100	mA
R1	bias resistor 1 (input)		[2]	33	47	61	k Ω

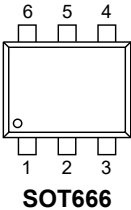
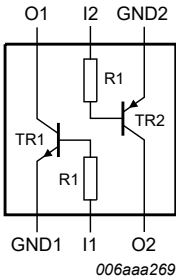
[1] For the PNP transistor with negative polarity.

[2] See section "Test information" for resistor calculation and test conditions.

50 V, 100 mA NPN/PNP resistor-equipped transistor; R1 = 47 kΩ, R2 = open

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1		
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PEMD14	SOT666	plastic, surface-mounted package; 6 leads; 0.5 mm pitch; 1.6 mm x 1.2 mm x 0.55 mm body	SOT666

7. Marking

Table 4. Marking codes

Type number	Marking code
PEMD14	5B

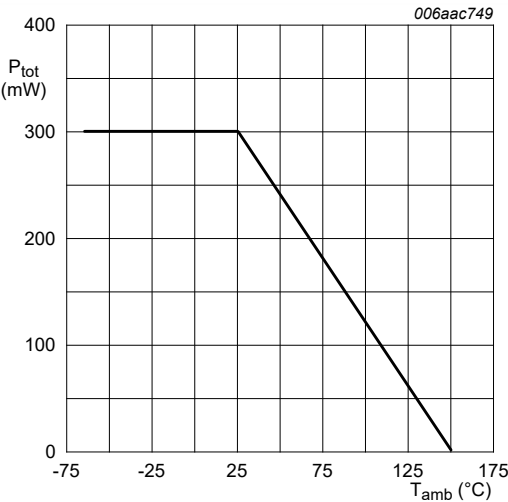
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{CBO}	collector-base voltage	open emitter	[1]	-	50	V
V _{CEO}	collector-emitter voltage	open base	[1]	-	50	V
V _{EBO}	emitter-base voltage	open collector	[1]	-	5	V
V _I	input voltage	TR1 (NPN)		-5	40	V
		TR2 (PNP)		-40	5	V
I _O	output current		[1]	-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[2] [3]	-	200	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[2] [3]	-	300	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] For the PNP transistor with negative polarity.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
[3] Reflow soldering is the only recommended soldering method.



FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint

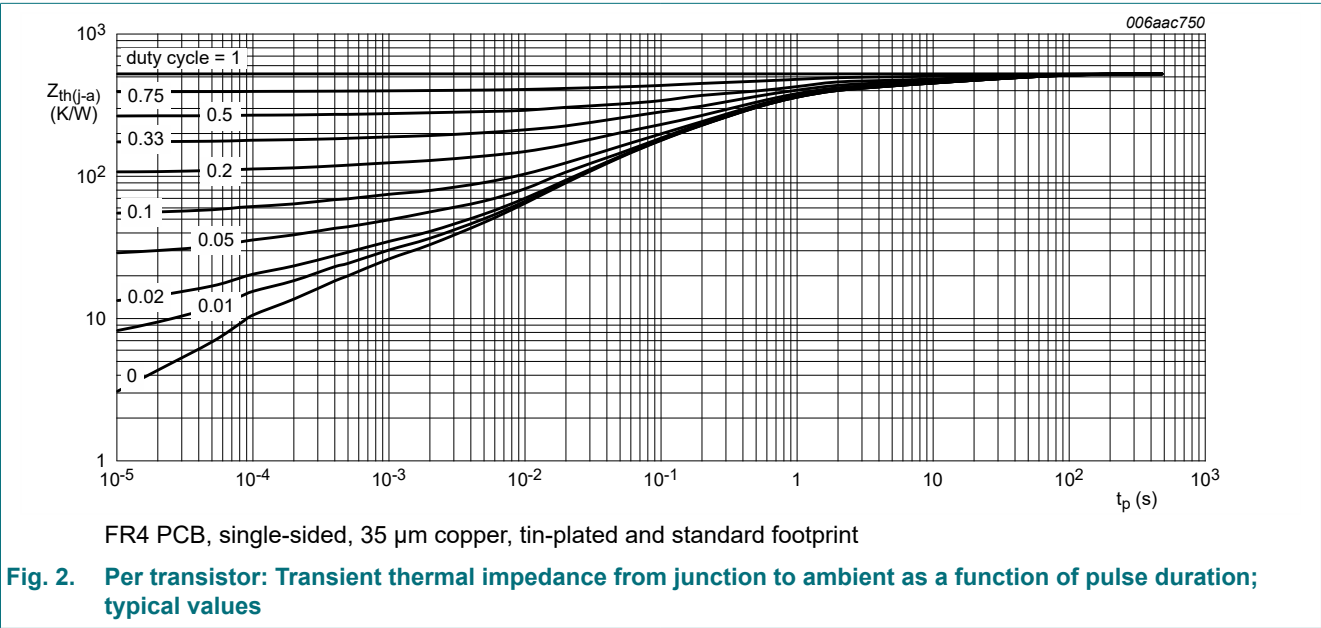
Fig. 1. Per device: Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	416	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Reflow soldering is the only recommended soldering method.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100\text{ }\mu\text{A}$; $I_E = 0\text{ A}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2\text{ mA}$; $I_B = 0\text{ A}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	50	-	-	V
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}$; $I_E = 0\text{ A}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-	1	μA
		$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$; $T_j = 150\text{ }^{\circ}\text{C}$	[1]	-	-	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}$; $I_C = 0\text{ A}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-	100	nA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}$; $I_C = 1\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	100	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}$; $I_B = 0.5\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}$; $I_C = 0.1\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	0.6	0.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}$; $I_C = 10\text{ mA}$	[1]	4	2.5	-	V
R1	bias resistor 1 (input)		[2]	33	47	61	kΩ
Transistor TR1 (NPN)							
C_c	collector capacitance	$V_{CB} = 10\text{ V}$; $I_E = 0\text{ A}$; $i_e = 0\text{ A}$; $f = 1\text{ MHz}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	2.5	pF
f_T	transition frequency	$V_{CE} = 5\text{ V}$; $I_C = 10\text{ mA}$; $f = 100\text{ MHz}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[3]	-	230	-	MHz
Transistor TR2 (PNP)							
C_c	collector capacitance	$V_{CB} = -10\text{ V}$; $I_E = 0\text{ A}$; $i_e = 0\text{ A}$; $f = 1\text{ MHz}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	3	pF
f_T	transition frequency	$V_{CE} = -5\text{ V}$; $I_C = -10\text{ mA}$; $f = 100\text{ MHz}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[3]	-	180	-	MHz

[1] For the PNP transistor with negative polarity.
[2] See section "Test information" for resistor calculation and test conditions.
[3] Characteristics of built-in transistor

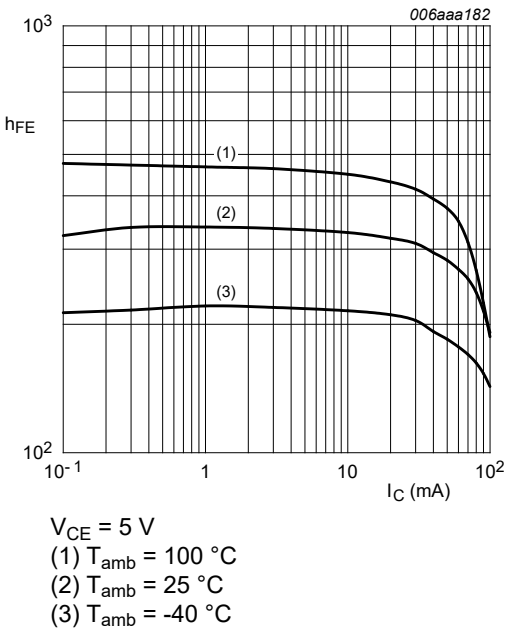


Fig. 3. TR1 (NPN): DC current gain as a function of collector current; typical values

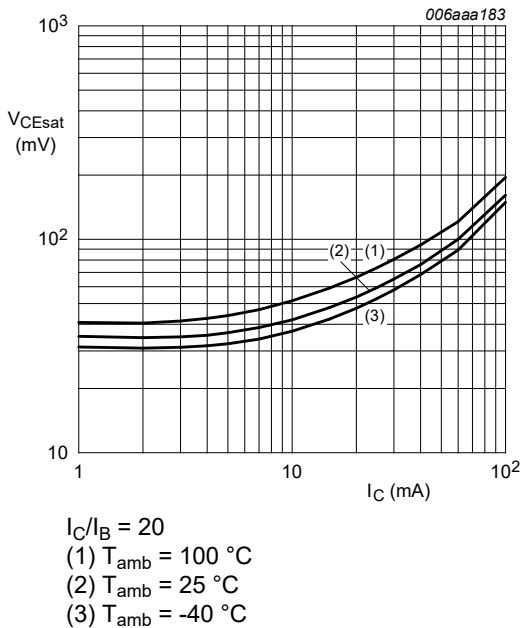


Fig. 4. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

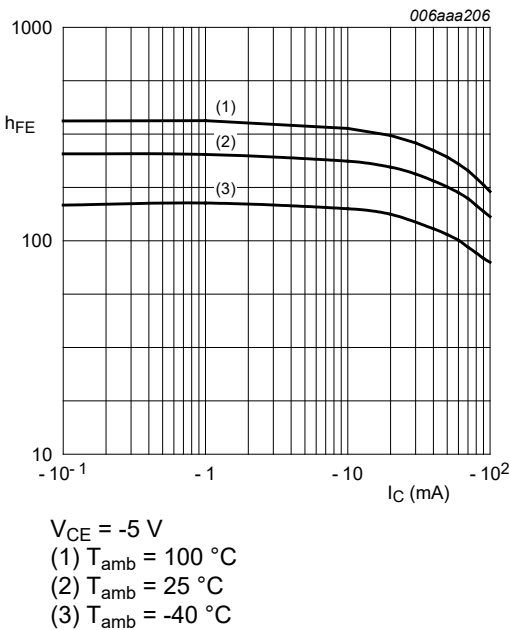


Fig. 5. TR2 (PNP): DC current gain as a function of collector current; typical values

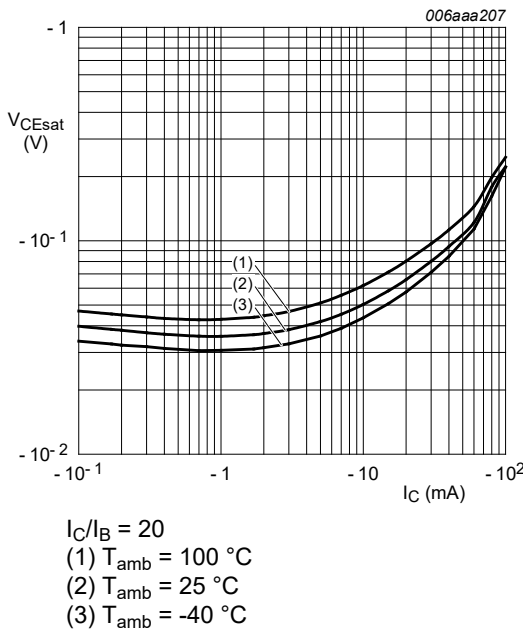


Fig. 6. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_I = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

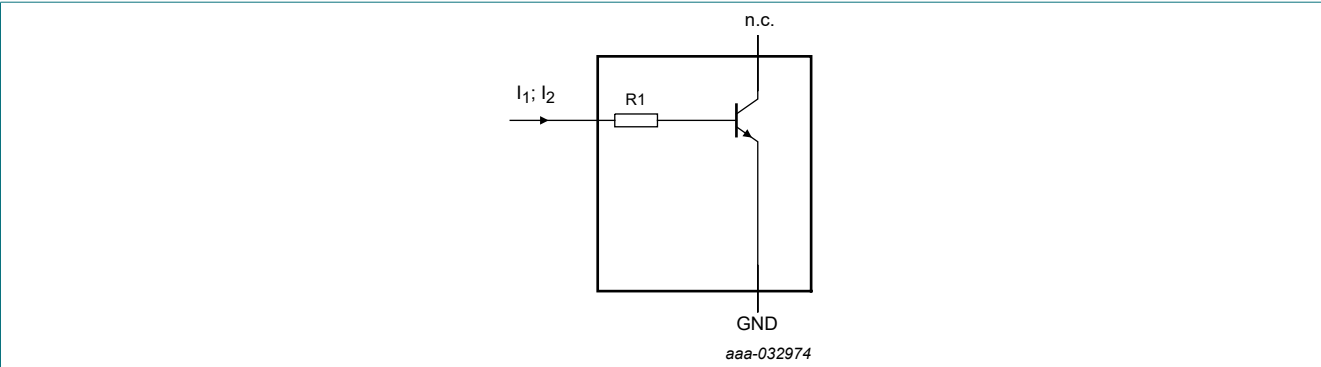


Fig. 7. TR1 (NPN): Resistor test circuit

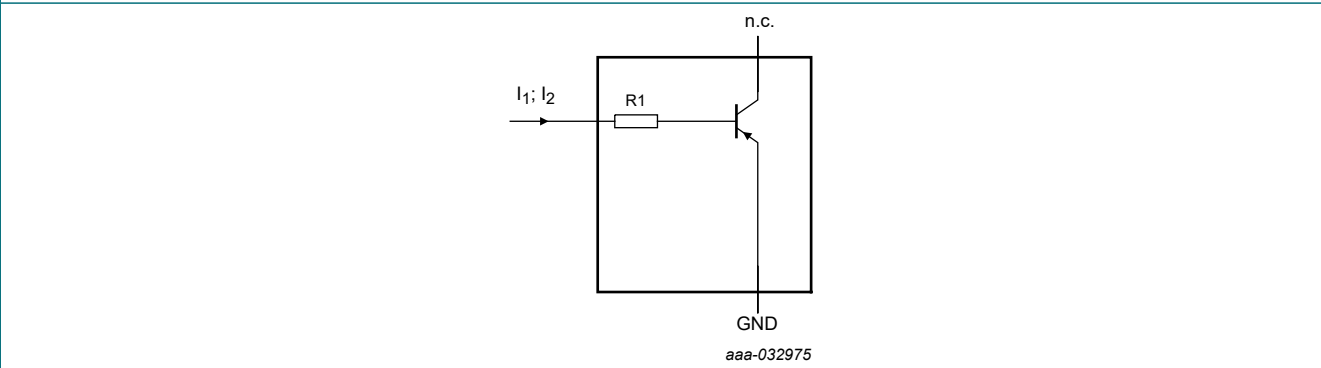


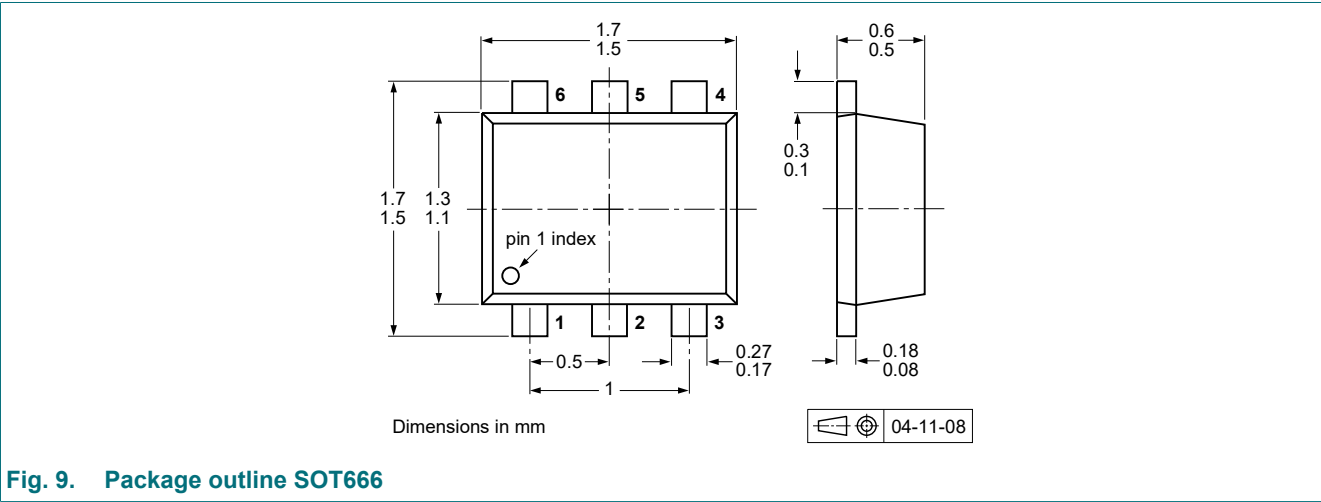
Fig. 8. TR2 (PNP): Resistor test circuit

Resistor test conditions

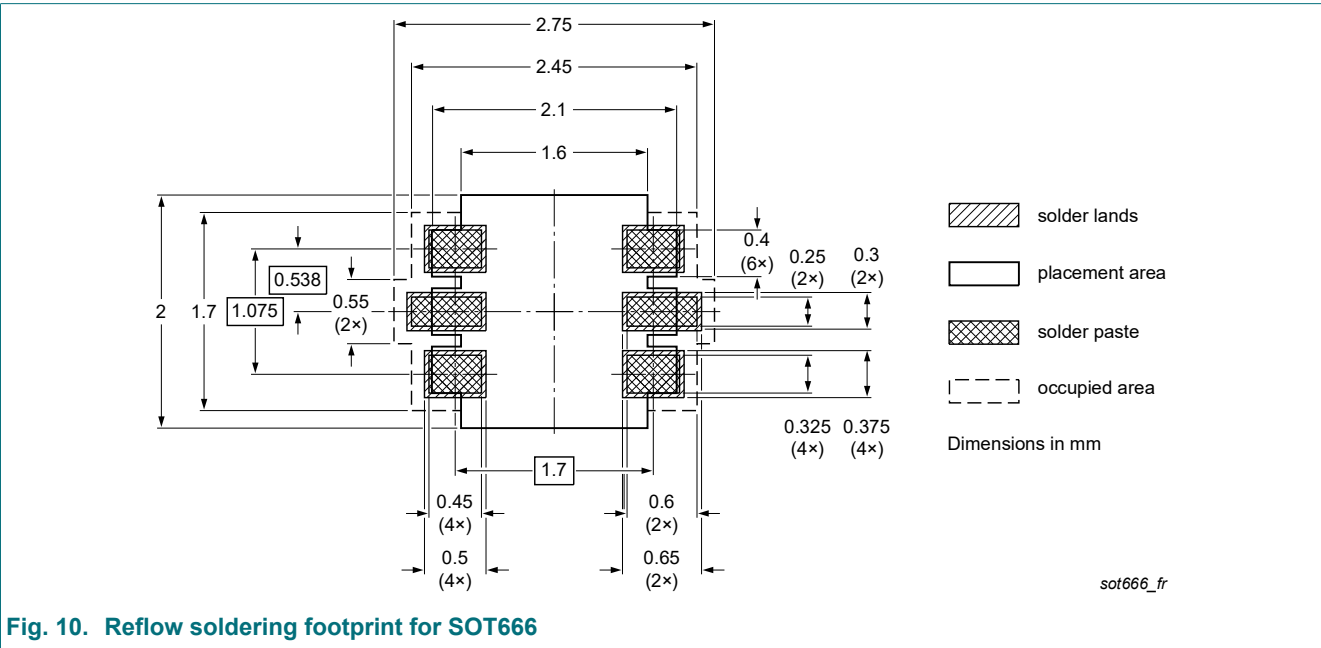
Table 8. Resistor test conditions

PEMD14	R1 (kΩ)	R2 (open)	Test conditions	
			I ₁	I ₂
TR1 (NPN)	47	-	60 μA	110 μA
TR2 (PNP)	47	-	-60 μA	-110 μA

12. Package outline



13. Soldering



14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PEMD14 v.3	20230427	Product data sheet	-	PEMD14_PUMD14_2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Family data sheet splitted to single type data sheets. • Section "Packing information" removed. • Product changed to non-automotive qualification.			
PEMD14_PUMD14_2	20090902	Product data sheet	-	PEMD14_PUMD14_1
PEMD14_PUMD14_1	20050114	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information.....2

6. Ordering information.....2

7. Marking.....2

8. Limiting values..... 3

9. Thermal characteristics..... 4

10. Characteristics..... 5

11. Test information..... 7

12. Package outline..... 8

13. Soldering..... 8

14. Revision history.....9

15. Legal information.....10

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