

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: NX3008PBKS,115
Manufacturer: Nexperia USA Inc.
Package: Please confirm with sales
Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nexperia-usa-inc/nx3008pbks-115.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



NX3008PBKS

30 V, 200 mA dual P-channel Trench MOSFET

Rev. 1 — 1 August 2011

Product data sheet

1. Product profile

1.1 General description

Dual P-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Very fast switching
- Low threshold voltage
- Trench MOSFET technology
- ESD protection up to 2 kV
- AEC-Q101 qualified

1.3 Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

1.4 Quick reference data

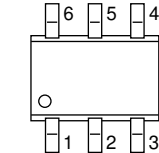
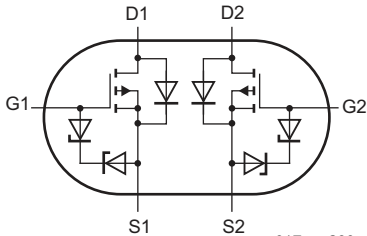
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-30	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V};$ $T_{amb} = 25\text{ °C}$	[1]	-	-200	mA
Static characteristics (per transistor)						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V};$ $I_D = -200\text{ mA}; T_j = 25\text{ °C}$	-	2.8	4.1	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 SOT363 (SC-88)	 017aaa260
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX3008PBKS	SC-88	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
NX3008PBKS	LC%

[1] % = placeholder for manufacturing site code.

5. Limiting values

Table 5. Limiting values

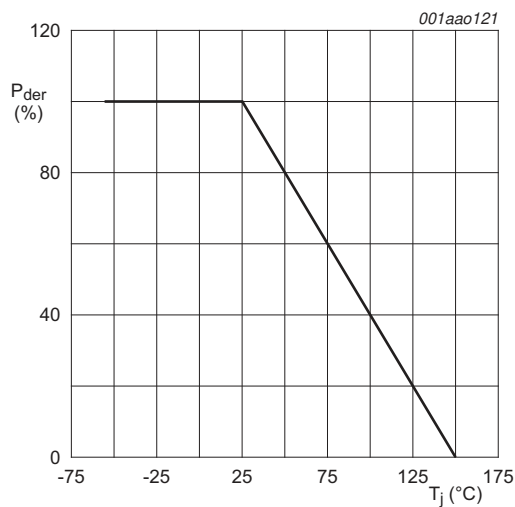
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor					
V _{DS}	drain-source voltage	T _j = 25 °C	-	-30	V
V _{GS}	gate-source voltage		-8	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1] -	-200	mA
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1] -	-125	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs	-	-0.8	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2] -	280	mW
			[1] -	320	mW
		T _{sp} = 25 °C	-	990	mW
Per device					
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2] -	445	mW
T _j	junction temperature		-55	150	°C
T _{amb}	ambient temperature		-55	150	°C
T _{stg}	storage temperature		-65	150	°C
Source-drain diode					
I _S	source current	T _{amb} = 25 °C	[1] -	-200	mA
ESD maximum rating					
V _{ESD}	electrostatic discharge voltage	HBM	[3] -	2000	V

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².

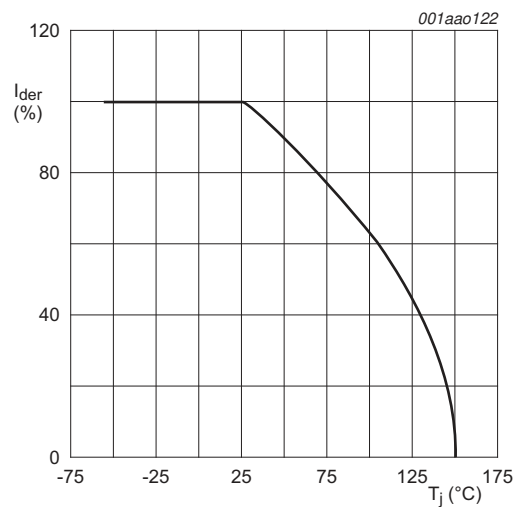
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



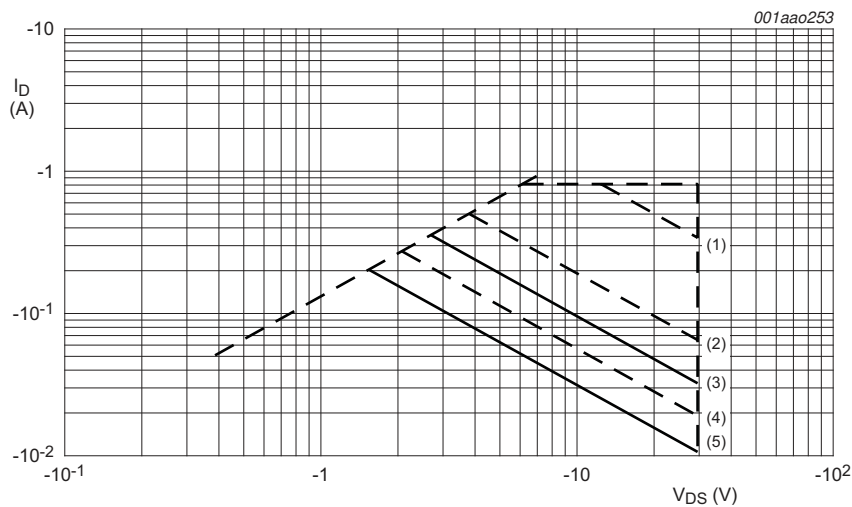
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} is a single pulse

(1) $t_p = 1$ ms

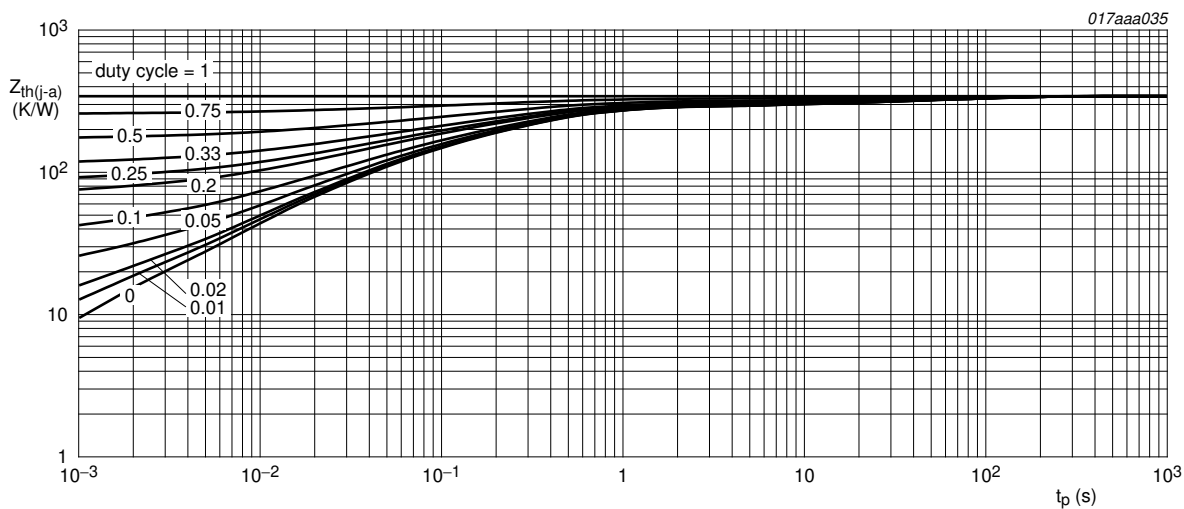
(2) $t_p = 10$ ms

(3) DC; $T_{sp} = 25^{\circ}\text{C}$

(4) $t_p = 100$ ms

(5) DC; $T_{amb} = 25^{\circ}\text{C}$; 1 cm^2 drain mounting pad

Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage



FR4 PCB, mounting pad for drain 1 cm²

Fig 5. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics (per transistor)						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250\ \mu\text{A}$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ\text{C}$	-0.6	-0.9	-1.1	V
I_{DSS}	drain leakage current	$V_{DS} = -30\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	-1	μA
		$V_{DS} = -30\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 150\ ^\circ\text{C}$	-	-	-10	μA
I_{GSS}	gate leakage current	$V_{GS} = 8\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-0.2	-1	μA
		$V_{GS} = -8\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-0.2	-1	μA
		$V_{GS} = 4.5\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-10	-	nA
		$V_{GS} = -4.5\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-10	-	nA
		$V_{GS} = 2.5\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-1	-	nA
		$V_{GS} = -2.5\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-1	-	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\ \text{V}$; $I_D = -200\ \text{mA}$; $T_j = 25\ ^\circ\text{C}$	-	2.8	4.1	Ω
		$V_{GS} = -4.5\ \text{V}$; $I_D = -200\ \text{mA}$; $T_j = 150\ ^\circ\text{C}$	-	5.3	7.8	Ω
		$V_{GS} = -2.5\ \text{V}$; $I_D = -10\ \text{mA}$; $T_j = 25\ ^\circ\text{C}$	-	5.3	6.5	Ω
g_{fs}	forward transconductance	$V_{DS} = -10\ \text{V}$; $I_D = -200\ \text{mA}$; $T_j = 25\ ^\circ\text{C}$	-	160	-	mS
Dynamic characteristics (per transistor)						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -15\ \text{V}$; $I_D = -200\ \text{mA}$; $V_{GS} = -4.5\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	0.55	0.72	nC
Q_{GS}	gate-source charge		-	0.23	-	nC
Q_{GD}	gate-drain charge		-	0.09	-	nC
C_{iss}	input capacitance	$V_{DS} = -15\ \text{V}$; $f = 1\ \text{MHz}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	31	46	pF
C_{oss}	output capacitance		-	6.5	-	pF
C_{rss}	reverse transfer capacitance		-	2.3	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -20\ \text{V}$; $R_L = 250\ \Omega$; $V_{GS} = -4.5\ \text{V}$; $R_{G(ext)} = 6\ \Omega$; $T_j = 25\ ^\circ\text{C}$	-	19	38	ns
t_r	rise time		-	30	-	ns
$t_{d(off)}$	turn-off delay time		-	65	130	ns
t_f	fall time		-	38	-	ns
Source-drain diode (per transistor)						
V_{SD}	source-drain voltage	$I_S = -200\ \text{mA}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-0.47	-0.88	-1.2	V

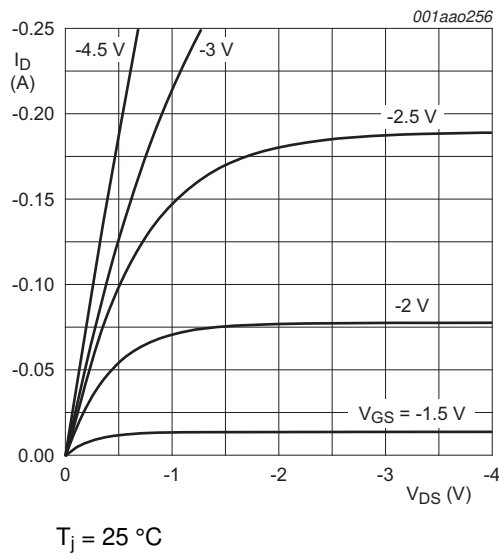


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

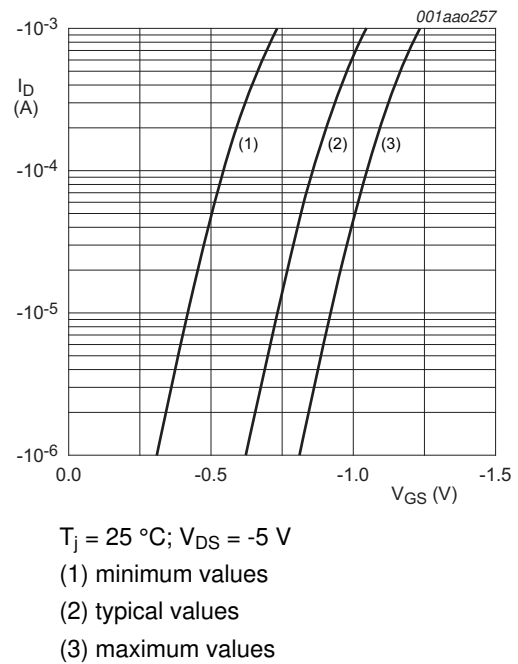


Fig 7. Sub-threshold drain current as a function of gate-source voltage

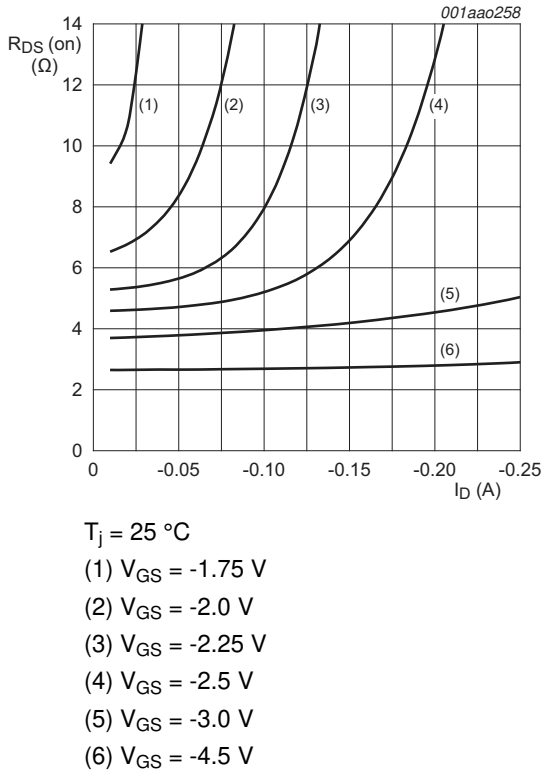


Fig 8. Drain-source on-state resistance as a function of drain current; typical values

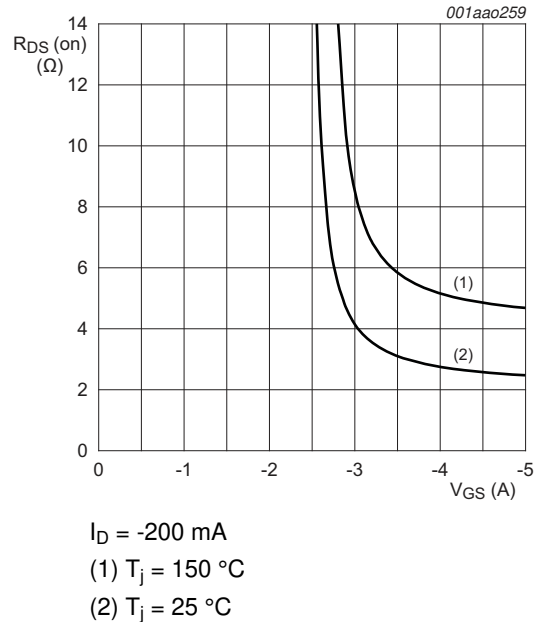
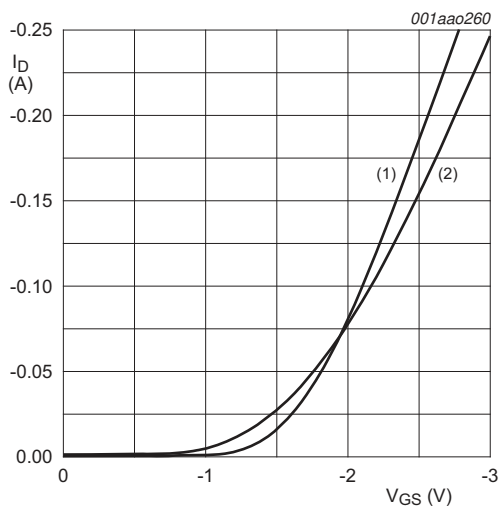
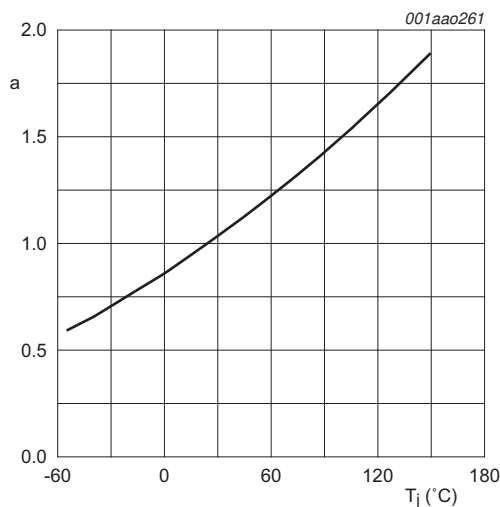


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



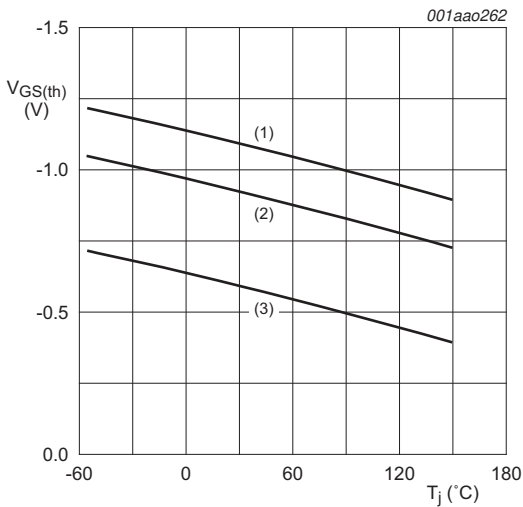
$V_{DS} > I_D \times R_{DS(on)}$
(1) $T_j = 25\text{ °C}$
(2) $T_j = 150\text{ °C}$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



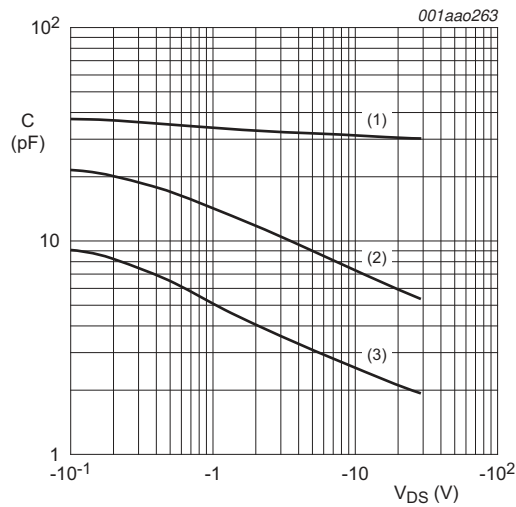
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^{\circ}\text{C})}}$$

Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



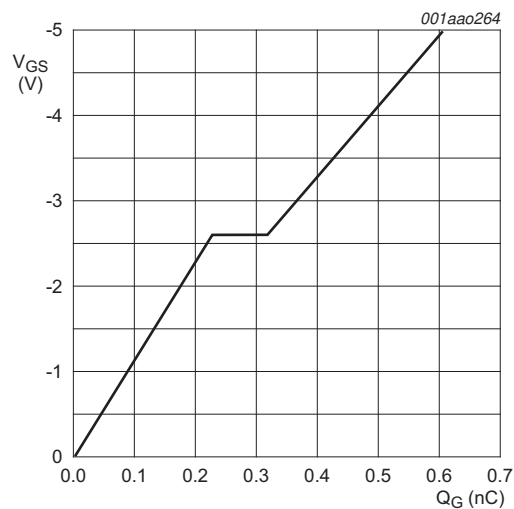
$I_D = -0.25\text{ mA}; V_{DS} = V_{GS}$
(1) maximum values
(2) typical values
(3) minimum values

Fig 12. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$
(1) C_{iss}
(2) C_{oss}
(3) C_{rss}

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = -200\text{ mA}$; $V_{DS} = -15\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig 14. Gate-source voltage as a function of gate charge; typical values

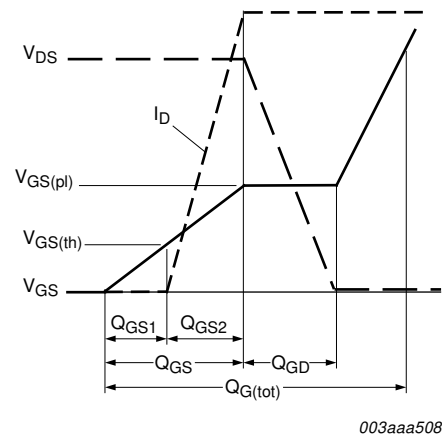
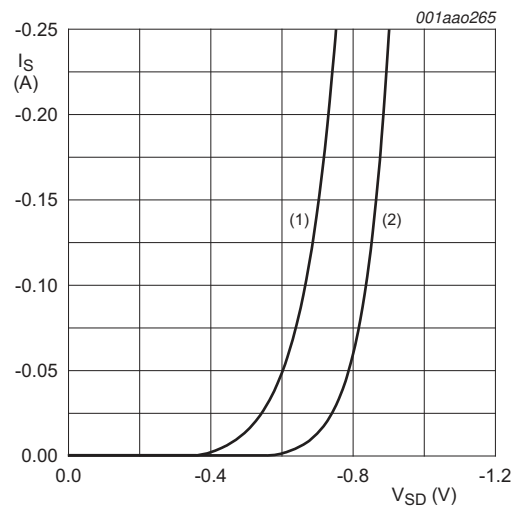


Fig 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$
(1) $T_j = 150\text{ }^{\circ}\text{C}$
(2) $T_j = 25\text{ }^{\circ}\text{C}$

Fig 16. Source current as a function of source-drain voltage; typical values

8. Test information

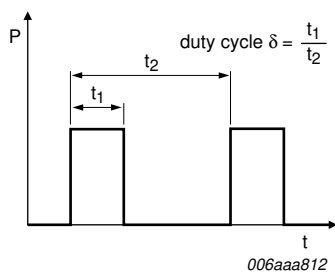


Fig 17. Duty cycle definition

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline

Plastic surface-mounted package; 6 leads

SOT363

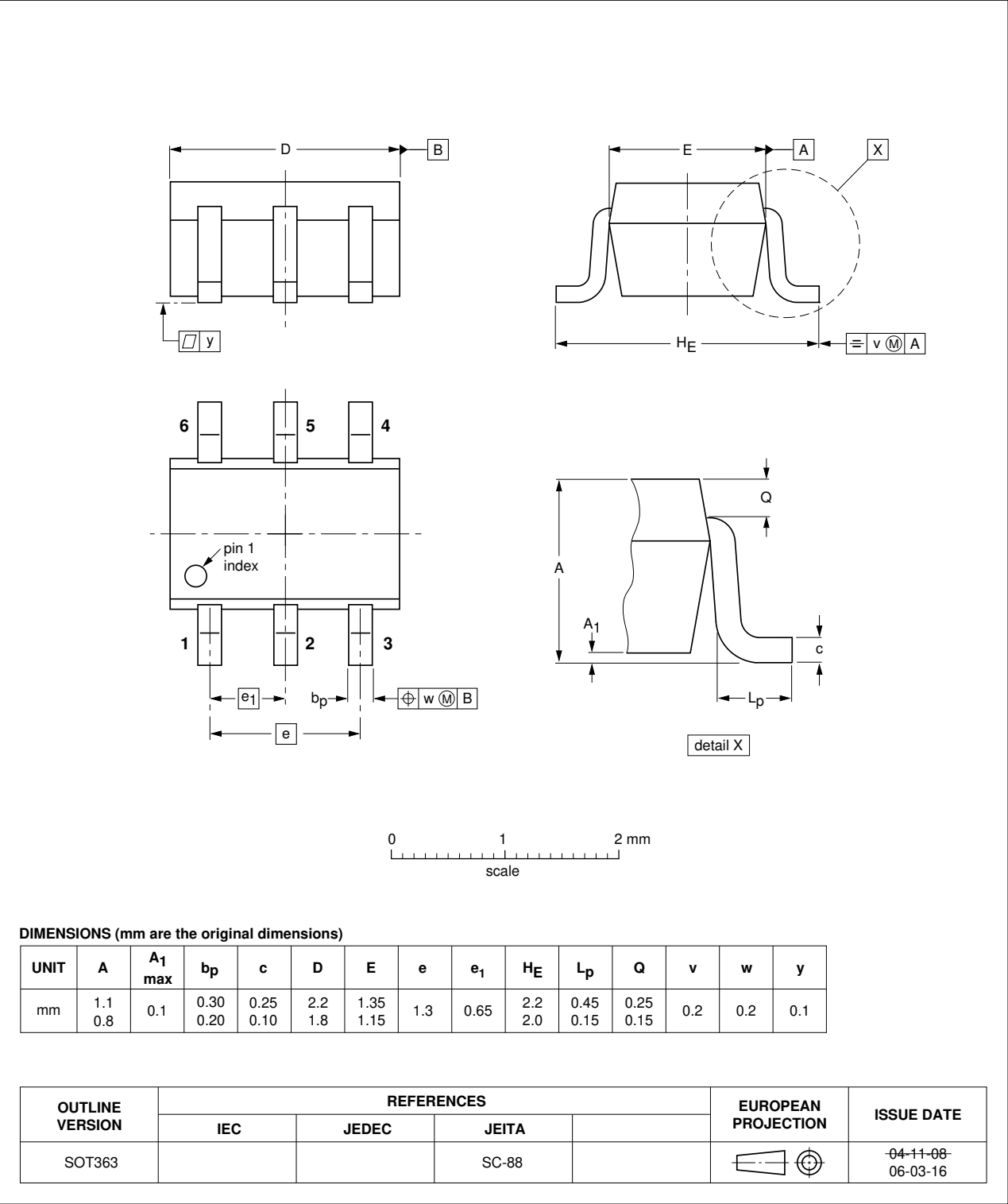
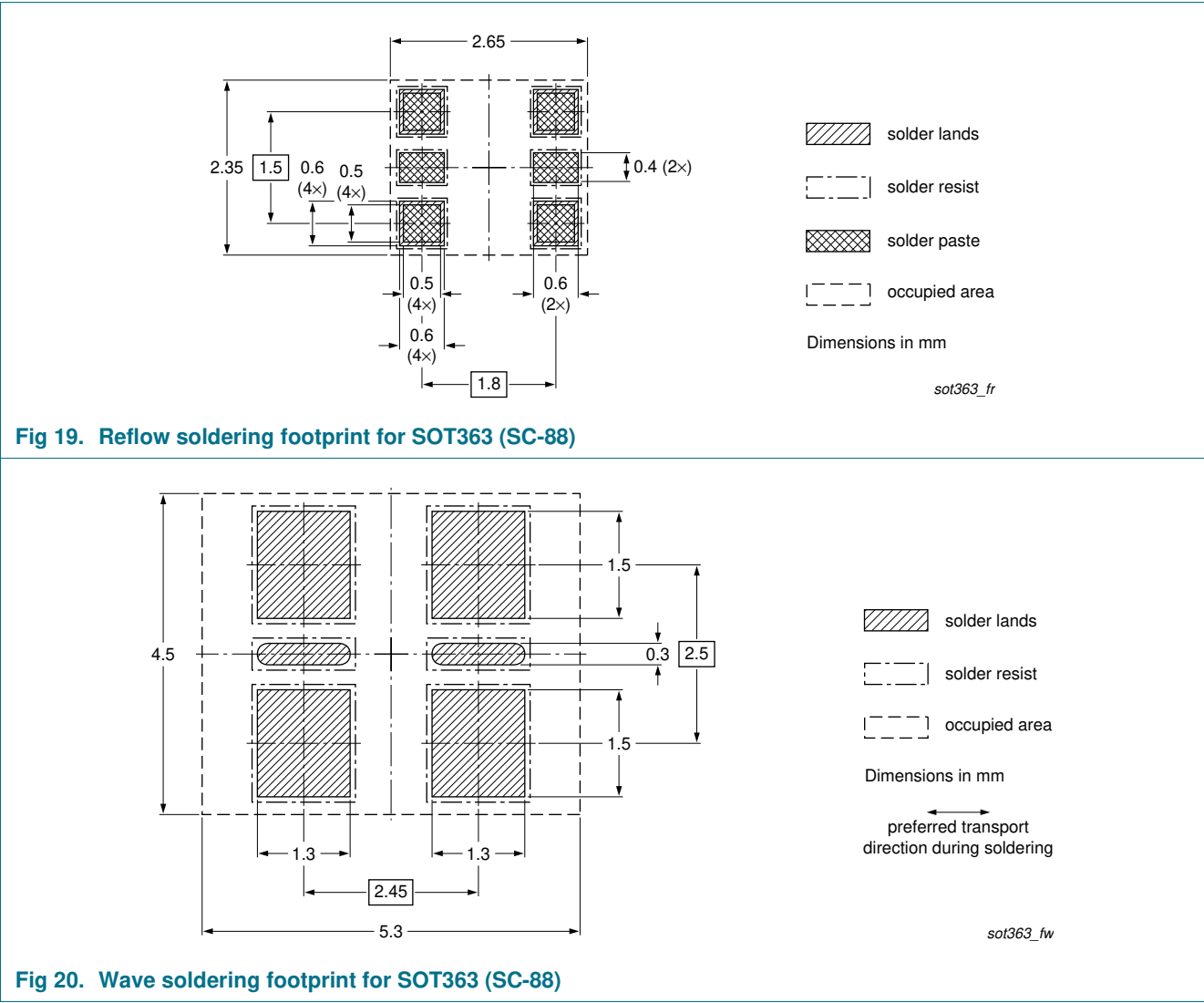


Fig 18. Package outline SOT363 (SC-88)

10. Soldering



11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3008PBKS v.1	20110801	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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