

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: GAN3R2-100CBEAZ
Manufacturer: Nexperia USA Inc.
Package: Please confirm with sales
Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nexperia-usa-inc/gan3r2-100cbeaz.html>

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This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



GAN3R2-100CBE

100 V, 3.2 mOhm Gallium Nitride (GaN) FET in a
3.5 mm x 2.13 mm Wafer Level Chip-Scale Package (WLCSP)

27 April 2023

Product data sheet

1. General description

The GAN3R2-100CBE is a general purpose 100 V, 3.2 mΩ Gallium Nitride (GaN) FET in a 15 bump Wafer Level Chip-Scale Package (WLCSP). It is a normally-off e-mode device offering superior performance.

2. Features and benefits

- Enhancement mode - normally-off power switch
- Ultra high frequency switching capability
- No body diode
- Low gate charge, low output charge
- Qualified for standard applications
- ESD protection
- RoHS, Pb-free, REACH-compliant
- High efficiency and high power density
- Wafer Level Chip-Scale Package (WLCSP) 3.5 mm x 2.13 mm

3. Applications

- High power density and high efficiency power conversion
- AC-to-DC converters, (secondary stage)
- High frequency DC-to-DC converters in 48 V systems
- Fast battery charging, mobile phone, laptop, tablet and USB type-C chargers
- Datacom and telecom (AC-to-DC and DC-to-DC) converters
- Motor drives
- LiDAR (non-automotive)
- Class D audio amplifiers

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage		-	-	100	V
V_{TDS}	transient drain to source voltage	pulsed; $t_p = 1 \mu s$; $\delta_{factor} = 0.01$	-	-	130	V
I_D	drain current	$V_{GS} = 5 V$	[1]	-	60	A
P_{tot}	total power dissipation	Fig. 1	-	-	394	W
T_j	junction temperature		-40	-	150	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 V$; $I_D = 25 A$; $T_j = 25 ^\circ C$; Fig. 9 ; Fig. 10 ; Fig. 11 ; Fig. 12	-	2.4	3.2	mΩ
R_G	gate resistance	$f = 5 MHz$; $T_j = 25 ^\circ C$	-	2.2	-	Ω

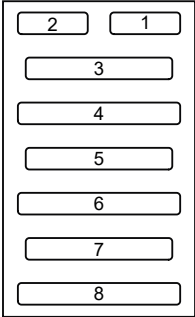
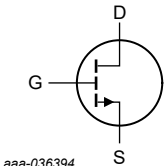
100 V, 3.2 mOhm Gallium Nitride (GaN) FET in a 3.5 mm x 2.13 mm Wafer Level Chip-Scale Package (WLCSP)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14		-	1.7	-	nC
$Q_{G(tot)}$	total gate charge			-	9.2	12	nC
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $T_j = 25\text{ °C}$	[2]	-	50	-	nC

- [1] Limited by package
- [2] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since $Q_r = Q_{oss} + Q_D$, and $Q_D = 0$. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view WLCSP8 (WLCSP8-SOT8072)	
2	S	source		
3	D	drain		
4	S	source		
5	D	drain		
6	S	source		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GAN3R2-100CBE	WLCSP8	wafer level chip-scale package; 8 solder bars; body: 3.5 x 2.13 x 0.429 mm	WLCSP8-SOT8072

7. Marking

Table 4. Marking codes

Type number	Marking code
GAN3R2-100CBE	3R2DCBE

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage			-	100	V

100 V, 3.2 mOhm Gallium Nitride (GaN) FET in a 3.5 mm x 2.13 mm Wafer Level Chip-Scale Package (WLCSP)

Symbol	Parameter	Conditions		Min	Max	Unit
V _{TDS}	transient drain to source voltage	pulsed; t _p = 1 μs; δ _{factor} = 0.01		-	130	V
V _{GS}	gate-source voltage			-4	6	V
P _{tot}	total power dissipation	Fig. 1		-	394	W
I _D	drain current	V _{GS} = 5 V	[1]	-	60	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; Fig. 2	[1]	-	230	A
T _{stg}	storage temperature			-40	150	°C
T _j	junction temperature			-40	150	°C
T _{slid(M)}	peak soldering temperature			-	260	°C

[1] Limited by package

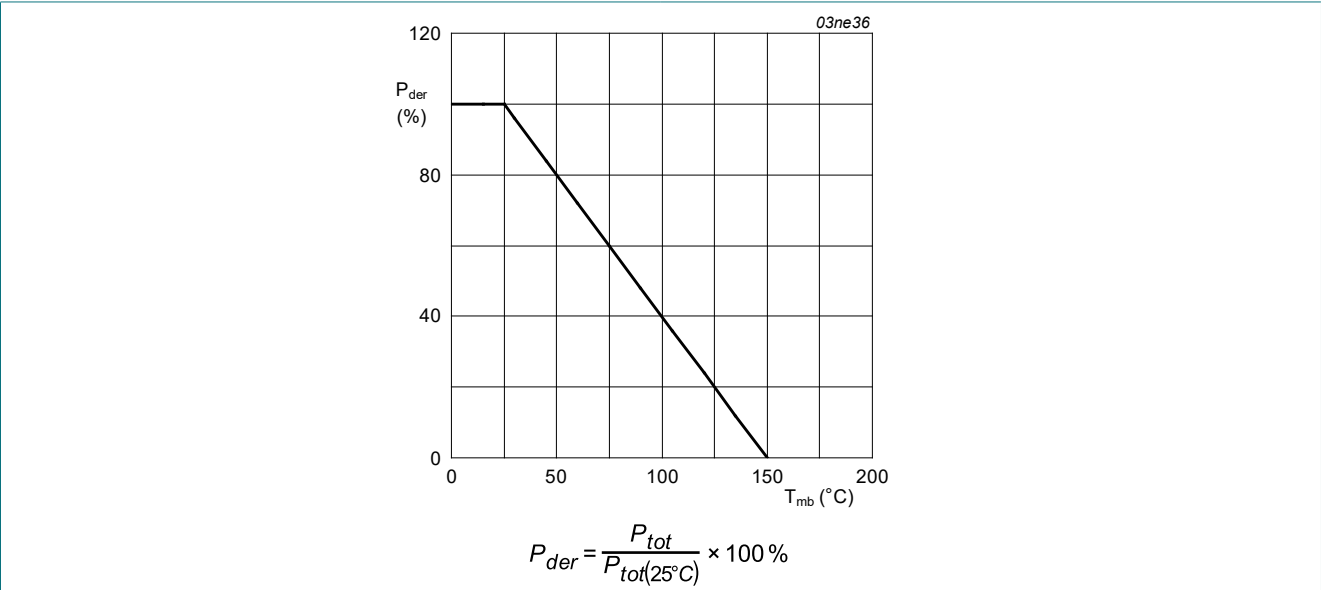


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

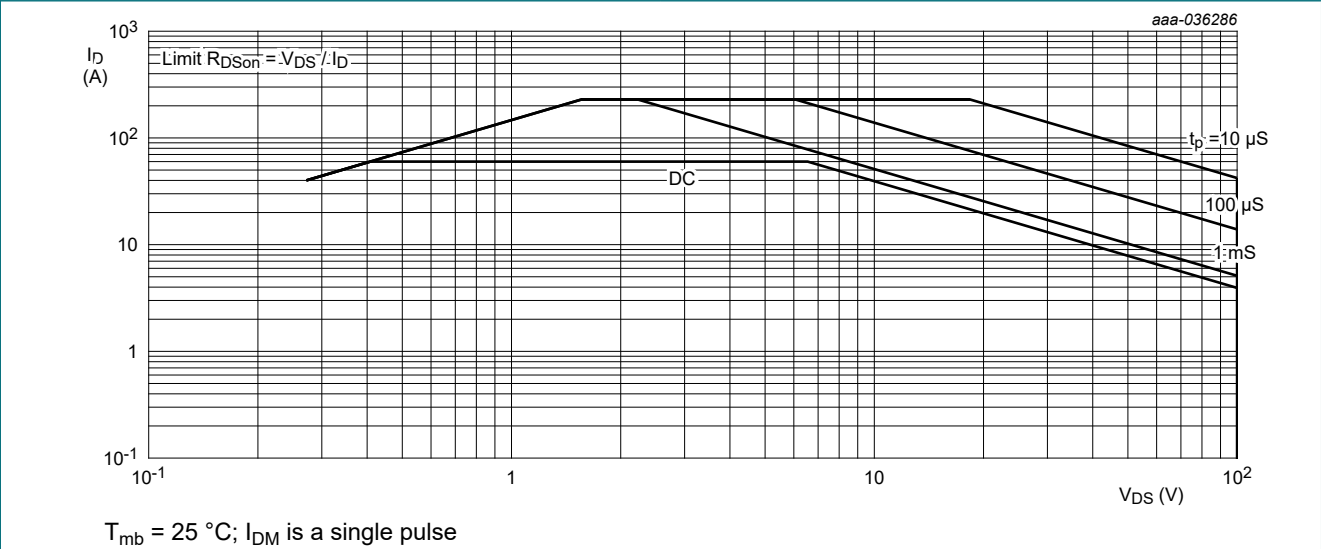


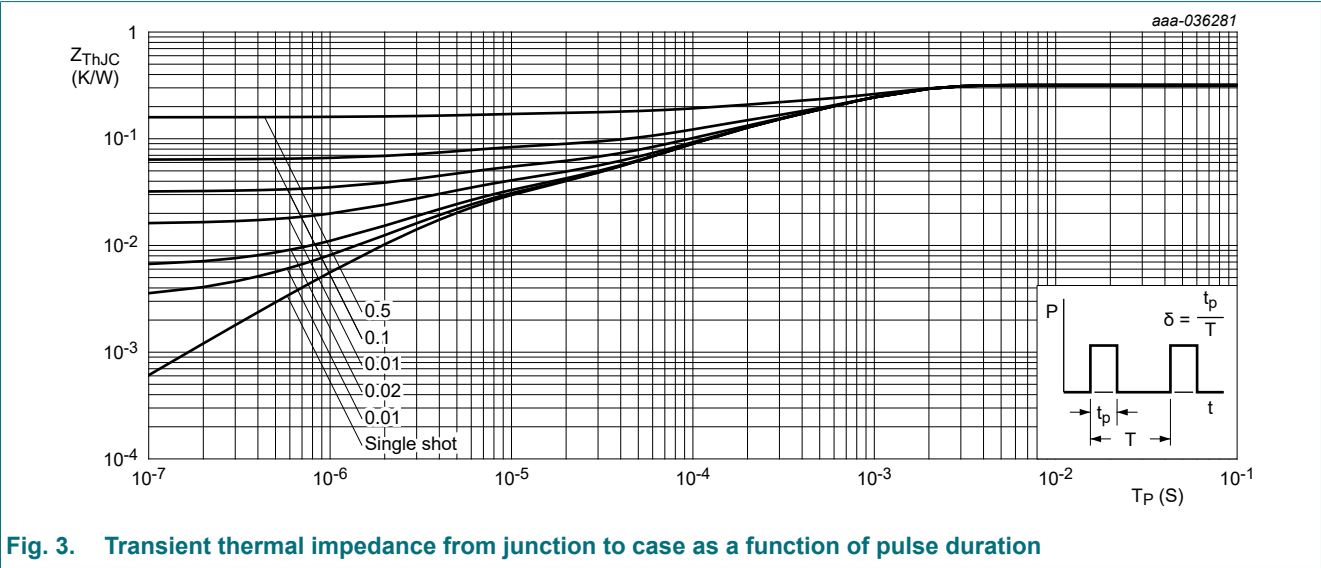
Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	Fig. 3	-	-	0.3	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	1.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	-	-	33	K/W

[1] $R_{th(j-a)}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 400 \mu A$; $V_{GS} = 0 V$; $T_j = 25^\circ C$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 9 mA$; $V_{DS} = V_{GS}$; $T_j = 25^\circ C$; Fig. 8	0.8	1.1	2.5	V
I_{DSS}	drain leakage current	$V_{DS} = 80 V$; $V_{GS} = 0 V$; $T_j = 25^\circ C$	-	80	350	μA
I_{GSS}	gate leakage current	$V_{GS} = 5 V$; $V_{DS} = 0 V$; $T_j = 25^\circ C$	-	20	5000	μA
		$V_{GS} = 5 V$; $V_{DS} = 0 V$; $T_j = 125^\circ C$	-	600	9000	μA
		$V_{GS} = -4 V$; $V_{DS} = 0 V$; $T_j = 25^\circ C$	-	60	400	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 V$; $I_D = 25 A$; $T_j = 25^\circ C$; Fig. 9; Fig. 10; Fig. 11; Fig. 12	-	2.4	3.2	m Ω
R_G	gate resistance	$f = 5 MHz$; $T_j = 25^\circ C$	-	2.2	-	Ω

100 V, 3.2 mOhm Gallium Nitride (GaN) FET in a 3.5 mm x 2.13 mm Wafer Level Chip-Scale Package (WLCSP)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 13 ; Fig. 14		-	9.2	12	nC
Q_{GS}	gate-source charge			-	1.9	-	nC
Q_{GD}	gate-drain charge			-	1.7	-	nC
C_{iss}	input capacitance	$V_{DS} = 50\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 100\text{ kHz}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 15		-	1000	-	pF
C_{oss}	output capacitance			-	460	-	pF
C_{rss}	reverse transfer capacitance			-	8.2	-	pF
$C_{o(er)}$	effective output capacitance, energy related	$0\text{ V} \leq V_{DS} \leq 50\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 16	[1]	-	700	-	pF
$C_{o(tr)}$	effective output capacitance, time related	$0\text{ V} \leq V_{DS} \leq 50\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$	[2]	-	1020	-	pF
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$	[3]	-	50	-	nC
Source-drain characteristics							
V_{SD}	source-drain voltage	$I_S = 0.5\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 17 ; Fig. 18 ; Fig. 19 ; Fig. 20		-	1.5	-	V

- [1] $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50 V
- [2] $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50 V
- [3] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since $Q_r = Q_{oss} + Q_D$, and $Q_D = 0$. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)

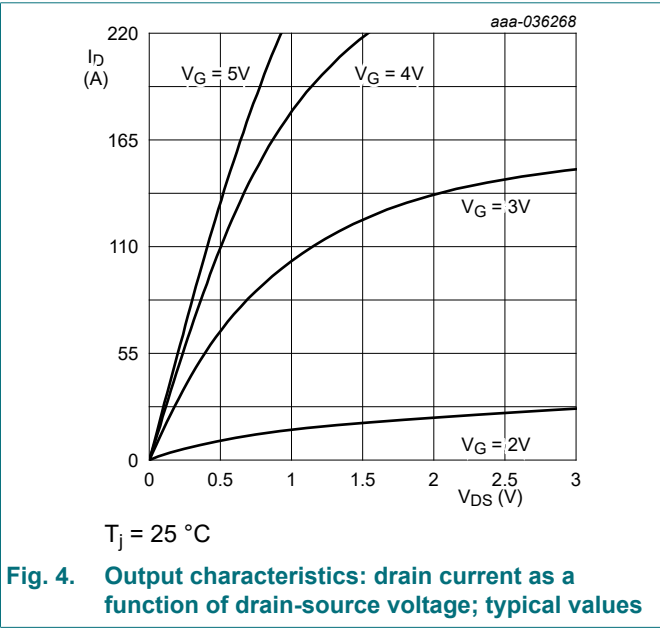


Fig. 4. Output characteristics: drain current as a function of drain-source voltage; typical values

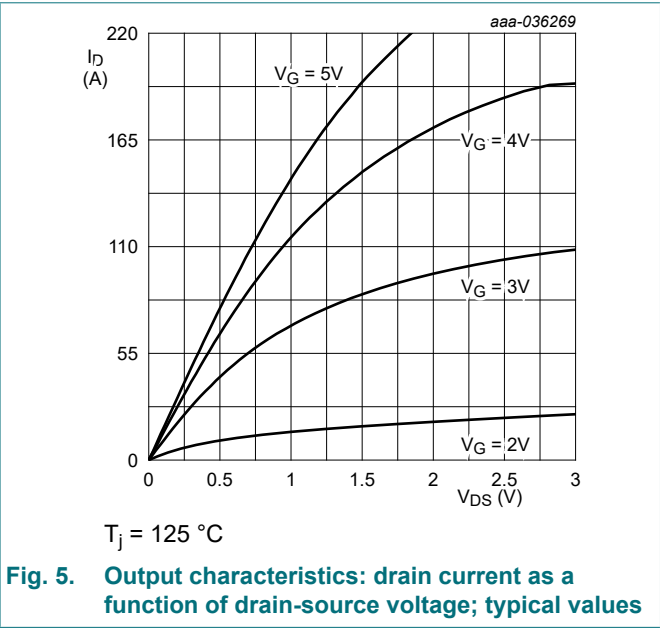


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

100 V, 3.2 mOhm Gallium Nitride (GaN) FET in a 3.5 mm x 2.13 mm Wafer Level Chip-Scale Package (WLCSP)

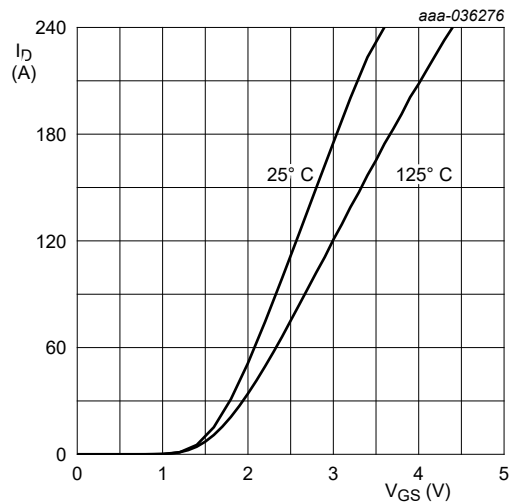
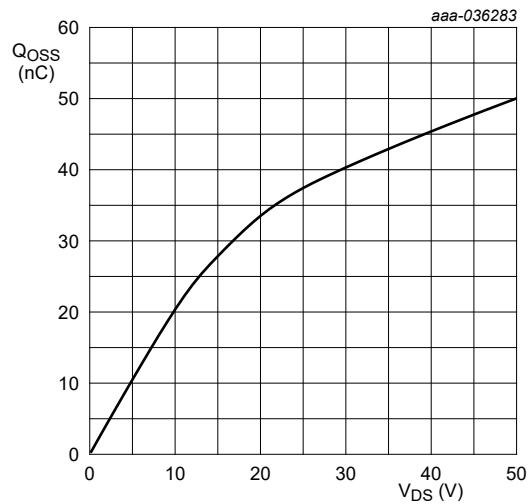
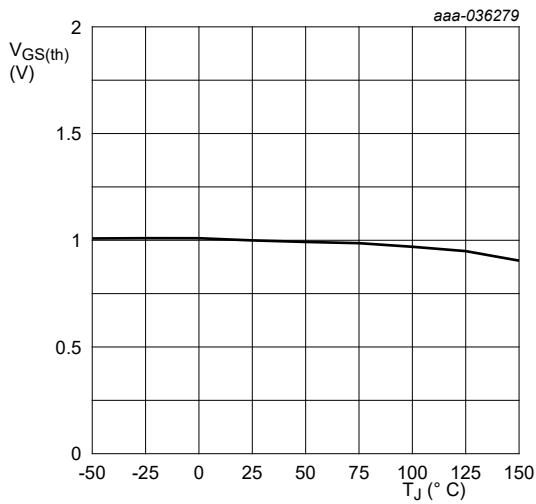


Fig. 6. Transfer characteristics; drain current as a function of gate-source voltage; typical values



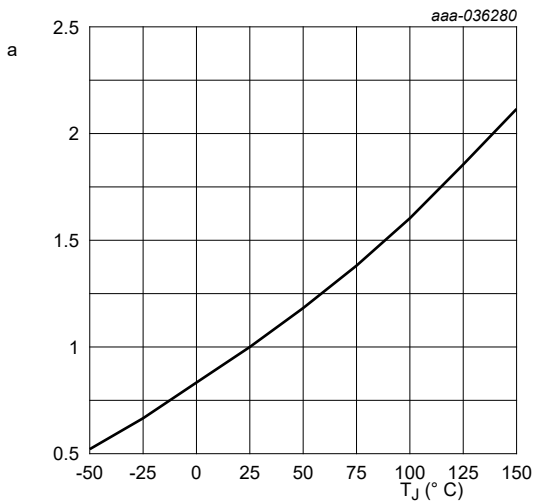
Freq. = 100 kHz

Fig. 7. Output charge as a function of drain-source voltage; typical values



$I_D = 9\text{ mA}$; $V_{DS} = V_{GS}$

Fig. 8. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 9. Normalized drain-source on-state resistance factor as a function of junction temperature

100 V, 3.2 mOhm Gallium Nitride (GaN) FET in a 3.5 mm x 2.13 mm Wafer Level Chip-Scale Package (WLCSP)

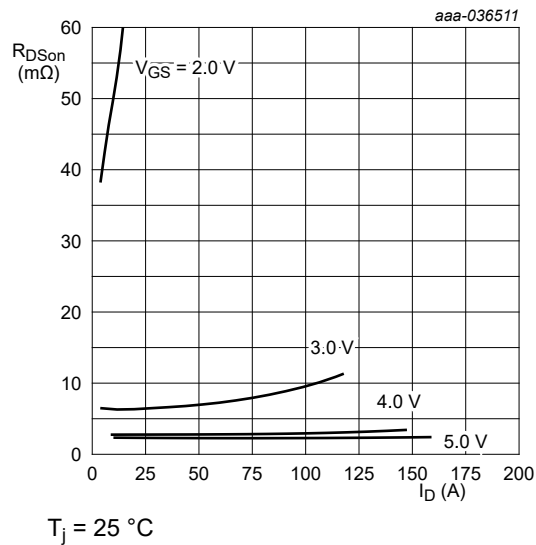


Fig. 10. Drain-source on-state resistance as a function of drain current ; typical values

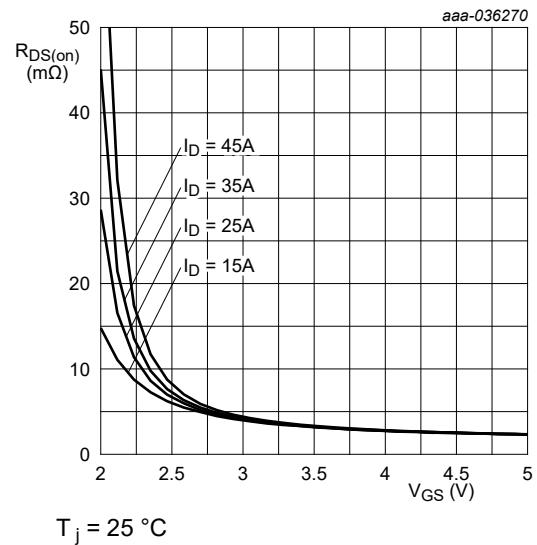


Fig. 11. Drain-source on-state resistance as a function of gate-source voltage; typical values

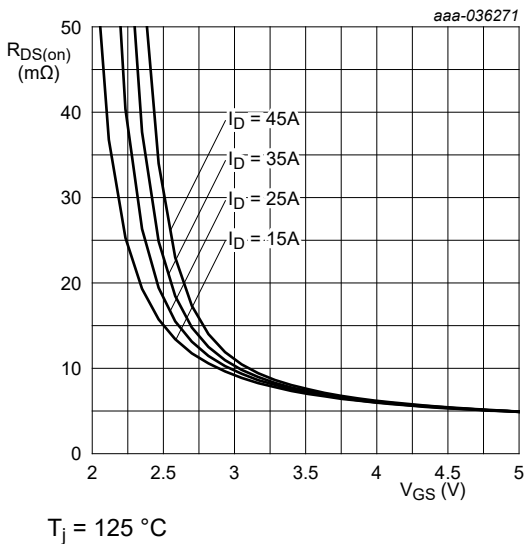


Fig. 12. Drain-source on-state resistance as a function of gate-source voltage; typical values

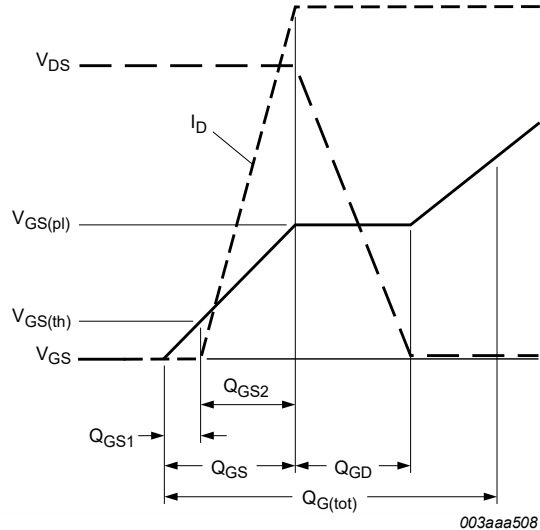
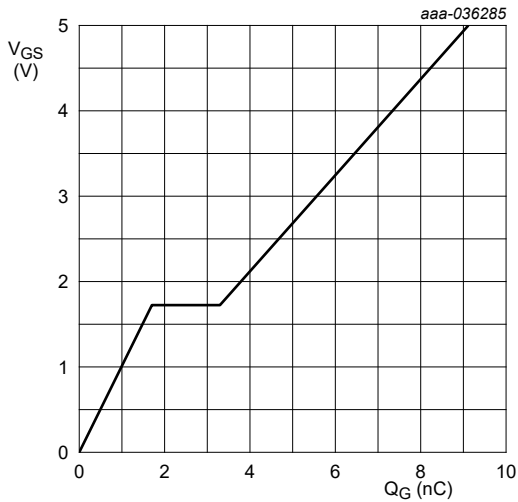


Fig. 13. Gate charge waveform definitions

100 V, 3.2 mOhm Gallium Nitride (GaN) FET in a 3.5 mm x 2.13 mm Wafer Level Chip-Scale Package (WLCSP)



$T_J = 25\text{ }^{\circ}\text{C}$; $I_D = 25\text{ A}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

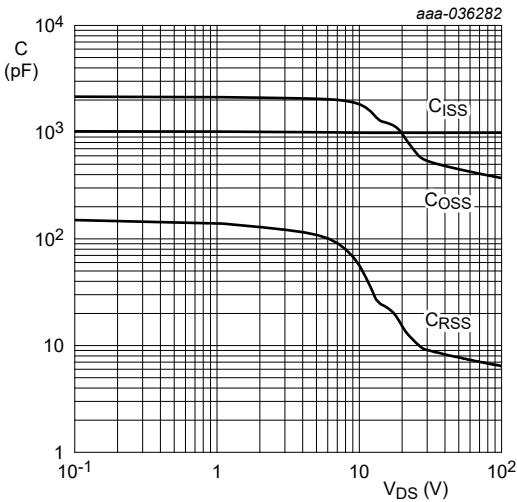
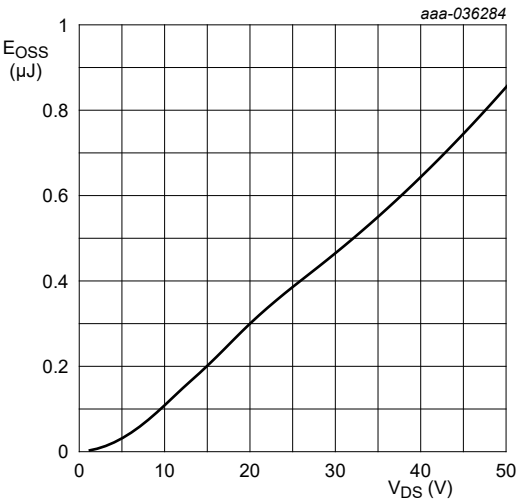
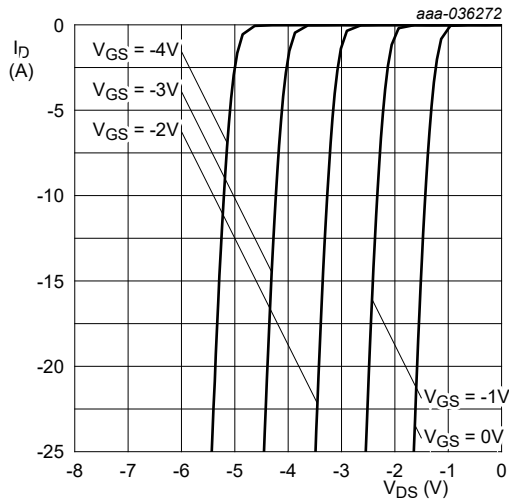


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



Freq. = 100 kHz

Fig. 16. COSS stored energy as a function of drain-source voltage; typical values



$T_J = 25\text{ }^{\circ}\text{C}$

Fig. 17. Source current as a function of source-drain voltage; typical values

100 V, 3.2 mOhm Gallium Nitride (GaN) FET in a 3.5 mm x 2.13 mm Wafer Level Chip-Scale Package (WLCSP)

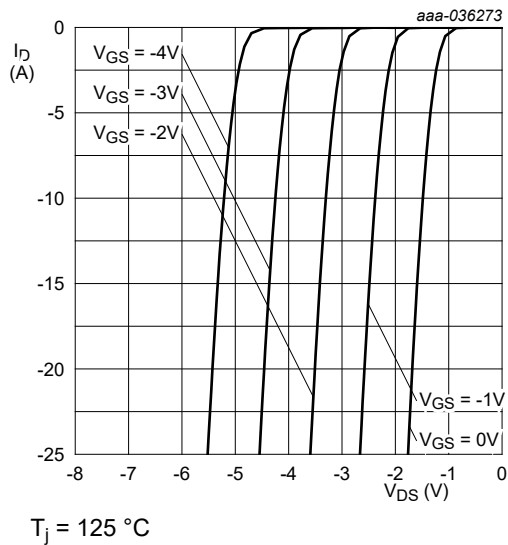


Fig. 18. Source current as a function of source-drain voltage; typical values

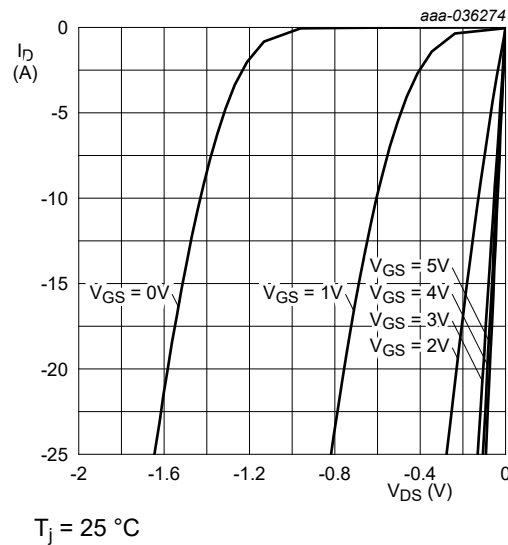


Fig. 19. Source current as a function of source-drain voltage; typical values

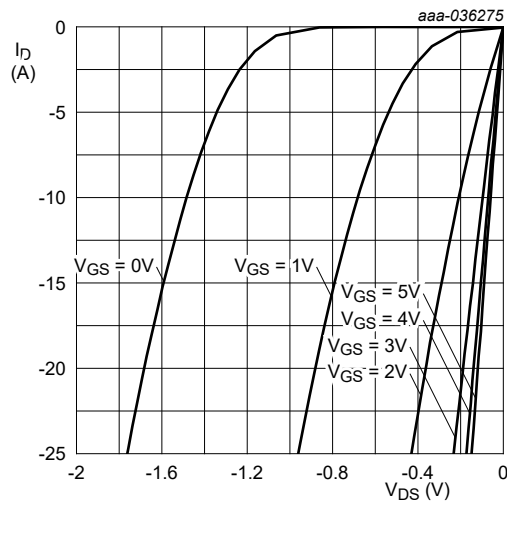


Fig. 20. Source current as a function of source-drain voltage; typical values

11. Package outline

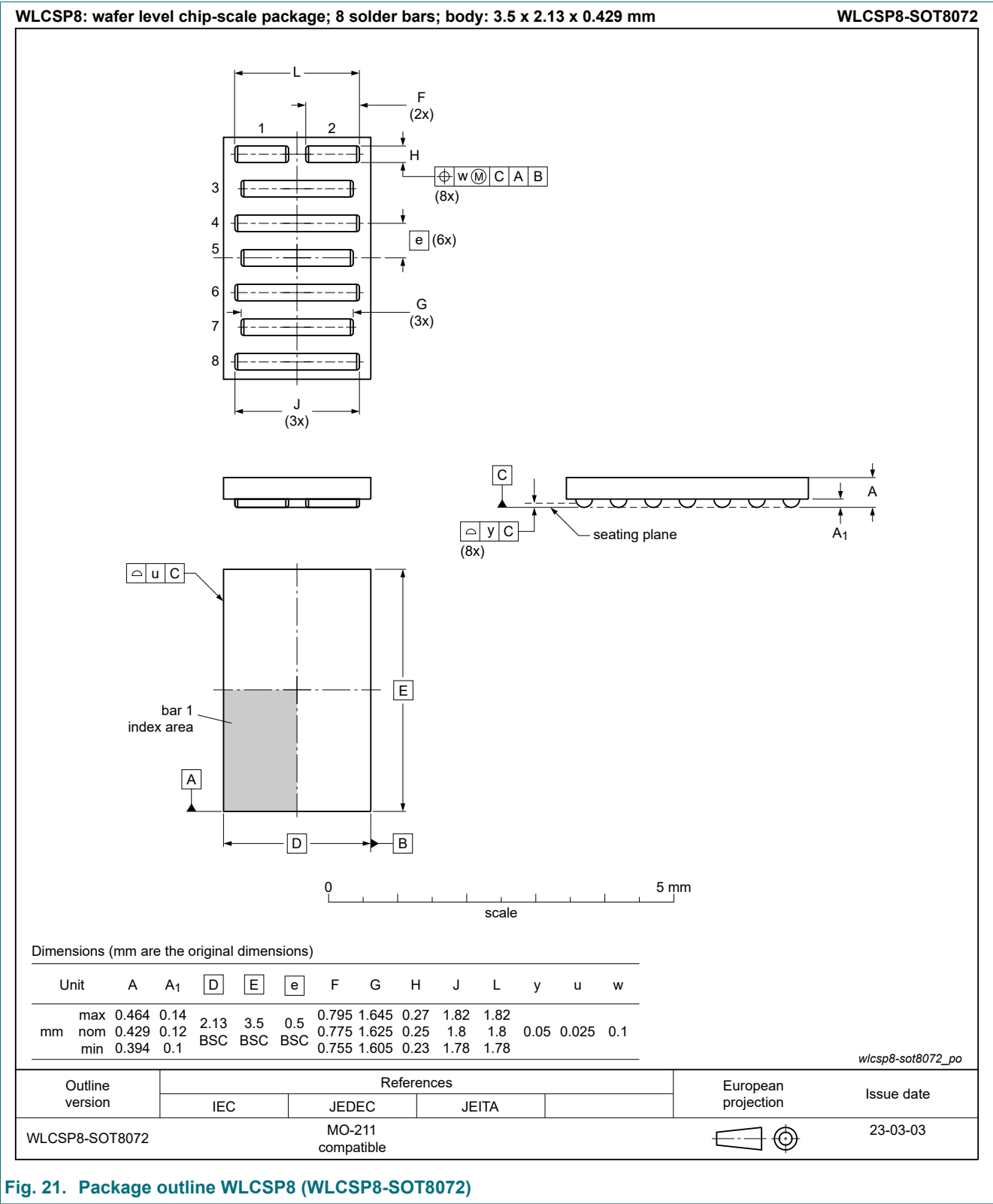


Fig. 21. Package outline WLCSP8 (WLCSP8-SOT8072)

12. Soldering

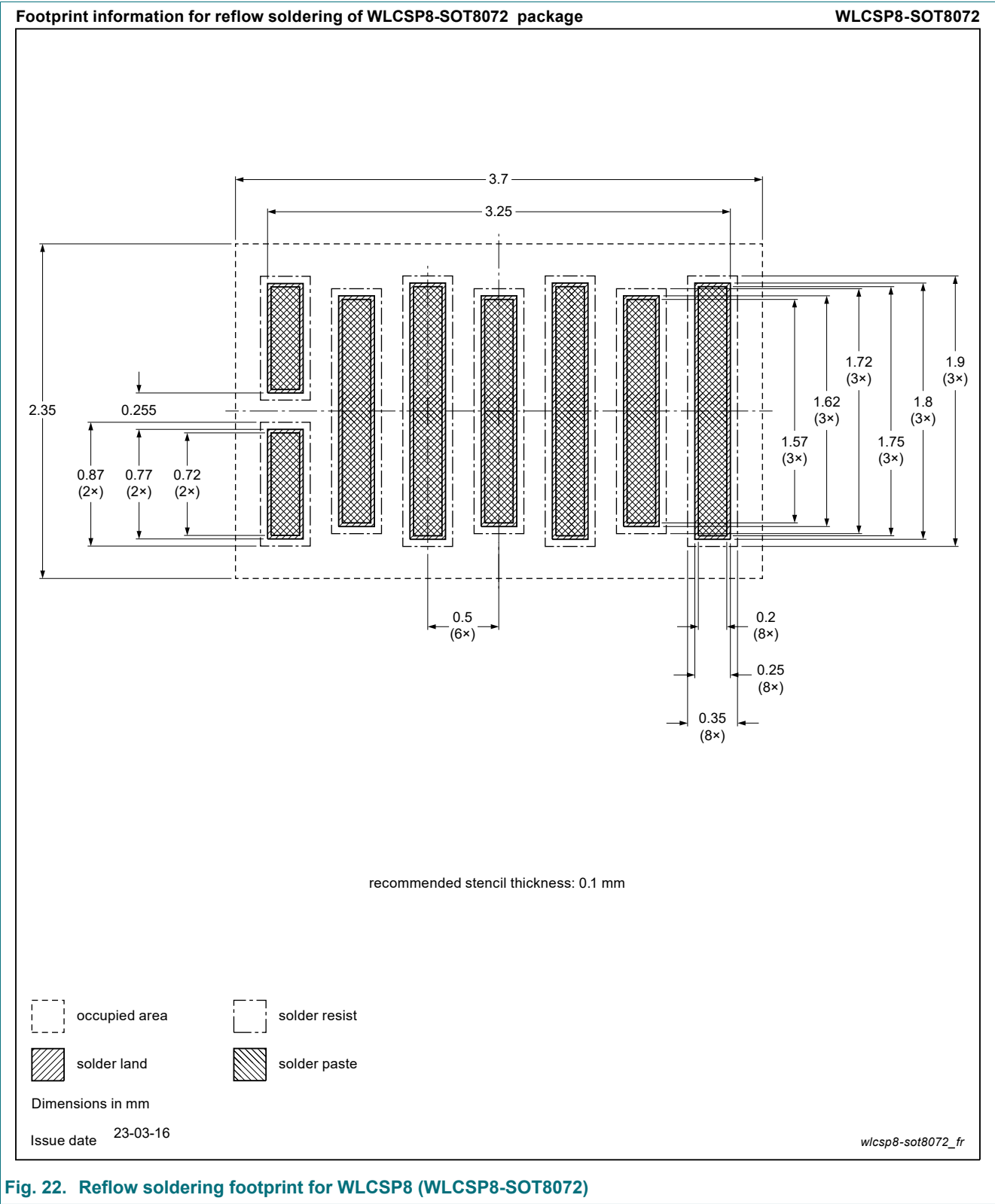


Fig. 22. Reflow soldering footprint for WLCSP8 (WLCSP8-SOT8072)

100 V, 3.2 mOhm Gallium Nitride (GaN) FET in a 3.5 mm x 2.13 mm Wafer Level Chip-Scale Package (WLCSP)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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