

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: BUK4D110-20PX
Manufacturer: Nexperia USA Inc.
Package: Please confirm with sales
Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nexperia-usa-inc/buk4d110-20px.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



BUK4D110-20P

20 V, P-channel Trench MOSFET

7 July 2020

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Extended temperature range $T_j = 175\text{ °C}$
- Trench MOSFET technology
- Very fast switching
- Side wettable flanks for optical solder inspection
- ElectroStatic Discharge (ESD) protection > 1 kV HBM (class H1C)
- AEC-Q101 qualified

3. Applications

- DC to DC conversion
- High-speed line driver
- High-side load switch
- Switching circuits

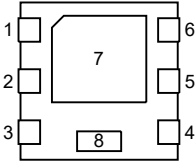
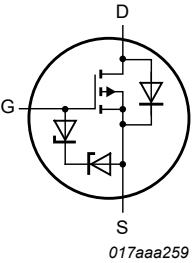
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
V_{GS}	gate-source voltage		-12	-	12	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{sp} = 25\text{ °C}$	-	-	-6.7	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$	-	-	7.5	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -3.4\text{ A}; T_j = 25\text{ °C}$	-	88	110	mΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 Transparent top view DFN2020MD-6 (SOT1220)	 017aaa259
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK4D110-20P	DFN2020MD-6	plastic, leadless thermal enhanced ultra thin small outline package with side-wettable flanks (SWF); 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1220

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK4D110-20P	6N

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage			-12	12	V
I _D	drain current	V _{GS} = -4.5 V; T _{sp} = 25 °C		-	-6.7	A
		V _{GS} = -4.5 V; T _{sp} = 100 °C		-	-4.2	A
		V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-3.4	A
I _{DM}	peak drain current	T _{sp} = 25 °C; single pulse; t _p ≤ 10 μs		-	-27	A
P _{tot}	total power dissipation	T _{sp} = 25 °C		-	7.5	W
		T _{amb} = 25 °C	[1]	-	2	W
T _j	junction temperature			-55	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-65	175	°C
Source-drain diode						
I _S	source current	T _{sp} = 25 °C		-	-6.7	A
		T _{amb} = 25 °C	[1]	-	-1.9	A
I _{SM}	peak source current	single pulse; t _p ≤ 10 μs; T _{sp} = 25 °C		-	-27	A
ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM	[2]	-	1000	V
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	T _{j(init)} = 25 °C; I _D = -0.5 A; DUT in avalanche (unclamped)		-	5	mJ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

[2] Measured between all pins.

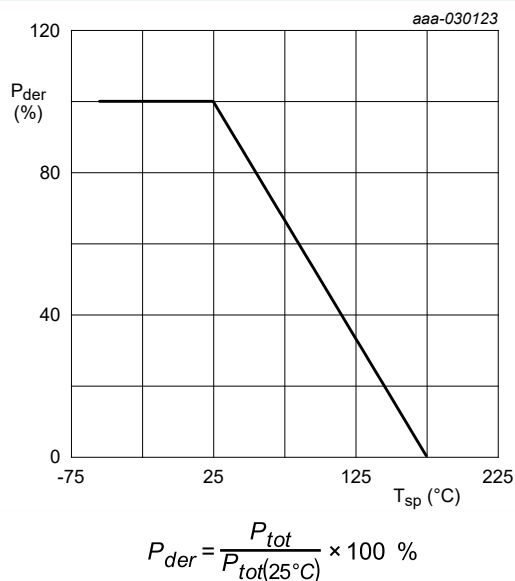


Fig. 1. Normalized total power dissipation as a function of solder point temperature

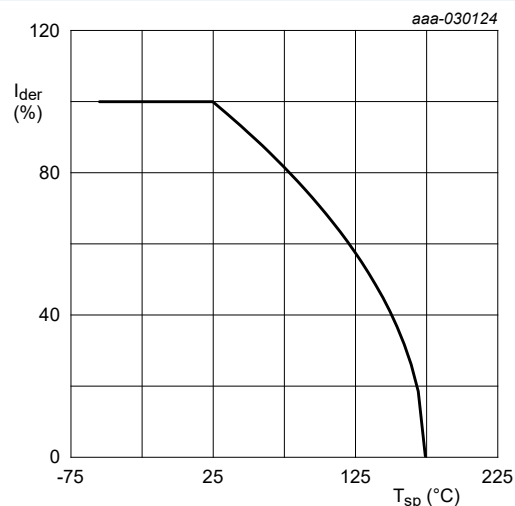


Fig. 2. Normalized continuous drain current as a function of solder point temperature

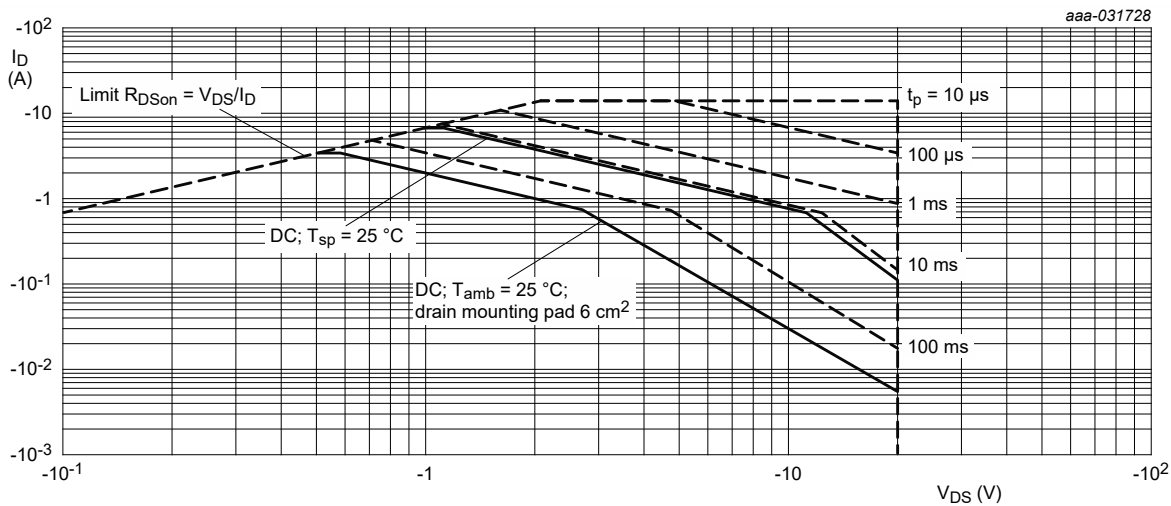


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	66	76	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	15	20	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

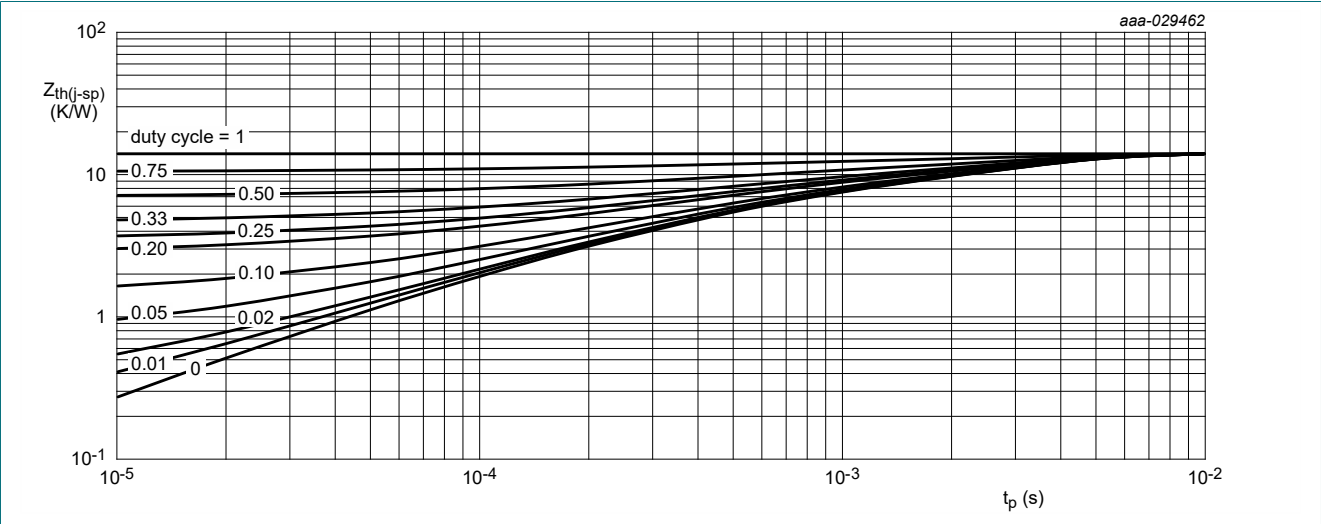


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration; typical values

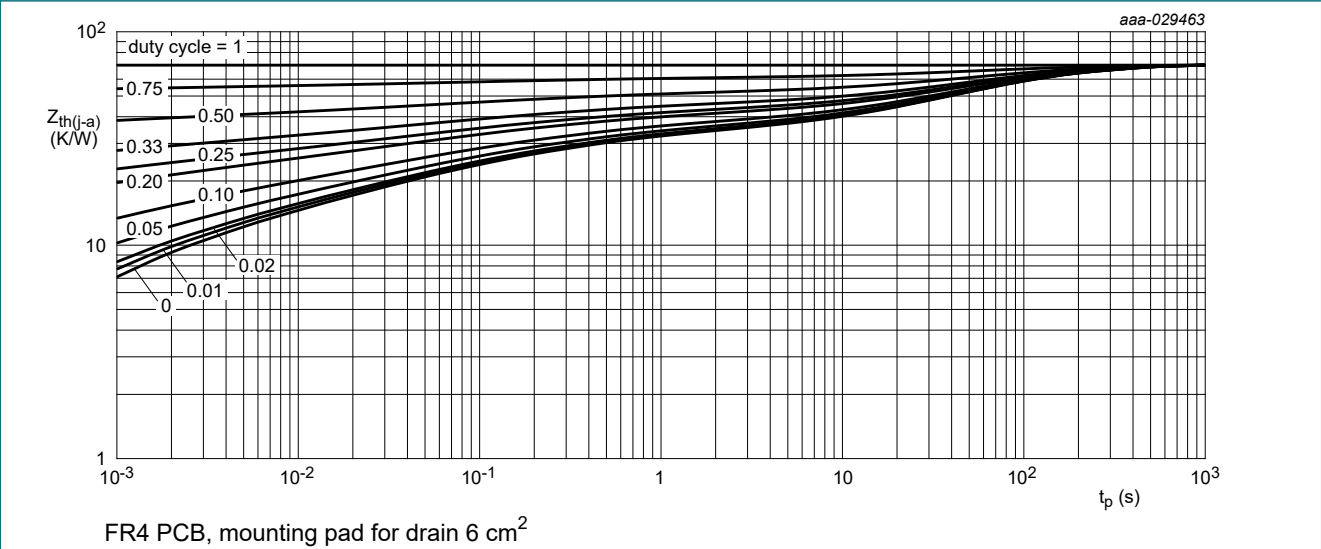


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-20	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} =V _{GS} ; T _j = 25 °C		-0.6	-0.95	-1.3	V
I _{DSS}	drain leakage current	V _{DS} = -20 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
		V _{DS} = -20 V; V _{GS} = 0 V; T _j = 125 °C		-	-	-20	μA
I _{GSS}	gate leakage current	V _{GS} = -12 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-10	μA
		V _{GS} = 12 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -4.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-2	μA
		V _{GS} = 4.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	2	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = -8 V; I _D = -3.4 A; T _j = 25 °C		-	75	96	mΩ
		V _{GS} = -8 V; I _D = -3.4 A; T _j = 175 °C		-	116	148	mΩ
		V _{GS} = -4.5 V; I _D = -3.4 A; T _j = 25 °C		-	88	110	mΩ
		V _{GS} = -2.5 V; I _D = -1 A; T _j = 25 °C		-	138	189	mΩ
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -3.4 A; T _j = 25 °C		-	6	-	S
R _G	gate resistance	f = 1 MHz		-	36	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -10 V; I _D = -3.2 A; V _{GS} = -4.5 V; T _j = 25 °C		-	3.6	5	nC
Q _{GS}	gate-source charge			-	0.8	-	nC
Q _{GD}	gate-drain charge			-	1.2	-	nC
C _{iss}	input capacitance	V _{DS} = -10 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	365	-	pF
C _{oss}	output capacitance			-	49	-	pF
C _{rss}	reverse transfer capacitance			-	39	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -10 V; I _D = -3.2 A; V _{GS} = -4.5 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	4	-	ns
t _r	rise time			-	7	-	ns
t _{d(off)}	turn-off delay time			-	9	-	ns
t _f	fall time			-	7	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -2 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.9	-1.2	V
t _{rr}	reverse recovery time	I _S = -2 A; dI _S /dt = 100 A/μs; V _{GS} = 0 V; V _{DS} = -10 V; T _j = 25 °C		-	9	-	ns
Q _r	recovered charge			-	2	-	nC

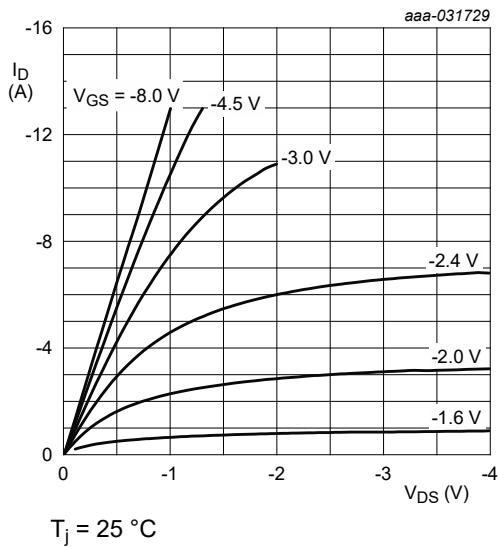


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

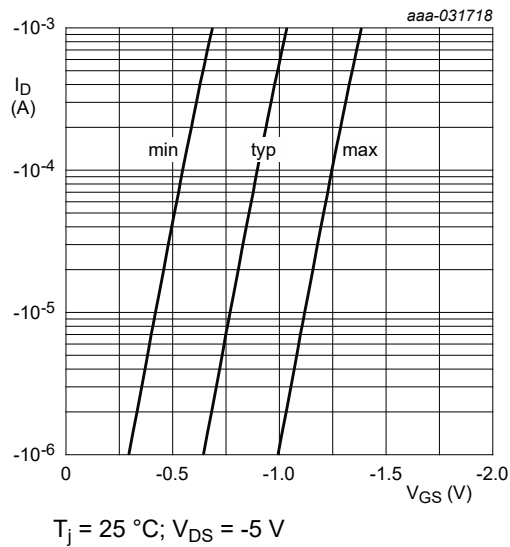


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

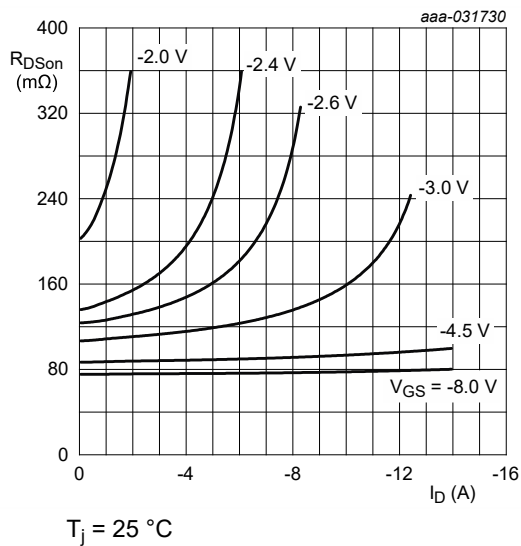


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

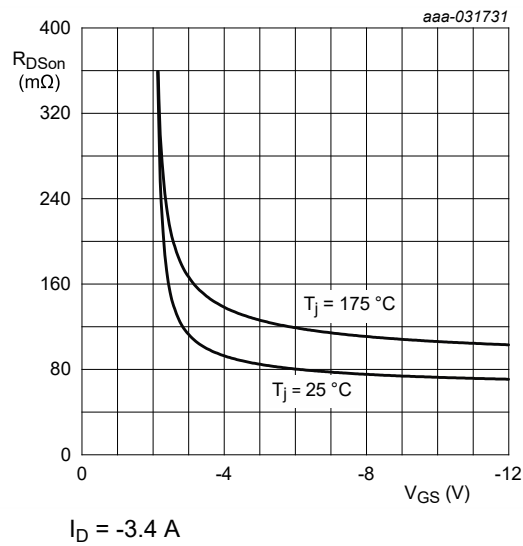


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

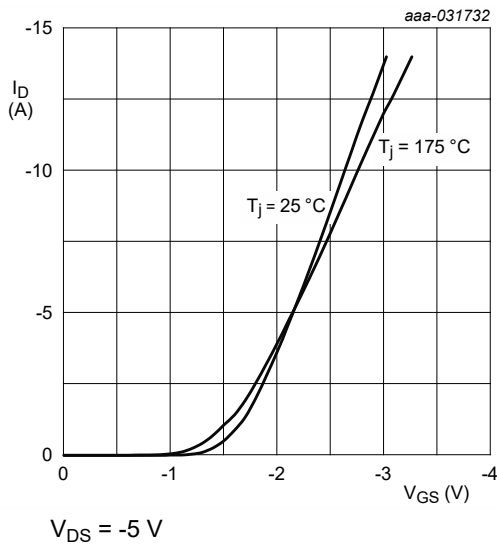


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

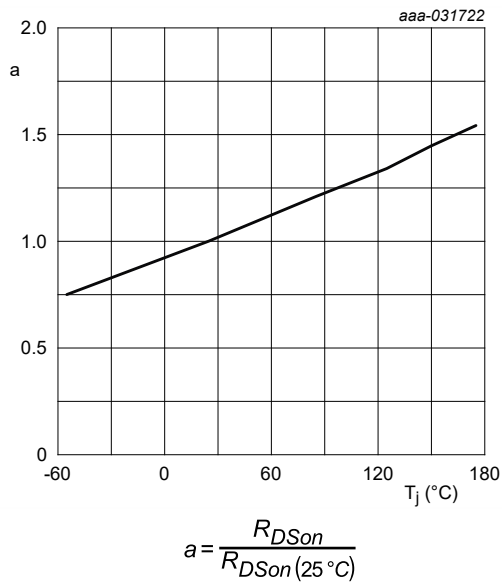


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

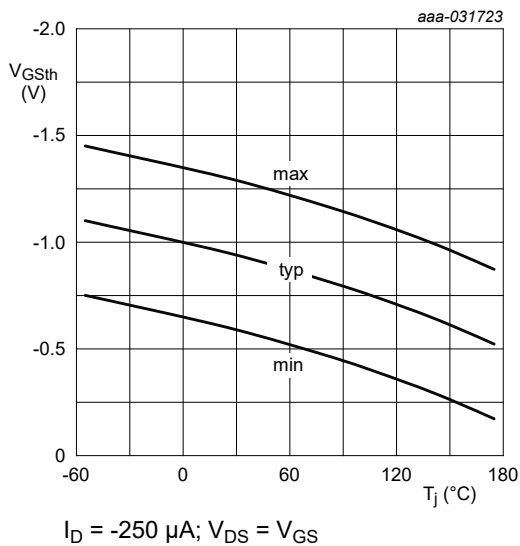


Fig. 12. Gate-source threshold voltage as a function of junction temperature

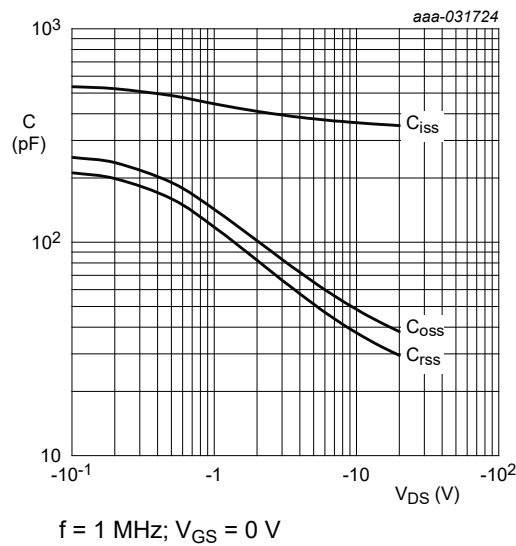


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

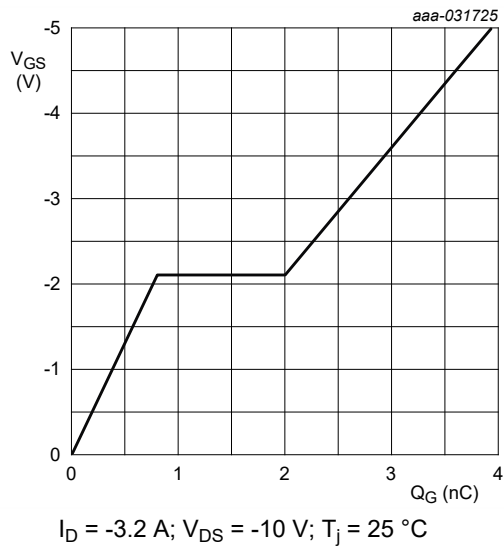


Fig. 14. Gate-source voltage as a function of gate charge; typical values

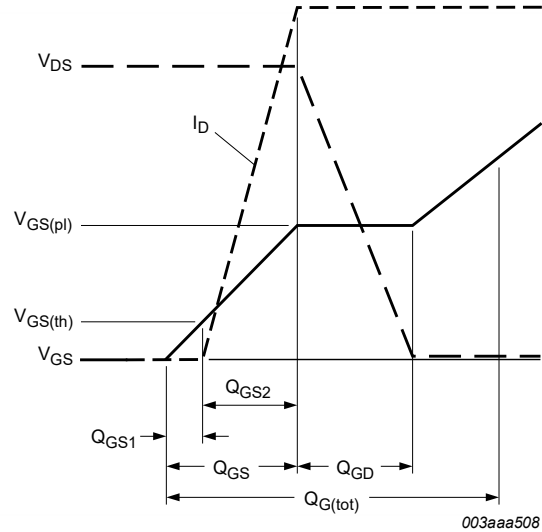


Fig. 15. Gate charge waveform definitions

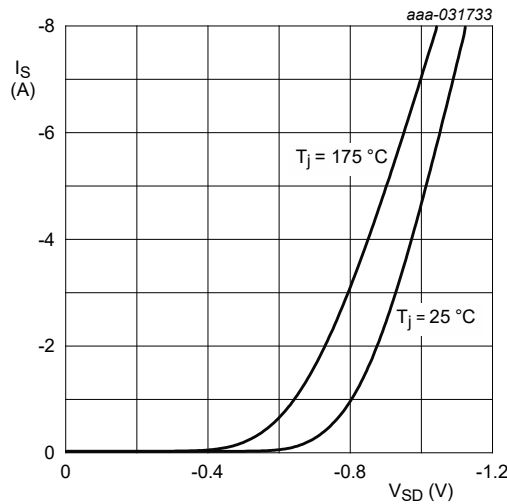


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

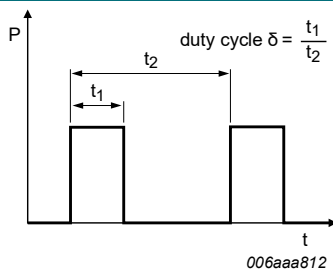


Fig. 17. Duty cycle definition

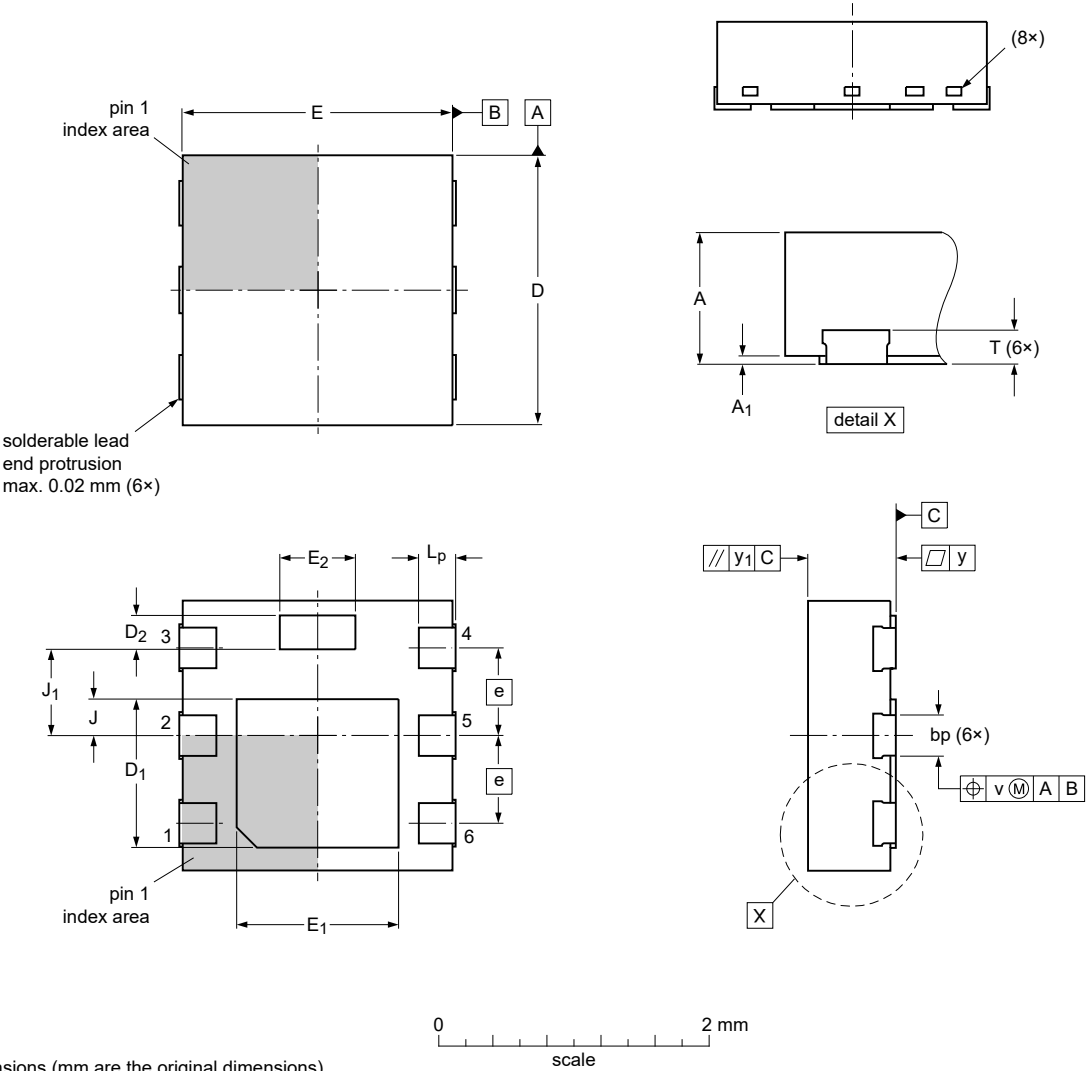
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads;
6 terminals; body 2 x 2 x 0.65 mm

SOT1220



Dimensions (mm are the original dimensions)

Unit	A	A ₁	bp	D	D ₁	D ₂	E	E ₁	E ₂	e	J	J ₁	L _p	T	v	y	y ₁
mm	min		0.25	1.9	1.0	0.2	1.9	1.1	0.51				0.2	0.10			
	nom									0.65	0.27	0.64		0.16	0.1	0.05	0.1
	max	0.65	0.04	0.35	2.1	0.3	2.1	1.3	0.61				0.3	0.22			

Note
1. Dimension A is including plating thickness.

sot1220_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1220						18-05-30 18-06-07

Fig. 18. Package outline DFN2020MD-6 (SOT1220)

13. Soldering

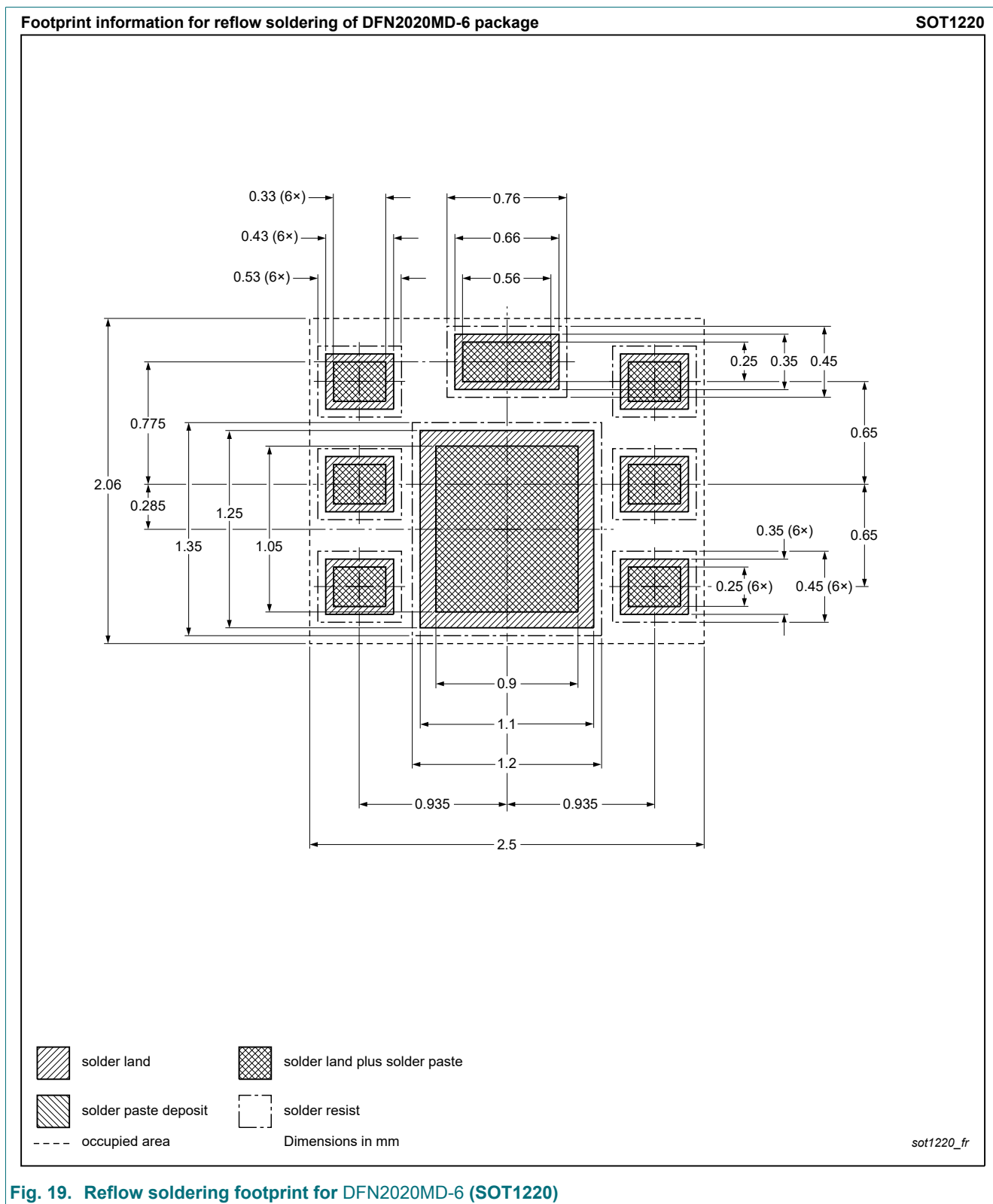


Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK4D110-20P v.1	20200707	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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