

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	BSS84AKW-BX
Manufacturer:	Nexperia USA Inc.
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/nexperia-usa-inc/bss84akw-bx.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.



BSS84AKW

50 V, 150 mA P-channel Trench MOSFET

Rev. 1 — 23 May 2011

Product data sheet

1. Product profile

1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT323 (SC-70) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- ESD protection up to 1 kV
- AEC-Q101 qualified

1.3 Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

1.4 Quick reference data

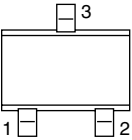
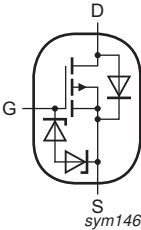
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-50	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ °C}$ [1]	-	-	-150	mA
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -100\text{ mA}; T_j = 25\text{ °C}$	-	4.5	7.5	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT323 (SC-70)	
2	S	source		
3	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BSS84AKW	SC-70	plastic surface-mounted package; 3 leads	SOT323

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
BSS84AKW	%VT

[1] % = placeholder for manufacturing site code

5. Limiting values

Table 5. Limiting values

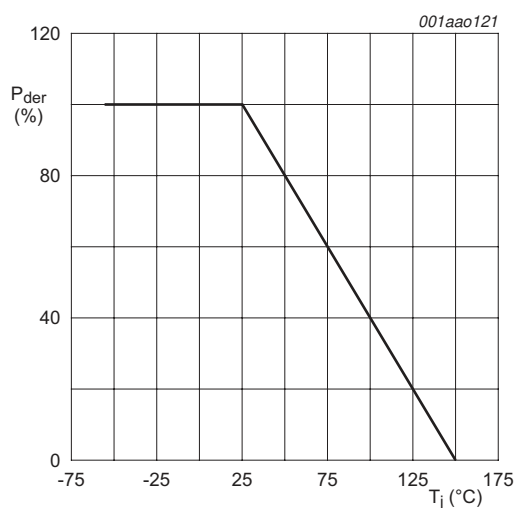
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$	-	-50	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-150 mA
		$V_{GS} = -10\text{ V}; T_{amb} = 100\text{ }^{\circ}\text{C}$	[1]	-	-95 mA
I_{DM}	peak drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$	-	-0.6	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	-	260 mW
			[1]	-	310 mW
		$T_{sp} = 25\text{ }^{\circ}\text{C}$	-	830	mW
T_j	junction temperature		-55	150	$^{\circ}\text{C}$
T_{amb}	ambient temperature		-55	150	$^{\circ}\text{C}$
T_{stg}	storage temperature		-65	150	$^{\circ}\text{C}$
Source-drain diode					
I_S	source current	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-150 mA
ESD maximum rating					
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	1000 V

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

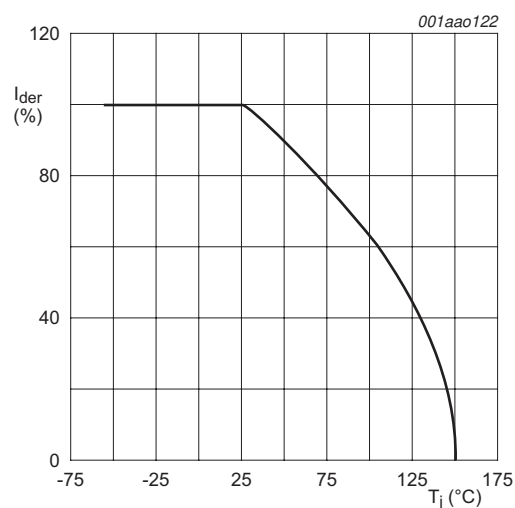
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



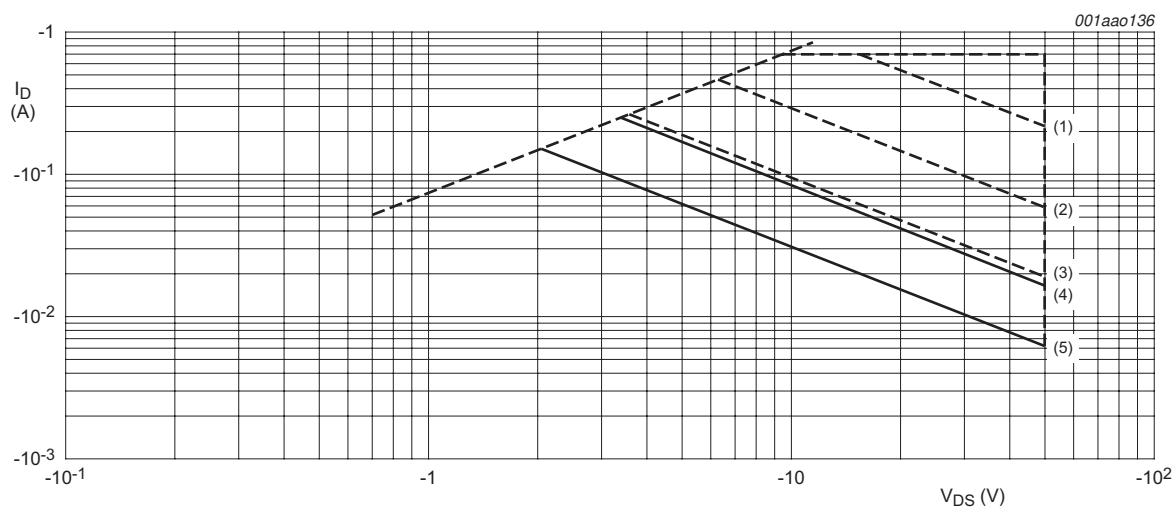
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} is single pulse

(1) $t_p = 1 \text{ ms}$

(2) $t_p = 10 \text{ ms}$

(3) $t_p = 100 \text{ ms}$

(4) DC; $T_{sp} = 25 \text{ °C}$

(5) DC; $T_{amb} = 25 \text{ °C}$; drain mounting pad 1 cm^2

Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	415	K/W
			[2]	-	350	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	150	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

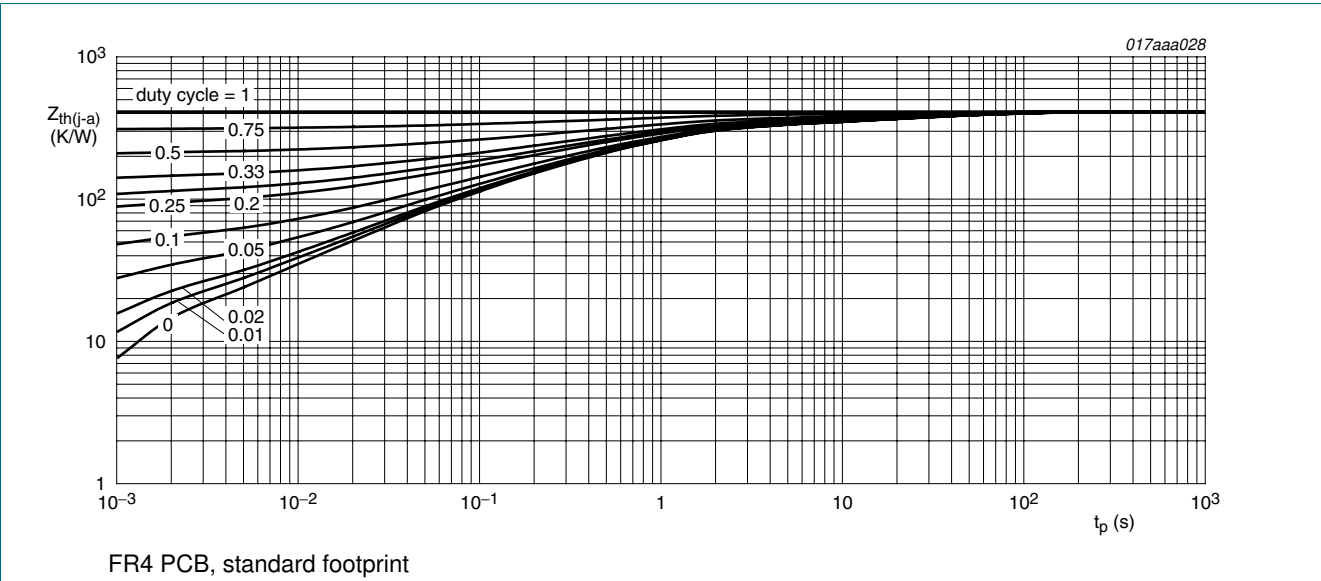


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

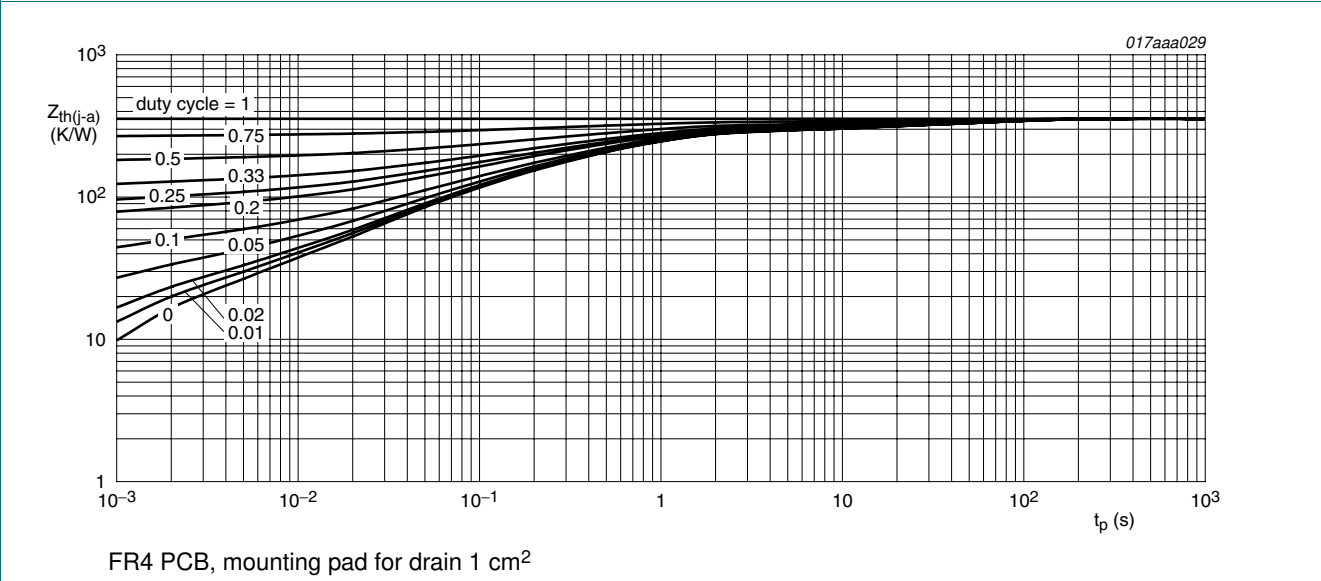


Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -10 μA; V _{GS} = 0 V; T _j = 25 °C	-50	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} = V _{GS} ; T _j = 25 °C	-1.1	-1.6	-2.1	V
I _{DSS}	drain leakage current	V _{DS} = -50 V; V _{GS} = 0 V; T _j = 25 °C	-	-	-1	μA
		V _{DS} = -50 V; V _{GS} = 0 V; T _j = 150 °C	-	-	-2	μA
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-10	μA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-10	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = -10 V; I _D = -100 mA; T _j = 25 °C	-	4.5	7.5	Ω
		V _{GS} = -10 V; I _D = -100 mA; T _j = 150 °C	-	8	13.5	Ω
		V _{GS} = -5 V; I _D = -100 mA; T _j = 25 °C	-	5.7	8.5	Ω
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -100 mA; T _j = 25 °C	-	150	-	mS
Dynamic characteristics						
Q _{G(tot)}	total gate charge	V _{DS} = -25 V; I _D = -200 mA; V _{GS} = -5 V; T _j = 25 °C	-	0.26	0.35	nC
Q _{GS}	gate-source charge		-	0.12	-	nC
Q _{GD}	gate-drain charge		-	0.09	-	nC
C _{iss}	input capacitance	V _{DS} = -25 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C	-	24	36	pF
C _{oss}	output capacitance		-	4.5	-	pF
C _{rss}	reverse transfer capacitance		-	1.3	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -30 V; R _L = 250 Ω; V _{GS} = -10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C	-	13	26	ns
t _r	rise time		-	11	-	ns
t _{d(off)}	turn-off delay time		-	48	96	ns
t _f	fall time		-	25	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = -115 mA; V _{GS} = 0 V; T _j = 25 °C	-0.48	-0.85	-1.2	V

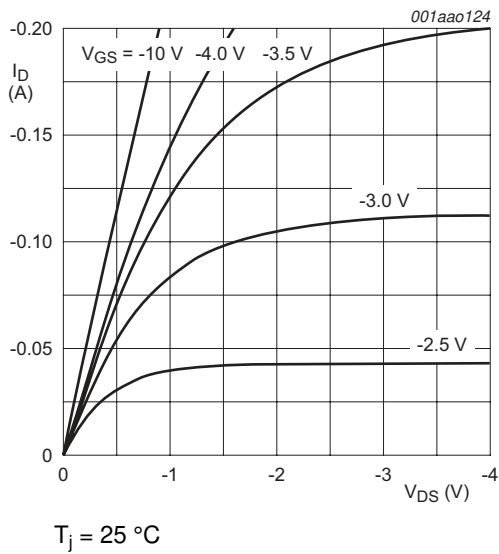


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values

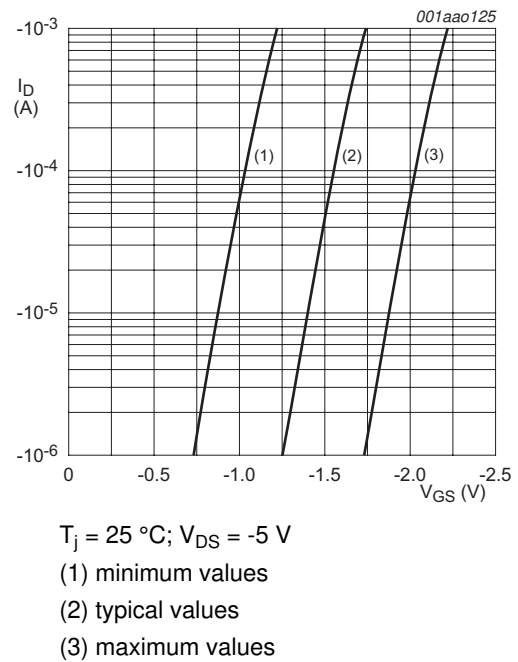


Fig 7. Sub-threshold drain current as a function of gate-source voltage

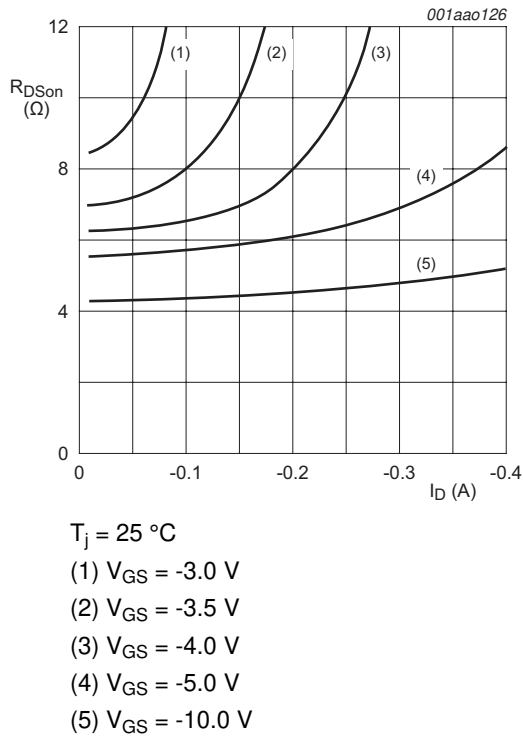


Fig 8. Drain-source on-state resistance as a function of drain current; typical values

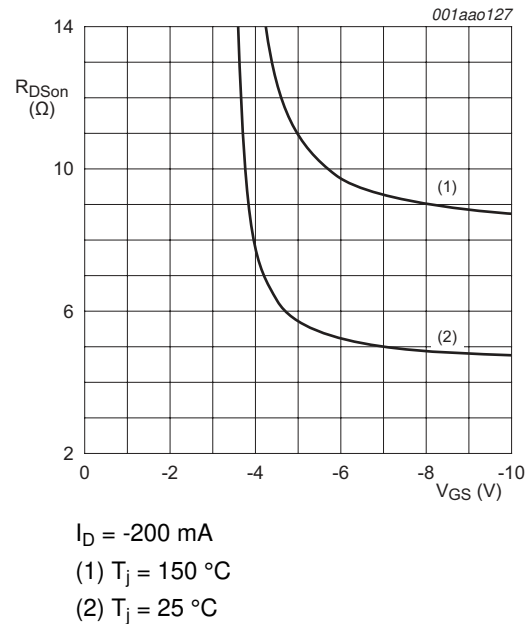
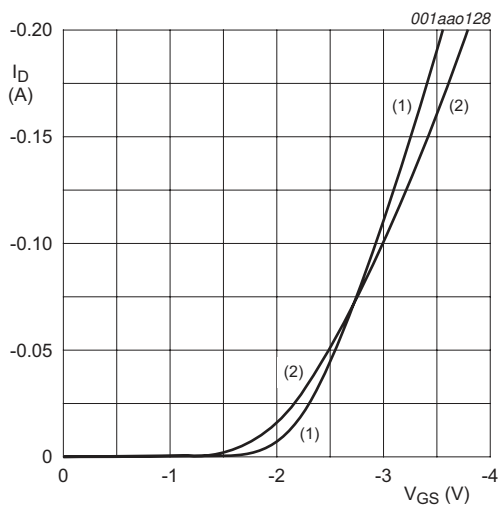
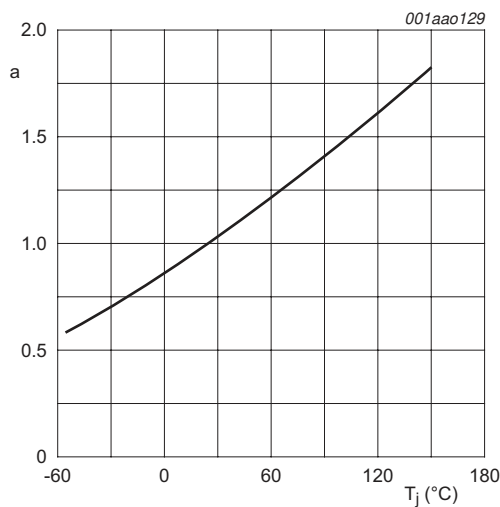


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



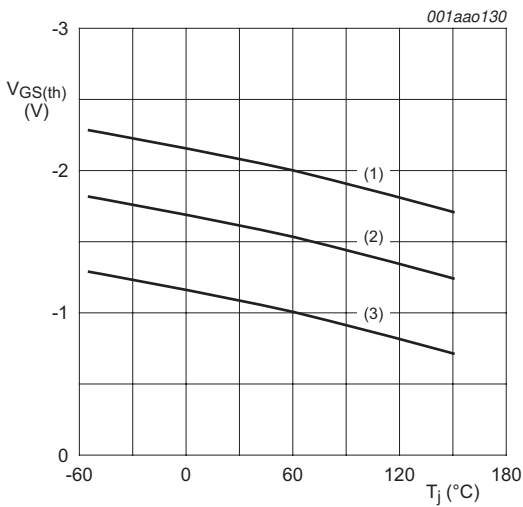
$V_{DS} > I_D \times R_{DSon}$
(1) $T_j = 25\text{ }^{\circ}\text{C}$
(2) $T_j = 150\text{ }^{\circ}\text{C}$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



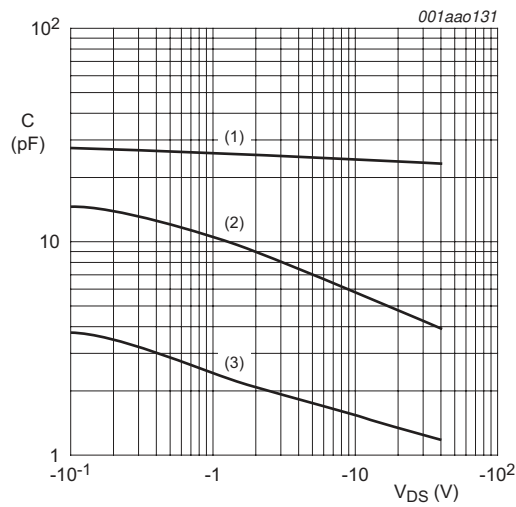
$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



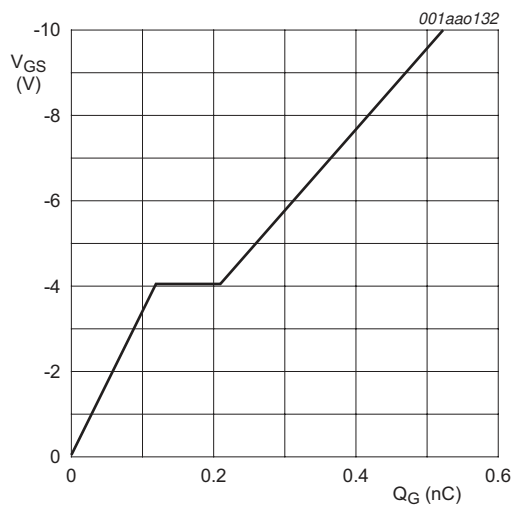
$I_D = -0.25\text{ mA}$; $V_{DS} = V_{GS}$
(1) maximum values
(2) typical values
(3) minimum values

Fig 12. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$
(1) C_{iss}
(2) C_{oss}
(3) C_{rss}

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = -0.2$ A; $V_{DS} = -25$ V; $T_{amb} = 25$ °C

Fig 14. Gate-source voltage as a function of gate charge; typical values

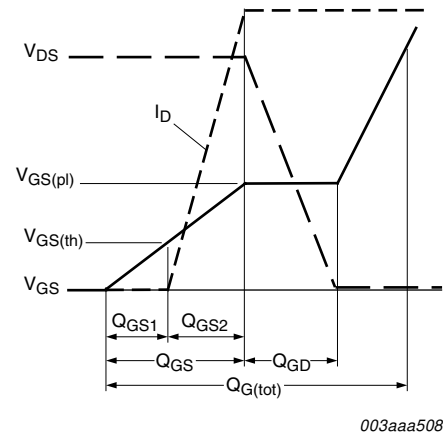
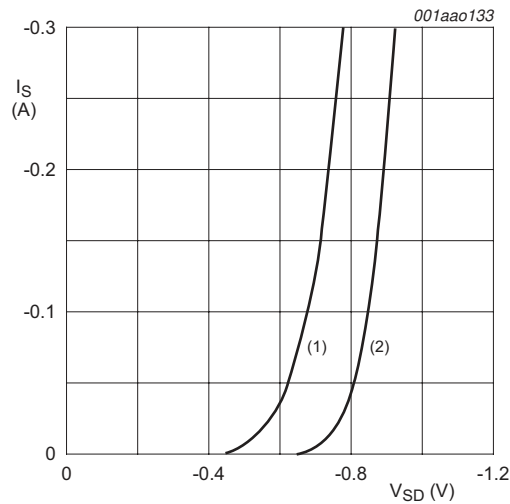


Fig 15. Gate charge waveform definitions



$V_{GS} = 0$ V
(1) $T_j = 150$ °C
(2) $T_j = 25$ °C

Fig 16. Source current as a function of source-drain voltage; typical values

8. Test information

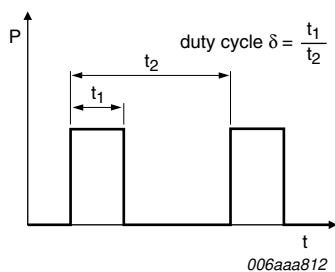


Fig 17. Duty cycle definition

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

9. Package outline

Plastic surface-mounted package; 3 leads

SOT323

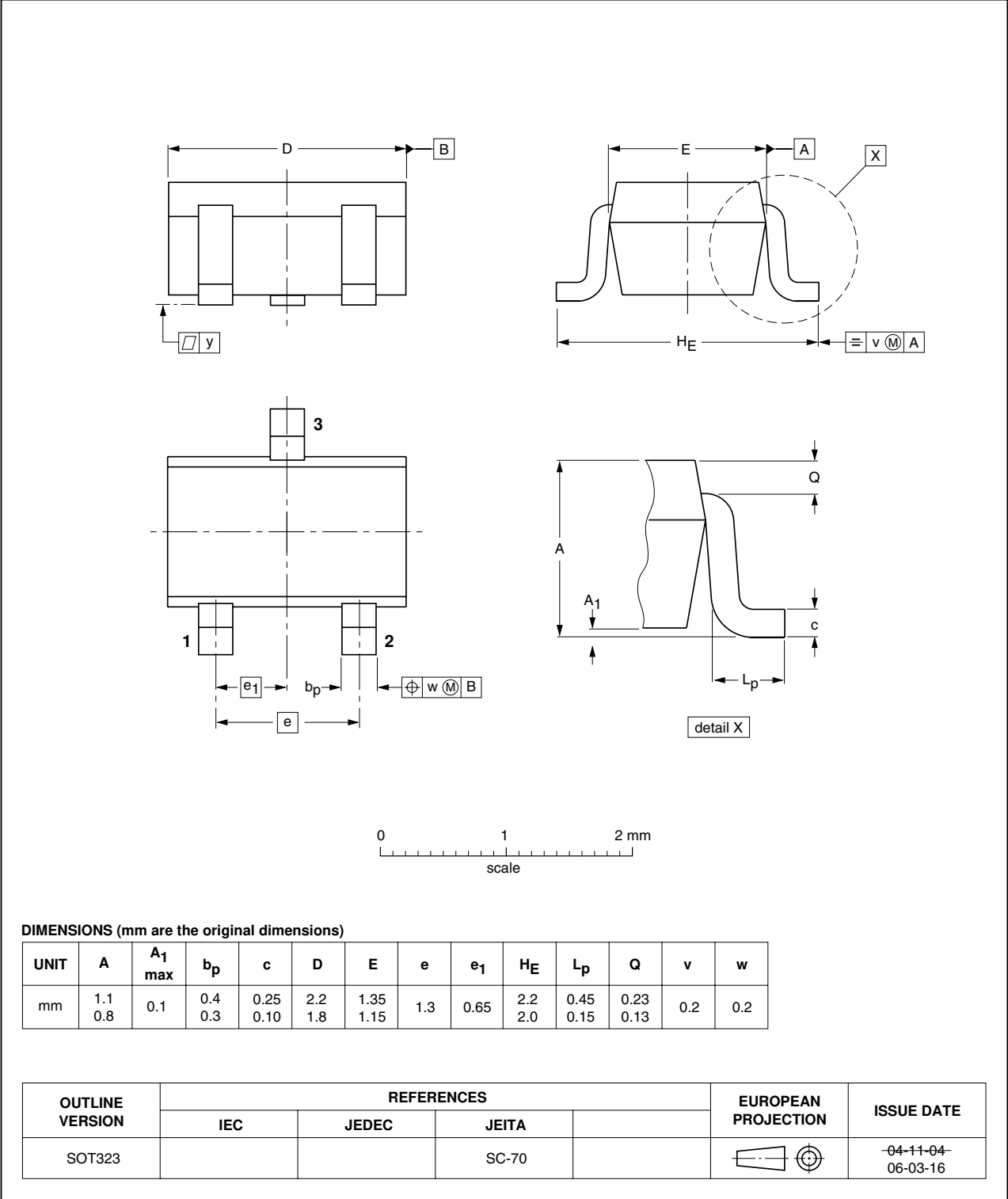
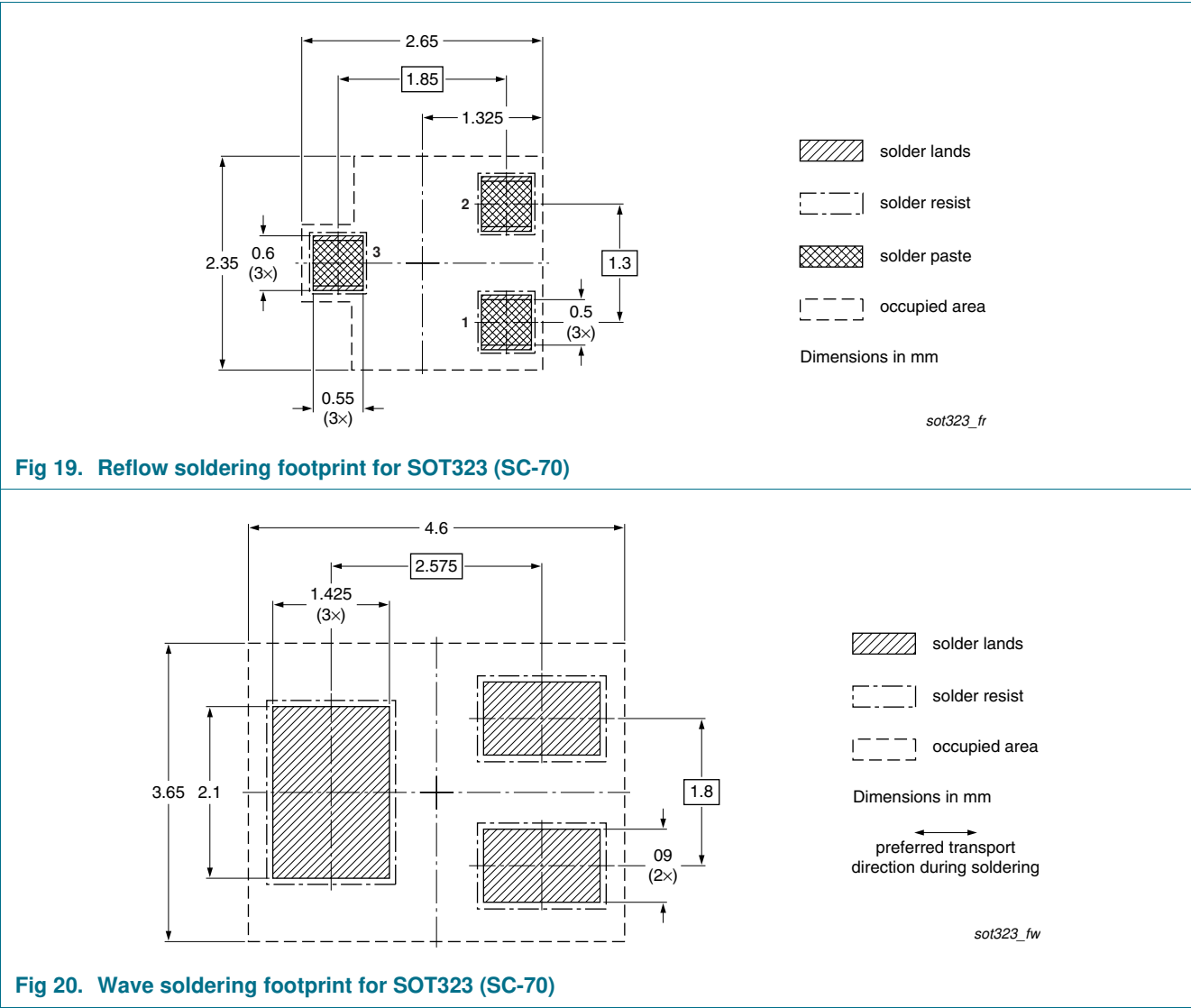


Fig 18. Package outline SOT323 (SC-70)

10. Soldering



11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BSS84AKW v.1	20110523	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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