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## Electronic Components Sourcing Information

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### Product Reference Information

|                      |                           |
|----------------------|---------------------------|
| <b>Part Number:</b>  | BSP220,115                |
| <b>Manufacturer:</b> | Nexperia USA Inc.         |
| <b>Package:</b>      | Please confirm with sales |
| <b>Availability:</b> | Please confirm with sales |

**Product Page:**

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**Note:**

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

# DATA SHEET

## **BSP220**

P-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

# P-channel enhancement mode vertical D-MOS transistor

# BSP220

FEATURES

- Low  $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line transformer drivers.

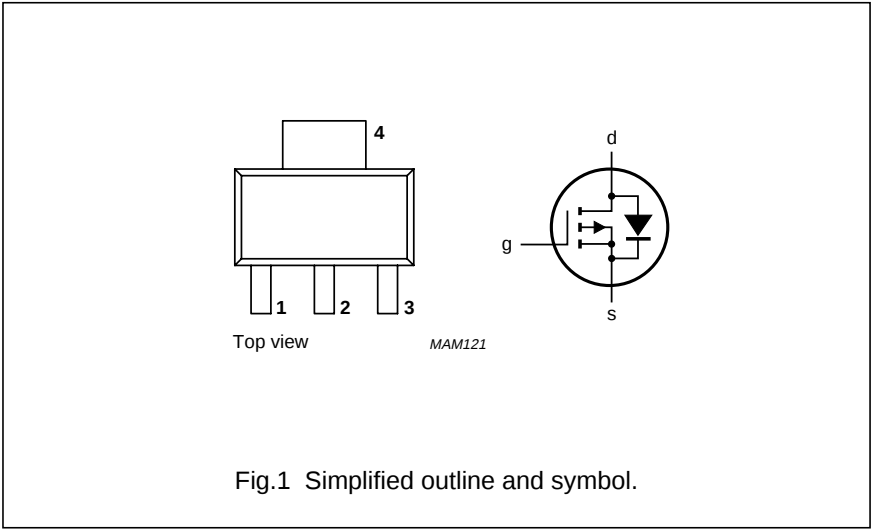
PINNING - SOT223

| PIN | DESCRIPTION |
|-----|-------------|
| 1   | gate        |
| 2   | drain       |
| 3   | source      |
| 4   | drain       |

QUICK REFERENCE DATA

| SYMBOL        | PARAMETER                     | CONDITIONS                                        | MAX. | UNIT     |
|---------------|-------------------------------|---------------------------------------------------|------|----------|
| $-V_{DS}$     | drain-source voltage          |                                                   | 200  | V        |
| $-I_D$        | drain current                 | DC value                                          | 225  | mA       |
| $R_{DS(on)}$  | drain-source on-resistance    | $-I_D = 200\text{ mA}$<br>$-V_{GS} = 10\text{ V}$ | 12   | $\Omega$ |
| $-V_{GS(th)}$ | gate-source threshold voltage |                                                   | 2.8  | V        |

PIN CONFIGURATION



# P-channel enhancement mode vertical D-MOS transistor

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## LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

| SYMBOL        | PARAMETER                 | CONDITIONS                              | MIN. | MAX. | UNIT |
|---------------|---------------------------|-----------------------------------------|------|------|------|
| $-V_{DS}$     | drain-source voltage      |                                         | –    | 200  | V    |
| $\pm V_{GSO}$ | gate-source voltage       | open drain                              | –    | 20   | V    |
| $-I_D$        | drain current             | DC value                                | –    | 225  | mA   |
| $-I_{DM}$     | drain current             | peak value                              | –    | 600  | mA   |
| $P_{tot}$     | total power dissipation   | up to $T_{amb} = 25\text{ °C}$ (note 1) | –    | 1.5  | W    |
| $T_{stg}$     | storage temperature range |                                         | –65  | 150  | °C   |
| $T_j$         | junction temperature      |                                         | –    | 150  | °C   |

## Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm<sup>2</sup>.

## THERMAL RESISTANCE

| SYMBOL        | PARAMETER                         | VALUE | UNIT |
|---------------|-----------------------------------|-------|------|
| $R_{th\ j-a}$ | from junction to ambient (note 1) | 83.3  | K/W  |

## Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm<sup>2</sup>.

# P-channel enhancement mode vertical D-MOS transistor

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## CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

| SYMBOL                                    | PARAMETER                      | CONDITIONS                                                                               | MIN. | TYP. | MAX. | UNIT          |
|-------------------------------------------|--------------------------------|------------------------------------------------------------------------------------------|------|------|------|---------------|
| $-V_{(BR)DSS}$                            | drain-source breakdown voltage | $-I_D = 10\text{ }\mu\text{A}$<br>$V_{GS} = 0$                                           | 200  | —    | —    | V             |
| $-I_{DSS}$                                | drain-source leakage current   | $-V_{DS} = 160\text{ V}$<br>$V_{GS} = 0$                                                 | —    | —    | 1    | $\mu\text{A}$ |
| $\pm I_{GSS}$                             | gate-source leakage current    | $\pm V_{GS} = 20\text{ V}$<br>$V_{DS} = 0$                                               | —    | —    | 100  | nA            |
| $-V_{GS(th)}$                             | gate-source threshold voltage  | $-I_D = 1\text{ mA}$<br>$V_{GS} = V_{DS}$                                                | 0.8  | —    | 2.8  | V             |
| $R_{DS(on)}$                              | drain-source on-resistance     | $-I_D = 200\text{ mA}$<br>$-V_{GS} = 10\text{ V}$                                        | —    | 10   | 12   | $\Omega$      |
| $ Y_{fs} $                                | transfer admittance            | $-I_D = 200\text{ mA}$<br>$-V_{DS} = 25\text{ V}$                                        | 100  | 200  | —    | mS            |
| $C_{iss}$                                 | input capacitance              | $-V_{DS} = 25\text{ V}$<br>$V_{GS} = 0$<br>$f = 1\text{ MHz}$                            | —    | 65   | 90   | pF            |
| $C_{oss}$                                 | output capacitance             | $-V_{DS} = 25\text{ V}$<br>$V_{GS} = 0$<br>$f = 1\text{ MHz}$                            | —    | 20   | 30   | pF            |
| $C_{rss}$                                 | feedback capacitance           | $-V_{DS} = 25\text{ V}$<br>$V_{GS} = 0$<br>$f = 1\text{ MHz}$                            | —    | 6    | 15   | pF            |
| <b>Switching times (see Figs 2 and 3)</b> |                                |                                                                                          |      |      |      |               |
| $t_{on}$                                  | turn-on time                   | $-I_D = 250\text{ mA}$<br>$-V_{DD} = 50\text{ V}$<br>$-V_{GS} = 0\text{ to }10\text{ V}$ | —    | 5    | 20   | ns            |
| $t_{off}$                                 | turn-off time                  | $-I_D = 250\text{ mA}$<br>$-V_{DD} = 50\text{ V}$<br>$-V_{GS} = 0\text{ to }10\text{ V}$ | —    | 20   | 30   | ns            |

P-channel enhancement mode vertical  
D-MOS transistor

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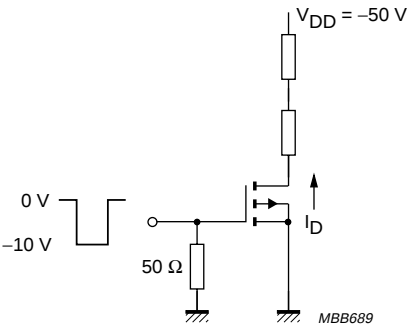


Fig.2 Switching time test circuit.

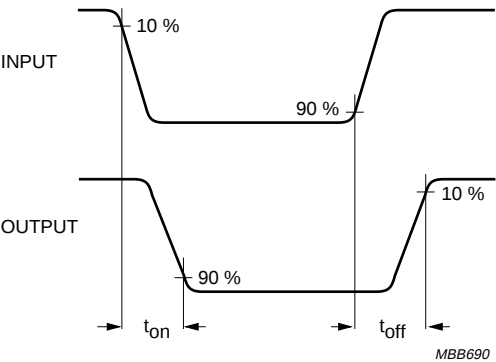


Fig.3 Input and output waveforms.

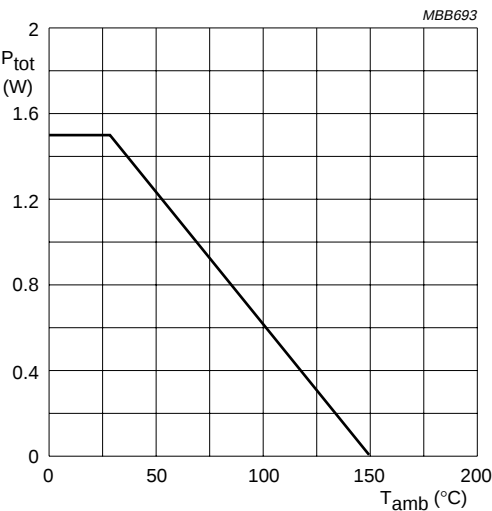


Fig.4 Power derating curve.

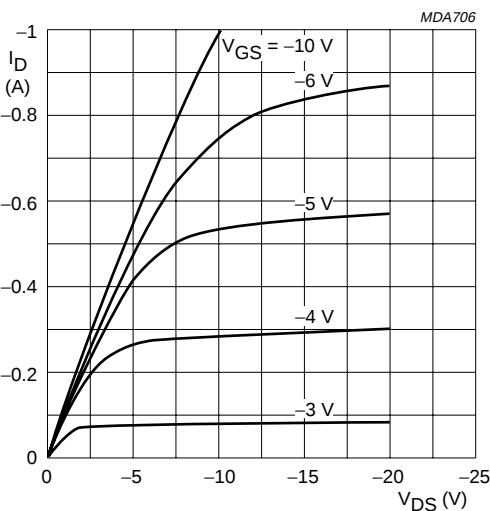


Fig.5 Typical output characteristics;  $T_j = 25\text{ °C}$ .

# P-channel enhancement mode vertical D-MOS transistor

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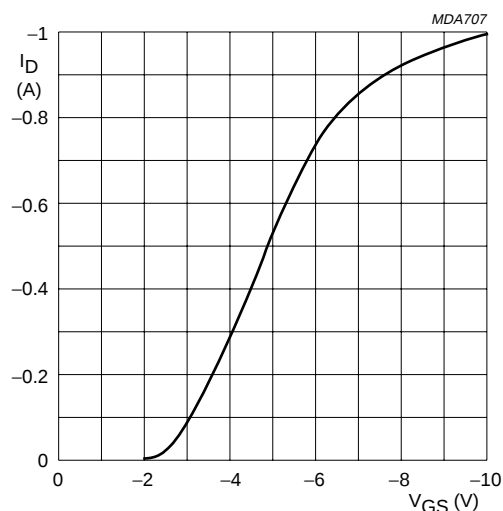


Fig.6 Typical transfer characteristic;  $-V_{DS} = 10$  V;  
 $T_j = 25$  °C.

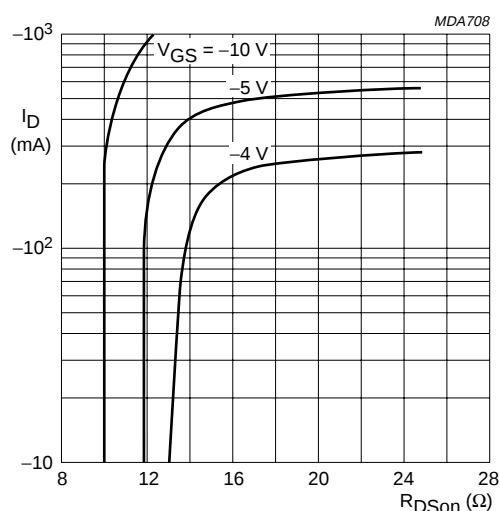


Fig.7 Typical on-resistance as a function of drain  
current;  $T_j = 25$  °C.

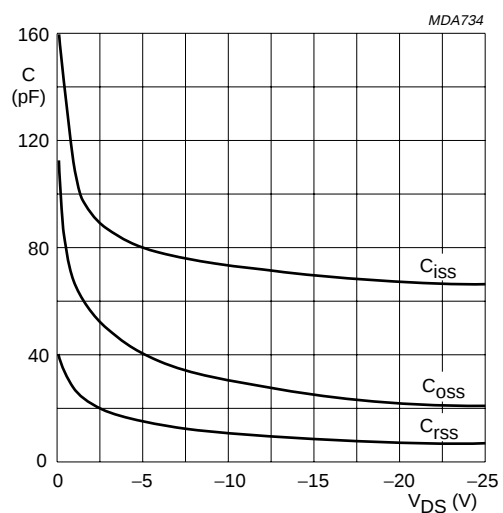


Fig.8 Typical capacitances as a function of  
drain-source voltage;  $V_{GS} = 0$ ;  $f = 1$  MHz;  
 $T_j = 25$  °C.

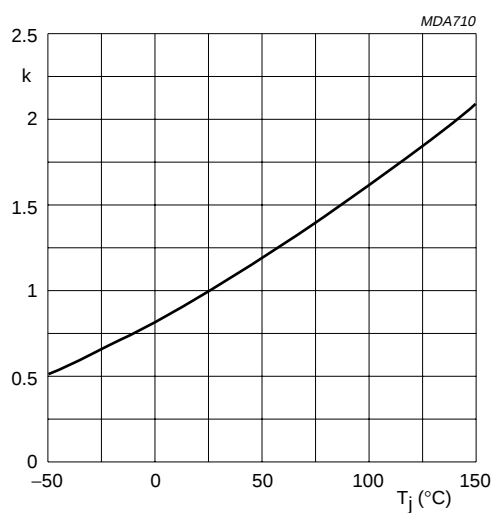


Fig.9 Temperature coefficient of drain-source  
on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25^\circ\text{C}};$$

typical  $R_{DS(on)}$  at  $-200$  mA/ $-10$  V.

# P-channel enhancement mode vertical D-MOS transistor

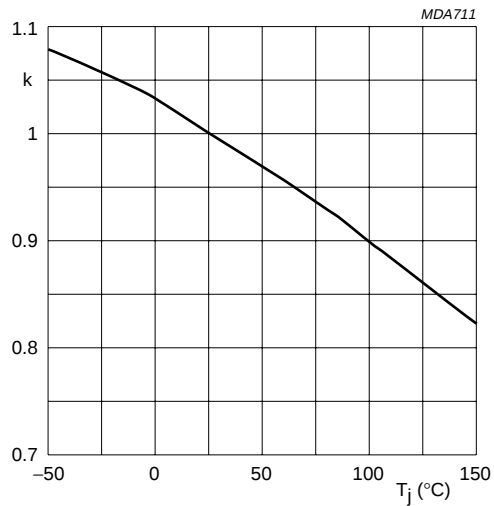
**BSP220**

Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25^\circ\text{C}};$$

typical  $-V_{GS(th)}$  at -1 mA.

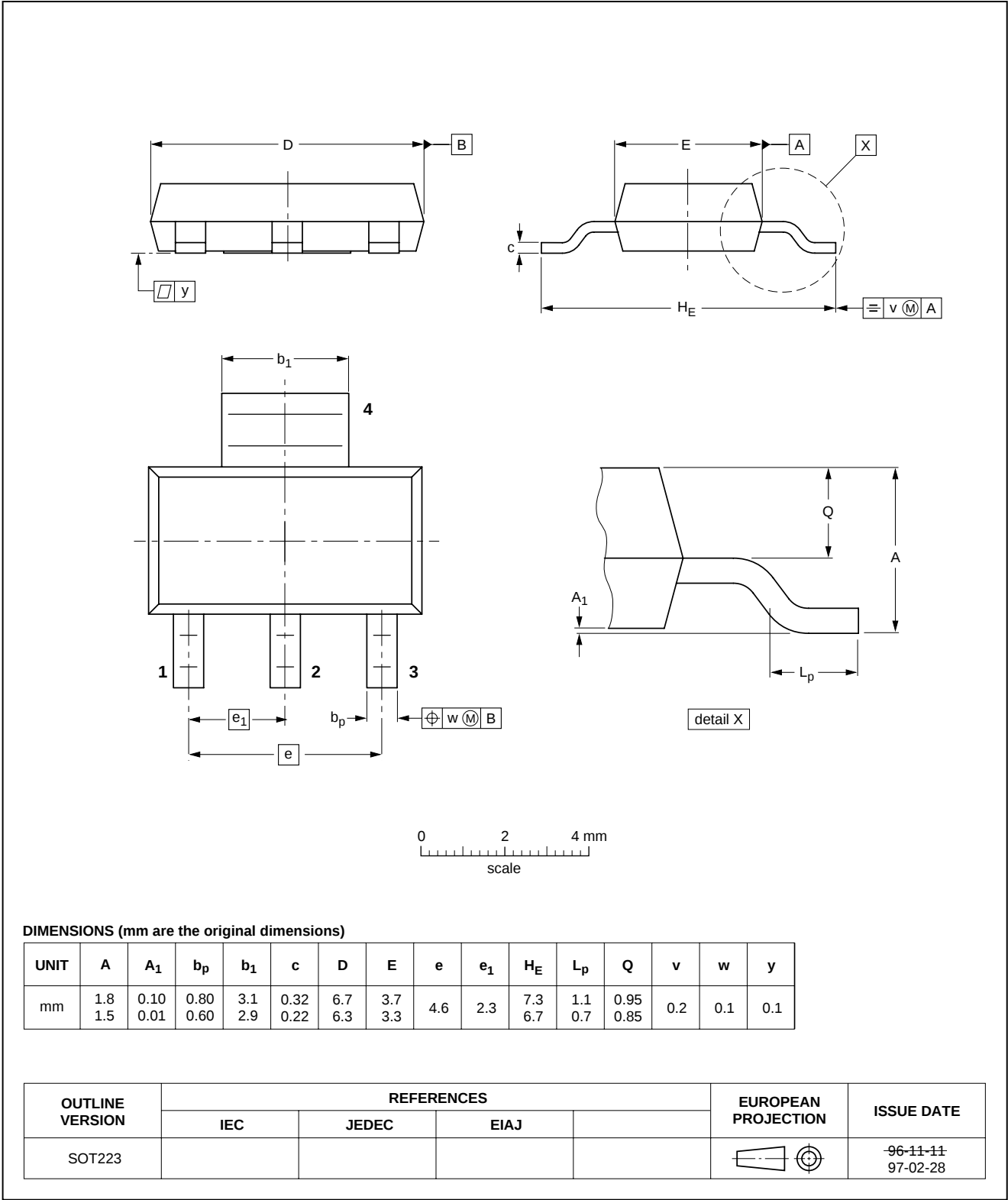
P-channel enhancement mode vertical  
D-MOS transistor

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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



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P-channel enhancement mode vertical  
D-MOS transistor

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**DEFINITIONS**

| <b>Data sheet status</b>                                                                            |                                                                                       |
|-----------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Objective specification                                                                             | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification                                                                           | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification                                                                               | This data sheet contains final product specifications.                                |
| <b>Application information</b>                                                                      |                                                                                       |
| Where application information is given, it is advisory and does not form part of the specification. |                                                                                       |

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|                                                         |        |
|---------------------------------------------------------|--------|
| P-channel enhancement mode vertical<br>D-MOS transistor | BSP220 |
|---------------------------------------------------------|--------|

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NOTES

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P-channel enhancement mode vertical  
D-MOS transistor

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