

# ANTREX Electronics

## Electronic Components Sourcing Information

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### Product Reference Information

|                      |                           |
|----------------------|---------------------------|
| <b>Part Number:</b>  | BSP122,115                |
| <b>Manufacturer:</b> | Nexperia USA Inc.         |
| <b>Package:</b>      | Please confirm with sales |
| <b>Availability:</b> | Please confirm with sales |

#### Product Page:

<https://antrexco.com/product/details/nexperia-usa-inc/bsp122-115.html>

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#### Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

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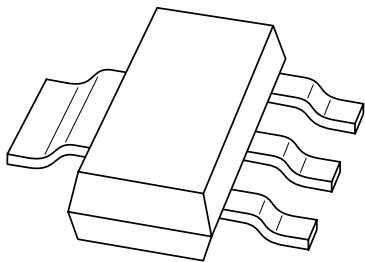
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Kind regards,

Team Nexperia

# DATA SHEET



## **BSP122**

N-channel enhancement mode  
vertical D-MOS transistor

Product specification  
Supersedes data of 1997 Jun 23

2001 May 18

N-channel enhancement mode  
vertical D-MOS transistor

BSP122

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

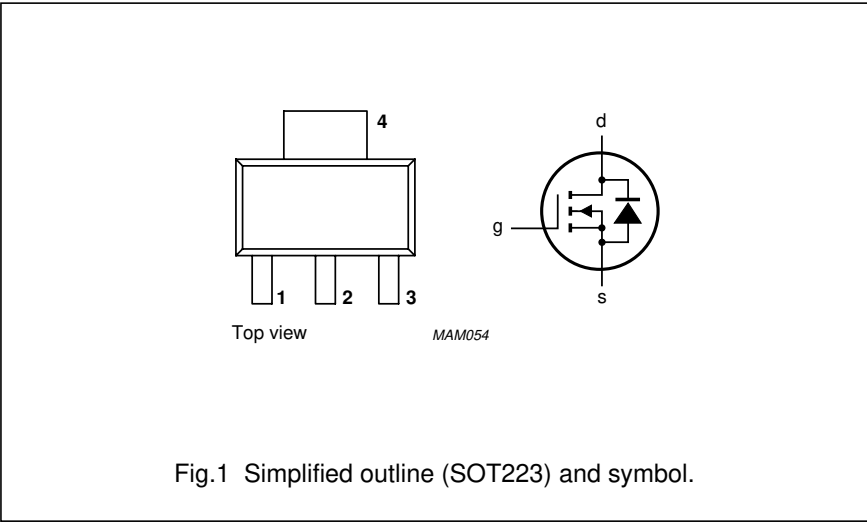
N-channel enhancement mode vertical D-MOS transistor in a SOT223 package and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

| PIN | DESCRIPTION |
|-----|-------------|
| 1   | gate        |
| 2   | drain       |
| 3   | source      |
| 4   | drain       |

QUICK REFERENCE DATA

| SYMBOL     | PARAMETER                        | MAX. | UNIT     |
|------------|----------------------------------|------|----------|
| $V_{DS}$   | drain-source voltage (DC)        | 200  | V        |
| $I_D$      | drain current (DC)               | 550  | mA       |
| $R_{DSon}$ | drain-source on-state resistance | 2.5  | $\Omega$ |
| $V_{GSth}$ | gate-source threshold voltage    | 2    | V        |



LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 60134).

| SYMBOL    | PARAMETER                 | CONDITIONS                                         | MIN. | MAX.     | UNIT               |
|-----------|---------------------------|----------------------------------------------------|------|----------|--------------------|
| $V_{DS}$  | drain-source voltage (DC) |                                                    | –    | 200      | V                  |
| $V_{GSO}$ | gate-source voltage (DC)  | open drain                                         | –    | $\pm 20$ | V                  |
| $I_D$     | drain current (DC)        |                                                    | –    | 550      | mA                 |
| $I_{DM}$  | peak drain current        |                                                    | –    | 3        | A                  |
| $P_{tot}$ | total power dissipation   | $T_{amb} \leq 25\text{ }^{\circ}\text{C}$ ; note 1 | –    | 1.5      | W                  |
| $T_{stg}$ | storage temperature       |                                                    | –55  | +150     | $^{\circ}\text{C}$ |
| $T_j$     | junction temperature      |                                                    | –    | 150      | $^{\circ}\text{C}$ |

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm<sup>2</sup>.

THERMAL CHARACTERISTICS

| SYMBOL        | PARAMETER                                           | VALUE | UNIT |
|---------------|-----------------------------------------------------|-------|------|
| $R_{th\ j-a}$ | thermal resistance from junction to ambient; note 1 | 83.3  | K/W  |

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm<sup>2</sup>.

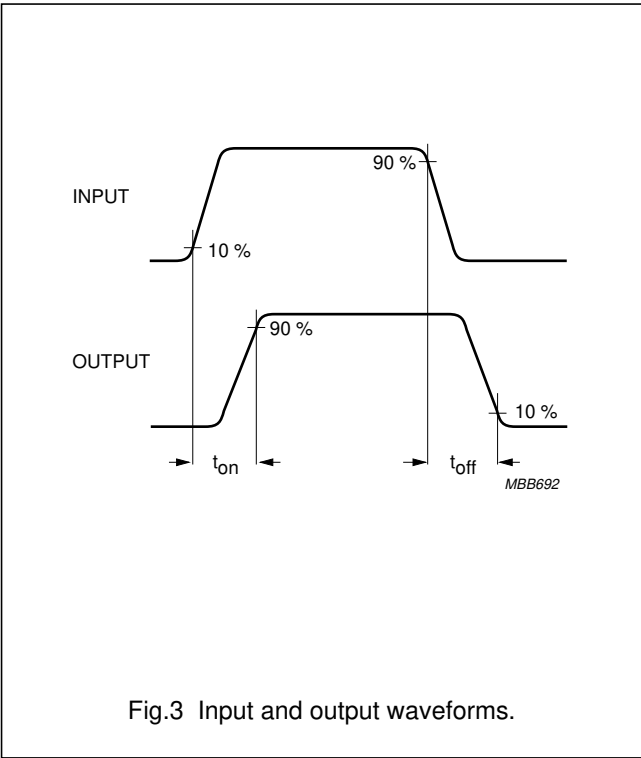
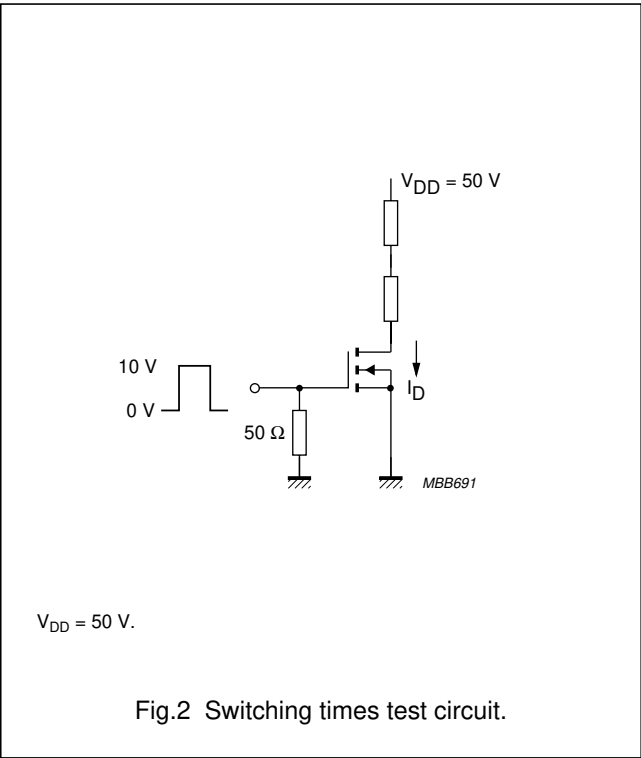
N-channel enhancement mode  
vertical D-MOS transistor

BSP122

CHARACTERISTICS

T<sub>j</sub> = 25 °C unless otherwise specified.

| SYMBOL                             | PARAMETER                      | CONDITIONS                                                                      | MIN. | TYP. | MAX. | UNIT |
|------------------------------------|--------------------------------|---------------------------------------------------------------------------------|------|------|------|------|
| V <sub>(BR)DSS</sub>               | drain-source breakdown voltage | I <sub>D</sub> = 10 μA; V <sub>GS</sub> = 0                                     | 200  | –    | –    | V    |
| I <sub>DSS</sub>                   | drain-source leakage current   | V <sub>DS</sub> = 160 V; V <sub>GS</sub> = 0                                    | –    | –    | 1    | μA   |
| I <sub>GSS</sub>                   | gate-source leakage current    | V <sub>GS</sub> = ±20 V; V <sub>DS</sub> = 0                                    | –    | –    | 100  | nA   |
| V <sub>GSth</sub>                  | gate-source threshold voltage  | I <sub>D</sub> = 1 mA; V <sub>GS</sub> = V <sub>DS</sub>                        | 0.4  | –    | 2    | V    |
| R <sub>DSon</sub>                  | drain-source on-resistance     | I <sub>D</sub> = 750 mA; V <sub>GS</sub> = 10 V                                 | –    | 1.7  | 2.5  | Ω    |
|                                    |                                | I <sub>D</sub> = 20 mA; V <sub>GS</sub> = 2.4 V                                 | –    | 3    | –    | Ω    |
| Y <sub>fs</sub>                    | transfer admittance            | I <sub>D</sub> = 750 mA; V <sub>DS</sub> = 25 V                                 | 400  | 900  | –    | mS   |
| C <sub>iss</sub>                   | input capacitance              | V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0; f = 1 MHz                          | –    | 100  | –    | pF   |
| C <sub>oss</sub>                   | output capacitance             | V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0; f = 1 MHz                          | –    | 20   | –    | pF   |
| C <sub>rss</sub>                   | reverse transfer capacitance   | V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0; f = 1 MHz                          | –    | 10   | –    | pF   |
| Switching times (see Figs 2 and 3) |                                |                                                                                 |      |      |      |      |
| t <sub>on</sub>                    | turn-on time                   | I <sub>D</sub> = 750 mA; V <sub>DD</sub> = 50 V;<br>V <sub>GS</sub> = 0 to 10 V | –    | 10   | 20   | ns   |
| t <sub>off</sub>                   | turn-off time                  | I <sub>D</sub> = 750 mA; V <sub>DD</sub> = 50 V;<br>V <sub>GS</sub> = 0 to 10 V | –    | 45   | 60   | ns   |



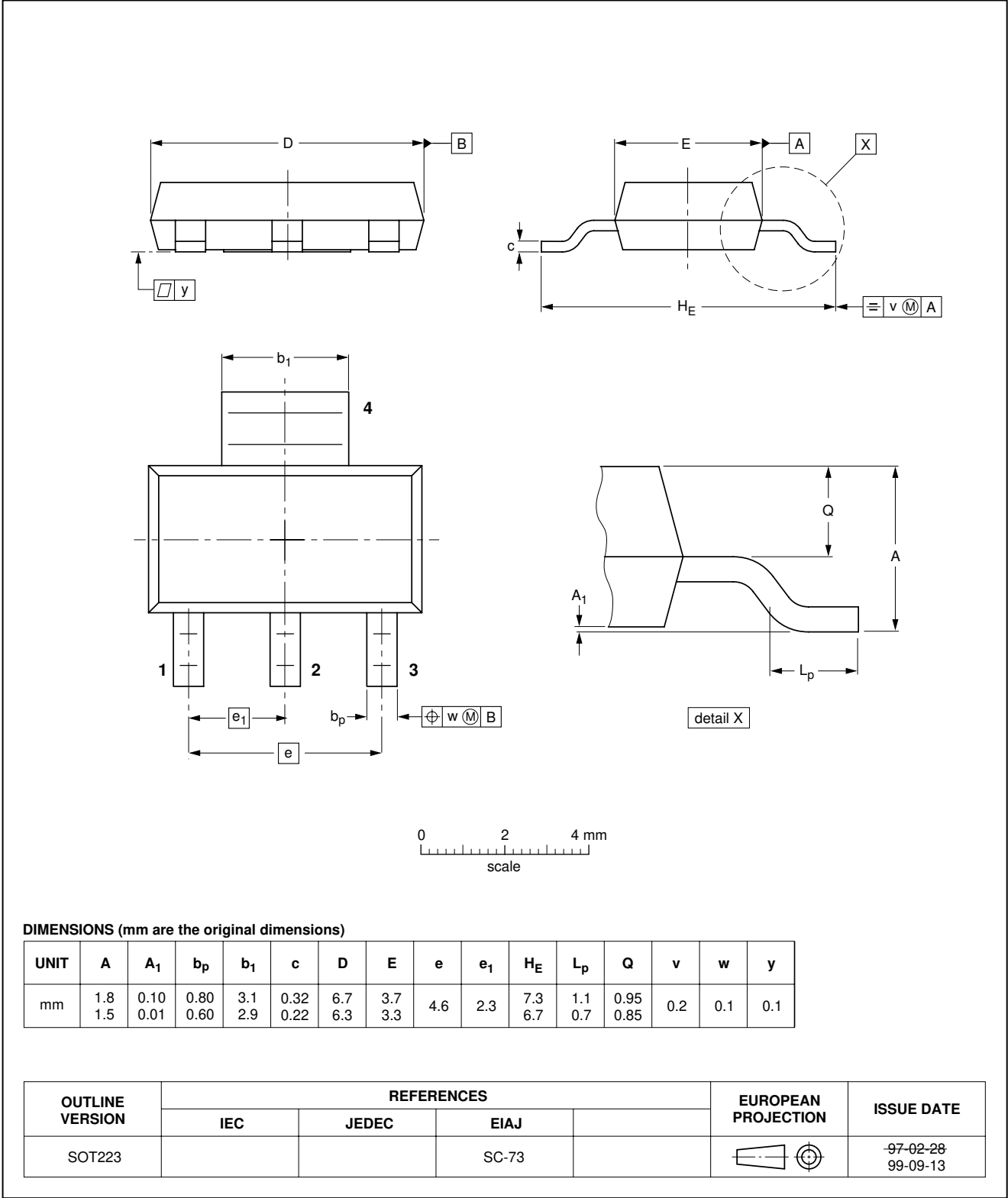
N-channel enhancement mode  
vertical D-MOS transistor

BSP122

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



# N-channel enhancement mode vertical D-MOS transistor

BSP122

## DATA SHEET STATUS

| DATA SHEET STATUS <sup>(1)</sup> | PRODUCT STATUS <sup>(2)</sup> | DEFINITIONS                                                                                                                                                                                                                                                                                                            |
|----------------------------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Objective data                   | Development                   | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.                                                                                                                            |
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N-channel enhancement mode  
vertical D-MOS transistor

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BSP122

**NOTES**

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N-channel enhancement mode  
vertical D-MOS transistor

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BSP122

**NOTES**

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