

# ANTREX Electronics

Electronic Components Sourcing Information

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## Product Reference Information

**Part Number:** 2N7002BKS,115  
**Manufacturer:** Nexperia USA Inc.  
**Package:** Please confirm with sales  
**Availability:** Please confirm with sales

**Product Page:**

<https://antrexco.com/product/details/nexperia-usa-inc/2n7002bks-115.html>

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**Note:**

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

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# 2N7002BKS

60 V, 300 mA dual N-channel Trench MOSFET

17 October 2024

Product data sheet

## 1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- ESD protection up to 2 kV
- AEC-Q101 qualified

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

## 4. Quick reference data

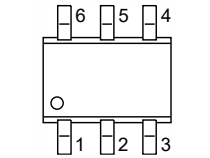
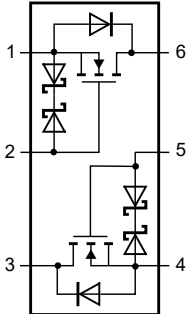
Table 1. Quick reference data

| Symbol                                         | Parameter                        | Conditions                                                                                                                      |     | Min | Typ | Max | Unit     |
|------------------------------------------------|----------------------------------|---------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|----------|
| <b>Per transistor</b>                          |                                  |                                                                                                                                 |     |     |     |     |          |
| $V_{DS}$                                       | drain-source voltage             | $T_{amb} = 25\text{ °C}$                                                                                                        |     | -   | -   | 60  | V        |
| $V_{GS}$                                       | gate-source voltage              |                                                                                                                                 |     | -20 | -   | 20  | V        |
| $I_D$                                          | drain current                    | $V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$                                                                                  | [1] | -   | -   | 300 | mA       |
| <b>Static characteristics (per transistor)</b> |                                  |                                                                                                                                 |     |     |     |     |          |
| $R_{DSon}$                                     | drain-source on-state resistance | $V_{GS} = 5\text{ V}; I_D = 50\text{ mA}; \text{pulsed}; t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.01; T_j = 25\text{ °C}$ |     | -   | 1.3 | 2   | $\Omega$ |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline                                                                                       | Graphic symbol                                                                                       |
|-----|--------|-------------|----------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
| 1   | S1     | source1     |  <p>TSSOP6 (SOT363)</p> |  <p>017aaa055</p> |
| 2   | G1     | gate1       |                                                                                                          |                                                                                                      |
| 3   | D2     | drain2      |                                                                                                          |                                                                                                      |
| 4   | S2     | source2     |                                                                                                          |                                                                                                      |
| 5   | G2     | gate2       |                                                                                                          |                                                                                                      |
| 6   | D1     | drain1      |                                                                                                          |                                                                                                      |

6. Ordering information

Table 3. Ordering information

| Type number | Package |                                                                                           |         |
|-------------|---------|-------------------------------------------------------------------------------------------|---------|
|             | Name    | Description                                                                               | Version |
| 2N7002BKS   | TSSOP6  | plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body | SOT363  |

7. Marking

Table 4. Marking codes

| Type number | Marking code[1] |
|-------------|-----------------|
| 2N7002BKS   | ZT%             |

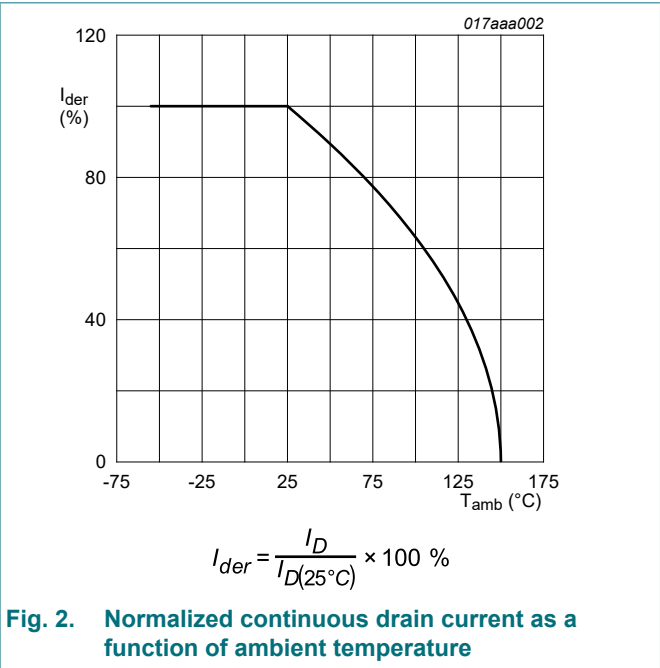
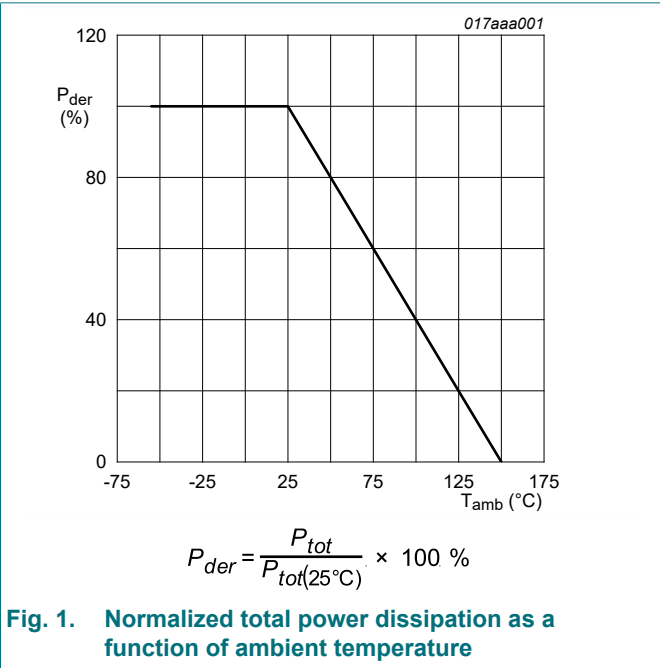
[1] % = placeholder for manufacturing site code

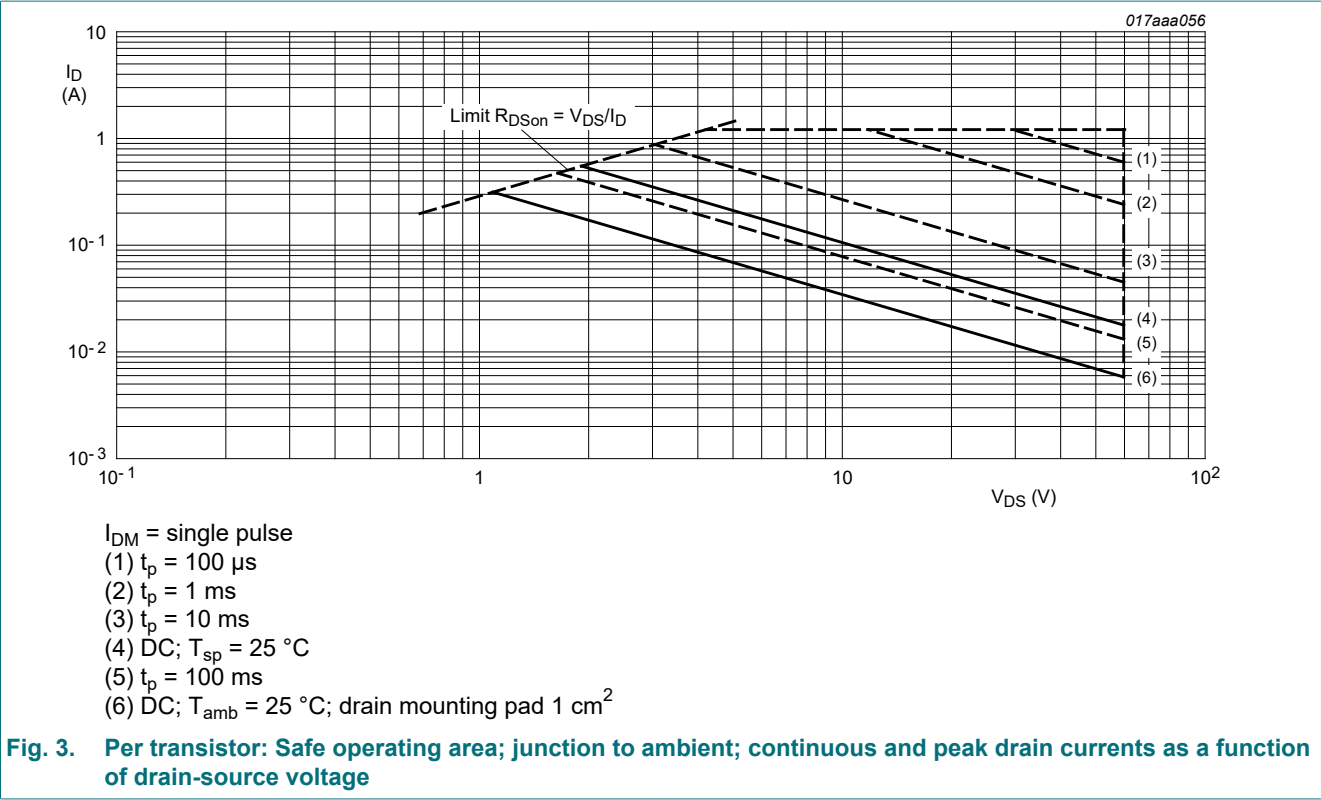
8. Limiting values

Table 5. Limiting values  
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol             | Parameter                       | Conditions                                                     |     | Min | Max  | Unit |
|--------------------|---------------------------------|----------------------------------------------------------------|-----|-----|------|------|
| Per transistor     |                                 |                                                                |     |     |      |      |
| V <sub>DS</sub>    | drain-source voltage            | T <sub>amb</sub> = 25 °C                                       |     | -   | 60   | V    |
| V <sub>GS</sub>    | gate-source voltage             |                                                                |     | -20 | 20   | V    |
| I <sub>D</sub>     | drain current                   | V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C               | [1] | -   | 300  | mA   |
|                    |                                 | V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 100 °C              | [1] | -   | 215  | mA   |
| I <sub>DM</sub>    | peak drain current              | T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs |     | -   | 1.2  | A    |
| P <sub>tot</sub>   | total power dissipation         | T <sub>amb</sub> = 25 °C                                       | [2] | -   | 295  | mW   |
|                    |                                 |                                                                | [1] | -   | 340  | mW   |
|                    |                                 | T <sub>sp</sub> = 25 °C                                        |     | -   | 1040 | mW   |
| Per device         |                                 |                                                                |     |     |      |      |
| P <sub>tot</sub>   | total power dissipation         | T <sub>amb</sub> = 25 °C                                       | [2] | -   | 445  | mW   |
| T <sub>j</sub>     | junction temperature            |                                                                |     | -   | 150  | °C   |
| T <sub>amb</sub>   | ambient temperature             |                                                                |     | -55 | 150  | °C   |
| T <sub>stg</sub>   | storage temperature             |                                                                |     | -65 | 150  | °C   |
| Source-drain diode |                                 |                                                                |     |     |      |      |
| I <sub>S</sub>     | source current                  | T <sub>amb</sub> = 25 °C                                       | [1] | -   | 300  | mA   |
| ESD maximum rating |                                 |                                                                |     |     |      |      |
| V <sub>ESD</sub>   | electrostatic discharge voltage | HBM                                                            | [3] | -   | 2    | kV   |

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.  
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.  
[3] Measured between all pins.



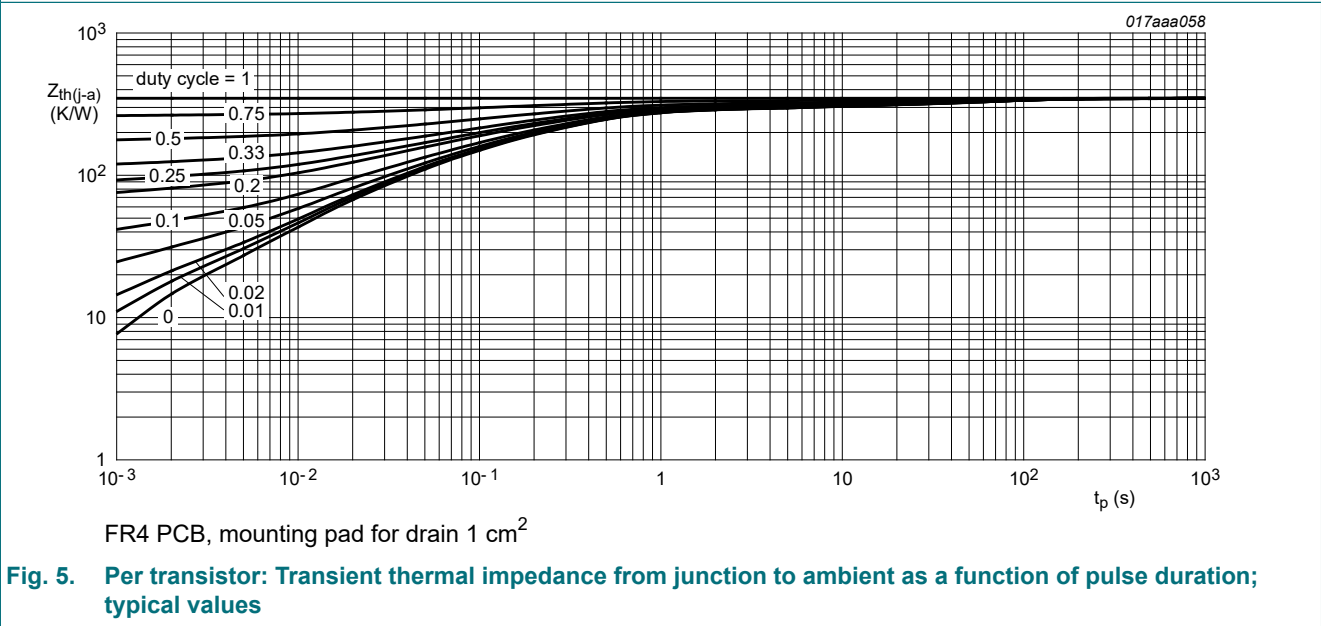
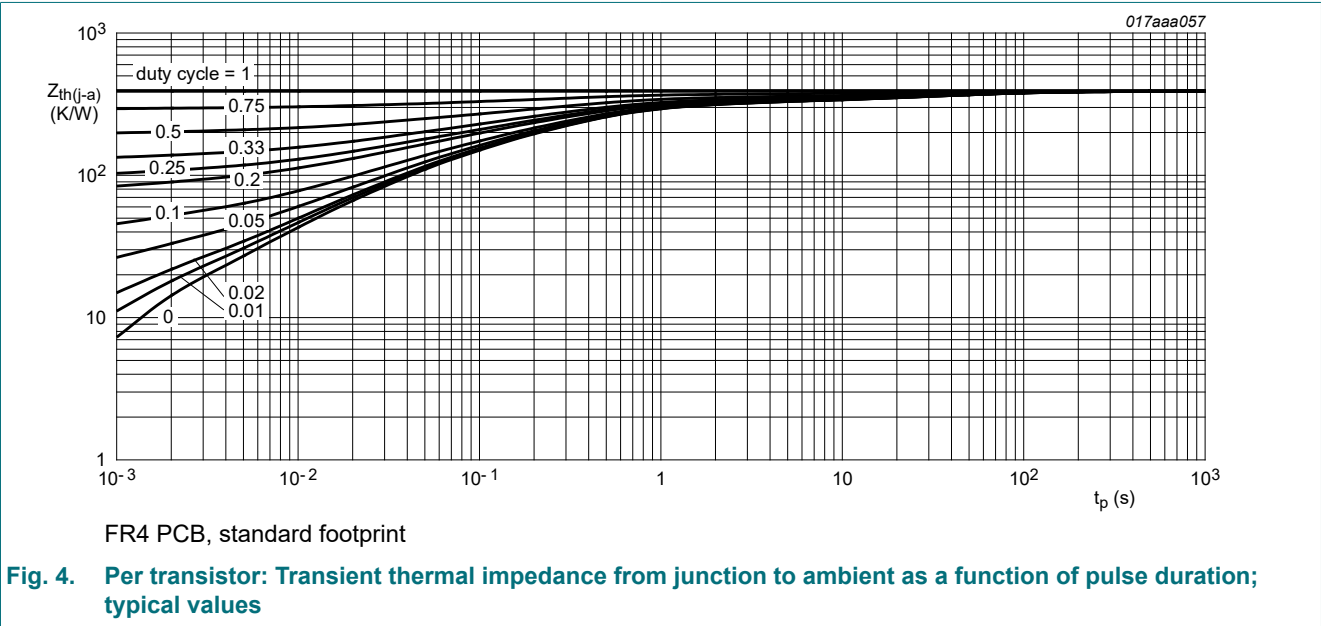


9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol         | Parameter                                        | Conditions  |     | Min | Typ | Max | Unit |
|----------------|--------------------------------------------------|-------------|-----|-----|-----|-----|------|
| Per device     |                                                  |             |     |     |     |     |      |
| $R_{th(j-a)}$  | thermal resistance from junction to ambient      | in free air | [1] | -   | -   | 275 | K/W  |
| Per transistor |                                                  |             |     |     |     |     |      |
| $R_{th(j-a)}$  | thermal resistance from junction to ambient      | in free air | [1] | -   | 370 | 425 | K/W  |
|                |                                                  |             | [2] | -   | 320 | 370 | K/W  |
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point |             |     | -   | -   | 120 | K/W  |

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.  
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.



10. Characteristics

Table 7. Characteristics

| Symbol                                   | Parameter                        | Conditions                                                                                                                |  | Min  | Typ  | Max | Unit |
|------------------------------------------|----------------------------------|---------------------------------------------------------------------------------------------------------------------------|--|------|------|-----|------|
| Static characteristics (per transistor)  |                                  |                                                                                                                           |  |      |      |     |      |
| V <sub>(BR)DSS</sub>                     | drain-source breakdown voltage   | I <sub>D</sub> = 10 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                     |  | 60   | -    | -   | V    |
| V <sub>GSth</sub>                        | gate-source threshold voltage    | I <sub>D</sub> = 250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C                                       |  | 1.1  | 1.6  | 2.1 | V    |
| I <sub>DSS</sub>                         | drain leakage current            | V <sub>DS</sub> = 60 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                     |  | -    | -    | 1   | μA   |
|                                          |                                  | V <sub>DS</sub> = 60 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 150 °C                                                    |  | -    | -    | 10  | μA   |
| I <sub>GSS</sub>                         | gate leakage current             | V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                     |  | -    | -    | 10  | μA   |
|                                          |                                  | V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                    |  | -    | -    | 10  | μA   |
| R <sub>DSon</sub>                        | drain-source on-state resistance | V <sub>GS</sub> = 5 V; I <sub>D</sub> = 50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.01; T <sub>j</sub> = 25 °C          |  | -    | 1.3  | 2   | Ω    |
|                                          |                                  | V <sub>GS</sub> = 10 V; I <sub>D</sub> = 500 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.01; T <sub>j</sub> = 25 °C        |  | -    | 1    | 1.6 | Ω    |
| g <sub>fs</sub>                          | forward transconductance         | V <sub>DS</sub> = 10 V; I <sub>D</sub> = 200 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.01; T <sub>j</sub> = 25 °C        |  | -    | 550  | -   | mS   |
| Dynamic characteristics (per transistor) |                                  |                                                                                                                           |  |      |      |     |      |
| Q <sub>G(tot)</sub>                      | total gate charge                | V <sub>DS</sub> = 30 V; I <sub>D</sub> = 300 mA; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C                          |  | -    | 0.5  | 0.6 | nC   |
| Q <sub>GS</sub>                          | gate-source charge               |                                                                                                                           |  | -    | 0.2  | -   | nC   |
| Q <sub>GD</sub>                          | gate-drain charge                |                                                                                                                           |  | -    | 0.1  | -   | nC   |
| C <sub>iss</sub>                         | input capacitance                | V <sub>DS</sub> = 10 V; f = 1 MHz; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                          |  | -    | 33   | 50  | pF   |
| C <sub>oss</sub>                         | output capacitance               |                                                                                                                           |  | -    | 7    | -   | pF   |
| C <sub>rss</sub>                         | reverse transfer capacitance     |                                                                                                                           |  | -    | 4    | -   | pF   |
| t <sub>d(on)</sub>                       | turn-on delay time               | V <sub>DS</sub> = 50 V; R <sub>L</sub> = 250 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C |  | -    | 5    | 10  | ns   |
| t <sub>r</sub>                           | rise time                        |                                                                                                                           |  | -    | 6    | -   | ns   |
| t <sub>d(off)</sub>                      | turn-off delay time              |                                                                                                                           |  | -    | 12   | 24  | ns   |
| t <sub>f</sub>                           | fall time                        |                                                                                                                           |  | -    | 7    | -   | ns   |
| Source-drain diode (per transistor)      |                                  |                                                                                                                           |  |      |      |     |      |
| V <sub>SD</sub>                          | source-drain voltage             | I <sub>S</sub> = 115 mA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                    |  | 0.47 | 0.75 | 1.1 | V    |

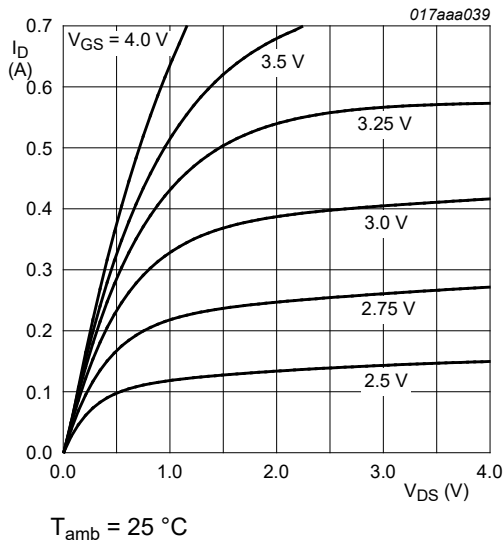


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

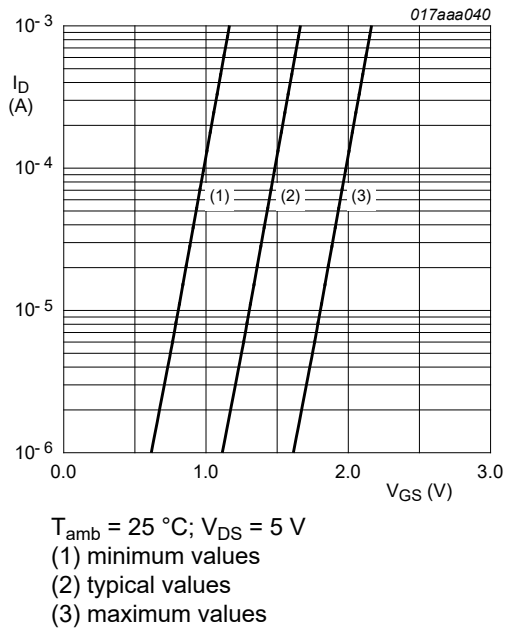


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

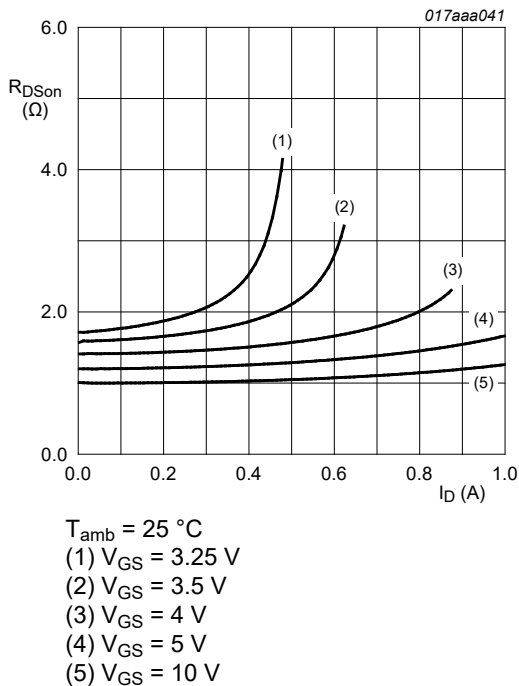


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

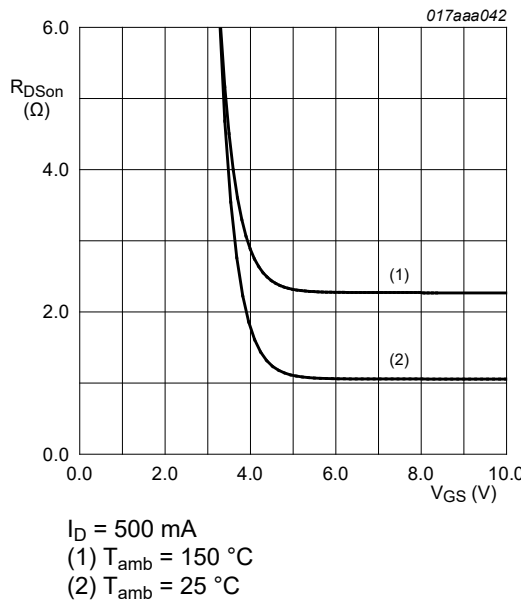


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

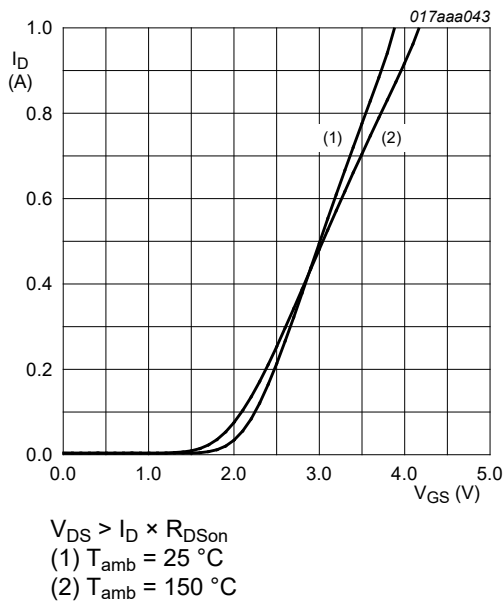


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

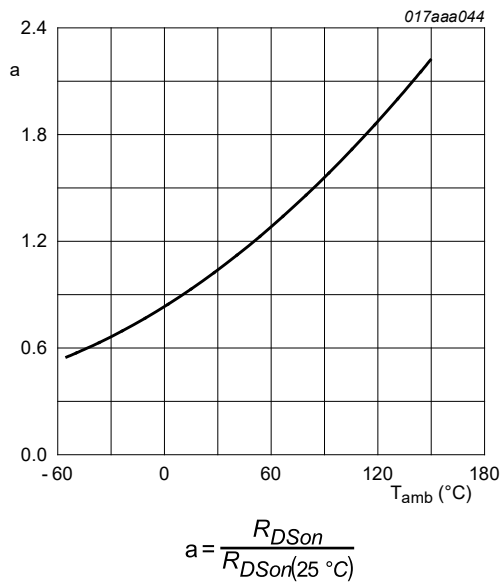


Fig. 11. Normalized drain-source on-state resistance as a function of ambient temperature; typical values

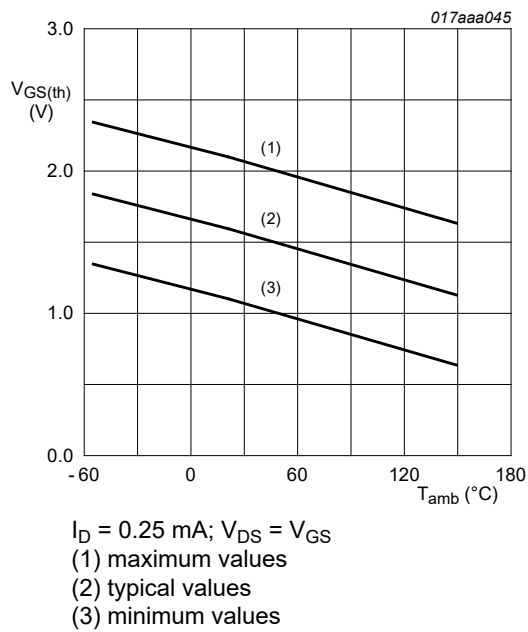


Fig. 12. Gate-source threshold voltage as a function of ambient temperature

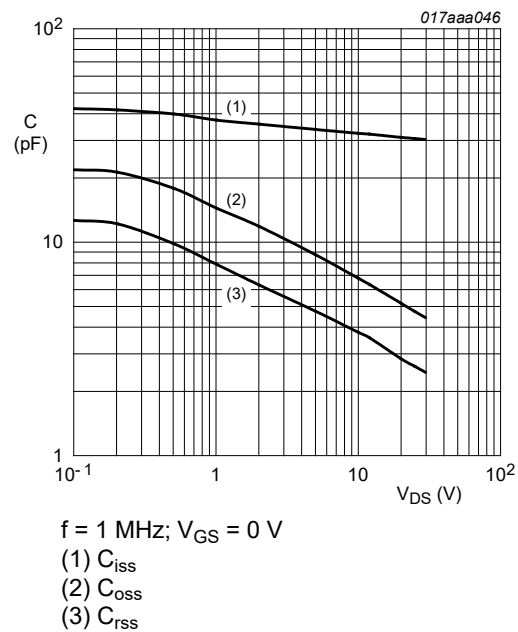


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

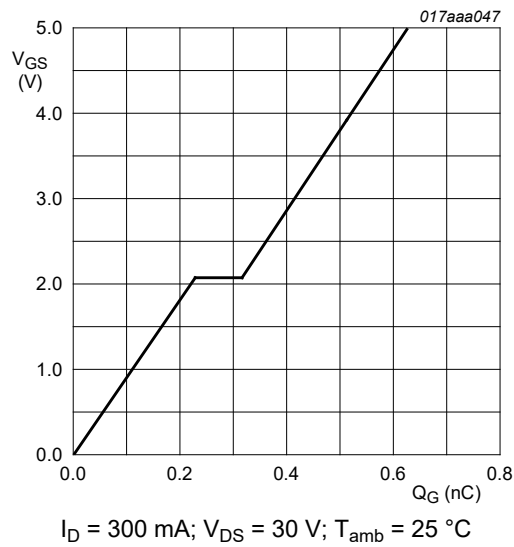


Fig. 14. Gate-source voltage as a function of gate charge; typical values

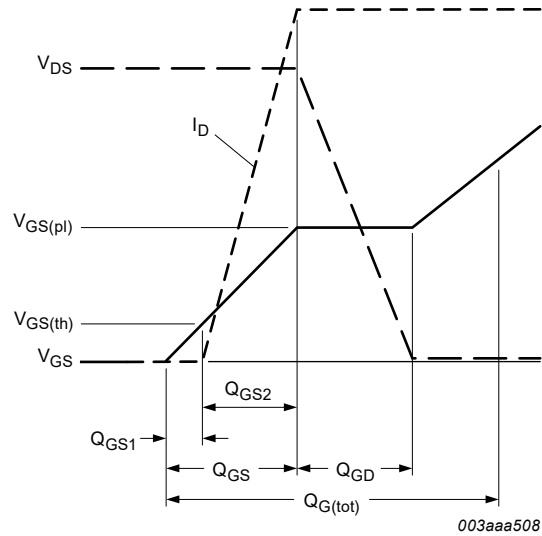
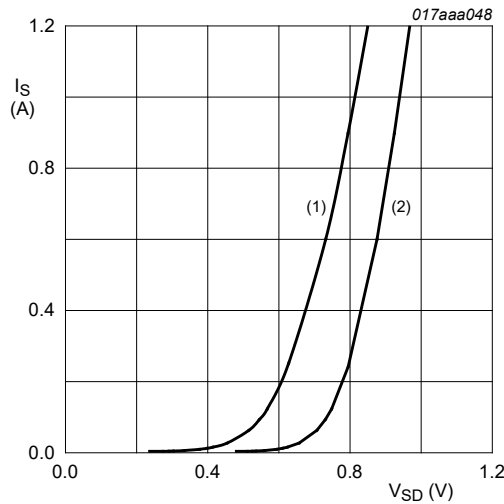


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0$  V  
(1)  $T_{amb} = 150$  °C  
(2)  $T_{amb} = 25$  °C

Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information

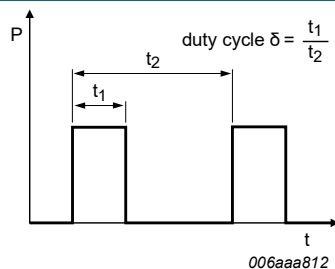


Fig. 17. Duty cycle definition

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

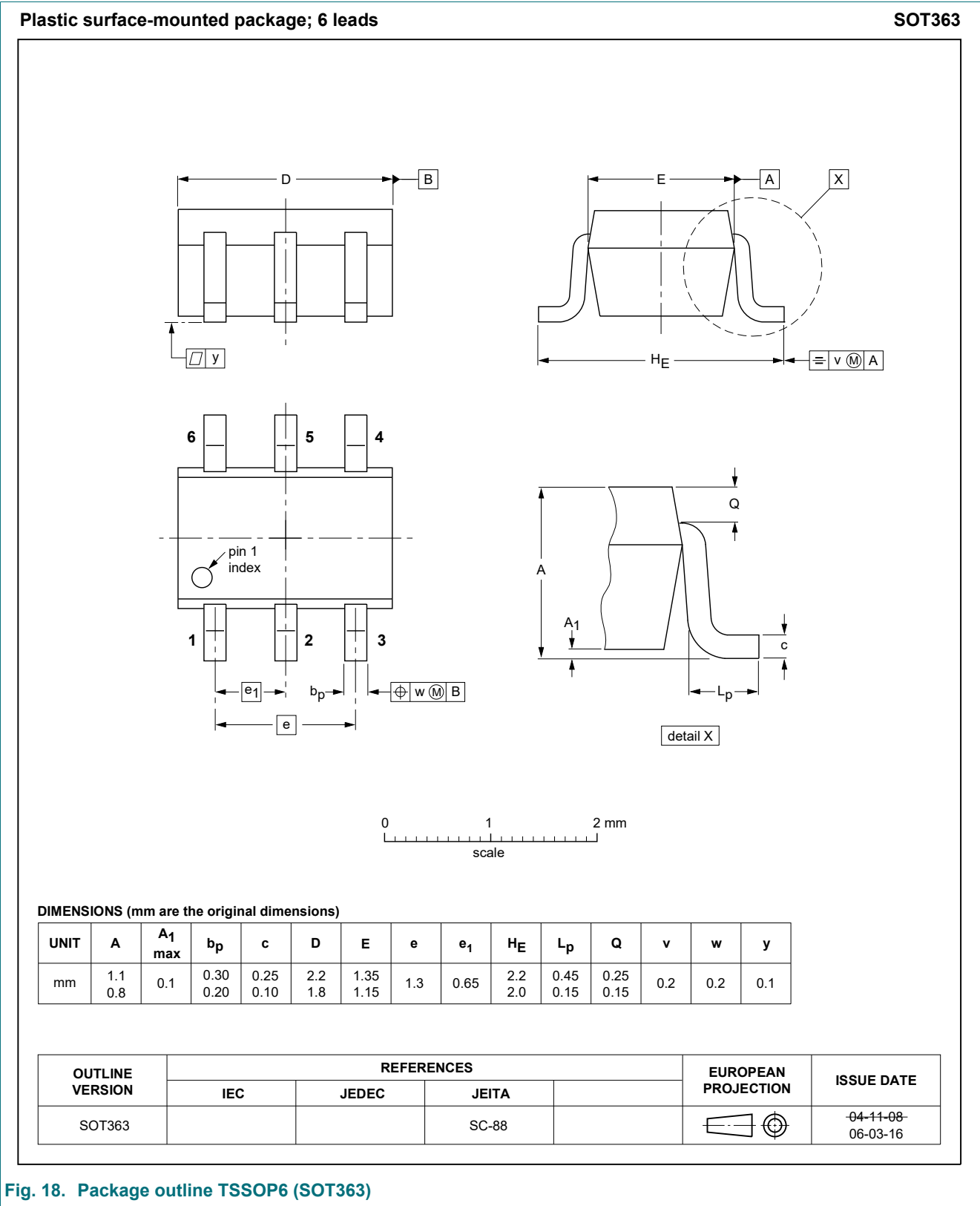
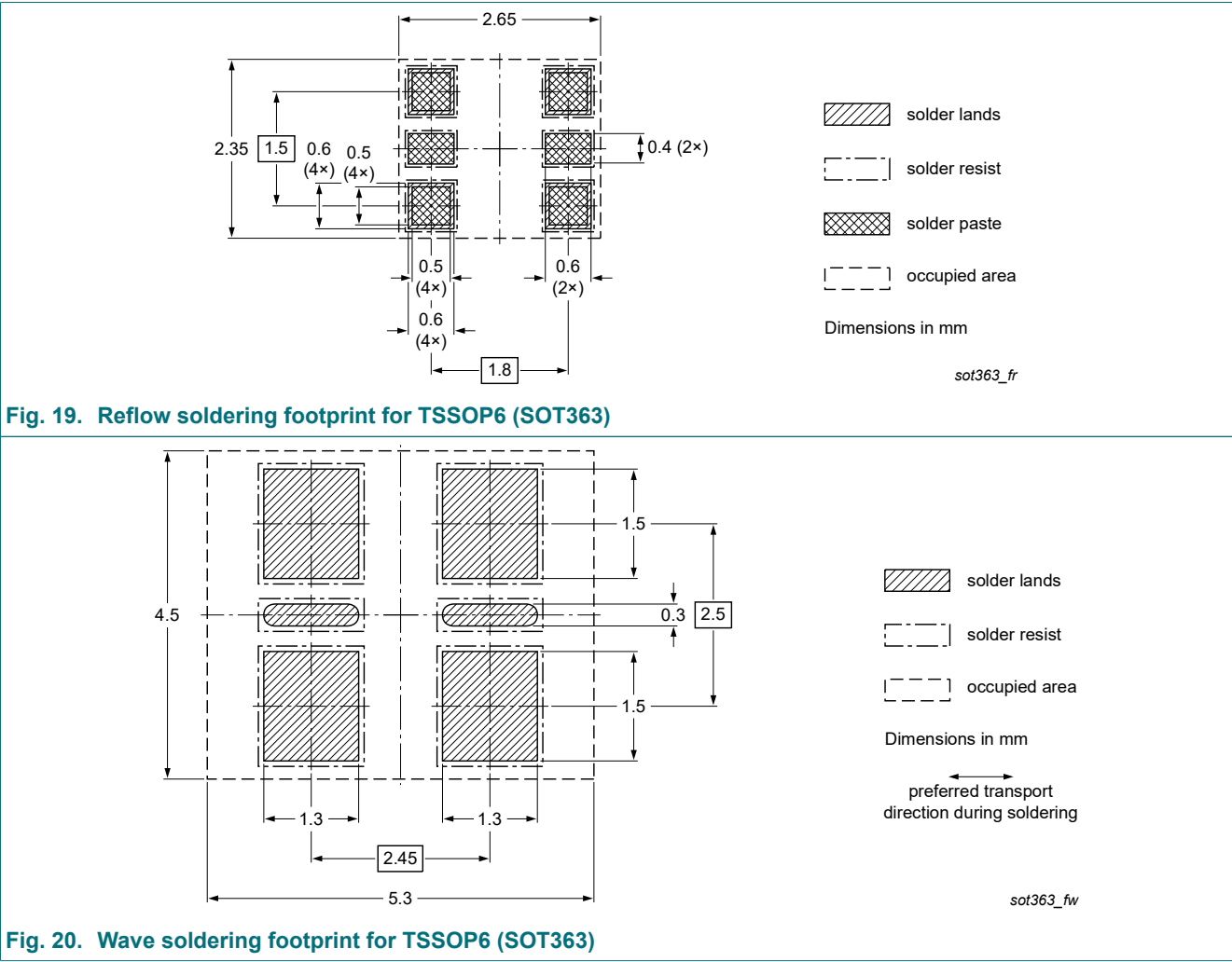


Fig. 18. Package outline TSSOP6 (SOT363)

13. Soldering



14. Revision history

Table 8. Revision history

| Data sheet ID  | Release date                                                                                                                                                                                                                                                           | Data sheet status  | Change notice | Supersedes    |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|---------------|---------------|
| 2N7002BKS v.3  | 20241017                                                                                                                                                                                                                                                               | Product data sheet | -             | 2N7002BKS v.2 |
| Modifications: | <ul style="list-style-type: none"><li>Chapter "Characteristics": Conditions corrected for parameters <math>t_{d(on)}</math>, <math>t_r</math>, <math>t_{d(off)}</math>, <math>t_f</math></li><li>Chapter "Characteristics": Conditions corrected for Fig. 14</li></ul> |                    |               |               |
| 2N7002BKS v.2  | 20100923                                                                                                                                                                                                                                                               | Product data sheet | -             | 2N7002BKS v.1 |
| 2N7002BKS v.1  | 20100617                                                                                                                                                                                                                                                               | Product data sheet | -             | -             |

## 15. Legal information

### Data sheet status

| Document status<br>[1][2]      | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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