ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	MCP47FEB08-20E/ST
Manufacturer:	Microchip Technology
Package:	20-TSSOP (0.173", 4.40mm Width)
Availability:	Please confirm with sales

Product Page:

https://antrexco.com/product/details/microchip-technology/mcp47feb08-20e-st.html

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

MCP47FXBX4/8

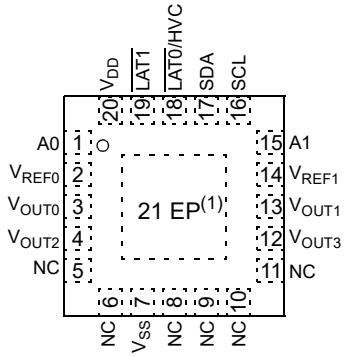
8/10/12-Bit Quad/Octal Voltage Output, 6 LSb INL Digital-to-Analog Converters with I²C Interface

Features

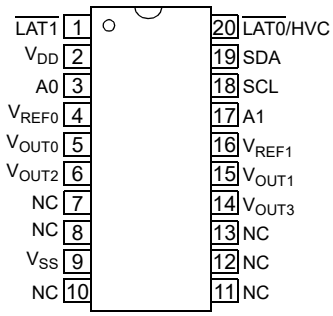
- Operating Voltage Range:
  - 2.7V to 5.5V - Full specifications
  - 1.8V to 2.7V - Reduced device specifications
- Output Voltage Resolutions:
  - 8-bit: **MCP47FXB0X** (256 steps)
  - 10-bit: **MCP47FXB1X** (1024 steps)
  - 12-bit: **MCP47FXB2X** (4096 steps)
- Rail-to-Rail Output
- Fast Settling Time of 7.8 µs (Typical)
- DAC Voltage Reference Source Options:
  - Device V_{DD}
  - External V_{REF} pin (buffered or unbuffered)
  - Internal band gap (1.22V typical)
- Output Gain Options:
  - 1x (unity)
  - 2x (available when not using internal V_{DD} as voltage source)
- Nonvolatile Memory (EEPROM) Option:
  - User-programmed Power-on Reset (POR)/Brown-out Reset (BOR) output setting and device Configuration bits recall
  - Auto recall of saved DAC register setting
  - Auto recall of saved device configuration (voltage reference, gain, power-down)
- Power-on/Brown-out Reset Protection
- Power-Down Modes:
  - Disconnects output buffer (high-impedance)
  - Selection of V_{OUT} pull-down resistors (125 kΩ or 1 kΩ)
- Low-Power Consumption:
  - Normal operation: < 1 mA (Quad), 1.8 mA (Octal)
  - Power-Down operation: 680 nA typical
  - EEPROM write cycle: 2.7 mA maximum
- I²C Interface:
  - Slave address options: four predefined addresses or user-programmable (all 7 bits)
  - Standard (100 kbps), Fast (400 kbps), and High-Speed (up to 3.4 Mbps) modes
- Package Types:
  - 20-lead TSSOP
  - 20-lead 5 x 5 mm VQFN
- Extended Temperature Range: -40°C to +125°C

Package Types

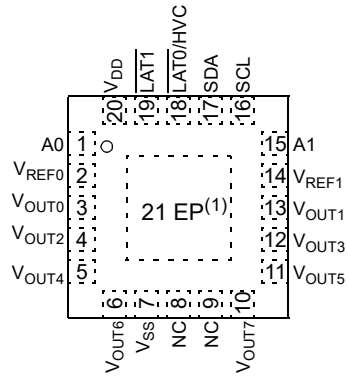
MCP47FXBX4
20-Lead VQFN
5x5 mm Quad



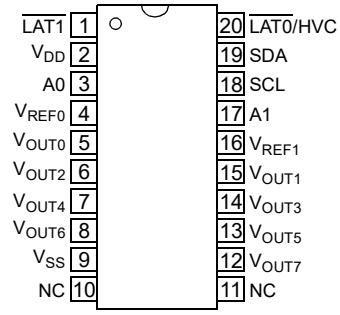
MCP47FXBX4
20-Lead TSSOP
Quad



MCP47FXBX8
20-Lead VQFN
5x5 mm Octal



MCP47FXBX8
20-Lead TSSOP
Octal



Note 1: Includes Exposed Thermal Pad (EP); see Table 3-1 and Table 3-2.

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General Description

The MCP47FXBX4/8 devices are a family of buffered voltage output Digital-to-Analog Converters (DAC), with the following options:

- quad or octal output channel configurations
- 8/10/12-bit resolution
- Volatile or nonvolatile user memory

The quad and octal options differ only by the number of output channels. The volatile and nonvolatile versions have an identical analog circuit structure.

There are three voltage reference sources: the external V_{REF} pin, the device's V_{DD} or an internal band gap voltage source.

When the V_{DD} mode is selected, it is internally connected to the DAC's reference circuit. When the external V_{REF} pin is used, the user has the option to select between a gain of 1 and 2 if the Buffered mode is used, or the internal buffer can be bypassed entirely in the external V_{REF} Unbuffered mode.

In the internal band gap voltage reference mode, the gain can be selected between 2 and 4.

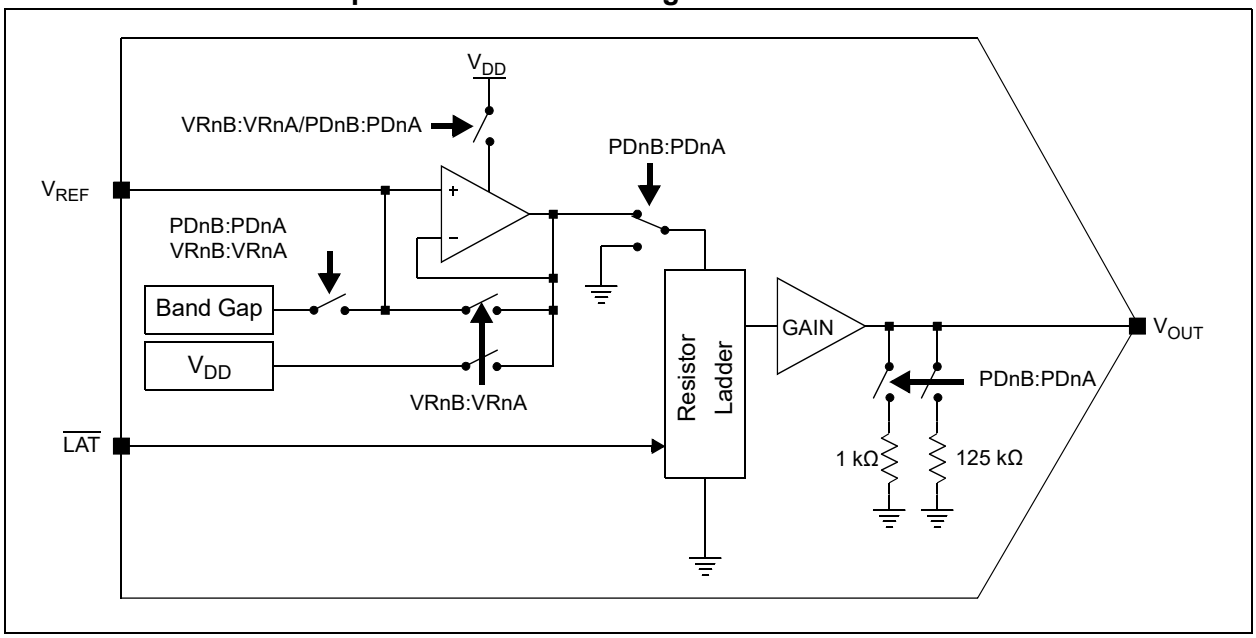
This family of devices features WiperLock™ functionality, which prevents inadvertent changes of the output value. It uses a high voltage on a specific pin, with dedicated commands, to lock the values that are stored in memory.

The MCP47FXBX4/8 devices communicate with the host controller using an I^2C compatible interface, supporting the following data transfer rates: Standard (100 kHz), Fast (400 kHz) and High-Speed (1.7 MHz and 3.4 MHz). They can only function as slave devices.

Applications

- Set Point or Offset Trimming
- Sensor Calibration
- Low-Power Portable Instrumentation
- PC Peripherals
- Data Acquisition Systems
- Motor Control

MCP47FXBX4/8 DAC Output Channel Block Diagram



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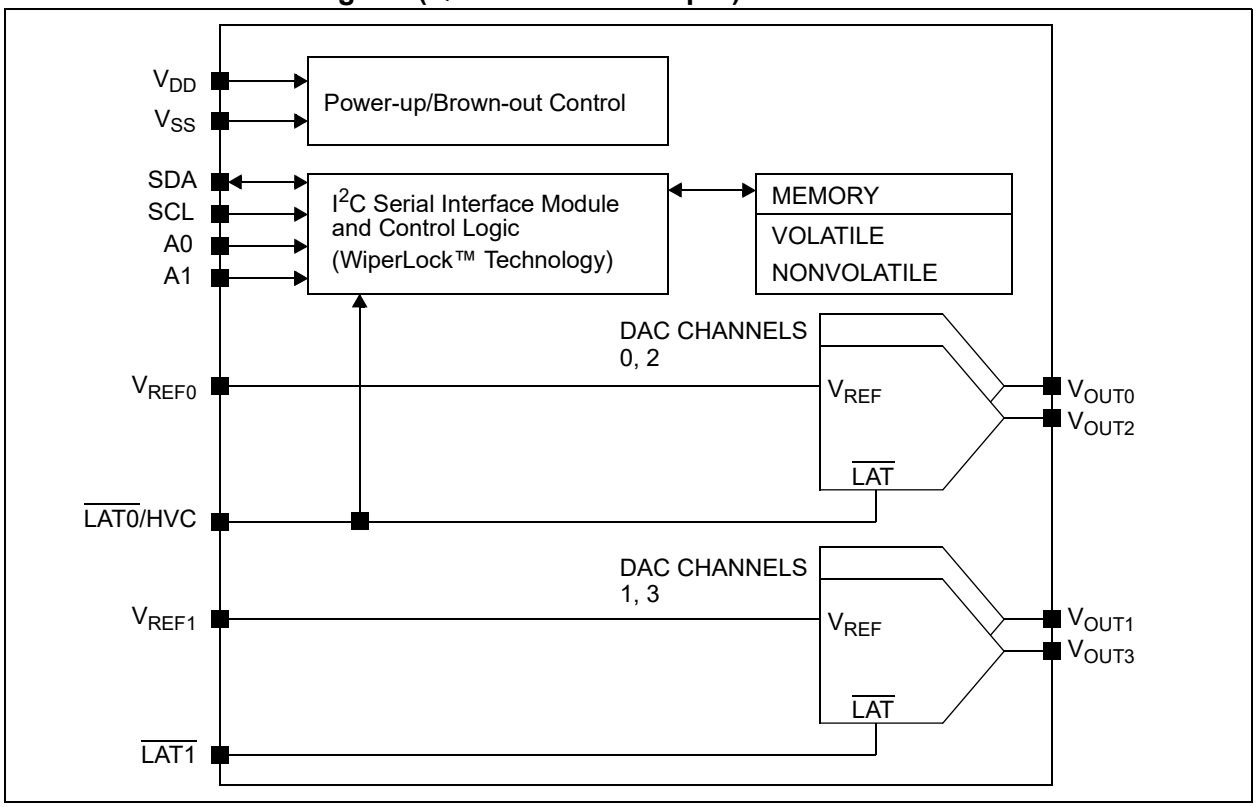
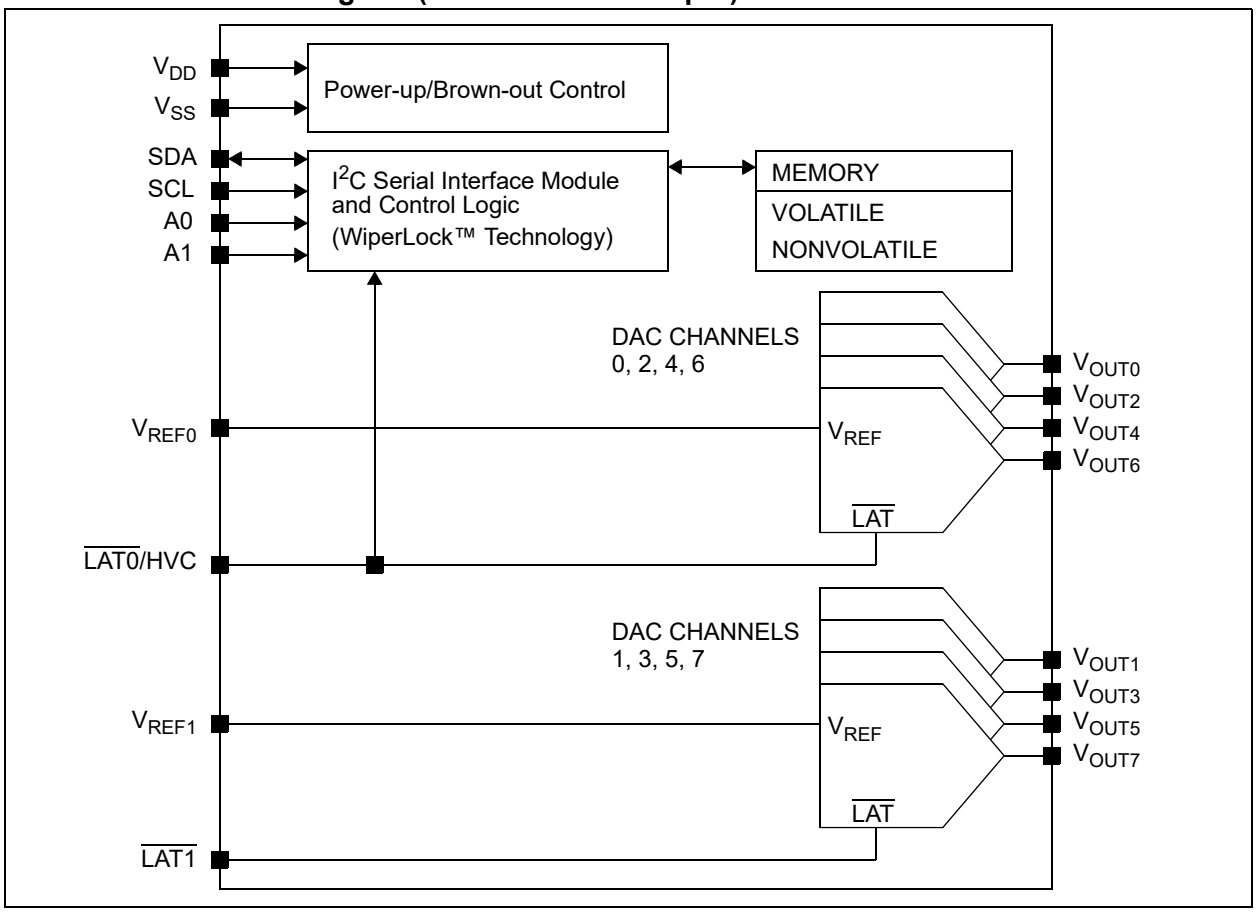
MCP47FXBX4 Block Diagram (Quad-Channel Output)



MCP47FXBX8 Block Diagram (Octal-Channel Output)



Device Features

Device	Package Type	# of Channels	Resolution (bits)	DAC Output POR/BOR Setting[1]	# of V_{REF} Inputs	# of $\overline{LAT}$ Inputs	Internal Band Gap	Memory
MCP47FVB04	VQFN-20 5 x 5, TSSOP-20	4	8	7Fh	2	2	Yes	RAM
MCP47FVB14	VQFN-20 5 x 5, TSSOP-20	4	10	1FFh	2	2	Yes	RAM
MCP47FVB24	VQFN-20 5 x 5, TSSOP-20	4	12	7FFh	2	2	Yes	RAM
MCP47FVB08	VQFN-20 5 x 5, TSSOP-20	8	8	7Fh	2	2	Yes	RAM
MCP47FVB18	VQFN-20 5 x 5, TSSOP-20	8	10	1FFh	2	2	Yes	RAM
MCP47FVB28	VQFN-20 5 x 5, TSSOP-20	8	12	7FFh	2	2	Yes	RAM
MCP47FEB04	VQFN-20 5 x 5, TSSOP-20	4	8	7Fh	2	2	Yes	EEPROM
MCP47FEB14	VQFN-20 5 x 5, TSSOP-20	4	10	1FFh	2	2	Yes	EEPROM
MCP47FEB24	VQFN-20 5 x 5, TSSOP-20	4	12	7FFh	2	2	Yes	EEPROM
MCP47FEB08	VQFN-20 5 x 5, TSSOP-20	8	8	7Fh	2	2	Yes	EEPROM
MCP47FEB18	VQFN-20 5 x 5, TSSOP-20	8	10	1FFh	2	2	Yes	EEPROM
MCP47FEB28	VQFN-20 5 x 5, TSSOP-20	8	12	7FFh	2	2	Yes	EEPROM

Note 1: The factory default value. The DAC output POR/BOR value can be modified via the nonvolatile DAC output register (available only on nonvolatile devices - MCP47FEBXX).

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Voltage on V_{DD} with Respect to V_{SS} ..... -0.6V to +6.5V

Voltage on all Pins with Respect to V_{SS} ..... -0.6V to V_{DD}+0.3V

Input Clamp Current, I_{IK} (V_I < 0, V_I > V_{DD}, V_I > V_{PP} on HV Pins) ..... ±20 mA

Output Clamp Current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA

Maximum Current out of the V_{SS} Pin (Quad) ..... 150 mA
(Octal) ..... 150 mA

Maximum Current into the V_{DD} Pin (Quad) ..... 150 mA
(Octal) ..... 150 mA

Maximum Current Sourced by the V_{OUT} Pin ..... 20 mA

Maximum Current Sunk by the V_{OUT} Pin ..... 20 mA

Maximum Current Sunk by the V_{REF} Pin ..... 125 µA

Maximum Input Current Source/Sunk by the SDA, SCL Pins ..... 2 mA

Maximum Output Current Sunk by the SDA Output Pin ..... 25 mA

Total Power Dissipation(1) ..... 400 mW

Package Power Dissipation (T_A = +50°C, T_J = +150°C)
TSSOP-20 ..... 1300 mW
VQFN-20 (5 x 5, ML) ..... 2800 mW

ESD Protection on all Pins ..... ≥ ±6 kV (HBM)
..... ≥ ±400V (MM)
..... ≥ ±2 kV (CDM)

Latch-Up (per JEDEC® JESD78A) at +125°C ..... ±100 mA

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Soldering Temperature of Leads (10 seconds) ..... +300°C

Maximum Junction Temperature (T_J) ..... +150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Power dissipation is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD} - V_{OH}) \times I_{OH}\} + \Sigma(V_{OL} \times I_{OL})$

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise specified)
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF}= +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}	2.7	—	5.5	V	
		1.8	—	2.7	V	Serial interface operational DAC operation with reduced analog specifications
V_{DD} Voltage (Rising) to Ensure Device Power-on Reset	$V_{POR/BOR}$	—	—	1.7	V	RAM retention voltage (V_{RAM}) < V_{POR} V_{DD} voltages greater than the $V_{POR/BOR}$ limit ensure that the device is out of reset
V_{DD} Rise Rate to Ensure Power-on Reset	V_{DDRR}	(**Note 3**)			V/ms	
High-Voltage Commands Voltage Range (HVC Pin)	V_{HV}	V_{SS}	—	12.5	V	The HVC pin will be at one of the three input levels (V_{IL}, V_{IH} or V_{IHH})(1)
High-Voltage Input Entry Voltage	V_{IHHEN}	9.0	—	—	V	Threshold for entry into WiperLock™ Technology
High-Voltage Input Exit Voltage	V_{IHHEX}	—	—	V_{DD} + 0.8V	V	**Note 1**

Note 1 This parameter is ensured by design.

Note 3 POR/BOR voltage trip point is not slope dependent. Hysteresis is implemented with time delay.

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DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified)
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF}= +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Supply Current	I_{DD}	—	—	1.0	mA	Quad	Serial interface active(2) (not High-Voltage Command) V_{OUT} is unloaded, V_{DD} = 5.5V VRnB:VRnA = 10 (4) Volatile DAC register = Midscale I^2C: F_{SCL} = 3.4 MHz
		—	—	1.8	mA	Octal	
		—	—	0.85	µA	Quad	Serial interface inactive(2) (not High-Voltage Command) VRnB:VRnA = All Modes SCL = SDA = V_{SS}, V_{OUT} is unloaded Volatile DAC register = Midscale
		—	—	1.60	µA	Octal	
		—	—	2.5	mA	Quad	EE write current V_{REF} = V_{DD} = 5.5V (after write, serial interface is inactive) write all 7FFh to nonvolatile DAC0 (address 10h), V_{OUT} pins are unloaded.
		—	—	3.0	mA	Octal	
		—	560	700	µA	Quad	HVC = 12.5V (High-Voltage command), serial interface inactive V_{REF} = V_{DD} = 5.5V, $\overline{LAT}$/HVC = V_{IHH} DAC registers = Midscale V_{OUT} pins are unloaded
		—	1100	1300	µA	Octal	
Power-Down Current	I_{DDP}	—	0.68	3.8	µA	PDnB:PDnA = 01(5) V_{OUT} not connected	

Note 2 This parameter is ensured by characterization.

Note 4 Supply current is independent of current through the resistor ladder in mode VRnB:VRnA = 10.

Note 5 The PDnB:PDnA = 00, 10, and 11 configurations should have the same current.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified)
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF}= +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Resistor Ladder Resistance	R_L	100	140	180	kΩ	VRnB:VRnA = 10 V_{REF} = V_{DD}(6)	
Resolution (# of Resistors and # of Taps) (see C.1 "Resolution")	N	256			Taps	8-bit	No missing codes
		1024			Taps	10-bit	No missing codes
		4096			Taps	12-bit	No missing codes
Nominal V_{OUT} Match(11)	$\lvert V_{OUT} - V_{OUTMEAN}\rvert / V_{OUTMEAN}$	—	0.5	1.0	%	2.7V ≤ V_{DD} ≤ 5.5V(2)	
		—	—	1.2	%	1.8V(2)	
V_{OUT} Temperature Coefficient (see C.19 "V_{OUT} Temperature Coefficient")	$\Delta V_{OUT}/\Delta T$	—	15	—	ppm/°C	Code = Midscale (7Fh, 1FFh or 7FFh)	
V_{REF} Pin Input Voltage Range	V_{REF}	V_{SS}	—	V_{DD}	V	1.8V ≤ V_{DD} ≤ 5.5V(1)	

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

Note 6 Resistance is defined as the resistance between the V_{REF} pin (mode VRnB:VRnA = 10) to V_{SS} pin. For octal-channel devices (MCP47FXBX8), this is the effective resistance of each resistor ladder. The resistance measurement is one of the two resistor ladders measured in parallel.

Note 11 Variation of one output voltage to mean output voltage.

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DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified)
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF}= +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Zero-Scale Error (Code = 000h) (see **C.5 "Zero-Scale Error (EZS)"**)	E_{ZS}	—	—	0.75	LSb	8-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		—	—	3	LSb	10-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		—	—	12	LSb	12-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRnB:VRnA = 11, Gx = 0, Gx = 1, V_{REF} = 0.5 × V_{DD} = 2.7, no load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7 – 5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRnB:VRnA = 10, Gx = 0, Gx= 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7 – 5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRnB:VRnA = 00, Gx = 0, V_{REF} = V_{DD} = 2.7–5.5V, no load
Full-Scale Error (see **C.4 "Full-Scale Error (EFS)"**)	E_{FS}	—	—	4.5	LSb	8-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		—	—	18	LSb	10-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		—	—	70	LSb	12-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRnB:VRnA = 11, Gx = 0, Gx = 1, V_{REF} = 0.5 × V_{DD} = 2.7, no load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7 – 5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7 – 5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRnB:VRnA = 00, Gx = 0, V_{REF} = V_{DD} = 2.7 – 5.5V, no load
Offset Error (see **C.7 "Offset Error (EOS)"**)	E_{OS}	-15	±1.5	+15	mV	VRnB:VRnA = 00, Gx = 0, no load	
Offset Voltage Temperature Coefficient	V_{OSTC}	—	±10	—	µV/°C		

Note 2 This parameter is ensured by characterization.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified)
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF}= +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Gain Error (see **C.9 "Gain Error (EG)"**)(8)	E_G	-1.0	±0.1	+1.0	% of FSR	8-bit	Code = 250, no load VRnB:VRnA = 00, Gx = 0
		-1.0	±0.1	+1.0	% of FSR	10-bit	Code = 1000, no load VRnB:VRnA = 00, Gx = 0
		-1.0	±0.1	+1.0	% of FSR	12-bit	Code = 4000, no load VRnB:VRnA = 00, Gx = 0
Gain Error Drift (see **C.10 "Gain Error Drift (EGD)"**)	ΔG/°C	—	-3	—	ppm/°C		
Total Unadjusted Error (see **C.6 "Total Unadjusted Error (ET)"**)(2)	E_T	-2.5	—	+0.5	LSb	8-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		-10.0	—	+2.0	LSb	10-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		-40.0	—	+8.0	LSb	12-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0 "Typical Performance Curves"**(2)					VRnB:VRnA = 11, Gx = 0, Gx = 1, V_{REF} = 0.5 × V_{DD} = 2.7, no load
		See **Section 2.0 "Typical Performance Curves"**(2)					VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7 – 5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(2)					VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7 – 5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(2)					VRnB:VRnA = 00, Gx = 0, V_{REF} = V_{DD} = 2.7 – 5.5V, no load

Note 2 This parameter is ensured by characterization.

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DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified)
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF}= +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Integral Nonlinearity (see **C.11 "Integral Nonlinearity (INL)"**)(7, 10)	INL	-0.5	±0.1	+0.5	LSb	8-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		-1.5	±0.4	+1.5	LSb	10-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		-6	±1.5	+6	LSb	12-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRnB:VRnA = 11, Gx = 0, Gx = 1, V_{REF} = 0.5 × V_{DD} = 2.7, no load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7 – 5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7 – 5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(2)			LSb		VRnB:VRnA = 00, Gx = 0, V_{REF} = V_{DD} = 2.7 – 5.5V, no load

Note 2 This parameter is ensured by characterization.

Note 7 INL and DNL are measured at V_{OUT} with V_{RL} = V_{DD} (VRnB:VRnA = 00).

Note 10 Code range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, 100 to 4000.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified)
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF}= +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Differential Nonlinearity (see **C.12 "Differential Nonlinearity (DNL)"**)[7, 10]	DNL	-0.25	±0.0125	+0.25	LSb	8-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		-0.5	±0.05	+0.5	LSb	10-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		-1.0	±0.2	+1.0	LSb	12-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		VRnB:VRnA = 11, Gx = 0, Gx = 1, V_{REF} = 0.5 × V_{DD} = 2.7, no load
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7 – 5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7 – 5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**[2]			LSb		VRnB:VRnA = 00, Gx = 0 V_{REF} = V_{DD} = 2.7 – 5.5V, no load

Note 2 This parameter is ensured by characterization.

Note 7 INL and DNL are measured at V_{OUT} with V_{RL} = V_{DD} (VRnB:VRnA = 00).

Note 10 Code range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, 100 to 4000.

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DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified)
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF}= +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
-3 dB Bandwidth (see **C.16 "-3 dB Bandwidth"**)	BW	—	86.5	—	kHz	V_{REF} = 2.048V ± 0.1V, VRnB:VRnA = 10, Gx = 0	
		—	67.7	—	kHz	V_{REF} = 2.048V ± 0.1V, VRnB:VRnA = 10, Gx = 1	
Output Amplifier							
Minimum Output Voltage	$V_{OUT(MIN)}$	—	0.01	—	V	1.8V ≤ V_{DD} < 5.5V, Output Amplifier's minimum drive	
Maximum Output Voltage	$V_{OUT(MAX)}$	—	V_{DD} – 0.016	—	V	1.8V ≤ V_{DD} < 5.5V, Output Amplifier's maximum drive	
Phase Margin	PM	—	58	—	°C	C_L = 400 pF, R_L = ∞	
Slew Rate[9]	SR	—	0.44	—	V/µs	R_L = 5 kΩ	
Short-Circuit Current	I_{SC}	3	9	22	mA	Short to V_{SS}	DAC code = Full Scale
		3	9	22	mA	Short to V_{DD}	DAC code = 000h
Internal Band Gap							
Band Gap Voltage	V_{BG}	1.18	1.22	1.26	V		
Band Gap Voltage Temperature Coefficient	V_{BGTC}	—	15	—	ppm/°C		
Operating Range	V_{DD}	2.0	—	5.5	V	V_{REF} pin voltage stable	
		2.2	—	5.5	V	V_{OUT} output linear	
External Reference (V_{REF})							
Input Range[1]	V_{REF}	V_{SS}	—	V_{DD} – 0.04	V	VRnB:VRnA = 11 (Buffered mode)	
		V_{SS}	—	V_{DD}	V	VRnB:VRnA = 10 (Unbuffered mode)	
Input Capacitance	C_{REF}	—	1	—	pF	VRnB:VRnA = 10 (Unbuffered mode)	
Total Harmonic Distortion[1]	THD	—	-64	—	dB	V_{REF} = 2.048V ± 0.1V, VRnB:VRnA = 10, Gx = 0, Frequency = 1 kHz	
Dynamic Performance							
Major Code Transition Glitch (see **C.14 "Major Code Transition Glitch"**)	—	—	45	—	nV-s	1 LSb change around major carry (7FFh to 800h)	
Digital Feedthrough (see **C.15 "Digital Feed-through"**)	—	—	< 10	—	nV-s		

Note 1 This parameter is ensured by design.

Note 9 Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in a 12-bit device).

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified)
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF}= +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Digital Inputs/Outputs ($\overline{LAT0}$, $\overline{LAT1}$, HVC)						
Schmitt Trigger High Input Threshold	V_{IH}	0.7 V_{DD}	—	—	V	2.7V ≤ V_{DD} ≤ 5.5V (allows 2.7V digital V_{DD} with 5V analog V_{DD})
		0.7 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 2.7V
Schmitt Trigger Low Input Threshold	V_{IL}	—	—	0.3 V_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.1 V_{DD}	—	V	
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD} and V_{IN} = V_{SS}
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 3.4 MHz
Digital Interface (SDA, SCL)						
Output Low Voltage	V_{OL}	—	—	0.4	V	V_{DD} ≥ 2.0V, I_{OL} = 3 mA
		—	—	0.2 V_{DD}	V	V_{DD} < 2.0V, I_{OL} = 1 mA
Input High Voltage (SDA and SCL Pins)	V_{IH}	0.7 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 5.5V
Input Low Voltage (SDA and SCL Pins)	V_{IL}	—	—	0.3 V_{DD}	V	1.8V ≤ V_{DD} ≤ 5.5V
Input Leakage	I_{LI}	-1	—	1	µA	SCL = SDA = V_{SS} or SCL = SDA = V_{DD}
Pin Capacitance	C_{PIN}	—	10	—	pF	f_C = 3.4 MHz

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DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified)
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF}= +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
RAM Value							
Value Range	N	0h	—	FFh	Hex	8-bit	
		0h	—	3FFh	Hex	10-bit	
		0h	—	FFFh	Hex	12-bit	
DAC Register POR/BOR Value	N	See Table 4-2			Hex	8-bit	
		See Table 4-2			Hex	10-bit	
		See Table 4-2			Hex	12-bit	
PDCON Initial Factory Setting	N	See Table 4-2			Hex		
EEPROM							
Endurance	EN_{EE}	—	1M	—	Cycles	Note 1, Note 2	
Data Retention	DR_{EE}	—	200	—	Years	At +25°C(1, 2)	
EEPROM Range	N	0h	—	FFh	Hex	8-bit	DACn register(s)
		0h	—	3FFh	Hex	10-bit	DACn register(s)
		0h	—	FFFh	Hex	12-bit	DACn register(s)
Initial Factory Setting	N	See Table 4-2					
EEPROM Programming Write Cycle Time	t_{WC}	—	11	16	ms	V_{DD} = +1.8V to 5.5V	
Power Requirements							
Power Supply Sensitivity (C.17 "Power-Supply Sensitivity (PSS)")	PSS	—	0.002	0.005	%/%	8-bit	Code = 7Fh
		—	0.002	0.005	%/%	10-bit	Code = 1FFh
		—	0.002	0.005	%/%	12-bit	Code = 7FFh

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

DC Notes:

1. This parameter is ensured by design.
2. This parameter is ensured by characterization.
3. POR/BOR voltage trip point is not slope dependent. Hysteresis is implemented with time delay.
4. Supply current is independent of current through the resistor ladder in mode VRnB:VRnA = `10`.
5. The PDnB:PDnA = `00`, `10`, and `11` configurations should have the same current.
6. Resistance is defined as the resistance between the V_{REF} pin (mode VRnB:VRnA = `10`) to V_{SS} pin. For octal-channel devices (MCP47FXBX8), this is the effective resistance of each resistor ladder. The resistance measurement is one of the two resistor ladders measured in parallel.
7. INL and DNL are measured at V_{OUT} with V_{RL} = V_{DD} (VRnB:VRnA = `00`).
8. This gain error does not include offset error.
9. Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in a 12-bit device).
10. Code range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, 100 to 4000.
11. Variation of one output voltage to mean output voltage.

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1.1 Timing Waveforms and Requirements

1.1.1 WIPER SETTLING TIME

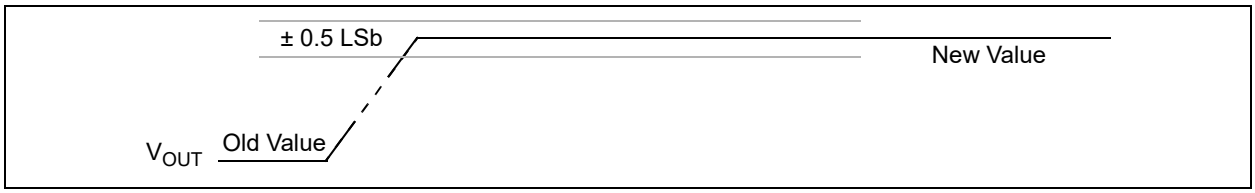

FIGURE 1-1: *V_{OUT} Settling Time Waveforms.*

TABLE 1-1: WIPER SETTLING TIMING

Timing Characteristics		Standard Operating Conditions (unless otherwise specified): Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +1.8V to 5.5V, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
V_{OUT} Settling Time (±0.5 LSb Error Band, C_L = 100 pF) (see **C.13 "Settling Time"**)	t_S	—	7.8	—	µs	12-bit	Code = 400h → C00h; C00h → 400h(1)

Note 1: Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR.

1.1.2 LATCH PIN ($\overline{LAT}$) TIMING

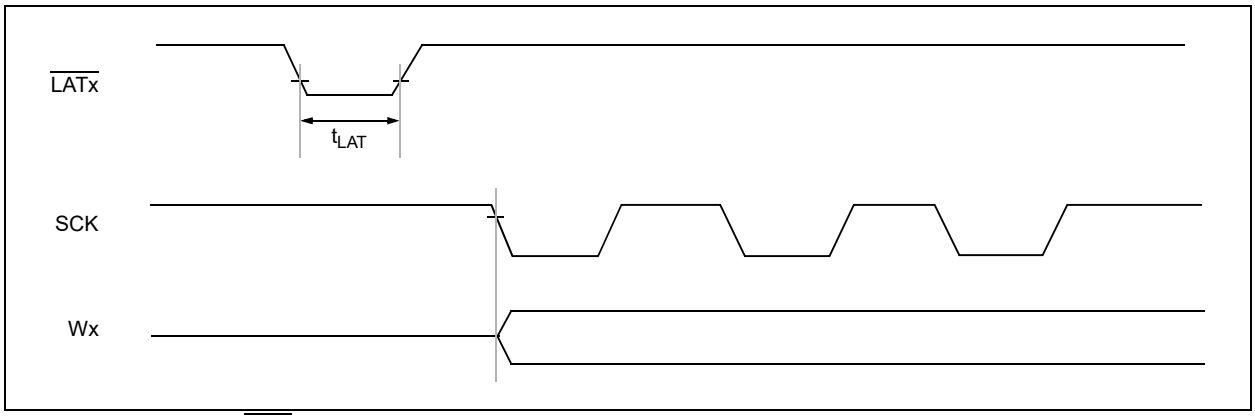

FIGURE 1-2: *$\overline{LAT}$ Pin Waveforms.*

TABLE 1-2: $\overline{LAT}$ PIN TIMING

Timing Characteristics		Standard Operating Conditions (unless otherwise specified): Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, RL = 2 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
$\overline{LAT}$x Pin Pulse Width	t_{LAT}	20	—	—	ns	

1.1.3 RESET AND POWER-DOWN TIMING

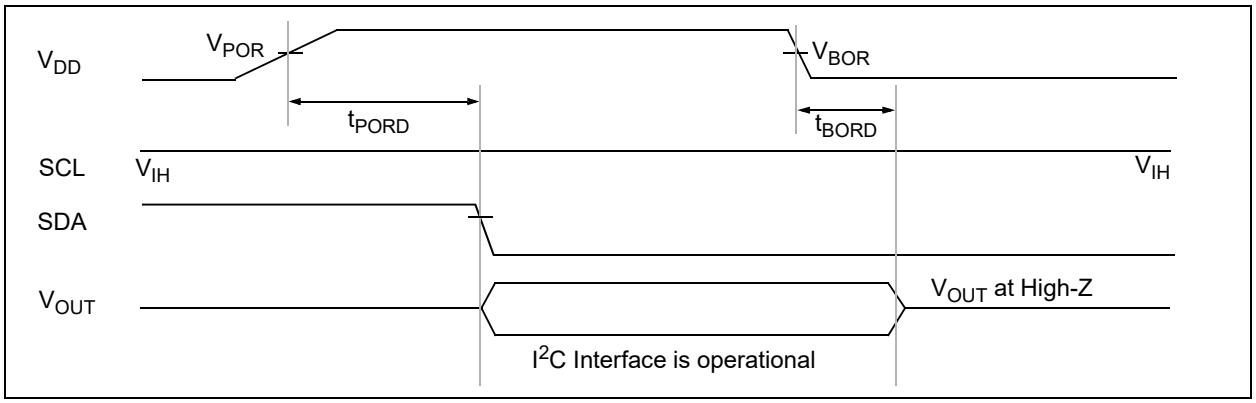

FIGURE 1-3: *Power-on and Brown-out Reset Waveforms.*

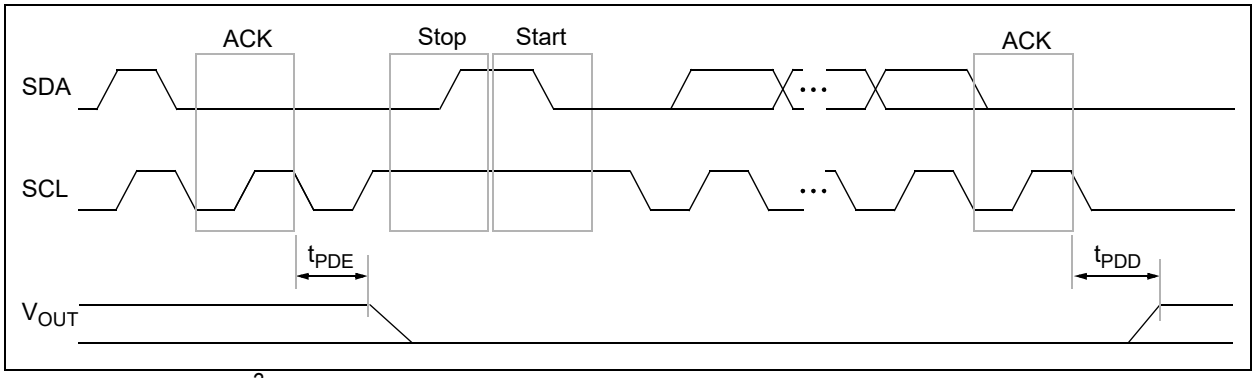

FIGURE 1-4: *I^2C Power-Down Command Waveforms.*

TABLE 1-3: RESET AND POWER-DOWN TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{SS} = 0V R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power-on Reset Delay	t_{PORD}	—	60	—	µs	
Brown-out Reset Delay	t_{BORD}	—	45	—	µs	V_{DD} transitions from $V_{DD(MIN)}$ → > V_{POR} V_{OUT} driven to V_{OUT} disabled
Power-Down DAC Output Disable Time Delay	T_{PDE}	—	10.5	—	µs	PDnB:PDnA = `00` → `11`, `10` or `01` started from the falling edge of the SCL at the end of the 8th clock cycle, V_{OUT} = V_{OUT} – 10 mV. V_{OUT} not connected.
Power-Down DAC Output Enable Time Delay	T_{PDD}	—	1	—	µs	PDnB:PDnA = `11`, `10` or `01` -> `00` started from the falling edge of the SCL at the end of the 8th clock cycle. Volatile DAC Register = FFh, V_{OUT} = 10 mV. V_{OUT} not connected.

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1.2 I²C Mode Timing Waveforms and Requirements

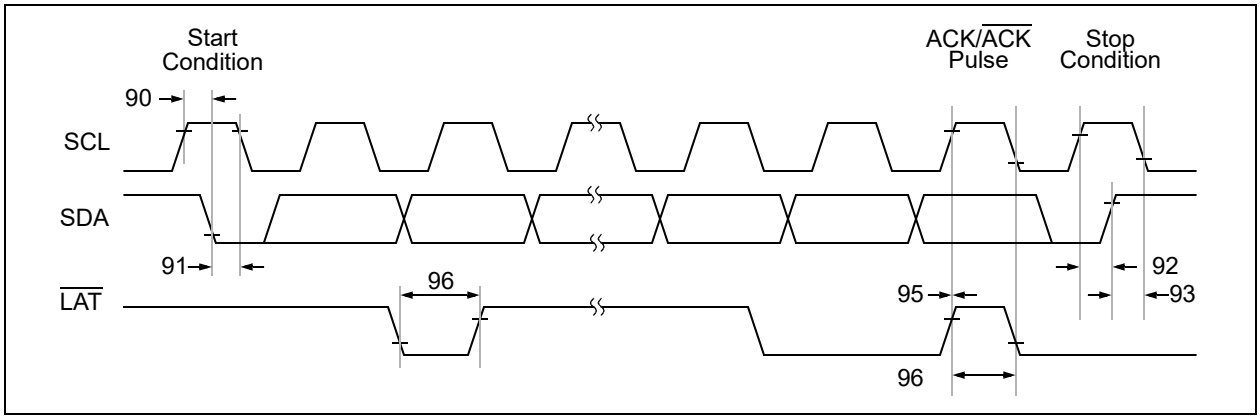

FIGURE 1-5: *I²C Bus Start/Stop Bits and LAT Timing Waveforms.*

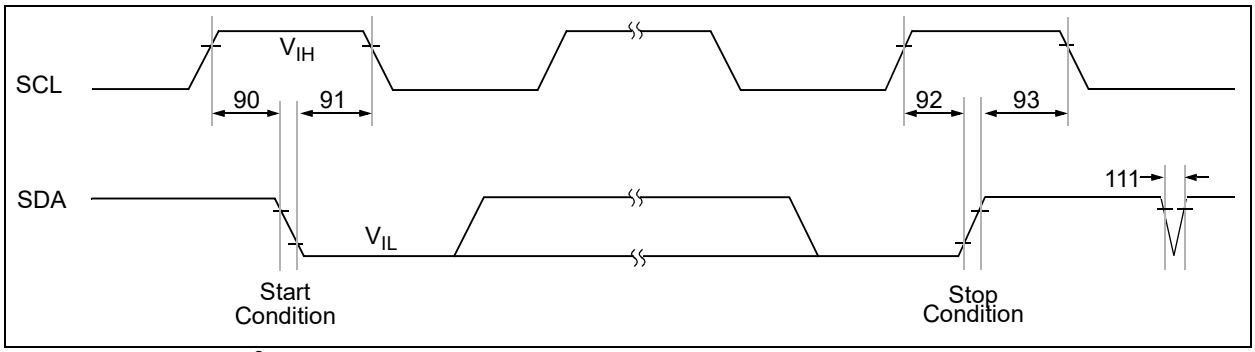

FIGURE 1-6: *I²C Bus Start/Stop Bits Timing Waveforms.*

TABLE 1-4: I²C BUS START/STOP BITS AND $\overline{LAT}$ REQUIREMENTS

I²C AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) The operating voltage range is described in **DC Characteristics**.				
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
—	F_{SCL}		Standard mode	0	100	kHz	C_b = 400 pF, 1.8V - 5.5V(2)
			Fast mode	0	400	kHz	C_b = 400 pF, 2.7V - 5.5V
			High-Speed 1.7	0	1.7	MHz	C_b = 400 pF, 4.5V - 5.5V
			High-Speed 3.4	0	3.4	MHz	C_b = 100 pF, 4.5V - 5.5V
D102	C_b	Bus Capacitive Loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
			1.7 MHz mode	—	400	pF	
			3.4 MHz mode	—	100	pF	
90	$T_{SU:STA}$	Start condition Setup time (only relevant for repeated Start condition)	100 kHz mode	4700	—	ns	**Note 2**
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
91	$T_{HD:STA}$	Start condition Hold time (after this period, the first clock pulse is generated)	100 kHz mode	4000	—	ns	**Note 2**
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
92	$T_{SU:STO}$	Stop condition Setup time	100 kHz mode	4000	—	ns	**Note 2**
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
93	$T_{HD:STO}$	Stop condition Hold time	100 kHz mode	4000	—	ns	**Note 2**
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
95	T_{LATHD}	SCL ↑ to $\overline{LAT}$↑ (write data ACK bit) Hold Time		250	—	ns	Write data delayed(3)
96	T_{LAT}	$\overline{LAT}$ High or Low time		50	—	ns	

Note 2 Not Tested. This parameter is ensured by characterization.

Note 3 The transition of the LAT signal between 10 ns before the rising edge (Spec 94) and 250 ns after the rising edge (Spec 95) of the SCL signal is indeterminate whether the change in V_{OUT} is delayed or not.

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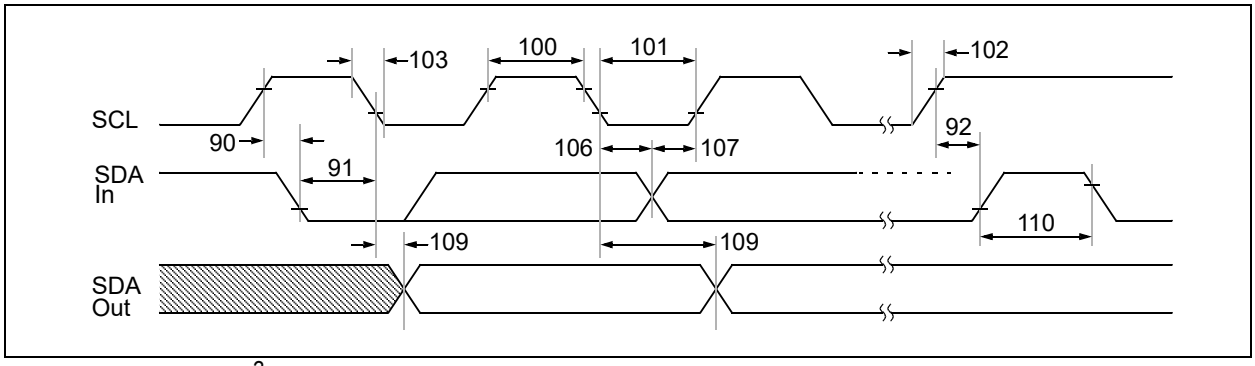

FIGURE 1-7: *I²C Bus Timing Waveforms.*

I²C BUS REQUIREMENTS (SLAVE MODE)

I²C AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) The operating voltage range is described in **DC Characteristics**.			
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
100	T_{HIGH}	Clock High Time	100 kHz mode	4000	—	ns	1.8V-5.5V(2)
			400 kHz mode	600	—	ns	2.7V-5.5V
			1.7 MHz mode	120	—	ns	4.5V-5.5V
			3.4 MHz mode	60	—	ns	4.5V-5.5V
101	T_{LOW}	Clock Low Time	100 kHz mode	4700	—	ns	1.8V-5.5V(2)
			400 kHz mode	1300	—	ns	2.7V-5.5V
			1.7 MHz mode	320	—	ns	4.5V-5.5V
			3.4 MHz mode	160	—	ns	4.5V-5.5V
102A(2)	T_{RSCL}	SCL Rise Time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)
			400 kHz mode	20 + 0.1C_b	300	ns	
			1.7 MHz mode	20	80	ns	
			1.7 MHz mode	20	160	ns	After a repeated Start condition or an Acknowledge bit
			3.4 MHz mode	10	40	ns	
			3.4 MHz mode	10	80	ns	After a repeated Start condition or an Acknowledge bit
102B(2)	T_{RSDA}	SDA Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)
			400 kHz mode	20 + 0.1C_b	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	

Note 2 Not Tested. This parameter is ensured by characterization.

I²C BUS REQUIREMENTS (SLAVE MODE) (CONTINUED)

I²C AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) The operating voltage range is described in **DC Characteristics**.			
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
103A(2)	T_{FSCL}	SCL Fall Time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)(4)
			400 kHz mode	20 + 0.1C_b	300	ns	
			1.7 MHz mode	20	80	ns	
			3.4 MHz mode	10	40	ns	
103B(2)	T_{FSDA}	SDA Fall Time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)(4)
			400 kHz mode	20 + 0.1C_b	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	
106	$T_{HD:DAT}$	Data Input Hold Time	100 kHz mode	0	—	ns	1.8V-5.5V(2, 5)
			400 kHz mode	0	—	ns	2.7V-5.5V(5)
			1.7 MHz mode	0	—	ns	4.5V-5.5V(5)
			3.4 MHz mode	0	—	ns	4.5V-5.5V(5)
107	$T_{SU:DAT}$	Data Input Setup Time	100 kHz mode	250	—	ns	**Note 2**, **Note 6**
			400 kHz mode	100	—	ns	**Note 6**
			1.7 MHz mode	10	—	ns	
			3.4 MHz mode	10	—	ns	
109	T_{AA}	Output Valid from Clock	100 kHz mode	—	3450	ns	**Note 2**, **Note 7**
			400 kHz mode	—	900	ns	**Note 7**
			1.7 MHz mode	—	150	ns	C_b = 100 pF(7, 8)
				—	310	ns	C_b = 400 pF(2, 7)
			3.4 MHz mode	—	150	ns	C_b = 100 pF(7)
110	T_{BUF}	Bus Free Time	100 kHz mode	4700	—	ns	Time when the bus must be free before a new transmission can start(2)
			400 kHz mode	1300	—	ns	
			1.7 MHz mode	N.A.	—	ns	
			3.4 MHz mode	N.A.	—	ns	
111	T_{SP}	Input Filter Spike Suppression (SDA and SCL)	100 kHz mode	—	50	ns	NXP Spec states N.A.(2)
			400 kHz mode	—	50	ns	
			1.7 MHz mode	—	10	ns	Spike suppression
			3.4 MHz mode	—	10	ns	Spike suppression

Note 2 Not Tested. This parameter is ensured by characterization.

Note 4 Use Cb in pF for the calculations.

Note 5 A master transmitter must provide a delay to ensure that the difference between SDA and SCL fall times does not unintentionally create a Start or Stop condition.

Note 6 A Fast mode (400 kHz) I²C bus device can be used in a standard mode (100 kHz) I²C bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line, T_R max. + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard mode I²C bus specification) before the SCL line is released.

Note 7 As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

Note 8 Ensured by the T_{AA} 3.4 MHz specification test.

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Timing Table Notes:

1. Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12- bit device).
2. Not Tested. This parameter is ensured by characterization.
3. The transition of the $\overline{LAT}$ signal between 10 ns before the rising edge (Spec 94) and 250 ns after the rising edge (Spec 95) of the SCL signal is indeterminate whether the change in V_{OUT} is delayed or not.
4. Use C_b in pF for the calculations.
5. A master transmitter must provide a delay to ensure that the difference between SDA and SCL fall times does not unintentionally create a Start or Stop condition.
6. A Fast mode (400 kHz) I^2C bus device can be used in a standard mode (100 kHz) I^2C bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line, T_R max. + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard mode I^2C bus specification) before the SCL line is released.
7. As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
8. Ensured by the T_{AA} 3.4 MHz specification test.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 20L-TSSOP	θ_{JA}	—	90	—	°C/W	
Thermal Resistance, 20L-VQFN (5 x 5, P8X)	θ_{JA}	—	36.1	—	°C/W	

Note 1: Operation in this range must not cause T_J to exceed the Maximum Junction Temperature of +150°C.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

2.1 Electrical Data

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

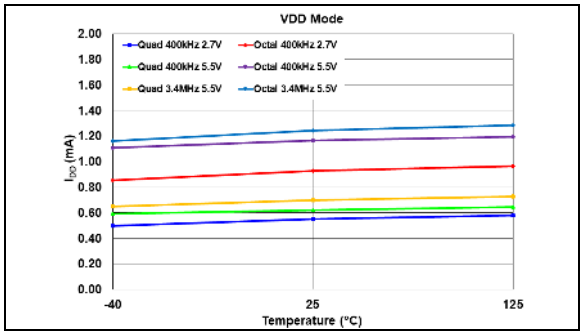

FIGURE 2-1: *Average Device Supply Current vs. F_{SCL} Frequency, Voltage and Temperature - Active Interface, VRnB:VRnA = 00, (V_{DD} Mode).*

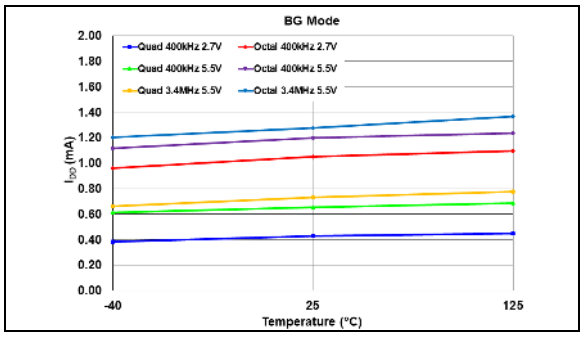

FIGURE 2-2: *Average Device Supply Current vs. F_{SCL} Frequency, Voltage and Temperature - Active Interface, VRnB:VRnA = 01 (Band Gap Mode).*

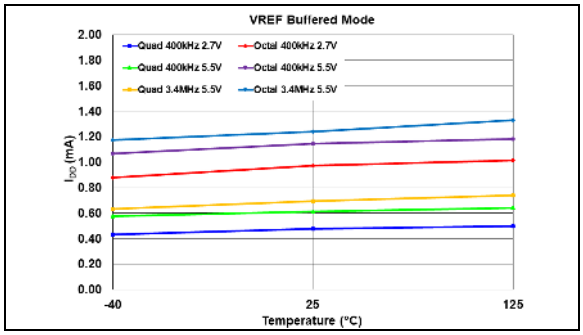

FIGURE 2-3: *Average Device Supply Current vs. F_{SCL} Frequency, Voltage and Temperature - Active Interface, VRnB:VRnA = 11 (V_{REF} Buffered Mode).*

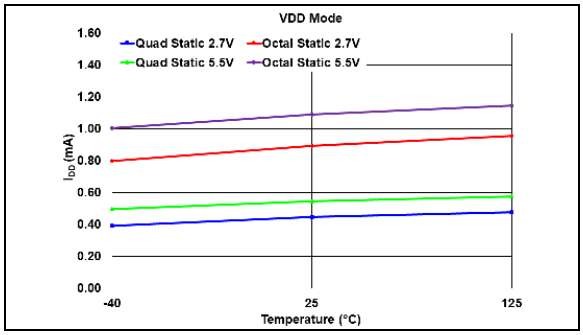

FIGURE 2-4: *Average Device Supply Current - Inactive Interface (SCL = V_{IH} or V_{IL}) vs. Voltage and Temperature, VRnB:VRnA = 00 (V_{DD} Mode).*

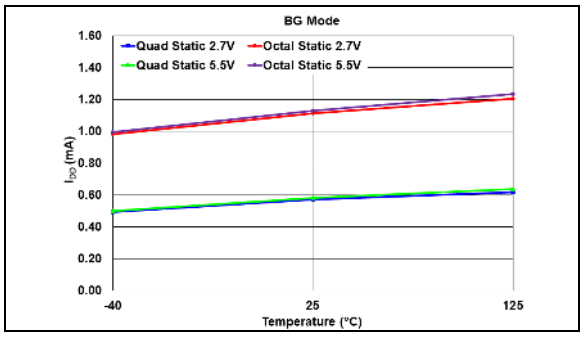

FIGURE 2-5: *Average Device Supply Current - Inactive Interface (SCL = V_{IH} or V_{IL}) vs. Voltage and Temperature, VRnB:VRnA = 01 (Band Gap Mode).*

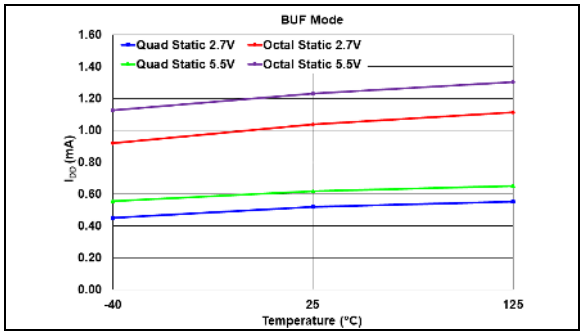

FIGURE 2-6: *Average Device Supply Current - Inactive Interface (SCL = V_{IH} or V_{IL}) vs. Voltage and Temperature, VRnB:VRnA = 11 (V_{REF} Buffered Mode).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

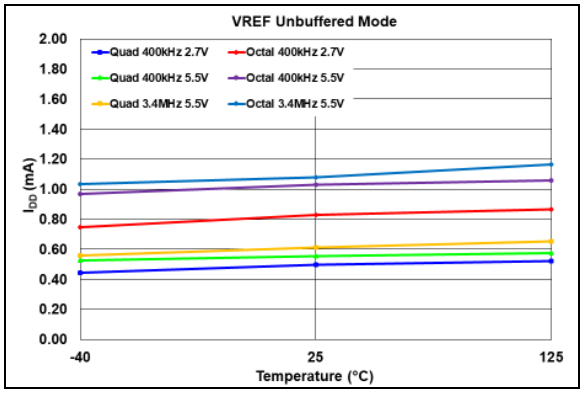

FIGURE 2-7: *Average Device Supply Current vs. F_{SCL} Frequency, Voltage and Temperature - Active Interface, VRnB:VRnA = 10 (V_{REF} Unbuffered Mode).*

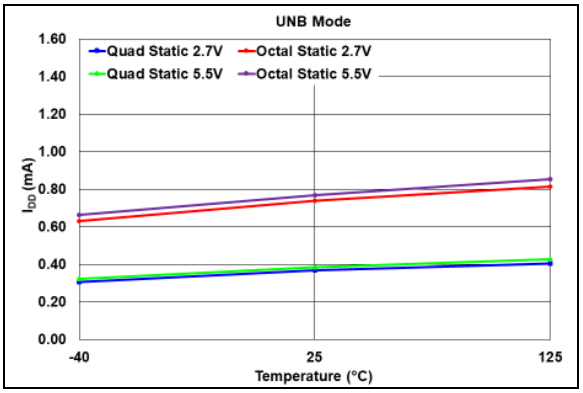

FIGURE 2-9: *Average Device Supply Current - Inactive Interface (SCL = V_{IH} or V_{IL}) vs. Voltage and Temperature, VRnB:VRnA = 10 (V_{REF} Unbuffered Mode).*

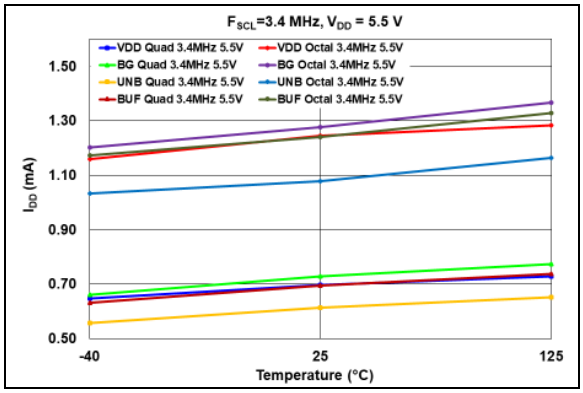

FIGURE 2-8: *Average Device Supply Active Current (I_{DDA}) (at 5.5V and F_{SCL} = 3.4 MHz) vs. Temperature and DAC Reference Voltage Mode.*

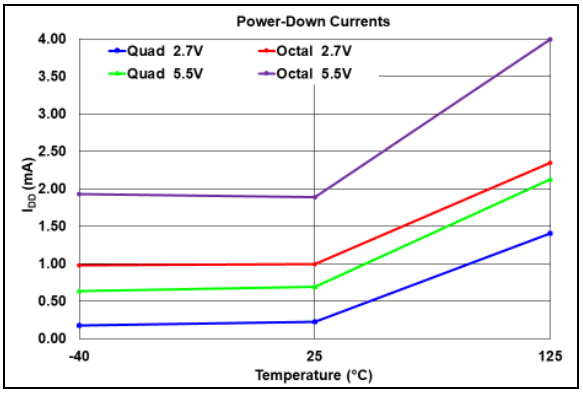

FIGURE 2-10: *Power-Down Currents.*

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2.2 Linearity Data

2.2.1 TOTAL UNADJUSTED ERROR (TUE) - MCP47FXB28 (12-BIT), $V_{REF} = V_{DD}$ (VRNB:VRNA = 00), GAIN = 1X, CODE 100-4000

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V

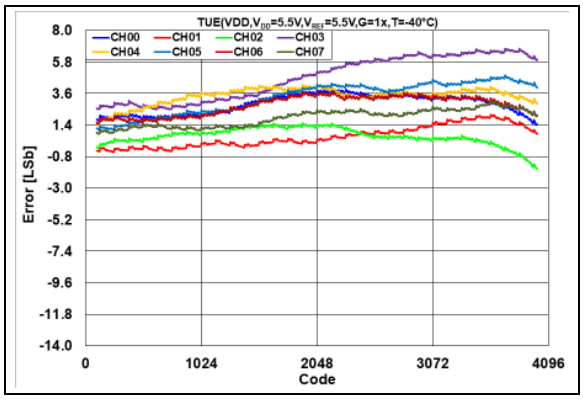

FIGURE 2-11: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

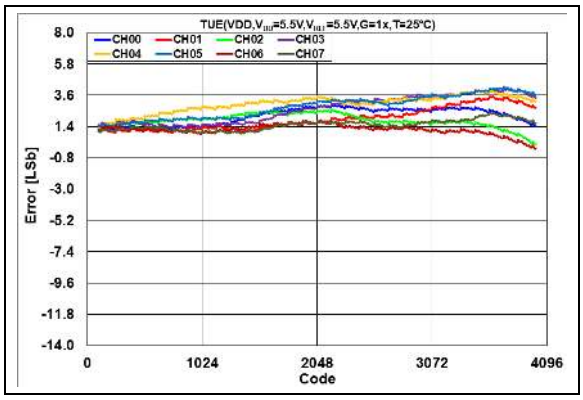

FIGURE 2-12: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

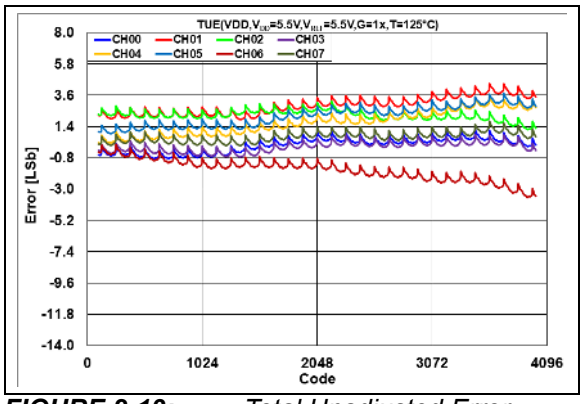

FIGURE 2-13: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

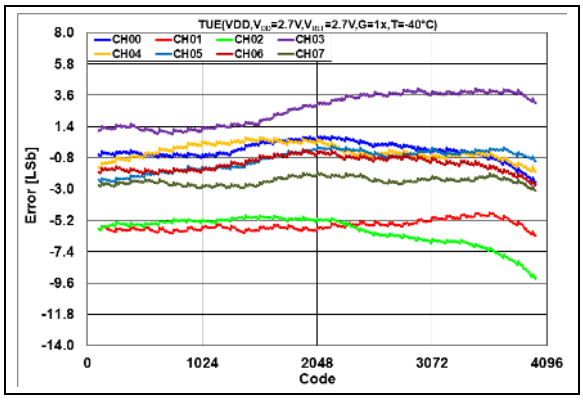

FIGURE 2-14: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

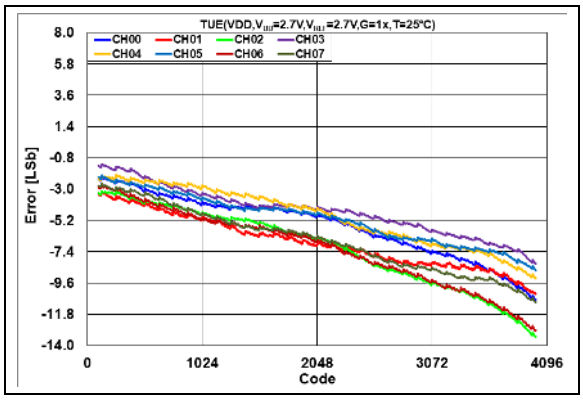

FIGURE 2-15: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

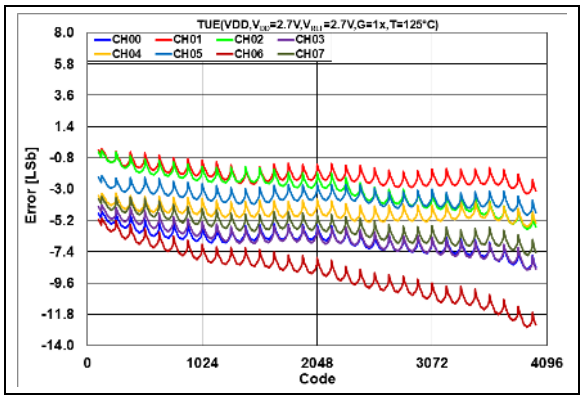

FIGURE 2-16: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.2 INTEGRAL NONLINEARITY (INL) - MCP47FXB28 (12-BIT), $V_{REF} = V_{DD}$ (VRNB:VRNA = 00), GAIN = 1X, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

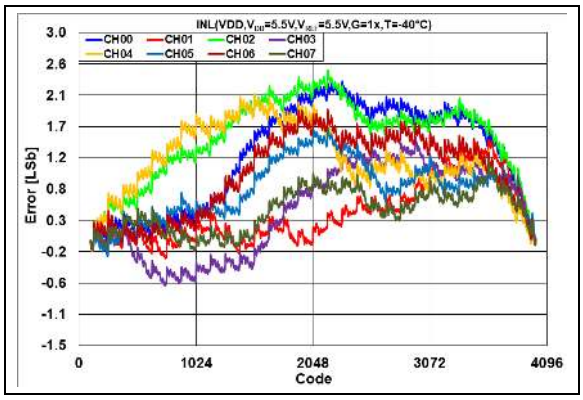

FIGURE 2-17: *INL Error vs. DAC Code, T = 40°C, V_{DD} = 5.5V.*

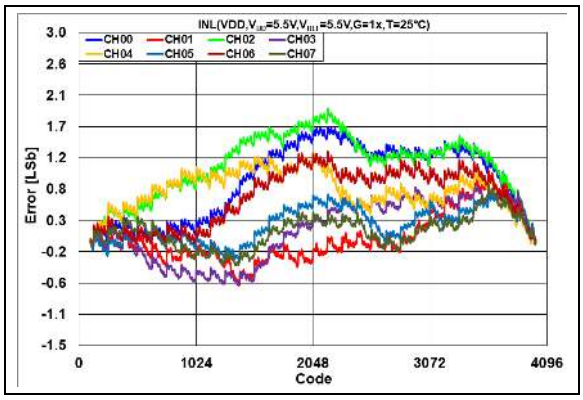

FIGURE 2-18: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

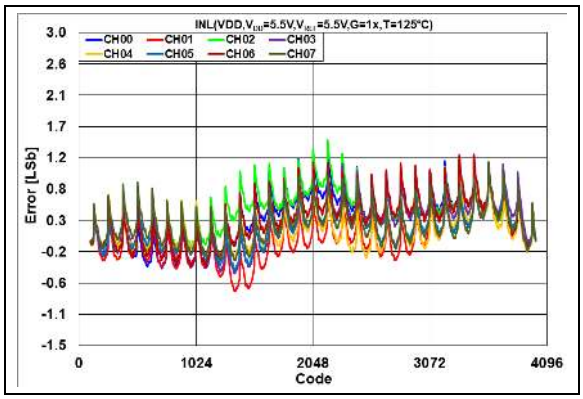

FIGURE 2-19: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

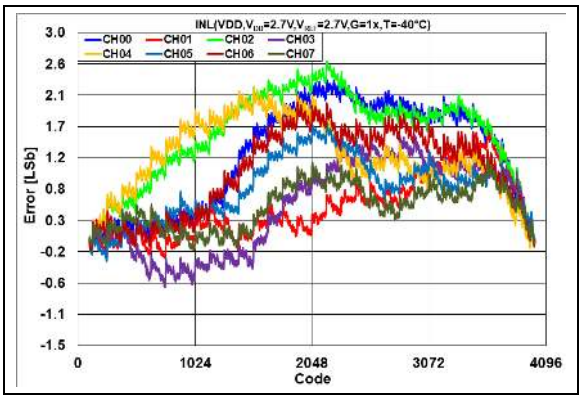

FIGURE 2-20: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

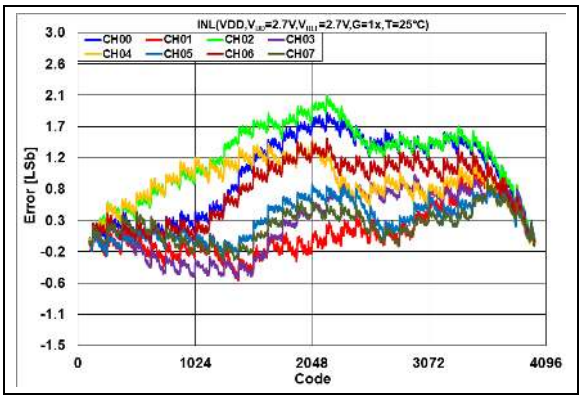

FIGURE 2-21: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

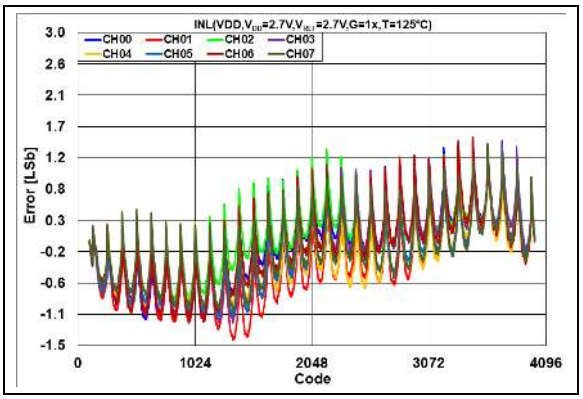

FIGURE 2-22: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

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2.2.3 DIFFERENTIAL NONLINEARITY (DNL) - MCP47FXB28 (12-BIT), $V_{REF} = V_{DD}$ (VRNB:VRNA = 00), GAIN = 1X, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

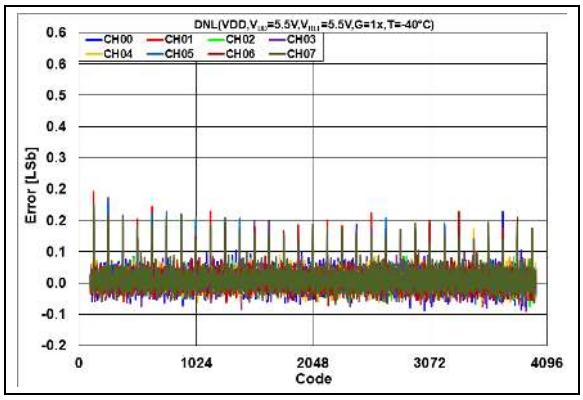

FIGURE 2-23: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

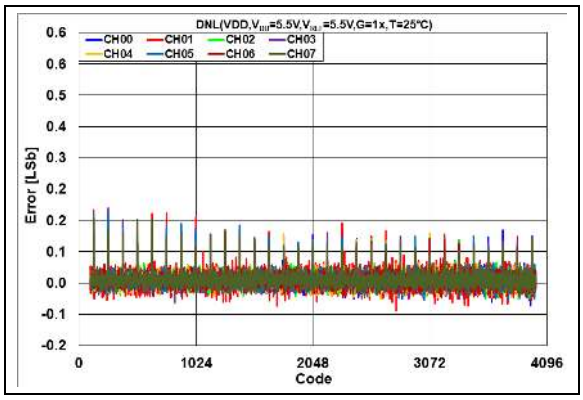

FIGURE 2-24: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

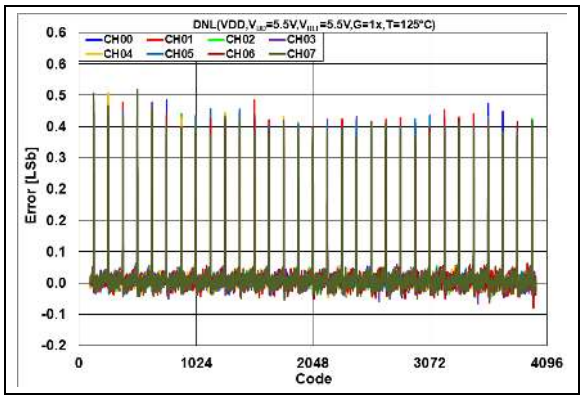

FIGURE 2-25: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

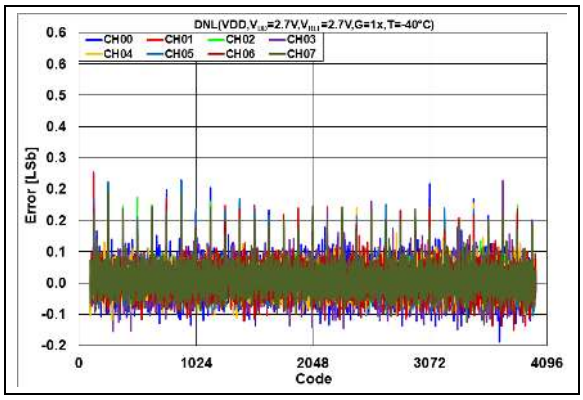

FIGURE 2-26: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

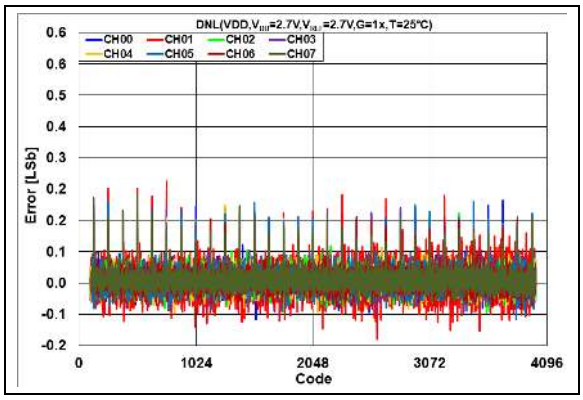

FIGURE 2-27: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

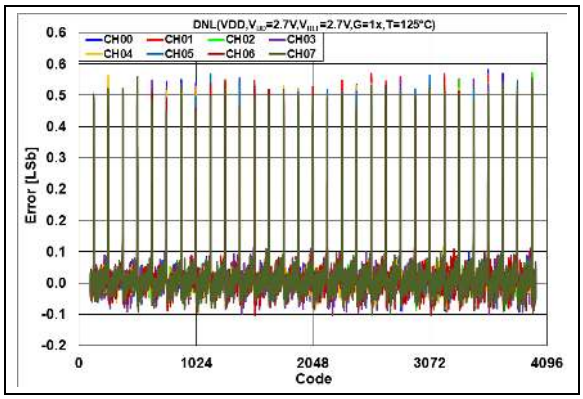

FIGURE 2-28: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.4 TOTAL UNADJUSTED ERROR (TUE) - MCP47FXB28 (12-BIT), BANDGAP MODE (VRNB:VRNA = 01), GAIN = 2X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

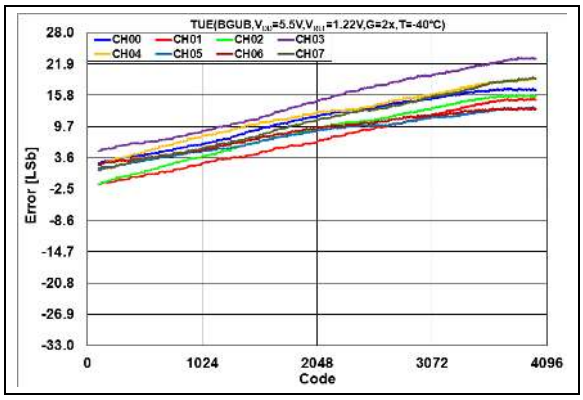

FIGURE 2-29: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

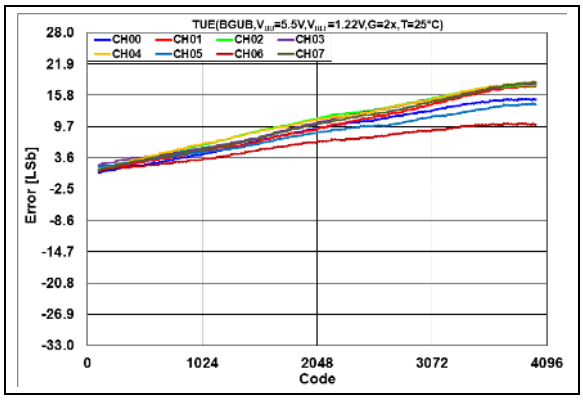

FIGURE 2-30: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

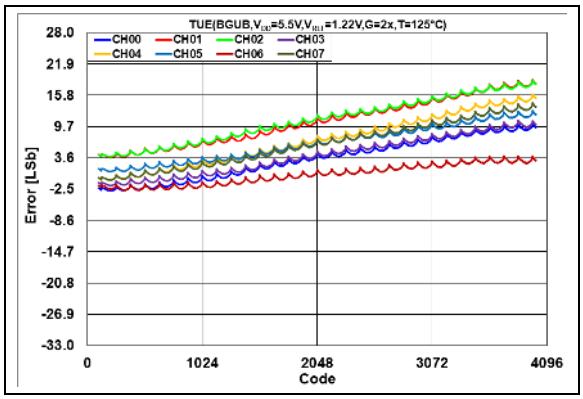

FIGURE 2-31: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

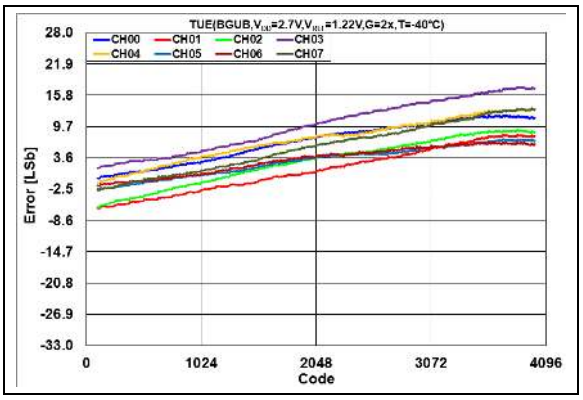

FIGURE 2-32: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

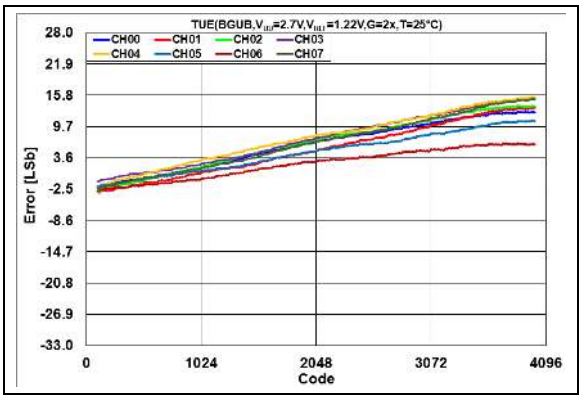

FIGURE 2-33: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

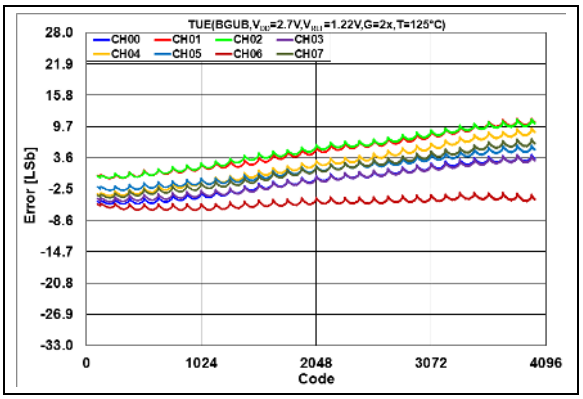

FIGURE 2-34: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

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2.2.5 TOTAL UNADJUSTED ERROR (TUE) - MCP47FXB28 (12-BIT), BAND GAP MODE (VRNB:VRNA = 01), GAIN = 4X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

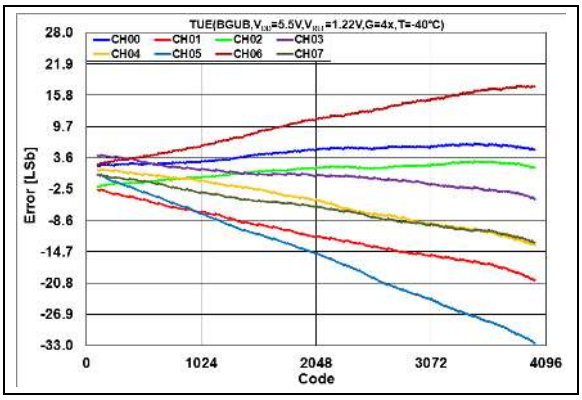

FIGURE 2-35: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

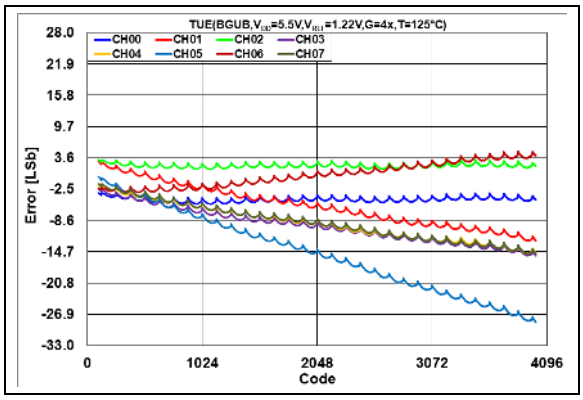

FIGURE 2-37: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

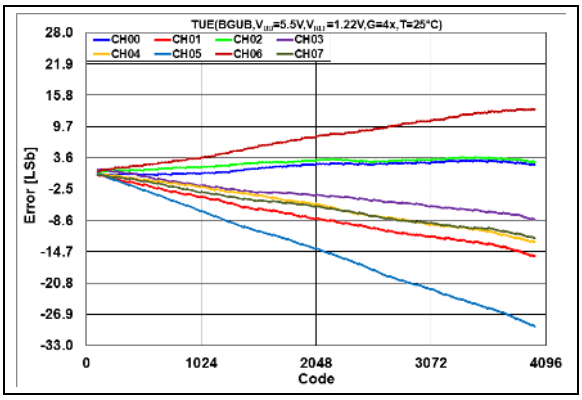

FIGURE 2-36: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

2.2.6 INTEGRAL NONLINEARITY (INL) - MCP47FXB28 (12-BIT), BAND GAP MODE (VRNB:VRNA = 01), GAIN = 2X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

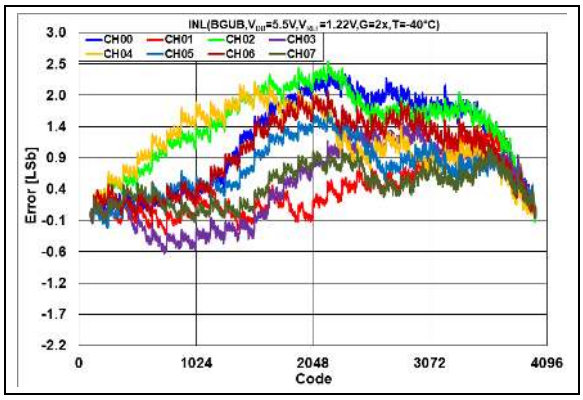

FIGURE 2-38: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

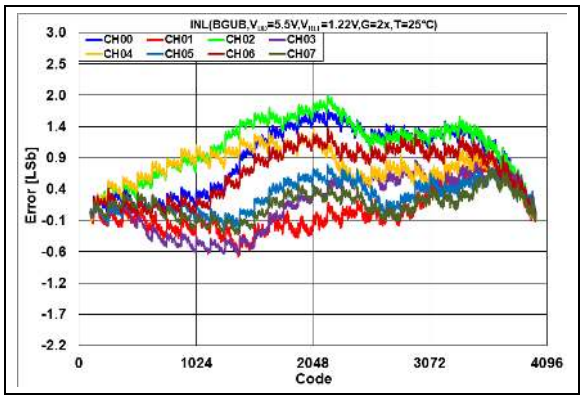

FIGURE 2-39: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

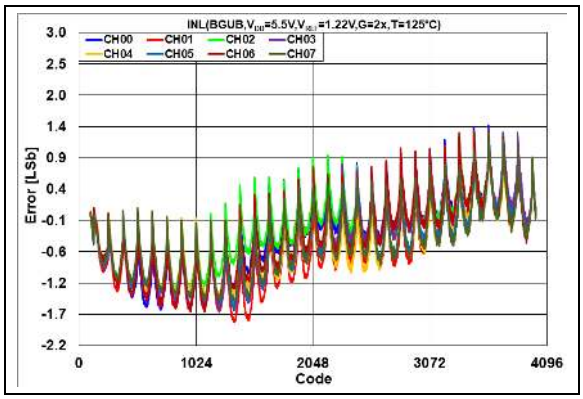

FIGURE 2-40: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

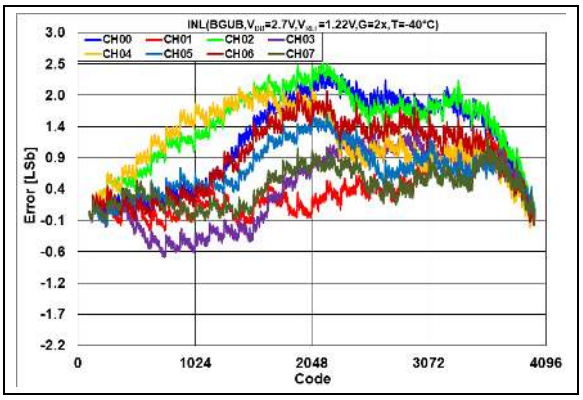

FIGURE 2-41: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

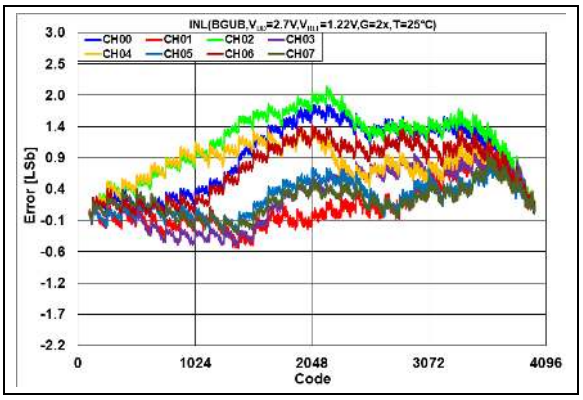

FIGURE 2-42: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

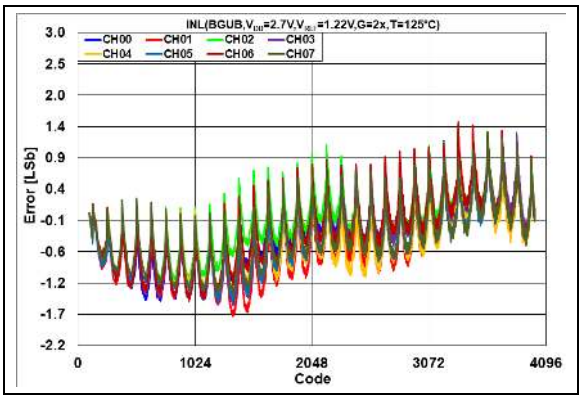

FIGURE 2-43: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

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2.2.7 INTEGRAL NONLINEARITY (INL) - MCP47FXB28 (12-BIT), BAND GAP MODE (VRNB:VRNA = 01), GAIN = 4X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

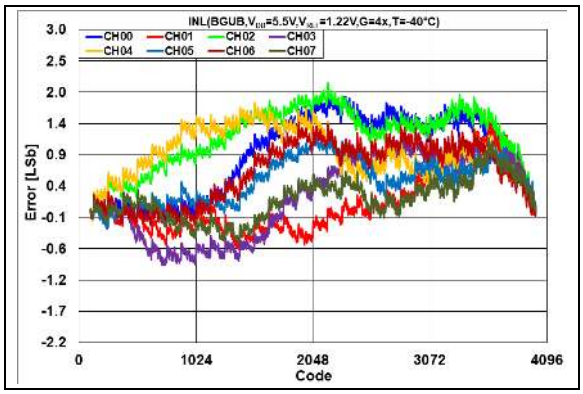

FIGURE 2-44: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

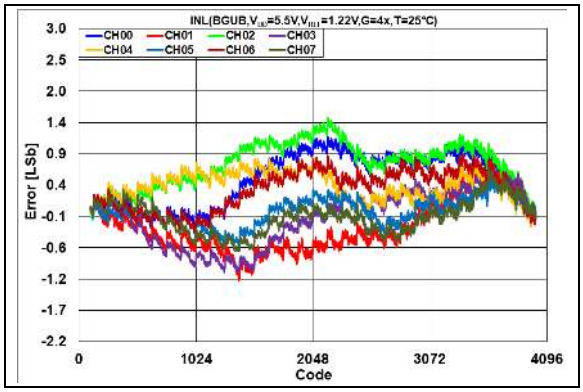

FIGURE 2-45: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

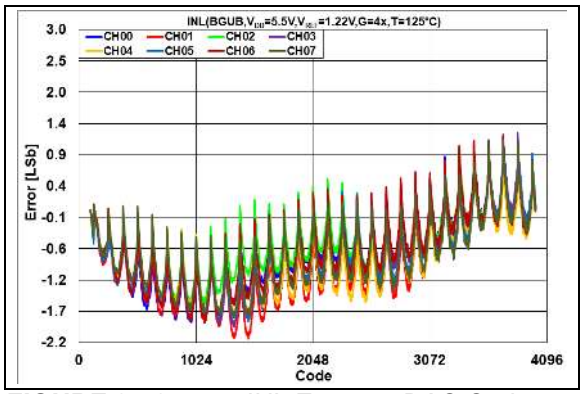

FIGURE 2-46: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

2.2.8 DIFFERENTIAL NONLINEARITY ERROR (DNL) - MCP47FXB28 (12-BIT), BAND GAP MODE (VRNB:VRNA = 01), GAIN = 2X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

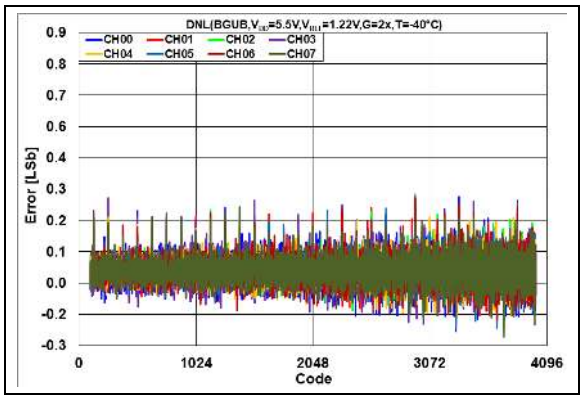

FIGURE 2-47: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

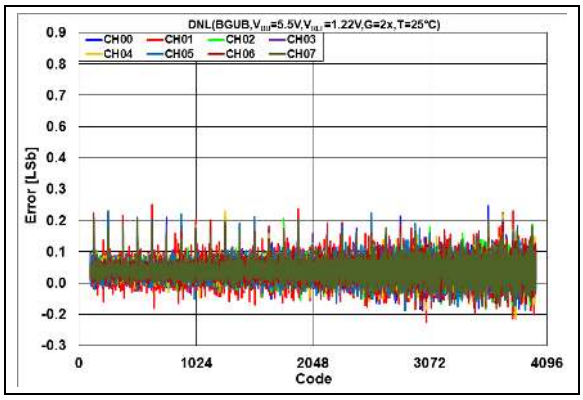

FIGURE 2-48: *DNL Error vs. DAC Code, T = +25°C V_{DD} = 5.5V.*

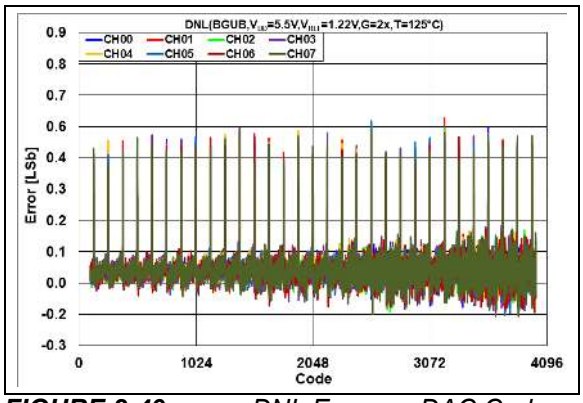

FIGURE 2-49: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

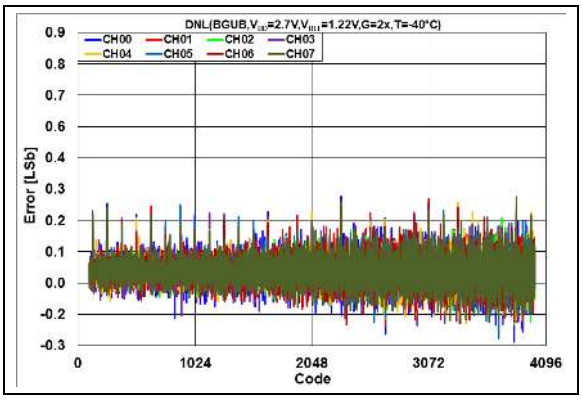

FIGURE 2-50: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

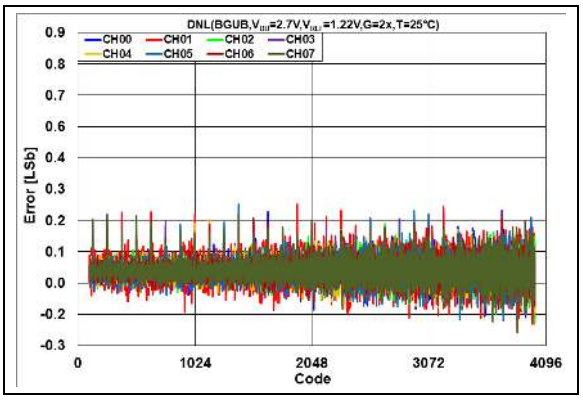

FIGURE 2-51: *DNL Error vs. DAC Code, T = +25°C V_{DD} = 2.7V.*

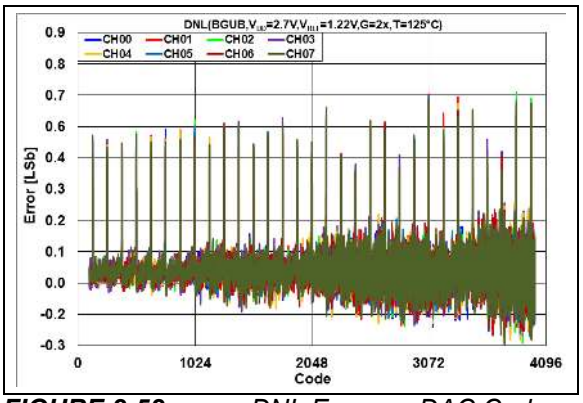

FIGURE 2-52: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

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2.2.9 DIFFERENTIAL NONLINEARITY ERROR (DNL) - MCP47FXB28 (12-BIT), BAND GAP MODE (VRNB:VRNA = 01), GAIN = 4X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

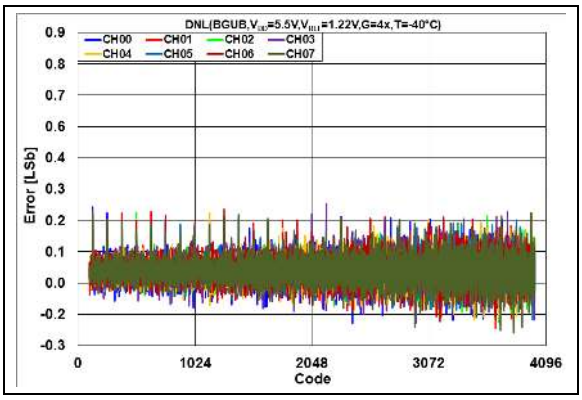

FIGURE 2-53: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

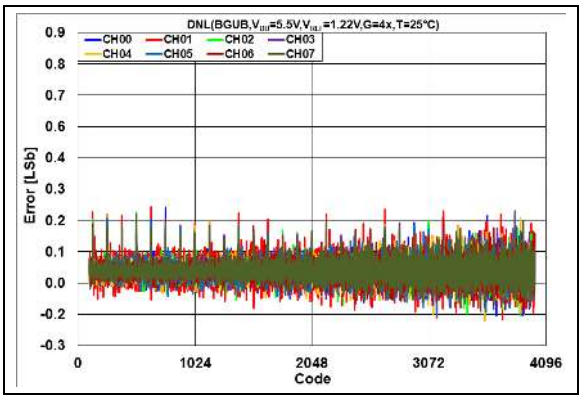

FIGURE 2-54: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

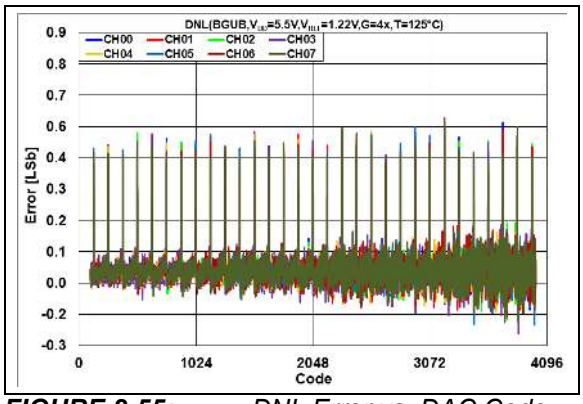

FIGURE 2-55: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

2.2.10 TOTAL UNADJUSTED ERROR (TUE) - MCP47FXB28 (12-BIT), EXTERNAL V_{REF} UNBUFFERED MODE (VRNB:VRNA = 10), $V_{REF} = V_{DD}$, GAIN = 1X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

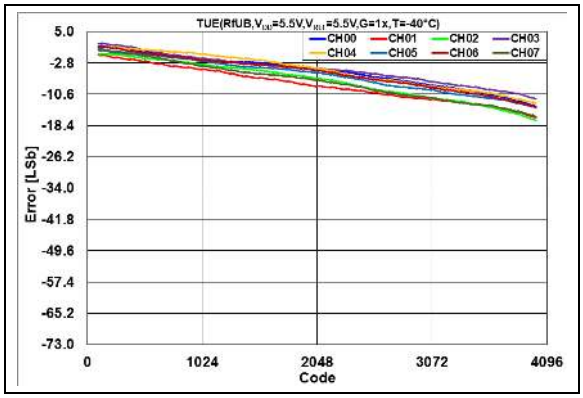

FIGURE 2-56: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

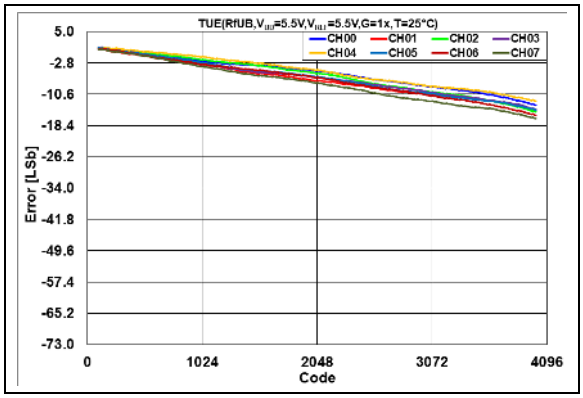

FIGURE 2-57: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C,V_{DD} = 5.5V.*

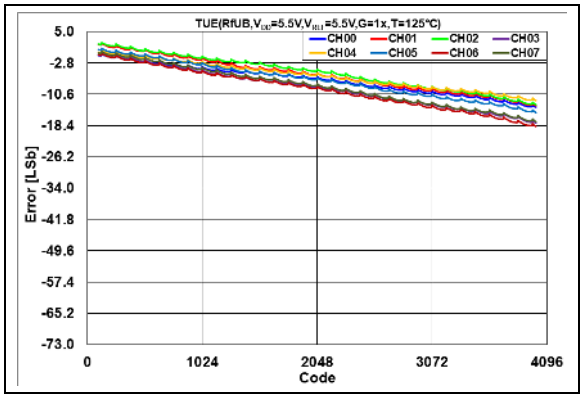

FIGURE 2-58: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

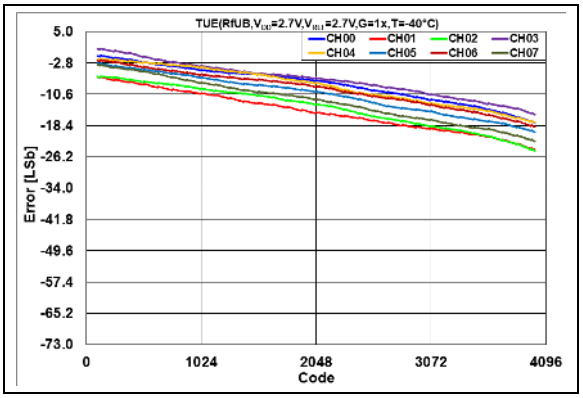

FIGURE 2-59: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

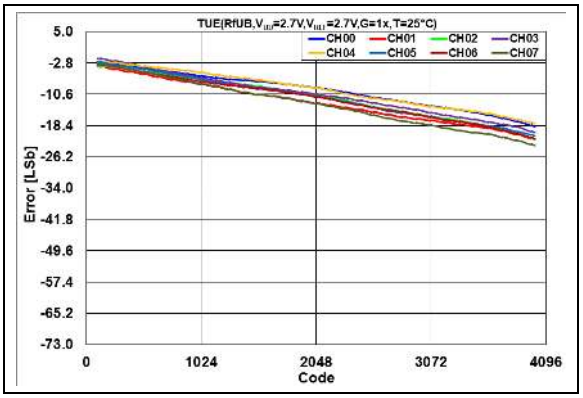

FIGURE 2-60: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

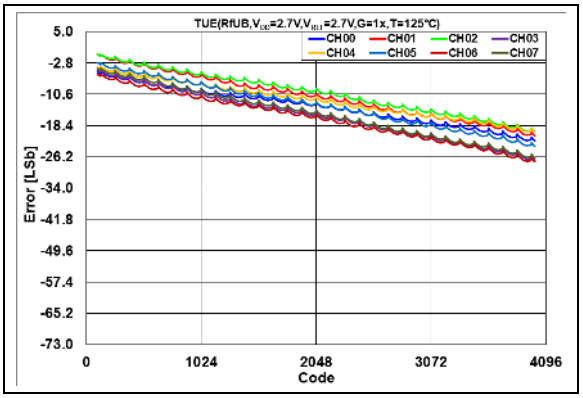

FIGURE 2-61: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

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2.2.11 TOTAL UNADJUSTED ERROR (TUE) - MCP47FXB28 (12-BIT), EXTERNAL V_{REF} UNBUFFERED MODE (VRNB:VRNA = 10), V_{REF} = V_{DD}/2, GAIN = 2X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

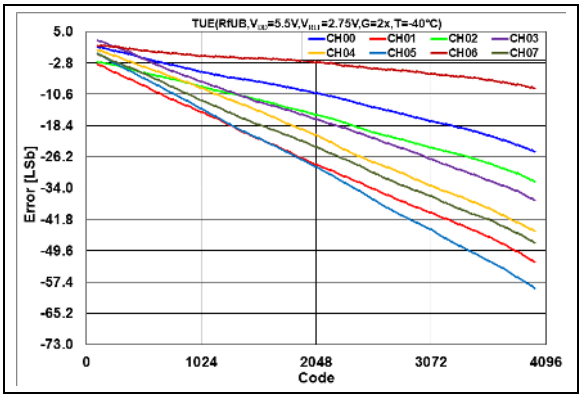

FIGURE 2-62: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

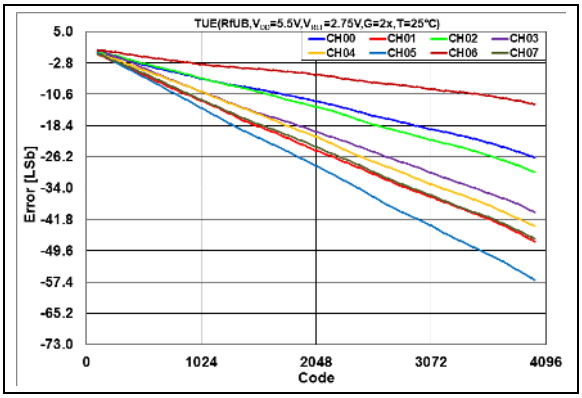

FIGURE 2-63: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C,V_{DD} = 5.5V.*

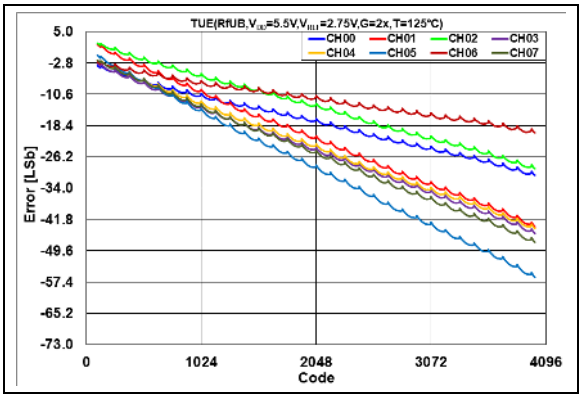

FIGURE 2-64: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

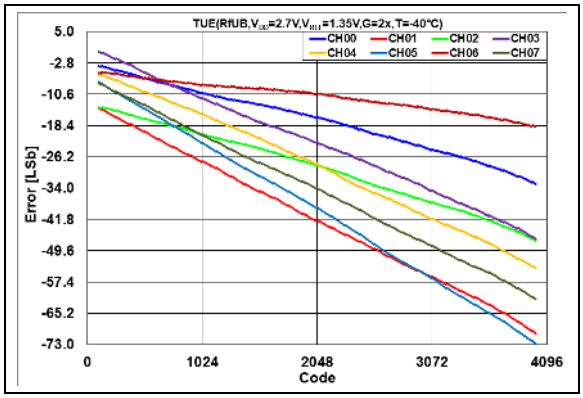

FIGURE 2-65: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

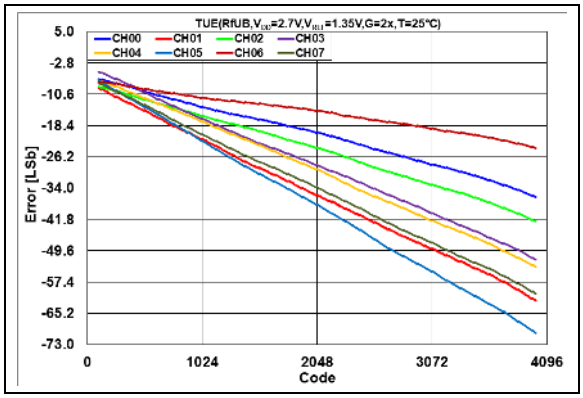

FIGURE 2-66: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

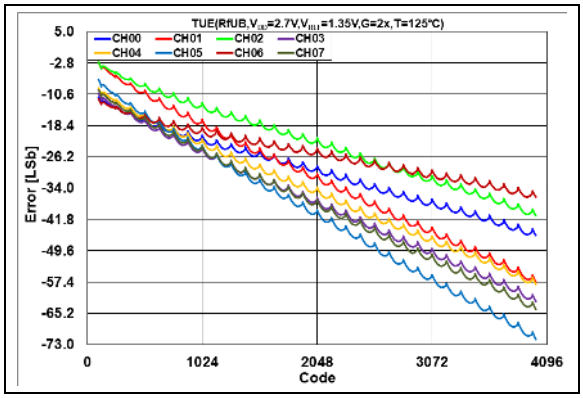

FIGURE 2-67: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.12 INTEGRAL NONLINEARITY ERROR (INL) - MCP47FXB28 (12-BIT), EXTERNAL V_{REF} MODE, UNBUFFERED (VRNB:VRNA = 10), V_{REF} = V_{DD}, GAIN = 1X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

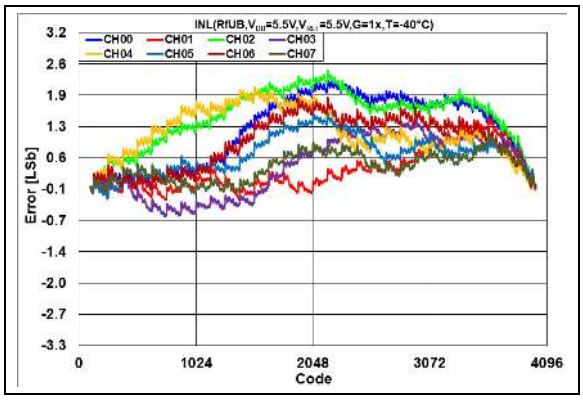

FIGURE 2-68: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

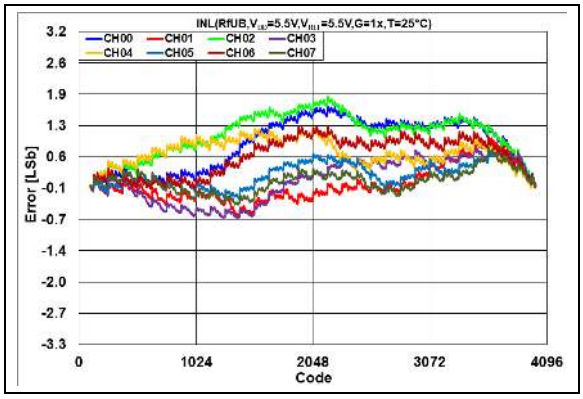

FIGURE 2-69: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

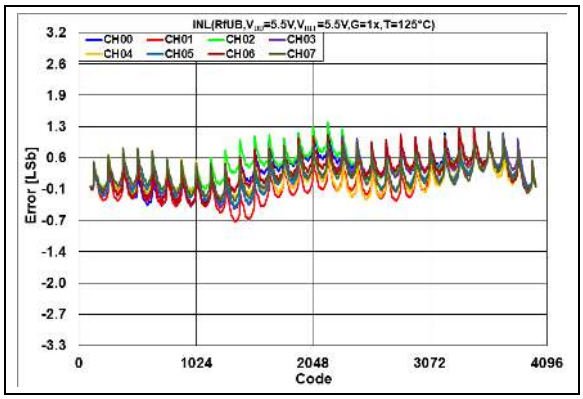

FIGURE 2-70: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

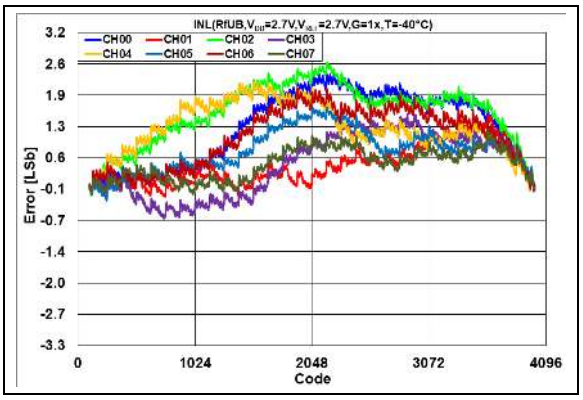

FIGURE 2-71: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

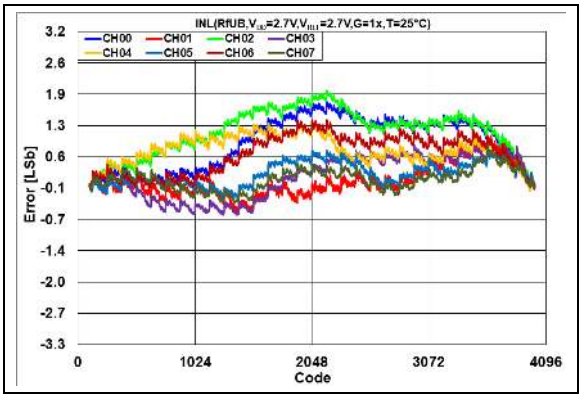

FIGURE 2-72: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

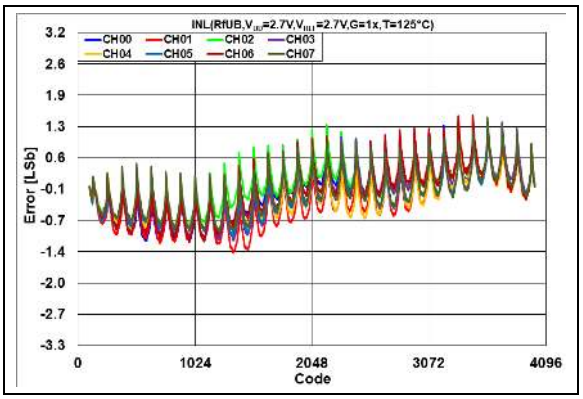

FIGURE 2-73: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

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2.2.13 INTEGRAL NONLINEARITY ERROR (INL) - MCP47FXB28 (12-BIT), EXTERNAL V_{REF} MODE, UNBUFFERED (VRNB:VRNA = 10), V_{REF} = V_{DD}/2, GAIN = 2X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

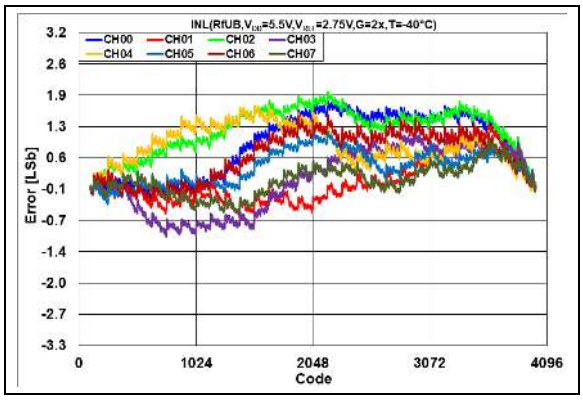

FIGURE 2-74: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

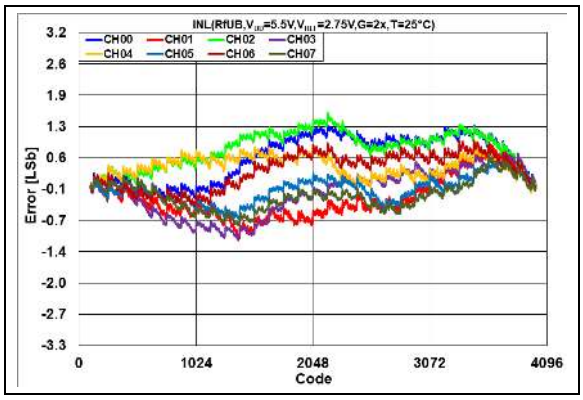

FIGURE 2-75: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

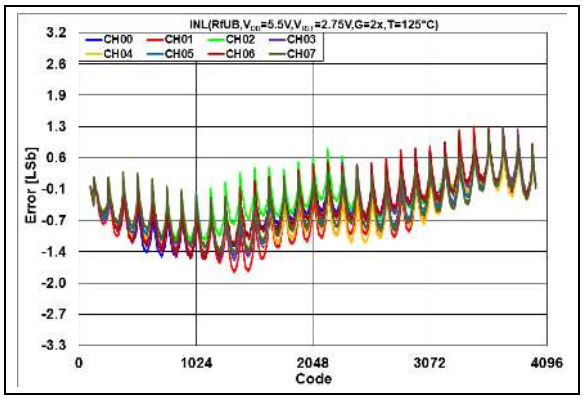

FIGURE 2-76: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

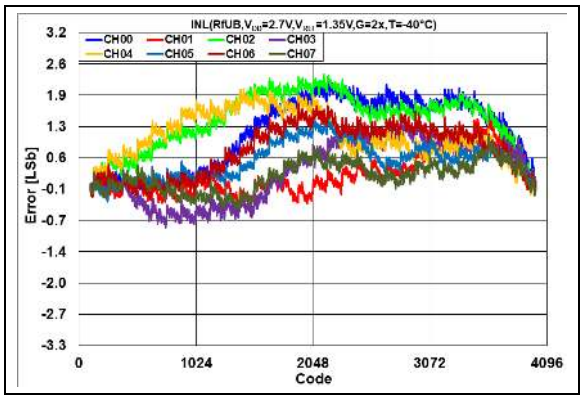

FIGURE 2-77: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

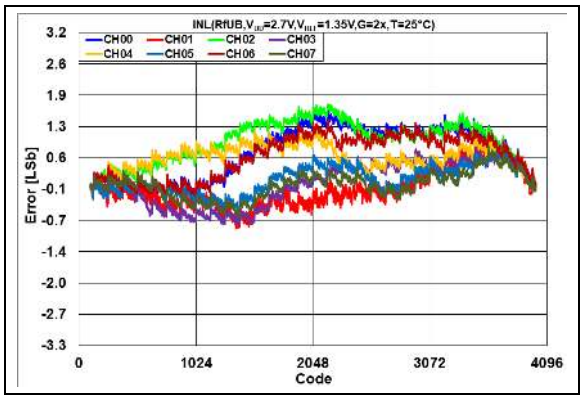

FIGURE 2-78: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

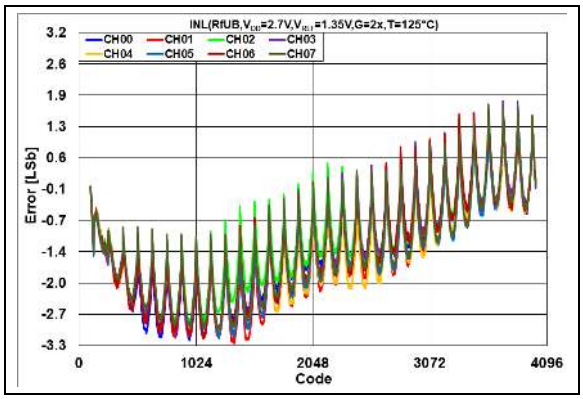

FIGURE 2-79: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.14 DIFFERENTIAL NONLINEARITY ERROR (DNL) - MCP47FXB28 (12-BIT), EXTERNAL V_{REF} MODE, UNBUFFERED (VRNB:VRNA = 10), V_{REF} = $_{VDD}$, GAIN = 1X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

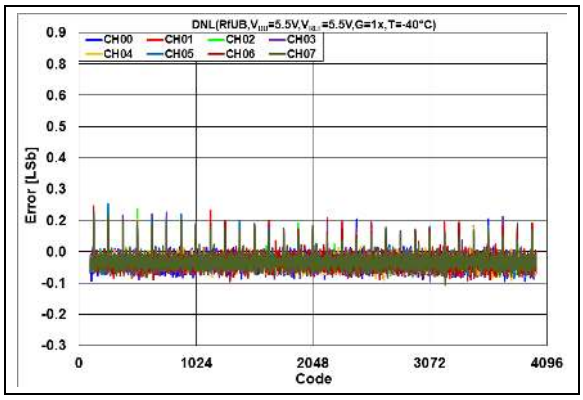

FIGURE 2-80: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

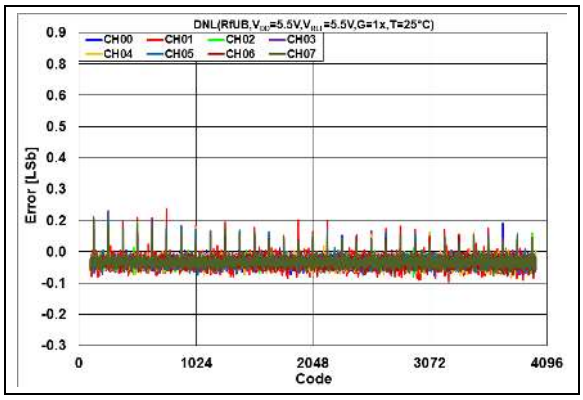

FIGURE 2-81: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

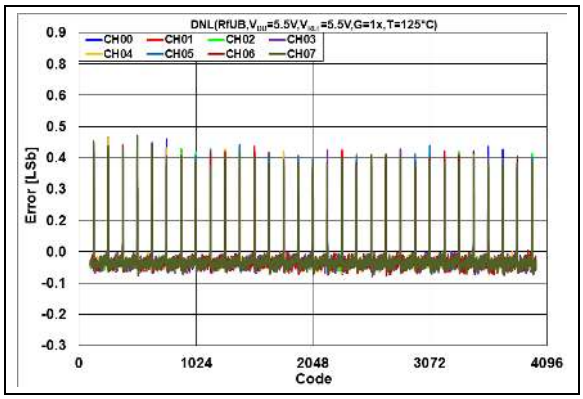

FIGURE 2-82: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

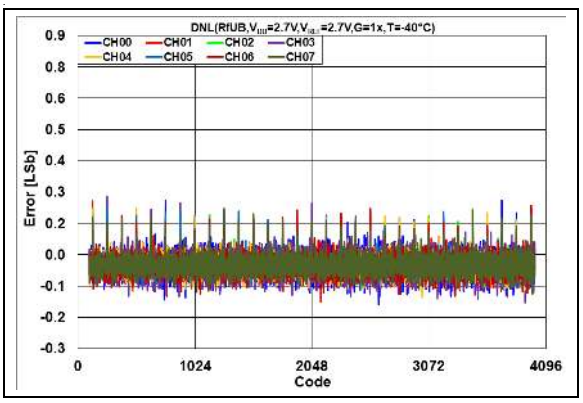

FIGURE 2-83: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

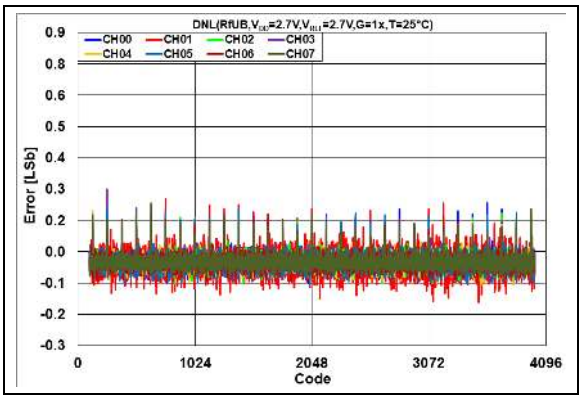

FIGURE 2-84: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

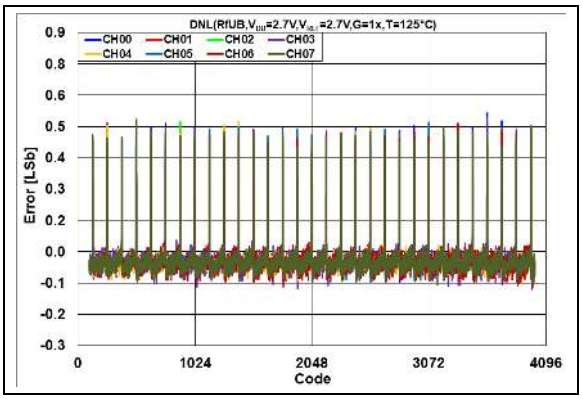

FIGURE 2-85: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

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2.2.15 DIFFERENTIAL NONLINEARITY ERROR (DNL) - MCP47FXB28 (12-BIT), EXTERNAL V_{REF} MODE, UNBUFFERED (VRNB:VRNA = 10), V_{REF} = V_{DD}/2, GAIN = 2X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

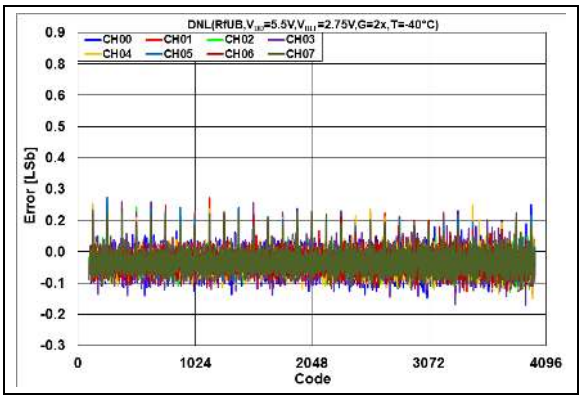

FIGURE 2-86: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

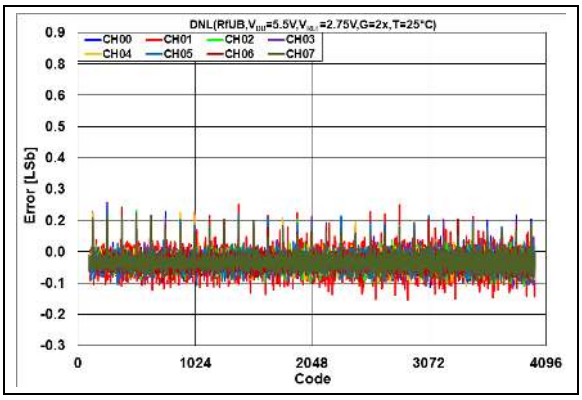

FIGURE 2-87: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

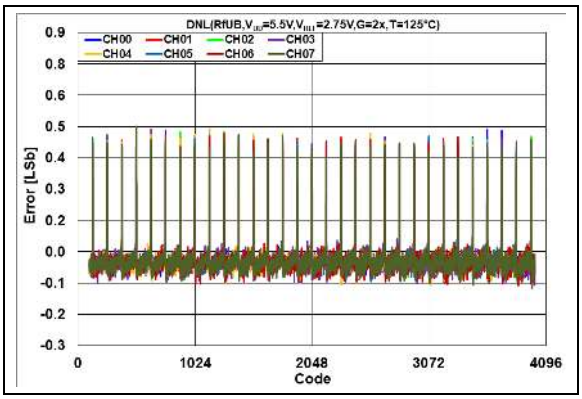

FIGURE 2-88: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

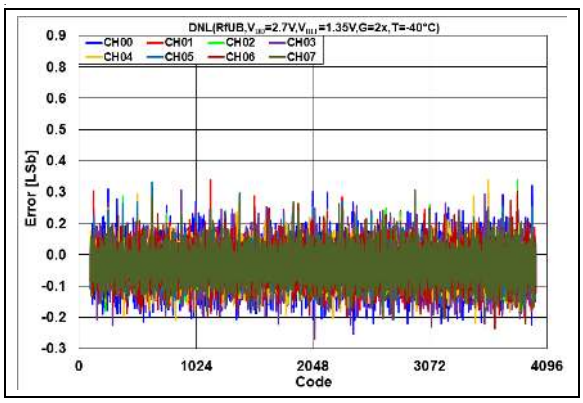

FIGURE 2-89: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

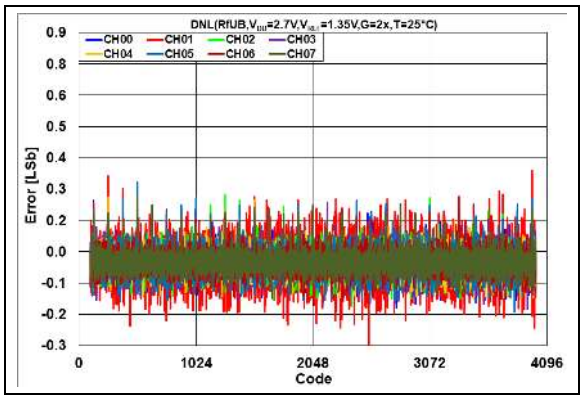

FIGURE 2-90: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

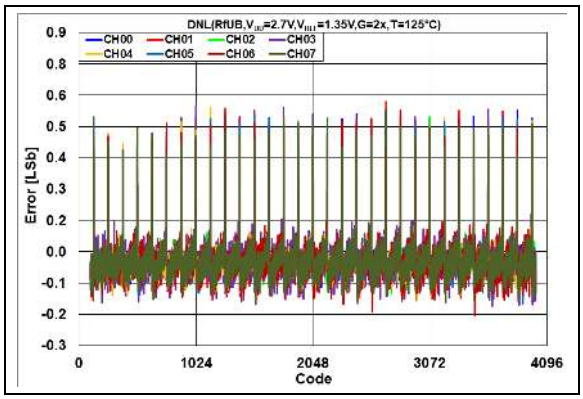

FIGURE 2-91: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.16 TOTAL UNADJUSTED ERROR (TUE) - MCP47FXB28 (12-BIT), EXTERNAL V_{REF} BUFFERED MODE (VRNB:VRNA = 10), V_{REF} = V_{DD}, GAIN = 1X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

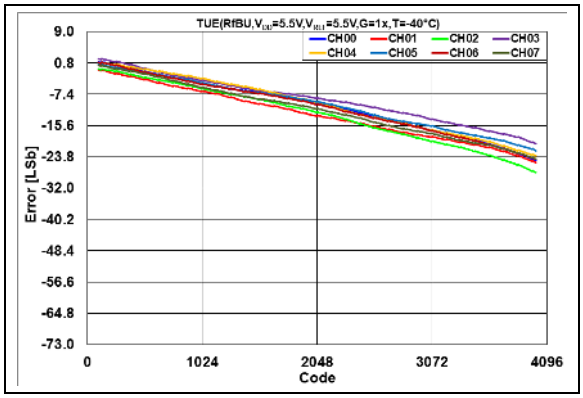

FIGURE 2-92: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

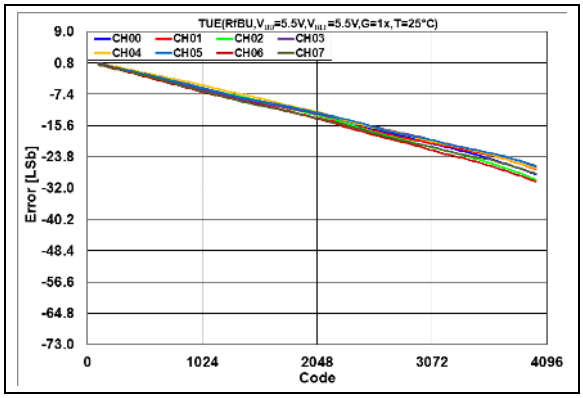

FIGURE 2-93: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C,V_{DD} = 5.5V.*

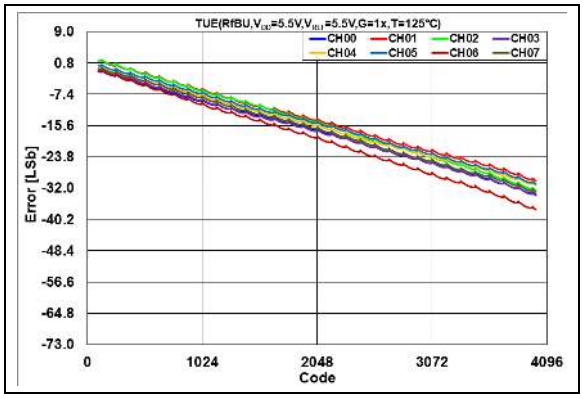

FIGURE 2-94: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

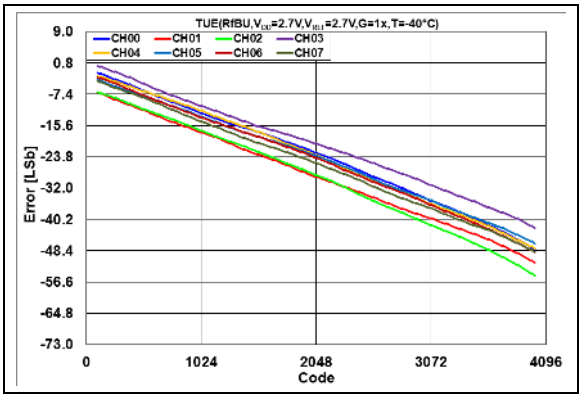

FIGURE 2-95: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

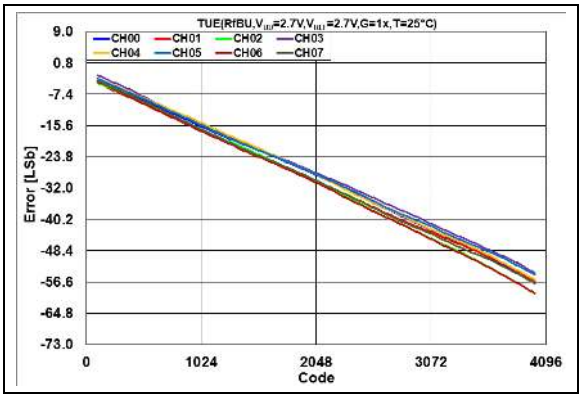

FIGURE 2-96: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

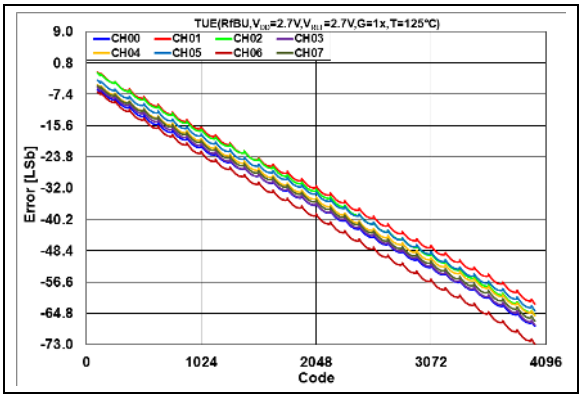

FIGURE 2-97: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

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2.2.17 TOTAL UNADJUSTED ERROR (TUE) - MCP47FXB28 (12-BIT), EXTERNAL V_{REF} BUFFERED MODE (VRNB:VRNA = 10), V_{REF} = V_{DD}/2, GAIN = 2X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

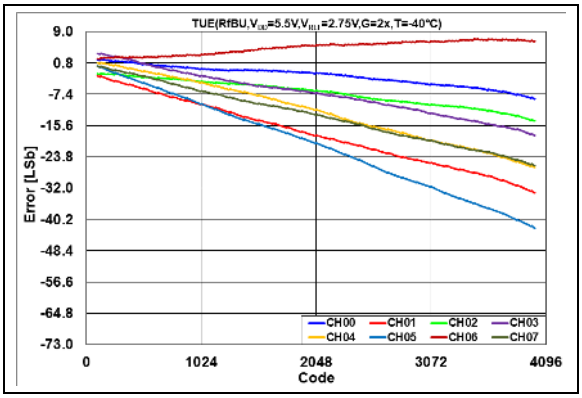

FIGURE 2-98: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

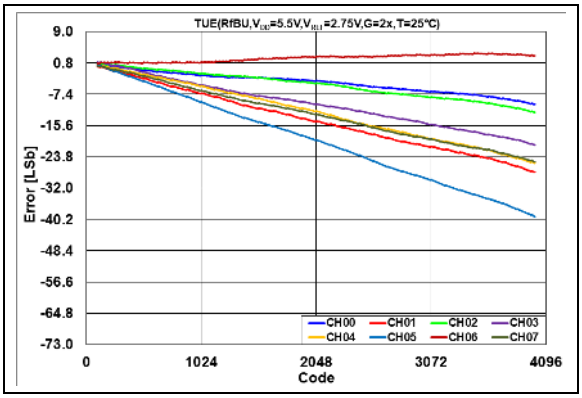

FIGURE 2-99: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C,V_{DD} = 5.5V.*

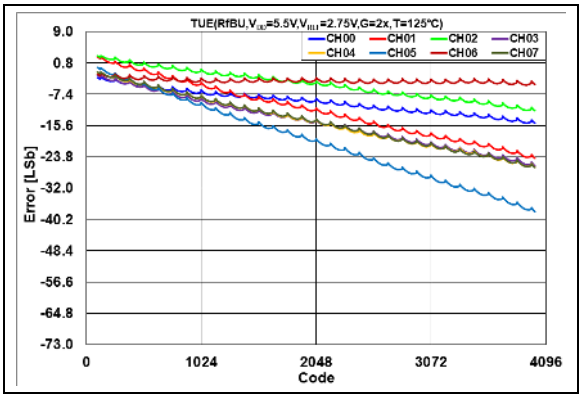

FIGURE 2-100: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

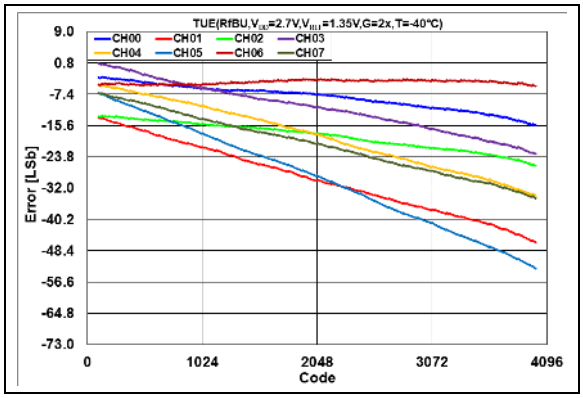

FIGURE 2-101: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

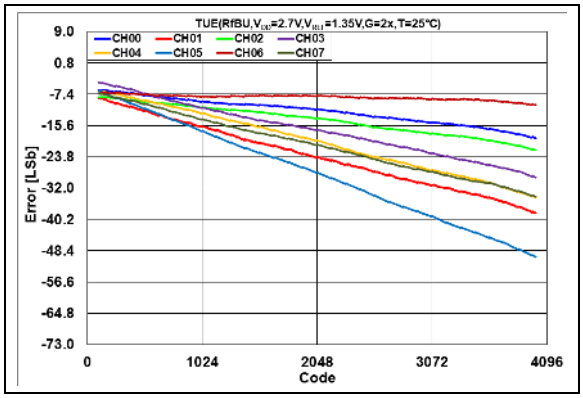

FIGURE 2-102: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

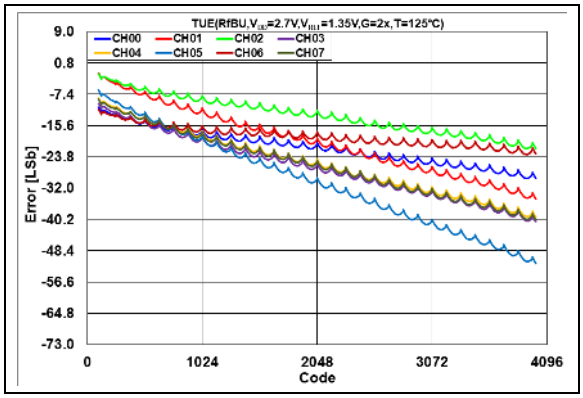

FIGURE 2-103: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.18 INTEGRAL NONLINEARITY ERROR (INL) - MCP47FXB28 (12-BIT), EXTERNAL V_{REF} MODE, BUFFERED (VRNB:VRNA = 11), V_{REF} = V_{DD}, GAIN = 1X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

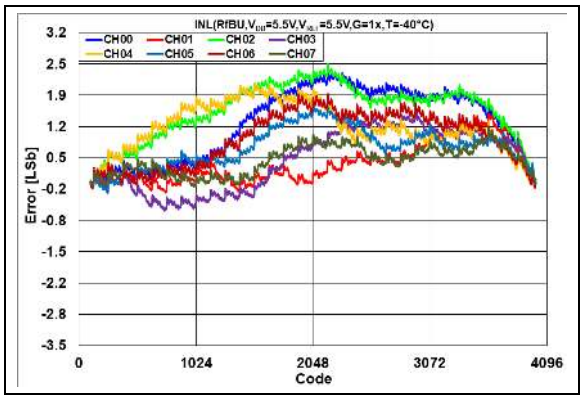

FIGURE 2-104: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

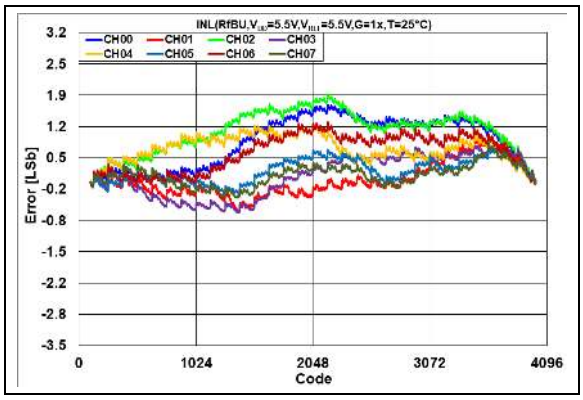

FIGURE 2-105: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

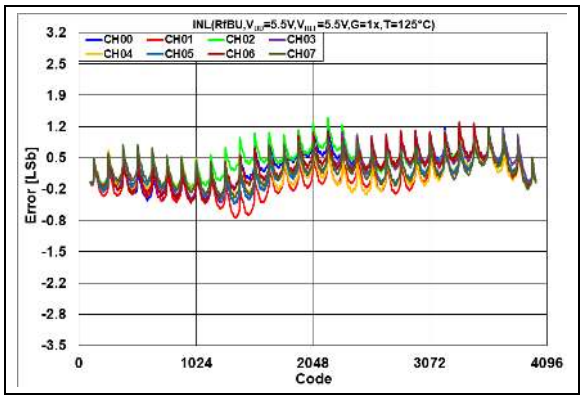

FIGURE 2-106: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

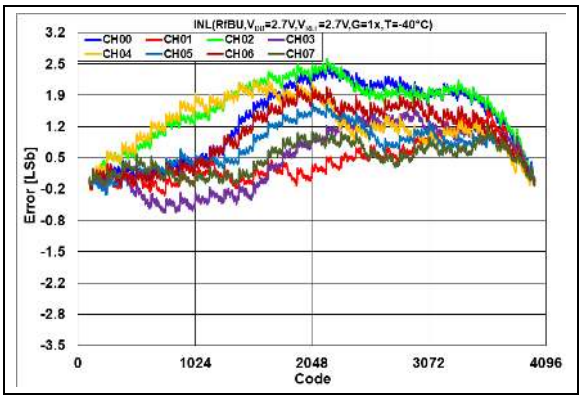

FIGURE 2-107: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

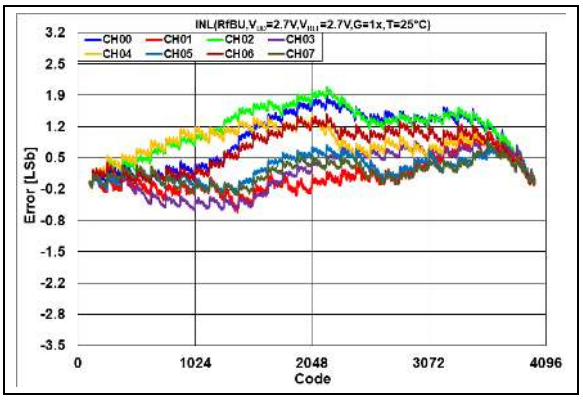

FIGURE 2-108: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

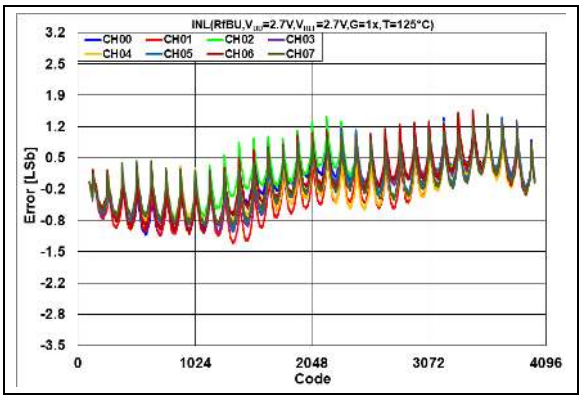

FIGURE 2-109: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

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2.2.19 INTEGRAL NONLINEARITY ERROR (INL) - MCP47FXB28 (12-BIT), EXTERNAL V_{REF} MODE, BUFFERED (VRNB:VRNA = 11), V_{REF} = V_{DD}/2, GAIN = 2X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

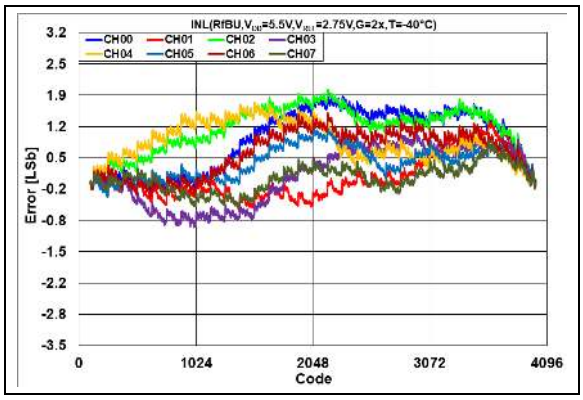

FIGURE 2-110: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

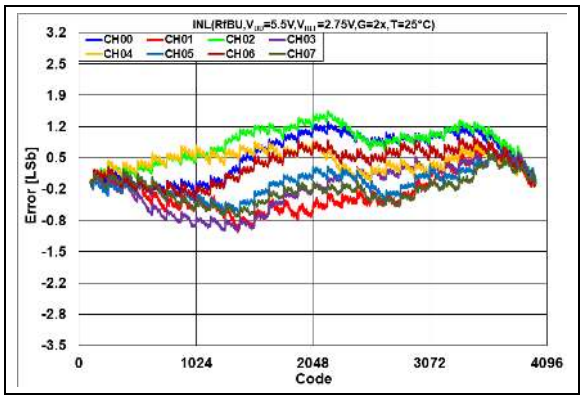

FIGURE 2-111: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

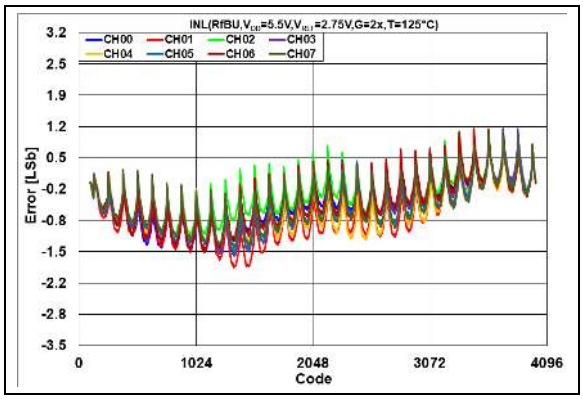

FIGURE 2-112: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

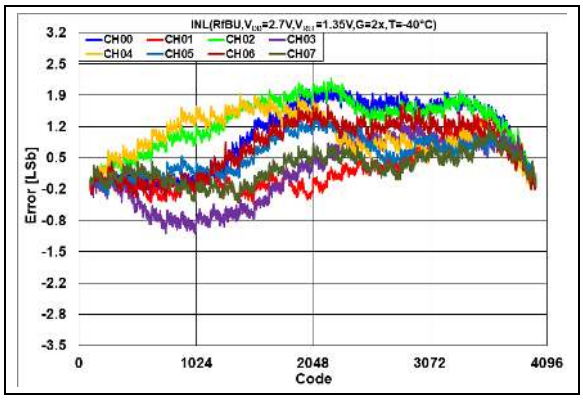

FIGURE 2-113: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

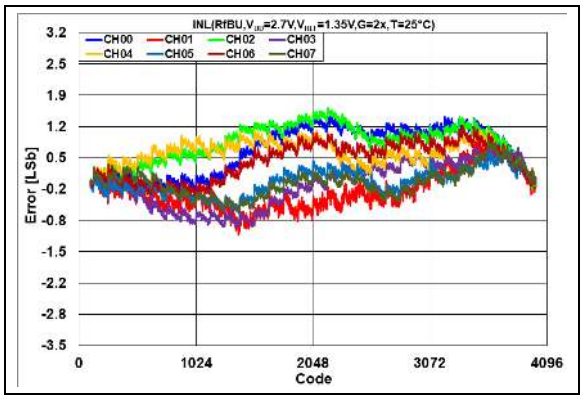

FIGURE 2-114: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

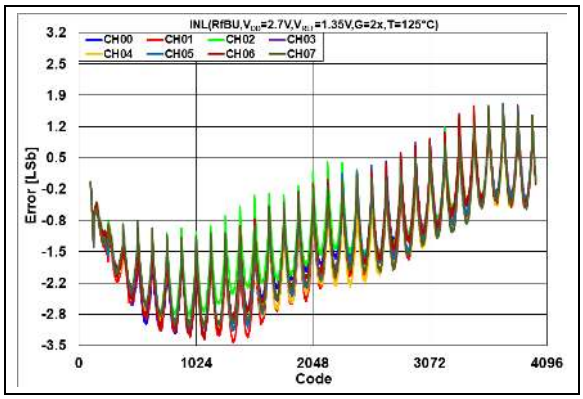

FIGURE 2-115: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.20 DIFFERENTIAL NONLINEARITY ERROR (DNL) - MCP47FXB28 (12-BIT), EXTERNAL V_{REF} MODE, BUFFERED (VRNB:VRNA = 11), V_{REF} = V_{DD}, GAIN = 1X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

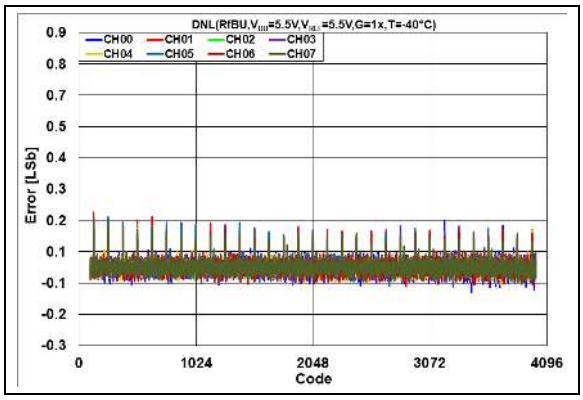

FIGURE 2-116: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

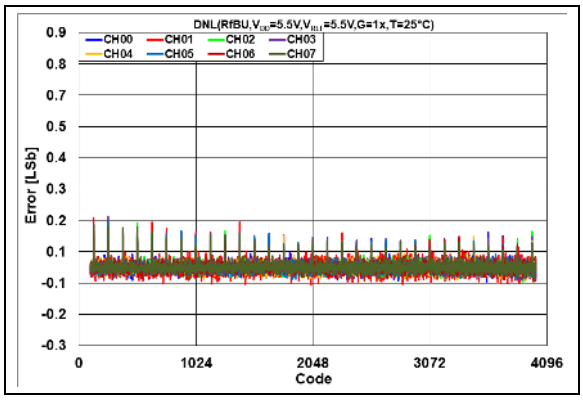

FIGURE 2-117: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

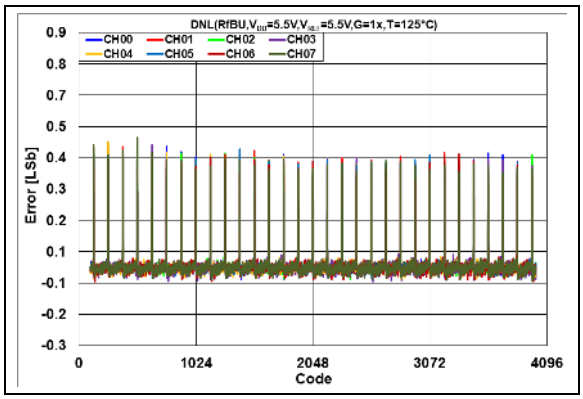

FIGURE 2-118: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

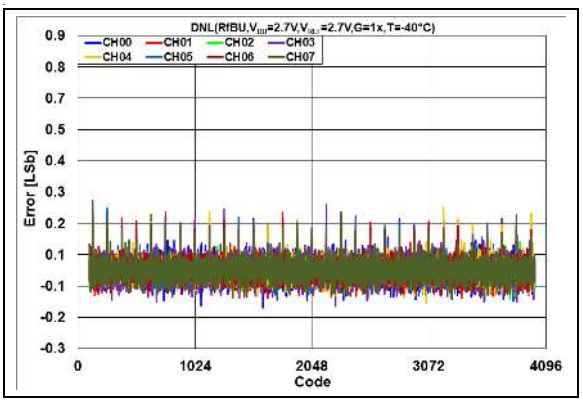

FIGURE 2-119: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

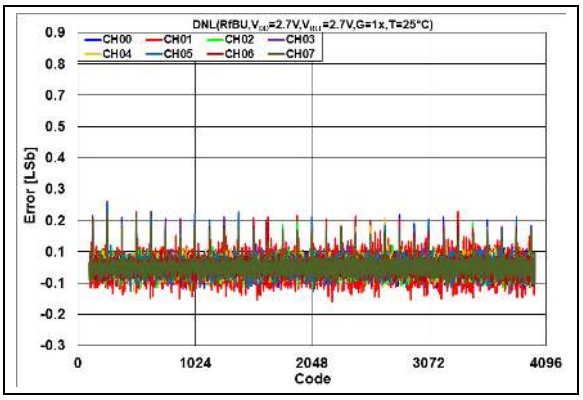

FIGURE 2-120: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

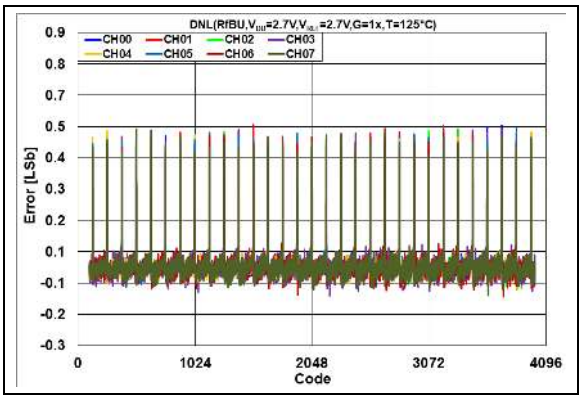

FIGURE 2-121: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

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2.2.21 DIFFERENTIAL NONLINEARITY ERROR (DNL) - MCP47FXB28 (12-BIT), EXTERNAL V_{REF} MODE, BUFFERED (VRNB:VRNA = 11), $V_{REF} = V_{DD}/2$, GAIN = 2X, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

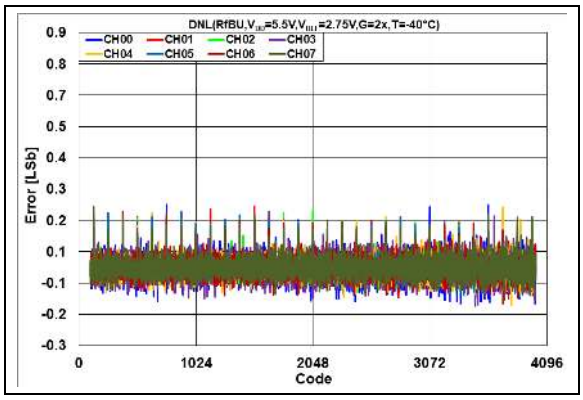

FIGURE 2-122: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

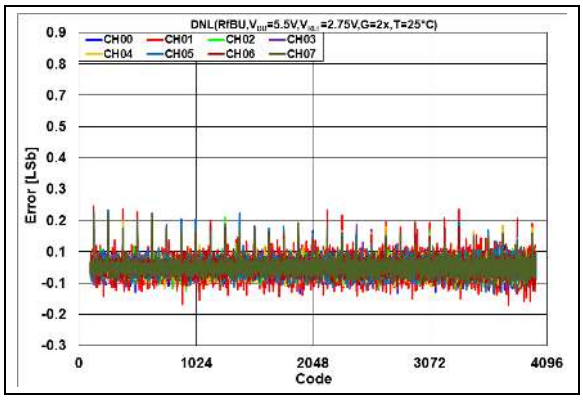

FIGURE 2-123: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

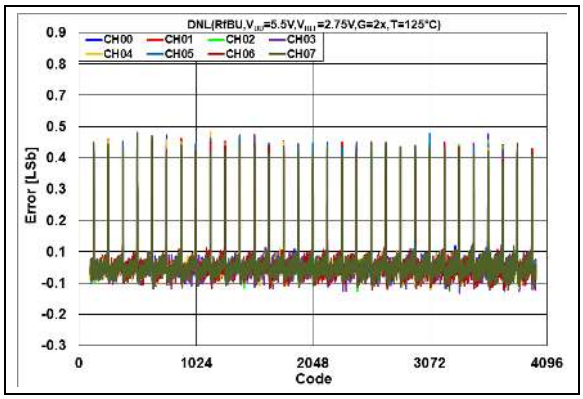

FIGURE 2-124: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

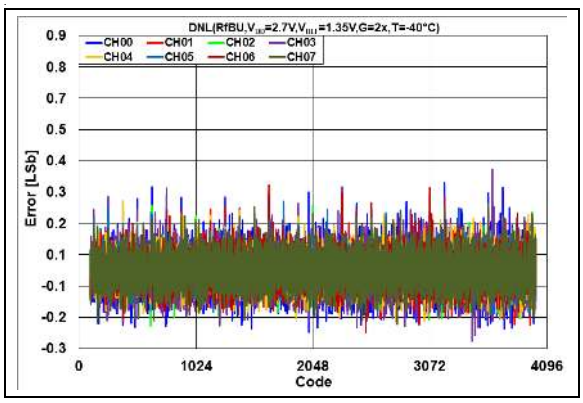

FIGURE 2-125: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

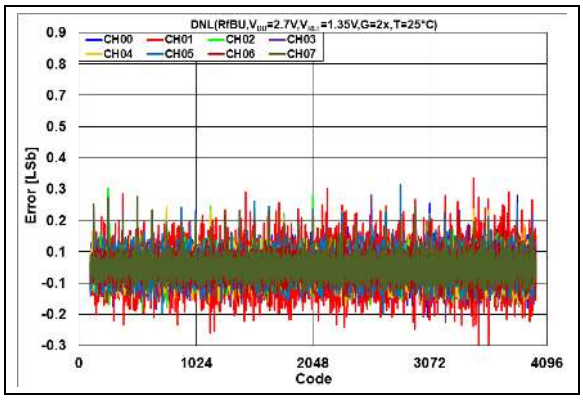

FIGURE 2-126: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

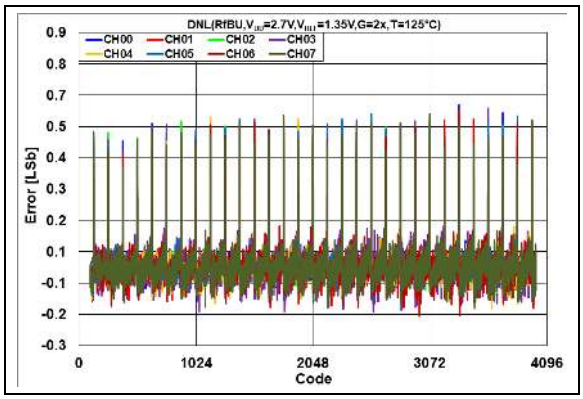

FIGURE 2-127: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

NOTES:

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3.0 PIN DESCRIPTIONS

Overviews of the pin functions are provided in **Section 3.1 "Positive Power Supply Input (V_{DD})"** through **Section 3.7 "I^2C - Serial Data Pin (SDA)"**. The descriptions of the pins for the quad-DAC output devices are listed in Table 3-1 and descriptions for the octal-DAC output devices are listed in Table 3-2.

TABLE 3-1: MCP47FXBX4 (QUAD-DAC) PIN FUNCTION TABLE

Pin					Description
20-Lead TSSOP	20-Lead VQFN	Symbol	I/O	Buffer Type	
1	19	$\overline{LAT1}$	I	ST	DAC Register Latch Pin. The Latch 1 Pin allows the value in the volatile DAC1/DAC3 registers (Wiper and Configuration bits) to be transferred to the DAC1/DAC3 outputs (V_{OUT1}, V_{OUT3}).
2	20	V_{DD}	—	P	Supply Voltage Pin
3	1	A0	I	ST	I^2C Slave Address Bit 0 Pin
4	2	V_{REF0}	A	Analog	Voltage Reference Input 0 Pin
5	3	V_{OUT0}	A	Analog	Buffered Analog Voltage Output – Channel 0 Pin
6	4	V_{OUT2}	A	Analog	Buffered Analog Voltage Output – Channel 2 Pin
7, 8, 10, 11, 12, 13	5, 6, 8, 9, 10,11	NC	—	—	Not Internally Connected
9	7	V_{SS}	—	P	Ground Reference Pin for all circuitries on the device
14	12	V_{OUT3}	—	—	Buffered Analog Voltage Output - Channel 3 Pin
15	13	V_{OUT1}	—	—	Buffered Analog Voltage Output - Channel 1 Pin
16	14	V_{REF1}	A	Analog	Voltage Reference Input 1 Pin
17	15	A1	I	—	I^2C Slave Address Bit 1 Pin
18	16	SCL	I	ST	I^2C Serial Clock Pin
19	17	SDA	I	ST	I^2C Serial Data Pin
20	18	$\overline{LAT0}$/HVC	I	ST	DAC Register Latch/High-Voltage Command Pin. The Latch 0 pin allows the value in the volatile DAC0/DAC2 registers (Wiper and Configuration bits) to be transferred to the DAC0/DAC2 outputs (V_{OUT0}, V_{OUT2}). The High-Voltage command allows user Configuration bits to be written.
—	21	EP	—	—	Exposed Thermal Pad(1)

Note 1: A = Analog, ST = Schmitt Trigger, HV = High Voltage, I = Input, O = Output, I/O = Input/Output, P = Power.

TABLE 3-2: MCP47FXBX8 (OCTAL-DAC) PIN FUNCTION TABLE

Pin					Description
TSSOP 20L	VQFN 20L	Symbol	I/O	Buffer Type	
1	19	$\overline{LAT1}$	I	ST	DAC Register Latch Pin. The Latch 1 pin allows the value in the volatile DAC1/DAC3/DAC5/DAC7 registers (Wiper and Configuration bits) to be transferred to the DAC1/DAC3/DAC5/DAC7 outputs (V_{OUT1}, V_{OUT3}, V_{OUT5}, V_{OUT7}).
2	20	V_{DD}	—	P	Supply Voltage Pin
3	1	A0	I	ST	I^2C Slave Address Bit 0 Pin
4	2	V_{REF0}	A	Analog	Voltage Reference Input 0 Pin
5	3	V_{OUT0}	A	Analog	Buffered Analog Voltage Output – Channel 0 Pin
6	4	V_{OUT2}	A	Analog	Buffered Analog Voltage Output – Channel 2 Pin
7	5	V_{OUT4}	A	Analog	Buffered Analog Voltage Output – Channel 4 Pin
8	6	V_{OUT6}	A	Analog	Buffered Analog Voltage Output – Channel 6 Pin
9	7	V_{SS}	—	P	Ground Reference Pin for all circuitries on the device
10, 11	8, 9	NC	—	—	Not Internally Connected
12	10	V_{OUT7}	A	Analog	Buffered Analog Voltage Output – Channel 7 Pin
13	11	V_{OUT5}	A	Analog	Buffered Analog Voltage Output – Channel 5 Pin
14	12	V_{OUT3}	A	Analog	Buffered Analog Voltage Output – Channel 3 Pin
15	13	V_{OUT1}	A	Analog	Buffered Analog Voltage Output – Channel 1 Pin
16	14	V_{REF1}	A	Analog	Voltage Reference Input 1 Pin
17	15	A1	I	—	I^2C Slave Address Bit 1 Pin
18	16	SCL	I	ST	I^2C Serial Clock Pin
19	17	SDA	I	ST	I^2C Serial Data Pin
20	18	$\overline{LAT0}$/HVC	I	ST	DAC Register Latch/High-Voltage Command Pin. The Latch 0 pin allows the value in the volatile DAC0/DAC2/DAC4/DAC6 registers (Wiper and Configuration bits) to be transferred to the DAC0/DAC2/DAC4/DAC6 outputs (V_{OUT0}, V_{OUT2}, V_{OUT4}, V_{OUT6}). The High-Voltage command allows user Configuration bits to be written.
—	21	EP	—	—	Exposed Thermal Pad(1)

Note 1: A = Analog, ST = Schmitt Trigger, HV = High Voltage, I = Input, O = Output, I/O = Input/Output, P = Power.

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3.1 Positive Power Supply Input (V_{DD})

V_{DD} is the positive supply voltage input pin. The input supply voltage is relative to V_{SS}.

The power supply at the V_{DD} pin should be as clean as possible for a good DAC performance. It is recommended to use an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate noise present in application boards.

3.2 Ground (V_{SS})

The V_{SS} pin is the device ground reference.

The user must connect the V_{SS} pin to a ground plane through a low-impedance connection. If an analog ground path is available in the application PCB (Printed Circuit Board), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.3 Voltage Reference Pins (V_{REF})

The V_{REF} pin is either an input or an output. When the DAC's voltage reference is configured as the V_{REF} pin, the pin is an input. When the DAC's voltage reference is configured as the internal band gap, the pin is an output.

When the DAC's voltage reference is configured as the V_{REF} pin, there are two options for this voltage input:

- V_{REF} pin voltage buffered
- V_{REF} pin voltage unbuffered

The buffered option is offered in cases where the external reference voltage does not have sufficient current capability to not drop its voltage when connected to the internal resistor ladder circuit.

When the DAC's voltage reference is configured as the device V_{DD}, the V_{REF} pin is disconnected from the internal circuit.

When the DAC's voltage reference is configured as the internal band gap, the V_{REF} pin's drive capability is minimal, so the output signal should be buffered.

There are two V_{REF} pins, each corresponding to a group of output channels. V_{REF0} is connected to even channels: 0-6, while V_{REF1} is connected to odd channels: 1-7. See **Section 5.2 "Voltage Reference Selection"** and Register 4-2 for more details on the Configuration bits.

3.4 Analog Output Voltage Pins (V_{OUTn})

V_{OUT} is the DAC analog voltage output pin. The DAC output has an output amplifier. The DAC output range depends on the selection of the voltage reference source (and potential output gain selection). These are:

- Device V_{DD} – The full-scale range of the DAC output is from V_{SS} to approximately V_{DD}.
- V_{REF} pin – The full-scale range of the DAC output is from V_{SS} to G × V_{RL}, where G is the gain selection option (1x or 2x).
- Internal Band Gap – The full-scale range of the DAC output is from V_{SS} to G × (2 × V_{BG}), where G is the gain selection option (1x or 2x).

In Normal mode, the DC impedance of the output pin is about 1Ω. In Power-Down mode, the output pin is internally connected to a known pull-down resistor of 1 kΩ, 125 kΩ, or open. The power-down selection bits settings are shown in Register 4-3 and Table 5-4.

3.5 Latch Pin ($\overline{LAT}$)/High-Voltage Command (HVC)

The DAC output value update event can be controlled and synchronized using the $\overline{LAT}$ pins, for one or both channels, on a single or different devices.

The $\overline{LAT}$ pins control the effect of the Volatile Wiper registers, VRnB:VRnA, PDnB:PDnA and Gx bits on the DAC output.

If the $\overline{LAT}$ pins are held at V_{IH}, the values sent to the Volatile Wiper registers and Configuration bits have no effect on the DAC outputs.

Once voltage on the pin transitions to V_{IL}, the values in the Volatile Wiper registers and Configuration bits are transferred to the DAC outputs.

The pin is level-sensitive, so writing to the Volatile Wiper registers and Configuration bits, while it is being held at V_{IL}, will trigger an immediate change in the outputs.

The HVC pin allows the device's nonvolatile user Configuration bits to be programmed when the voltage on the pin is greater than the V_{IHH} entry voltage.

3.6 I^2C - Serial Clock Pin (SCL)

The SCL pin is the serial clock pin of the I^2C interface. The MCP47FXBX4/8 I^2C interface only acts as a slave and the SCL pin accepts only external serial clocks. The input data from the master device is shifted into the SDA pin on the rising edges of the SCL clock and output from the device occurs at the falling edges of the SCL clock. The SCL pin is an open-drain, N-channel driver. Therefore, it needs an external pull-up resistor from the V_{DD} line to the SCL pin. Refer to **Section 6.0 "I^2C Serial Interface Module"** for more details on the I^2C serial interface communication.

3.7 I^{2}C - Serial Data Pin (SDA)

The SDA pin is the serial data pin of the I^{2}C interface. The SDA pin is used to write or read the DAC registers and Configuration bits. The SDA pin is an open-drain, N-channel driver. Therefore, it needs an external pull-up resistor from the V_{DD} line to the SDA pin. Except for Start and Stop conditions, the data on the SDA pin must be stable during the high period of the clock. The High or Low state of the SDA pin can only change when the clock signal on the SCL pin is low. See **Section 6.0 "I^{2}C Serial Interface Module"**.

3.8 A0 and A1 Slave Address Bits

These pins control the last two bits of the I^{2}C address. Connect them to V_{DD} to make the corresponding address bit a '1', or to V_{SS} for a '0'. See **Section 6.8 "Device I^{2}C Slave Addressing"** and Register 4-5 for more details.

3.9 No Connect (NC)

The NC pins are not connected to the device.

3.10 Exposed Pad

This pad is conductively connected to the device's substrate. It should be tied to the same potential as the V_{SS} pin (or left unconnected). This pad could be used to assist in heat dissipation for the device, when connected to a PCB heat sink. The pad is only present on the VQFN package.

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4.0 GENERAL DESCRIPTION

The MCP47FXBX4 (MCP47FXB04, MCP47FXB14, and MCP47FXB24) devices are quad-channel voltage output devices. The MCP47FXBX8 (MCP47FXB08, MCP47FXB18 and MCP47FXB28) devices are octal-channel voltage output devices.

These devices are offered with 8-bit (MCP47FXB0X), 10-bit (MCP47FXB1X) and 12-bit (MCP47FXB2X) resolutions and include nonvolatile memory (EEPROM), an I^2C serial interface and two write Latch pins ($\overline{LAT0}$, $\overline{LAT1}$) to control the update of the written DAC value to the DAC output pin.

The devices use a resistor ladder architecture. The resistor ladder DAC is driven from a software-selectable voltage reference source. The source can be either the device's internal V_{DD}, an external V_{REF} pin voltage (buffered or unbuffered), or an internal band gap voltage source.

The DAC output is buffered with a low power and precision output amplifier (op amp). This output amplifier provides a rail-to-rail output with low offset voltage and low noise. The gain (1x or 2x) of the output buffer is software configurable.

This device family also has user-programmable nonvolatile memory (EEPROM) option, which allows the user to save the desired POR/BOR value of the DAC register and device Configuration bits.

High-voltage lock bits can be used to ensure that the device's output settings are not accidentally modified.

The device operates from a single-supply voltage. This voltage is specified from 2.7V to 5.5V for full specified operation, and from 1.8V to 5.5V for digital operation. The device can operate between 1.8V and 2.7V, but its analog performance is significantly reduced; therefore, most device parameters are not specified for this range.

The main functional blocks are:

- **Power-on Reset/Brown-out Reset (POR/BOR)**
- **Device Memory**
- **Resistor Ladder**
- **Output Buffer/V_{OUT} Operation**
- **Internal Band Gap**
- **I^2C Serial Interface Module**

4.1 Power-on Reset/Brown-out Reset (POR/BOR)

The internal POR/BOR circuit monitors the power supply voltage (V_{DD}) during operation. This circuit ensures correct device start-up at system power-up and power-down events. The device's RAM retention voltage (V_{RAM}) is lower than the POR/BOR voltage trip point (V_{POR}/V_{BOR}). The maximum V_{POR}/V_{BOR} voltage is less than 1.8V.

POR occurs as the voltage rises (typically from 0V), while BOR occurs as the voltage falls (typically from $V_{DD(MIN)}$ or higher).

The POR and BOR trip points are at the same voltage and the condition is determined by whether the V_{DD} voltage is rising or falling (see Figure 4-1). What occurs is different depending on whether the reset is a POR or BOR.

When $V_{POR}/V_{BOR} < V_{DD} < 2.7V$, the electrical performance may not meet the data sheet specifications. In this region, the device is capable of reading and writing to its EEPROM and reading and writing to its volatile memory if the proper serial command is executed.

4.1.1 POWER-ON RESET

The Power-on Reset is the case where the V_{DD} has power applied to it, ramping up from the V_{SS} voltage level. As the device powers up, the V_{OUT} pin floats to an unknown value. When V_{DD} is above the transistor threshold voltage of the device, the output starts to be pulled low. After the V_{DD} is above the POR/BOR trip point (V_{BOR}/V_{POR}), the resistor network's wiper is loaded with the POR value (midscale). The volatile memory determines the analog output (V_{OUT}) pin voltage. After the device is powered up, the user can update the device's memory.

When the rising V_{DD} voltage crosses the V_{POR} trip point, the following occurs:

- The nonvolatile DAC register value is latched into volatile DAC register.
- The nonvolatile Configuration bit values are latched into volatile Configuration bits.
- The POR Status bit is set ('1').
- The reset delay timer (t_{PORD}) starts; when the reset delay timer (t_{PORD}) times out, the I^2C serial interface is operational. During this delay time, the I^2C interface will not accept commands.
- The Device Memory Address pointer is forced to 00h.

The Analog Output (V_{OUT}) state is determined by the state of the volatile Configuration bits and the DAC register. This is called a Power-on Reset (event).

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

4.1.2 BROWN-OUT RESET

The Brown-out Reset occurs when a device has power applied to it and that power (voltage) drops below the specified range.

When the falling V_{DD} voltage crosses the V_{POR} trip point (BOR event), the following occurs:

- The serial interface is disabled.
- EEPROM writes are disabled.
- The device is forced into a Power-Down state (PDnB:PDnA = '11'). Analog circuitry is turned off.
- The volatile DAC register is forced to 000h.
- Volatile Configuration bits VRnB:VRnA and Gx are forced to '0'.

If the V_{DD} voltage decreases below the V_{RAM} voltage, all volatile memory may become corrupted.

As the voltage recovers above the V_{POR}/V_{BOR} voltage, see **Section 4.1.1 "Power-on Reset"**.

Serial commands not completed due to a brown-out condition may cause the memory location (volatile and nonvolatile) to become corrupted.

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

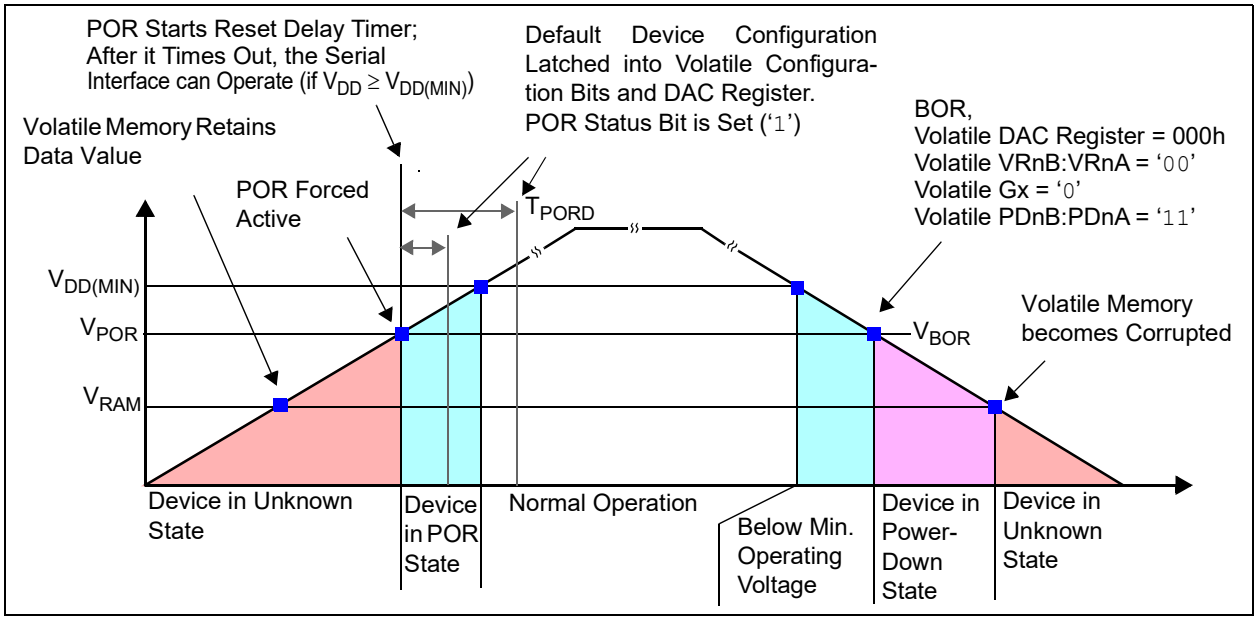

FIGURE 4-1: *Power-On/Brown-Out Reset Operation.*

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4.2 Device Memory

User memory includes the following types:

- **Volatile Register Memory (RAM)**
- **Nonvolatile Register Memory**
- **Device Configuration Memory**

Each memory address is 16 bits wide. There are up to 17 nonvolatile user control bits that do not reside in memory-mapped register space (see **Section 4.2.3 "Device Configuration Memory"**).

4.2.1 VOLATILE REGISTER MEMORY (RAM)

There are up to twelve volatile memory locations:

- DAC0 through DAC7 Output Value registers
- V_{REF} Select register
- Power-Down Configuration register
- Gain and STATUS register
- WiperLock Technology STATUS register

The volatile memory starts functioning when the device V_{DD} is at (or above) the RAM retention voltage (V_{RAM}). The volatile memory will be loaded with the default device values when the V_{DD} rises across the V_{POR}/V_{BOR} voltage trip point.

4.2.2 NONVOLATILE REGISTER MEMORY

This device family uses the nonvolatile memory for the DAC output value and Configuration registers:

- Nonvolatile DAC0 through DAC7 Output Value registers
- Nonvolatile V_{REF} Select register
- Nonvolatile Power-Down Configuration register
- Nonvolatile Gain and I^2C Address register

The nonvolatile memory starts functioning below the device's V_{POR}/V_{BOR} trip point, and is loaded into the corresponding volatile registers whenever the device rises above the POR/BOR voltage trip point.

The device starts writing the nonvolatile (EEPROM) memory location at the completion of the serial interface command, after the Acknowledge pulse of the `WRITE` Single command. Continuous write commands addressing the nonvolatile memory are not permitted.

Note:	When the nonvolatile memory is written, the corresponding volatile memory is **not** modified.

Nonvolatile DAC registers enable the stand-alone operation of the device (without microcontroller control) after being programmed to the desired value.

4.2.3 DEVICE CONFIGURATION MEMORY

There are up to seventeen nonvolatile user bits that are not directly mapped into the address space. These nonvolatile device Configuration bits control the following functions:

- WiperLock technology for DAC registers and Configuration (2 bits per DAC)
- I^2C Slave Address Write Protect (Lock)

The STATUS register shows the states of the device WiperLock technology Configuration bits. The STATUS register is described in Register 4-6.

The operation of WiperLock technology is discussed in **Section 4.2.6 "WiperLock Technology"**, while I^2C Slave Address Write Protect is discussed in **Section 4.2.7 "I2C Slave Address Write Protect"**.

4.2.4 UNIMPLEMENTED REGISTER BITS

`READ` commands of a valid location will read unimplemented bits as '`0`'.

4.2.5 UNIMPLEMENTED (RESERVED) LOCATIONS

Normal (voltage) commands (`READ` or `WRITE`) to any unimplemented memory address (reserved) will result in a command error condition (NACK). `READ` commands of a reserved location will read bits as '`1`'.

High-Voltage commands (enable or disable) to any unimplemented Configuration bits will result in a command error condition (NACK).

4.2.5.1 Default Factory POR Memory State of Nonvolatile Memory (EEPROM)

Table 4-2 shows the default factory POR initialization of the device memory map for the 8, 10 and 12-bit devices. In case of volatile memory devices (MCP47FVBXX), the factory default values cannot be modified.

Note:	The volatile memory locations will be determined by the nonvolatile memory states (registers and device Configuration bits).

TABLE 4-1: MCP47FXBX4/8 MEMORY MAP

Address	Function	Config Bit(1)	Quad	Octal
00h	Volatile DAC0 Register	CL0	Y	Y
01h	Volatile DAC1 Register	CL1	Y	Y
02h	Volatile DAC2 Register	CL2	Y	Y
03h	Volatile DAC3 Register	CL3	Y	Y
04h	Volatile DAC4 Register	CL4	—	Y
05h	Volatile DAC5 Register	CL5	—	Y
06h	Volatile DAC6 Register	CL6	—	Y
07h	Volatile DAC7 Register	CL7	—	Y
08h	V_{REF} Register	—	Y	Y
09h	Power-Down Register	—	Y	Y
0Ah	Gain and STATUS Register	—	Y	Y
0Bh	WiperLock™ Technology STATUS Register	—	Y	Y

Address	Function	Config Bit(1)	Quad	Octal
10h	Nonvolatile DAC0 Register	DL0	Y	Y
11h	Nonvolatile DAC1 Register	DL1	Y	Y
12h	Nonvolatile DAC2 Register	DL2	Y	Y
13h	Nonvolatile DAC3 Register	DL3	Y	Y
14h	Nonvolatile DAC4 Register	DL4	—	Y
15h	Nonvolatile DAC5 Register	DL5	—	Y
16h	Nonvolatile DAC6 Register	DL6	—	Y
17h	Nonvolatile DAC7 Register	DL7	—	Y
18h	Nonvolatile V_{REF} Register	—	Y	Y
19h	Nonvolatile Power-Down Register	—	Y	Y
1Ah	NV Gain and I^2C 7-bits Slave Address	SALCK	Y	Y
1Bh	Reserved	—	—	—

Volatile Memory Address Range

Nonvolatile Memory Address Range

Note 1: Device Configuration Memory bits require a high-voltage enable or disable command ($\overline{LATn}$ = V_{IHH}) to modify the bit value.

TABLE 4-2: FACTORY DEFAULT POR/BOR VALUES

Address	Function	POR/BOR Value		
		8-bit	10-bit	12-bit
00h	Volatile DAC0 Register	7Fh	1FFh	7FFh
01h	Volatile DAC1 Register	7Fh	1FFh	7FFh
02h	Volatile DAC2 Register	FFh	3FFh	FFFh
03h	Volatile DAC3 Register	FFh	3FFh	FFFh
04h	Volatile DAC4 Register	FFh	3FFh	FFFh
05h	Volatile DAC5 Register	FFh	3FFh	FFFh
06h	Volatile DAC6 Register	FFh	3FFh	FFFh
07h	Volatile DAC7 Register	FFh	3FFh	FFFh
08h	V_{REF} Register	0000h	0000h	0000h
09h	Power-Down Register	0000h	0000h	0000h
0Ah	Gain and STATUS Register	0080h	0080h	0080h
0Bh	WiperLock™ Technology STATUS Register	0000h	0000h	0000h

Address	Function	POR/BOR Value		
		8-bit	10-bit	12-bit
10h	Nonvolatile DAC0 Register	7Fh	1FFh	7FFh
11h	Nonvolatile DAC1 Register	7Fh	1FFh	7FFh
12h	Nonvolatile DAC2 Register	FFh	3FFh	FFFh
13h	Nonvolatile DAC3 Register	FFh	3FFh	FFFh
14h	Nonvolatile DAC4 Register	FFh	3FFh	FFFh
15h	Nonvolatile DAC5 Register	FFh	3FFh	FFFh
16h	Nonvolatile DAC6 Register	FFh	3FFh	FFFh
17h	Nonvolatile DAC7 Register	FFh	3FFh	FFFh
18h	Nonvolatile V_{REF} Register	0000h	0000h	0000h
19h	Nonvolatile Power-Down Register	0000h	0000h	0000h
1Ah	NV Gain and I^2C 7-bit Slave Address(1)	00E0h	00E0h	00E0h
1Bh	Reserved(2)	—	—	—

Volatile Memory Address Range

Nonvolatile Memory Address Range

Note 1: Default I^2C 7-bit Slave Address is '`110 0000`' and the SALCK bit is enabled ('`1`').

2: `READ` or `WRITE` commands to a reserved memory location will generate a NACK.

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4.2.6 WIPERLOCK TECHNOLOGY

The MCP47FXBX4/8 WiperLock technology allows application-specific device settings (DAC register and configuration) to be secured without requiring the use of an additional write-protect pin. There are two Configuration bits (DLn:CLn) for each DAC channel (DAC0 through DAC7).

Dependent on the state of the DLn:CLn Configuration bits, WiperLock technology prevents the serial commands from the following actions on the DACn registers and bits:

- Writing to the specified volatile DACn register memory location
- Writing to the specified nonvolatile DACn register memory location
- Writing to the specified volatile DACn Configuration bits
- Writing to the specified nonvolatile DACn Configuration bits

Each pair of these Configuration bits controls one of the four modes. These modes are shown in Table 4-4. The addresses for the Configuration bits are shown in Table 4-4.

To modify the Configuration bits, the HVC pin must be forced to the V_{IHH} state and then an enable or disable command must be received for the desired pair of DAC register addresses.

Example: To modify the CL0 bit, the enable or disable command specifies address 00h, while to modify the DL0 bit, the enable or disable command specifies address 10h.

Refer to **Section 7.4.2 "Enable Configuration Bit (High-Voltage)"** and **Section 7.4.3 "Disable Configuration Bit (High-Voltage)"** commands for operation.

Note: During device communication, if the device address/command combination is invalid or an unimplemented address is specified, the MCP47FXBX4/8 will NACK that byte. To reset the I²C state machine, the I²C communication must detect a Start bit.

4.2.6.1 POR/BOR Operation with WiperLock Technology Enabled

The WiperLock Technology state is not affected by a POR/BOR event. A POR/BOR event will load the volatile DACn register values with the nonvolatile or default factory values (in case of volatile memory only devices).

4.2.7 I²C SLAVE ADDRESS WRITE PROTECT

The MCP47FEBX4/8 I²C Slave Address is stored in the EEPROM memory. This allows the address to be modified to the application's requirement. To ensure that the I²C Slave address is not unintentionally modified, the memory has a high-voltage write protect bit. This Configurations bit is shown in Table 4-3.

Note: To modify the SALCK bit, the Enable or Disable command specifies address 1Ah.

TABLE 4-3: SALCK FUNCTIONAL DESCRIPTION

SALCK	Operation
1	The nonvolatile I²C Slave Address bits (ADD6:ADD2) are locked
0	The nonvolatile I²C Slave Address bits (ADD6:ADD2) are unlocked

TABLE 4-4: WIPERLOCK™ TECHNOLOGY CONFIGURATION BITS - FUNCTIONAL DESCRIPTION

DLn:CLn(1)	Register/Bits				Comments
	DACn Wiper		DACn Configuration(1)		
	Volatile	Nonvolatile	Volatile	Nonvolatile	
11	Locked	Locked	Locked	Locked	All DACn registers are locked.
10	Locked	Locked	Unlocked	Locked	All DACn registers are locked, except for volatile DACn Configuration registers. This allows operation of Power-Down modes.
01	Unlocked	Locked	Unlocked	Locked	Volatile DACn registers unlocked, nonvolatile DACn registers locked.
00	Unlocked	Unlocked	Unlocked	Unlocked	All DACn registers are unlocked.

Note 1: The state of these Configuration bits (DLn:CLn) is reflected in WLnB:WLnA bits, as shown in Register 4-6. DAC Configuration bits include Voltage Reference Control bits (VRnB:VRnA), Power-Down Control bits (PDnB:PDnA), and Output Gain bits (Gx).

4.2.8 DEVICE REGISTERS

Register 4-1 shows the format of the DAC Output Value registers for both volatile and nonvolatile memory locations. These registers will be either 8 bits, 10 bits, or 12 bits wide. The values are right justified.

REGISTER 4-1: DAC0 TO DAC7 OUTPUT VALUE REGISTERS ADDRESSES 00H THROUGH 07H/10H THROUGH 17H (VOLATILE/NONVOLATILE)

	U-0	U-0	U-0	U-0	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
12-bit	—	—	—	—	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
10-bit	—	—	—	—	—(1)	—(1)	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
8-bit	—	—	—	—	—(1)	—(1)	—(1)	—(1)	D07	D06	D05	D04	D03	D02	D01	D00
	bit 15															bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
= 12-bit device	= 10-bit device	= 8-bit device	

12-bit	10-bit	8-bit	
bit 15-12	bit 15-10	bit 15-8	**Unimplemented:** Read as ‘0’
bit 11-0	—	—	**D11-D00:** DAC Output Value - 12-bit devices FFFh =Full-Scale output value 7FFh =Mid-Scale output value 000h =Zero-Scale output value
—	bit 9-0	—	**D09-D00:** DAC Output Value - 10-bit devices 3FFh =Full-Scale output value 1FFh =Mid-Scale output value 000h =Zero-Scale output value
—	—	bit 7-0	**D07-D00:** DAC Output Value - 8-bit devices FFh =Full-Scale output value 7Fh =Mid-Scale output value 000h=Zero-Scale output value

Note 1: Unimplemented bit, read as ‘0’.

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Register 4-2 shows the format of the Voltage Reference Control register. Each DAC has two bits to control the source of the DAC's voltage reference. This register is for both volatile and nonvolatile memory locations.

REGISTER 4-2: VOLTAGE REFERENCE (VREF) CONTROL REGISTER ADDRESSES 08H AND 18H (VOLATILE/NONVOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
Octal	VR7B	VR7A	VR6B	VR6A	VR5B	VR5A	VR4B	VR4A	VR3B	VR3A	VR2B	VR2A	VR1B	VR1A	VR0B	VR0A
Quad	__(1)	__(1)	__(1)	__(1)	__(1)	__(1)	__(1)	__(1)	VR3B	VR3A	VR2B	VR2A	VR1B	VR1A	VR0B	VR0A
	bit 15															bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad-channel device		= Octal-channel device	

Octal	Quad	
—	bit 15-8	**Unimplemented:** Read as '0'
bit 15-0	bit 7-0	**VRnB-VRnA:** DAC Voltage Reference Control bits 11 =V_{REF} pin (buffered); V_{REF} buffer enabled 10 =V_{REF} pin (unbuffered); V_{REF} buffer disabled 01 =Internal band gap (1.22V typical); V_{REF} buffer enabled V_{REF} voltage driven when powered down 00 =V_{DD} (unbuffered); V_{REF} buffer disabled Use this state with Power-Down bits for lowest current.

Note 1: Unimplemented bit, read as '0'.

Register 4-3 shows the format of the Power-Down Control register. Each DAC has two bits to control the Power-Down state of the DAC. This register is for both volatile and nonvolatile memory locations.

REGISTER 4-3: POWER-DOWN CONTROL REGISTER (VOLATILE/NONVOLATILE) (ADDRESSES 09h, 19h)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
Octal	PD7B	PD7A	PD6B	PD6A	PD5B	PD5A	PD4B	PD4A	PD3B	PD3A	PD2B	PD2A	PD1B	PD1A	PD0B	PD0A
Quad	__(1)	__(1)	__(1)	__(1)	__(1)	__(1)	__(1)	__(1)	PD0B	PD0A	PD0B	PD0A	PD0B	PD0A	PD0B	PD0A
	bit 15															bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
= Quad-channel device		= Octal-channel device	

Octal	Quad	
—	bit 15-8	**Unimplemented:** Read as ‘1’
bit 15-0	bit 7-0	**PDnB-PDnA:** DAC Power-Down Control bits(2) 11 =Powered Down - V_{OUT} is open circuit 10 =Powered Down - V_{OUT} is loaded with a 125 kΩ resistor to ground 01 =Powered Down - V_{OUT} is loaded with a 1 kΩ resistor to ground 00 =Normal Operation (not powered down)

Note 1: Unimplemented bit, read as ‘0’.

2: See Table 5-4 for more details.

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Register 4-4 shows the format of the volatile Gain Control and System STATUS register. Each DAC has one bit to control the gain of the DAC and three Status bits.

REGISTER 4-4: GAIN CONTROL AND SYSTEM STATUS REGISTER ADDRESS 0Ah (VOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/C-1	R-0	U-0	U-0	U-0	U-0	U-0	U-0
Octal	G7	G6	G5	G4	G3	G2	G1	G0	POR	EEWA	—	—	—	—	—	—
Quad	—(1)	—(1)	—(1)	—(1)	G3	G2	G1	G0	POR	EEWA	—	—	—	—	—	—
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	C = Clear-able bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
= Quad-channel device		= Octal-channel device	

Octal	Quad	
—	bit 15-12	**Unimplemented:** Read as ‘0’
bit 15-8	bit 11-8	**Gn:** DAC Channel n Output Driver Gain Control bit 1 = 2x Gain 0 = 1x Gain
bit 7	bit 7	**POR:** Power-on Reset (Brown-out Reset) Status bit This bit indicates if a POR or BOR event has occurred since the last READ command of this register. Reading this register clears the state of the POR Status bit. 1 = A POR (BOR) event has occurred since the last read of this register. Reading this register clears this bit. 0 = A POR (BOR) event has not occurred since the last read of this register.
bit 6	bit 6	**EEWA:** EEPROM Write Active Status bit This bit indicates if the EEPROM Write Cycle is occurring. 1 = An EEPROM Write Cycle is currently occurring. Only serial commands to the volatile memory are allowed. 0 = An EEPROM Write Cycle is NOT currently occurring.
bit 5-0	bit 5-0	**Unimplemented:** Read as ‘0’

Note 1: Unimplemented bit, read as ‘0’.

Register 4-5 shows the format of the nonvolatile Gain Control register. Each DAC has one bit to control the gain of the DAC.

REGISTER 4-5: GAIN CONTROL AND I²C SLAVE ADDRESS REGISTER ADDRESS 1Ah (NONVOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
Octal	G7	G6	G5	G4	G3	G2	G1	G0	ADLCK	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
Quad	—(1)	—(1)	—(1)	—(1)	G3	G2	G1	G0	ADLCK	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
= Quad-channel device		= Octal-channel device	

Octal	**Quad**	
—	bit 15-12	**Unimplemented:** Read as ‘0’
bit 15-8	bit 11-8	**Gn:** DACn Output Driver Gain Control bits 1 = 2x Gain 0 = 1x Gain
bit 7	bit 7	**ADLCK:** I²C Address Lock Status bit (reflects the state of the high-voltage SALCK bit). 1 = I²C Slave Address is Locked (requires HV command to disable, so I²C address can be changed) 0 = I²C Slave Address is NOT Locked, the nonvolatile I²C Slave Address can be changed
bit 6-0	bit 6-0	**ADD6-ADD0:** I²C 7-bit Slave Address bits. For **nonvolatile** devices, the ADD6-ADD2 bits form the upper five bits of the I²C address and can be user-modified. For **volatile** devices, the upper five bits of the I²C address are fixed at '0b11000' and cannot be changed by the user. Other values could be available on demand, contact a sales representative for more information. The lower two bits are determined by the state of the A0 and A1 pins. A V_{IH} level corresponds to a bit value of '1', while a V_{IL} level to a '0'. Leaving the pins unconnected is the equivalent of a '0' bit value.

Note 1: Unimplemented bit, read as ‘0’.

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Register 4-6 shows the format of the DAC WiperLock technology STATUS register.

REGISTER 4-6: DAC WIPERLOCK™ TECHNOLOGY STATUS REGISTER (VOLATILE, ADDRESS 0BH)

	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)
Octal	WL7B	WL7A	WL6B	WL6A	WL5B	WL5A	WL4B	WL4A	WL3B	WL3A	WL2B	WL2A	WL1B	WL1A	WL0B	WL0A
Quad	—(2)	—(2)	—(2)	—(2)	—(2)	—(2)	—(2)	—(2)	WL3B	WL3A	WL2B	WL2A	WL1B	WL1A	WL0B	WL0A
	bit 15															bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
= Quad-channel device		= Octal-channel device	

Octal	Quad	
—	bit 15-8	**Unimplemented:** Read as ‘0’
bit 15-0	bit 7-0	**WLnB-WLnA:** WiperLock™ Technology Status bits: These bits reflect the state of the DLn:CLn nonvolatile Configuration bits. 11 =DAC Wiper and DAC Configuration (volatile and nonvolatile registers) are locked (DLn = CLn = Enabled). 10 =DAC Wiper (volatile and nonvolatile) and DAC Configuration (nonvolatile registers) are locked (DLn = Enabled; CLn = Disabled). 01 =DAC Wiper (nonvolatile) and DAC Configuration (nonvolatile registers) are locked (DLn = Disabled; CLn = Enabled). 00 =DAC Wiper and DAC Configuration are unlocked (DLn = CLn = Disabled).

Note 1: POR value depends on the programmed values of the DLn:CLn Configuration bits. The devices are shipped with a default DLn:CLn Configuration bit state of ‘0’.

2: Unimplemented bit, read as ‘0’.

NOTES:

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5.0 DAC CIRCUITRY

The Digital-to-Analog Converter circuitry converts a digital value into its analog representation. The description shows the functional operation of the device.

The DAC circuit uses a resistor ladder implementation. Devices have up to eight DACs.

Figure 5-1 shows the functional block diagram for the MCP47FXBX4/8 DAC circuitry.

The functional blocks of the DAC include:

- **Resistor Ladder**
- **Voltage Reference Selection**
- **Output Buffer/V_{OUT} Operation**
- **Internal Band Gap**
- **Latch Pins (LATn)**
- **Power-Down Operation**

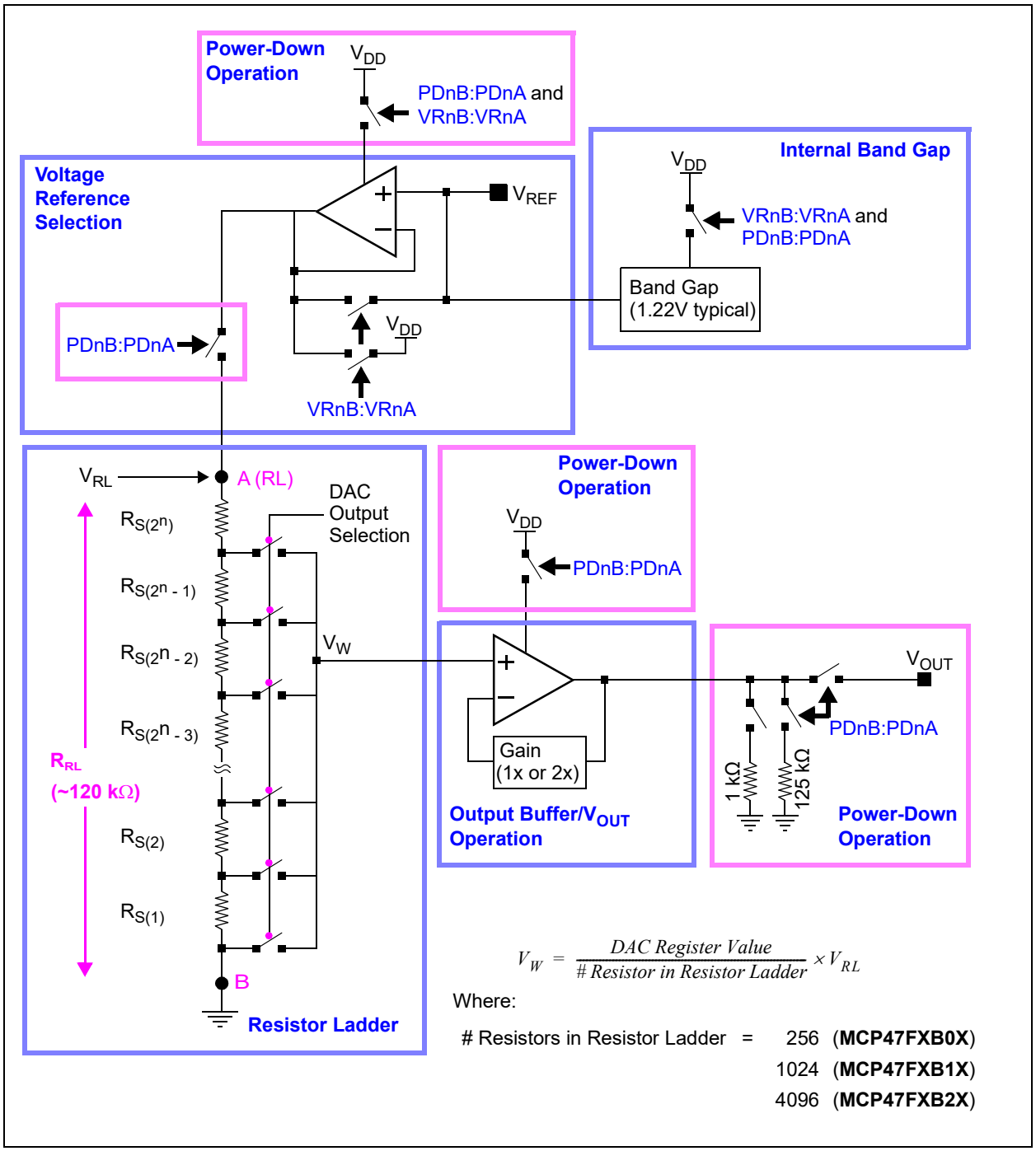
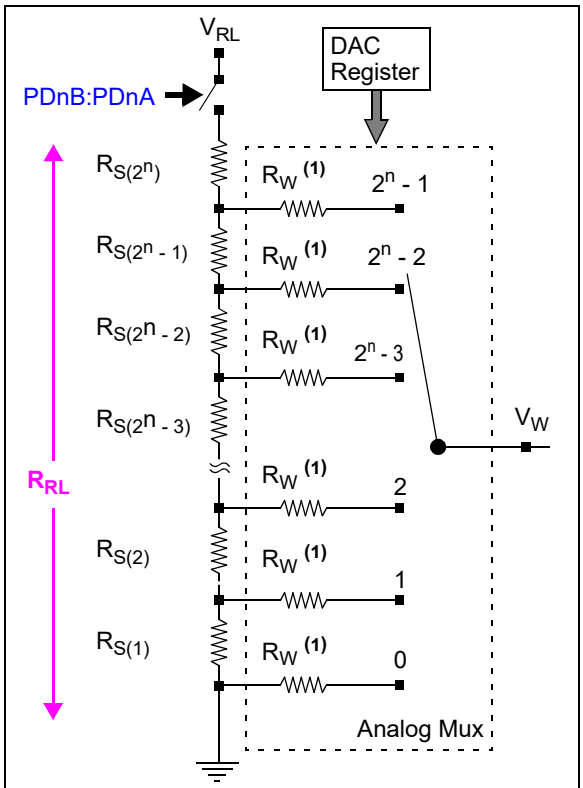


FIGURE 5-1: *MCP47FXBX4/8 DAC Module Block Diagram.*

5.1 Resistor Ladder

The resistor ladder is a digital potentiometer with the B Terminal internally grounded and the A Terminal connected to the selected reference voltage (see Figure 5-2). The volatile DAC register controls the wiper position. The wiper voltage (V_W) is proportional to the DAC register value divided by the number of resistor elements (R_S) in the ladder (256, 1024 or 4096) related to the V_{RL} voltage.

The output of the resistor network will drive the input of an output buffer.



Note 1: The analog switch resistance (R_W) does not affect performance due to the voltage divider configuration.

FIGURE 5-2: *Resistor Ladder Model.*

The resistor network is made of these three parts:

- Resistor ladder (string of R_S elements)
- Wiper switches
- DAC register decode

The resistor ladder (R_{RL}) has a typical impedance of approximately 120 kΩ. This resistance may vary from device to device by up to ±20%. Since this is a voltage divider configuration, the actual R_{RL} resistance does not affect the output given a fixed voltage at V_{RL}.

Equation 5-1 shows the calculation for the step resistance:

EQUATION 5-1: R_S CALCULATION

$$R_S = \frac{R_{RL}}{(256)} \quad \text{8-bit Device}$$

$$R_S = \frac{R_{RL}}{(1024)} \quad \text{10-bit Device}$$

$$R_S = \frac{R_{RL}}{(4096)} \quad \text{12-bit Device}$$

Note: The maximum wiper position is $2^n - 1$, while the number of resistors in the resistor ladder is 2^n. This means that when the DAC register is at full scale, there is one resistor element (R_S) between the wiper and the V_{RL} voltage.

If the unbuffered V_{REF} pin is used as the V_{RL} voltage source, this voltage source should have a low output impedance.

When the DAC is powered down, the resistor ladder is disconnected from the selected reference voltage.

5.2 Voltage Reference Selection

The resistor ladder has up to four sources for the reference voltage. Two user control bits (VRnB:VRnA) are used to control the selection, with the selection connected to the V_{RL} node (see Figure 5-3 and Figure 5-4).

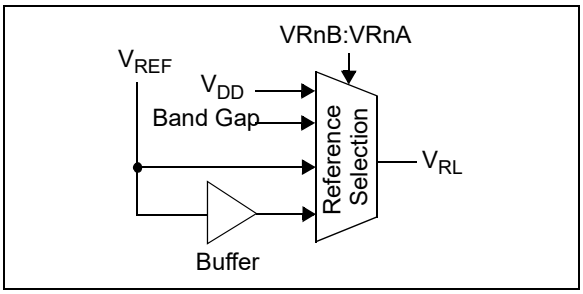


FIGURE 5-3: *Resistor Ladder Reference Voltage Selection Block Diagram.*

The four voltage source options for the resistor ladder are:

1. V_{DD} pin voltage
2. Internal voltage reference (V_{BG})
3. V_{REF} pin voltage unbuffered
4. V_{REF} pin voltage internally buffered

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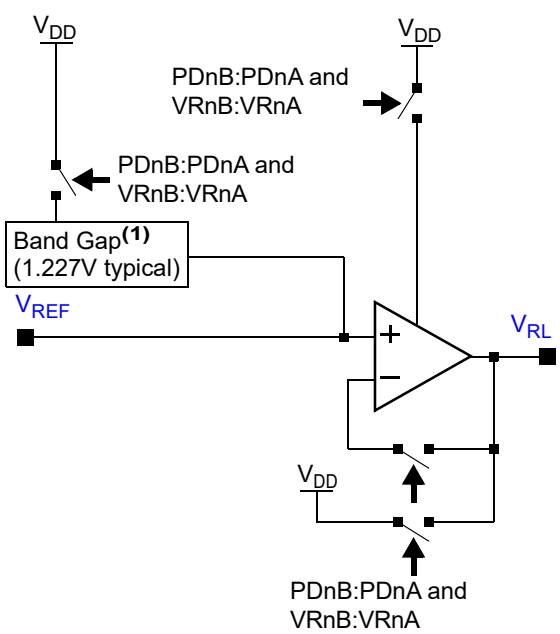
The selection of the voltage is specified with the volatile VRnB:VRnA Configuration bits (see Register 4-2). There are nonvolatile and volatile VRnB:VRnA Configuration bits. On a POR/BOR event, the state of the nonvolatile VRnB:VRnA Configuration bits is latched into the volatile VRnB:VRnA Configuration bits.

When the user selects the V_{DD} as reference, the V_{REF} pin voltage is not connected to the resistor ladder.



Note 1: The band gap voltage (V_{BG}) is 1.22V typical. The band gap output goes through the buffer with a 2x gain to create the V_{RL} voltage. See Table 5-1 for additional information on the band gap circuit.

FIGURE 5-4: *Reference Voltage Selection Implementation Block Diagram.*

If the V_{REF} pin is selected, then a selection has to be made between the Buffered and Unbuffered mode.

5.2.1 BUFFERED MODE

The V_{REF} pin voltage may be from 0.01V to V_{DD} - 0.04V. The input buffer (amplifier) provides low offset voltage, low noise, and a very high input impedance, with only minor limitations on the input range and frequency response.

Note 1: Any variation or noises on the reference source can directly affect the DAC output. The reference voltage needs to be as clean as possible for accurate DAC performance.

2: If the V_{REF} pin is tied to the V_{DD} voltage, the V_{DD} mode (VRnB:VRnA = '00') is recommended.

5.2.2 UNBUFFERED MODE

The V_{REF} pin voltage may be from V_{SS} to V_{DD}.

Note 1: The voltage source should have a low output impedance. If the voltage source has a high output impedance, then the voltage on the V_{REF} pin is lower than expected. The resistor ladder has a typical impedance of 140 kΩ and a typical capacitance of 29 pF.

2: If the V_{REF} pin is tied to the V_{DD} voltage, the V_{DD} mode (VRnB:VRnA = '00') is recommended.

5.2.3 BAND GAP MODE

If the internal band gap is selected, then the external V_{REF} pin should not be driven and should only use high-impedance loads.

The band gap output is buffered, but the internal switches limit the current that the output should source to the V_{REF} pin. The resistor ladder buffer is used to drive the band gap voltage for the cases of multiple DAC outputs. This ensures that the resistor ladders are always properly sourced when the band gap is selected.

5.3 Internal Band Gap

The internal band gap is designed to drive the resistor ladder buffer.

The resistance of a resistor ladder (R_{RL}) is targeted to be 140 kΩ (±40 kΩ), which means a minimum resistance of 100 kΩ.

The band gap selection can be used across the V_{DD} voltages while maximizing the V_{OUT} voltage ranges. For V_{DD} voltages below the 2 × Gain × V_{BG} voltage, the output for the upper codes will be clipped to the V_{DD} voltage. Table 5-1 shows the maximum DAC register code given device V_{DD} and Gain bit setting.

TABLE 5-1: V_{OUT} USING BAND GAP

V_{DD}(3)	DAC Gain	Max DAC Code(1)			Comment
		12-bit	10-bit	8-bit	
5.5	1	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 2.44V(2)
	2	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 4.88V(2)
2.7	1	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 2.44V(2)
	2	8CDh	233h	8Ch	~ 0 to 56% range

Note 1: Without the V_{OUT} pin voltage being clipped.
2: When V_{BG} = 1.22V typical.
3: Band gap performance achieves full performance starting from a V_{DD} of 2.0V.

5.4 Output Buffer/V_{OUT} Operation

The Output Driver buffers the wiper voltage (V_W) of the resistor ladder.

The DAC output is buffered with a low power and precision output amplifier (op amp). This amplifier provides a rail-to-rail output with low offset voltage and low noise. The amplifier's output can drive the resistive and high-capacitive loads without oscillation. The amplifier provides a maximum load current which is enough for most programmable voltage reference applications. See **Section 1.0 "Electrical Characteristics"** for the specifications of the output amplifier.

Note:	The load resistance must be kept higher than 5 kΩ for the stable and expected analog output (to meet electrical specifications).

Figure 5-5 shows the block diagram of the output driver circuit.

The user can select the output gain of the output amplifier. The gain options are:

a) Gain of 1, when either the V_{DD}, external V_{REF}, or Band Gap mode are used. In case of the Band Gap mode, the effective gain is 2, see **Section 5.3 "Internal Band Gap"**.

b) Gain of 2, when the external V_{REF} or internal Band Gap modes are used. In case of the Band Gap mode, the effective gain is 4, see **Section 5.3 "Internal Band Gap"**.

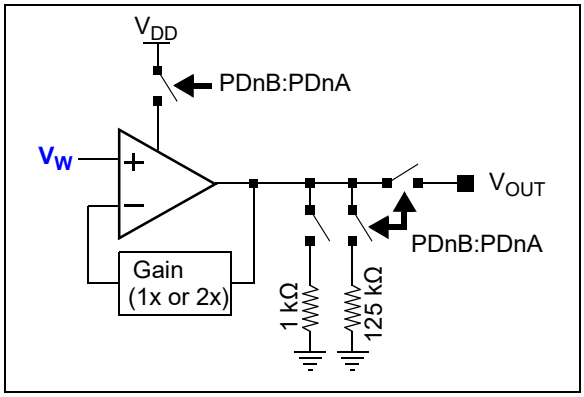


FIGURE 5-5: *Output Driver Block Diagram.*

5.4.1 PROGRAMMABLE GAIN

The amplifier's gain is controlled by the Gain (G) Configuration bit (see Register 4-5) and the V_{RL} reference selection.

The volatile Gain bit value can be modified by:

- POR events
- BOR events
- I²C `WRITE` commands

5.4.2 OUTPUT VOLTAGE

The volatile DAC register values, along with the device's Configuration bits, control the analog V_{OUT} voltage. The volatile DAC register's value is unsigned binary. The formula for the output voltage is given in Equation 5-2. Table 5-5 shows examples of volatile DAC register values and the corresponding theoretical V_{OUT} voltage for the MCP47FXBX4/8 devices.

EQUATION 5-2: CALCULATING OUTPUT VOLTAGE (V_{OUT})

$$V_{OUT} = \frac{V_{RL} \times DAC\ Register\ Value}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

Resistors in R-Ladder = 4096 (**MCP47FXB2X**)
1024 (**MCP47FXB1X**)
256 (**MCP47FXB0X**)

Note:	When Gain = 2 (V_{RL} = V_{REF}) and if V_{REF} > V_{DD}/2, the V_{OUT} voltage will be limited to V_{DD}. So if V_{REF} = V_{DD}, then the V_{OUT} voltage will not change for volatile DAC register values mid-scale and greater, since the op amp is at full-scale output.

The following events update the DAC register value and therefore the analog voltage output (V_{OUT}):

- POR
- BOR
- `WRITE` command

The V_{OUT} voltage starts driving to the new value after the event has occurred.

5.4.3 STEP VOLTAGE (V_S)

The step voltage depends on the device resolution and the calculated output voltage range. 1 LSb is defined as the ideal voltage difference between two successive codes. The step voltage can be easily calculated by using Equation 5-3 (DAC register value is equal to 1). Theoretical step voltages are shown in Table 5-2 for several V_{REF} voltages.

EQUATION 5-3: V_S CALCULATION

$$V_S = \frac{V_{RL}}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

Resistors in R-Ladder = 4096 (**12-bit**)
1024 (**10-bit**)
256 (**8-bit**)

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TABLE 5-2: THEORETICAL STEP VOLTAGE (V_S)[1]

	V_{REF}					
	5.0	**2.7**	**1.8**	**1.5**	**1.0**	
V_S	1.22 mV	659 µV	439 µV	366 µV	244 µV	12-bit
	4.88 mV	2.64 mV	1.76 mV	1.46 mV	977 µV	10-bit
	19.5 mV	10.5 mV	7.03 mV	5.86 mV	3.91 mV	8-bit

Note 1: When Gain = 1x, $V_{FS} = V_{RL}$, and V_{ZS} = 0V.

5.4.4 OUTPUT SLEW RATE

Figure 5-6 shows an example of the slew rate for the V_{OUT} pin. The slew rate can be affected by the characteristics of the circuit connected to the V_{OUT} pin.

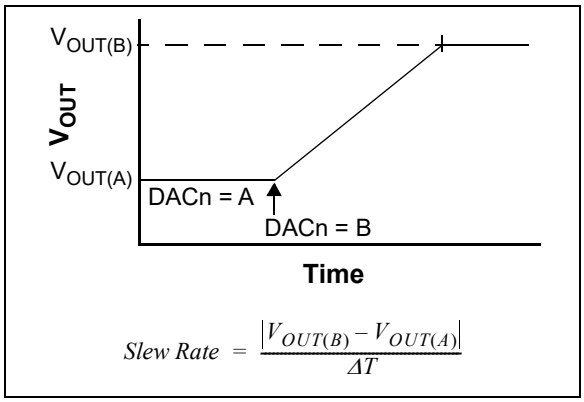

FIGURE 5-6: *V_{OUT} Pin Slew Rate.*

5.4.4.1 Small Capacitive Load

With a small capacitive load (C_L), the output buffer's current is not affected. But the V_{OUT} pin's voltage is not a step transition from one output value (DAC register value) to the next output value. The change of the V_{OUT} voltage is limited by the output buffer's characteristics, so the V_{OUT} pin voltage will have a slope from the old voltage to the new one. This slope is fixed for the output buffer and is referred to as the buffer slew rate (SR_{BUF}).

5.4.4.2 Large Capacitive Load

With a larger capacitive load, the slew rate is determined by two factors:

- The output buffer's short-circuit current (I_{SC})
- The V_{OUT} pin's external load

I_{OUT} cannot exceed the output buffer's short-circuit current (I_{SC}), which fixes the output buffer slew rate (SR_{BUF}). The voltage on the capacitive load, V_{CL}, changes at a rate proportional to I_{OUT}, which fixes a capacitive load slew rate (SR_{CL}).

The V_{CL} voltage slew rate is limited to the slower of the output buffer's internally set slew rate (SRBUF) and the capacitive load slew rate (SR_{CL}).

5.4.5 DRIVING RESISTIVE AND CAPACITIVE LOADS

The V_{OUT} pin can drive up to 100 pF of capacitive load in parallel with a 5 kΩ resistive load (to meet electrical specifications).

V_{OUT} drops slowly as the load resistance decreases after about 3.5 kΩ. It is recommended to use a load with R_L greater than 5 kΩ.

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response with overshoot and ringing in the step response. That is, since the V_{OUT} pin's voltage does not quickly follow the buffer's input voltage (due to the large capacitive load), the output buffer will overshoot the desired target voltage. Once the driver detects this overshoot, it compensates by forcing it to a voltage below the target. This causes voltage ringing on the V_{OUT} pin.

When driving large capacitive loads with the output buffer, a small series resistor (R_{ISO}) at the output (see Figure 5-7) improves the output buffer's stability (feedback loop's phase margin) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

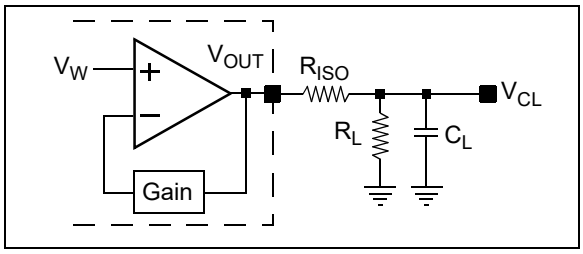

FIGURE 5-7: *Circuit to Stabilize Output Buffer for Large Capacitive Loads (C_L).*

The R_{ISO} resistor value for your circuit needs to be selected. The resulting frequency response peaking and step response overshoot for this R_{ISO} resistor value should be verified on the bench. Modify the R_{ISO}'s resistance value until the output characteristics meet your requirements.

A method to evaluate the system's performance is to inject a step voltage on the V_{REF} pin and observe the V_{OUT} pin's characteristics.

Note: Additional insight into circuit design for driving capacitive loads can be found in AN884 – *"Driving Capacitive Loads with Op Amps"* (DS00884).

5.5 Power-Down Operation

To allow the application to conserve power when the DAC operation is not required, three Power-Down modes are available. The Power-Down Configuration bits (PDnB:PDnA) control the power-down operation (Figure 5-8 and Table 5-3). On devices with multiple DACs, each DACs Power-Down mode is individually controllable. All Power-Down modes do the following:

- Turn off most DAC module's internal circuits (output op amp, resistor ladder, et al.)
- Op amp output becomes high impedance to the V_{OUT} pin
- Disconnect the resistor ladder from the Reference Voltage (V_{RL})
- Retain the value of the volatile DAC register and Configuration bits and the nonvolatile (EEPROM) DAC register and Configuration bits

Depending on the selected Power-Down mode, the following will occur:

- V_{OUT} pin is switched to one of the two resistive pull-downs (see Table 5-4):
  - 125 kΩ (typical)
  - 1 kΩ (typical)
- Op amp is powered down and the V_{OUT} pin becomes high impedance

There is a delay (T_{PDE}) between the PDnB:PDnA bits changing from '00' to either '01', '10' or '11' with the op amp no longer driving the V_{OUT} output and the pull-down resistors sinking current.

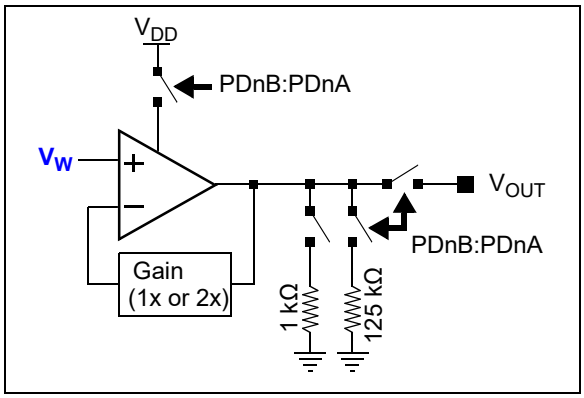

FIGURE 5-8: *V_{OUT} Power-Down Block Diagram.*

In any of the Power-Down modes where the V_{OUT} pin is not externally connected (sinking or sourcing current), the power-down current will typically be 680 nA for a quad-DAC device. As the number of DACs increases, the device's power-down current will also increase.

The Power-Down bits are modified by using a `WRITE` command to the volatile Power-Down register, or a POR event which transfers the nonvolatile Power-Down register to the volatile Power-Down register.

TABLE 5-3: POWER-DOWN BITS AND OUTPUT RESISTIVE LOAD

PDnB	PDnA	Function
0	0	Normal operation
0	1	1 kΩ resistor to ground
1	0	125 kΩ resistor to ground
1	1	Open circuit

Table 5-4 shows the current sources for the DAC based on the selected source of the DAC's reference voltage and if the device is in a normal operating mode or in one of the Power-Down modes.

TABLE 5-4: DAC CURRENT SOURCES

Device V_{DD} Current Source	PDnB:A = '00', VRnB:A =				PDnB:A ≠ '00', VRnB:A =			
	00	01	10	11	00	01	10	11
Output Op Amp	Y	Y	Y	Y	N	N	N	N
Resistor Ladder	Y	Y	N(1)	Y	N	N	N(1)	N
RL Op Amp	N	Y	N	Y	N	N	N	N
Band Gap	N	Y	N	N	N	Y	N	N

Note 1: Current is sourced from the V_{REF} pin, not the device V_{DD}.

Section 7.0 "I2C Device Commands" describes the I^2C commands for writing the power-down bits. The commands that can update the volatile PDnB:PDnA bits are:

- `Write` (normal and high-voltage)
- General Call Reset
- General Call Wake-up

Note: The I^2C serial interface circuit is not affected by the Power-Down mode. This circuit remains active in order to receive any command that might come from the I^2C master device.

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5.5.1 EXITING POWER-DOWN

When the device exits Power-Down mode, the following occurs:

- Disabled circuits (op amp, resistor ladder, et al.) are turned on
- The resistor ladder is connected to the selected Reference Voltage (V_{RL})
- The selected pull-down resistor is disconnected
- The V_{OUT} output will be driven to the voltage represented by the volatile DAC register's value and Configuration bits

The V_{OUT} output signal requires time as these circuits are powered up and the output voltage is driven to the specified value as determined by the volatile DAC register and Configuration bits.

Note:	Since the op amp and resistor ladder are powered-off (0V), the op amp's Input Voltage (V_W) can be considered 0V. There is a delay (T_{PDD}) between the PDnB:PDnA bits updating to '00' and the op amp driving the V_{OUT} output. The op amp's settling time (from 0V) needs to be taken into account to ensure the V_{OUT} voltage reflects the selected value.

The following events change the PDnB:PDnA bits to '00' and therefore exit the Power-Down mode. These are:

- Any I^2C `WRITE` command where the PDnB:PDnA bits are '00'
- I^2C General Call Wake-up command
- I^2C General Call Reset command (if nonvolatile PDnB:PDnA bits are '00').

Note:	On quad-channel devices, after issuing a General Call Wake-up command, a current higher than normal will be drawn. To avoid this issue, on quad-channel devices, General Call Wake-up should be followed by a General Call Reset command. No other functionality is affected.

5.5.2 RESET COMMANDS

When the MCP47FXBX4/8 devices are in the valid operating voltage range, the I^2C General Call Reset command forces a Reset event. This is similar to the POR, except that the Reset delay timer is not started.

If the I^2C interface bus does not seem to be responsive, the technique shown in **Section 8.1.3 "Software I^2C Interface Reset Sequence"** can be used to force the I^2C interface to reset.

5.6 DAC Registers, Configuration Bits, and Status Bits

The MCP47FXBX4/8 device family has both volatile and nonvolatile (EEPROM) memory options. Table 4-2 shows the volatile and nonvolatile memory and their interaction due to a POR event.

There are five Configuration bits, DAC registers, and two volatile status bits in both the volatile and nonvolatile memory. The DAC registers (volatile and nonvolatile) will be either twelve bits (MCP47FXB2X), ten bits (MCP47FEB1X), or eight bits (MCP47FXB0X) wide.

When the device is first powered-up, it automatically uploads the EEPROM memory values or factory default values (in case of MCP47FVBXX devices) to the volatile memory. The volatile memory determines the analog output (V_{OUT}) pin voltage. After the device is powered-up, the user can update the memory.

This memory is read and written through the I^2C interface. See **Section 6.0 "I^2C Serial Interface Module"** and **Section 7.0 "I2C Device Commands"** for more details on reading and writing the device's memory.

When the nonvolatile memory is written, the device starts writing the EEPROM cell at the Acknowledge pulse of the `WRITE` single memory location command.

Register 4-4 shows the operation of the device status bits and Table 4-2 shows the factory default value of a POR/BOR event for the device Configuration bits.

There are two status bits. These are only in volatile memory and indicate the status of the device. The POR bit indicates if the device V_{DD} is above or below the POR trip point. During normal operation, this bit should be '1'. The EEWA bit indicates if an EEPROM write cycle is in progress. While the EEWA bit is '1' (during the EEPROM writing), all commands are ignored, except for the `READ` command.

5.7 Latch Pins ($\overline{\text{LATn}}$)

The Latch pins control when the volatile DAC register value is transferred to the DAC wiper. This is useful for applications that need to synchronize the wiper(s) updates to an external event, such as zero crossing or updates to the other wipers on the device. The $\overline{\text{LAT}}$ pin functionality is asynchronous to the serial interface operation.

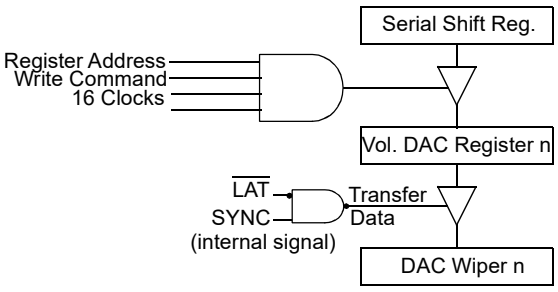
When the $\overline{\text{LAT}}$ pin is high, transfers from the volatile DAC register to the DAC wiper are inhibited. The volatile DAC register value(s) can continue to update.

When the $\overline{\text{LAT}}$ pin is low, the volatile DAC register value is transferred to the DAC wiper.

> **Note:** This allows the volatile DAC0 through DAC7 registers to be updated while the $\overline{\text{LATn}}$ pins are high, and to have outputs synchronously updated as the $\overline{\text{LATn}}$ pins are driven low.

Figure 5-9 shows the interaction of the $\overline{\text{LAT}}$ pin and the loading of the DAC Wiper n (from the volatile DAC register n). The transfers are level-driven. If the $\overline{\text{LAT}}$ pin is held low, the corresponding DAC wiper is updated as soon as the volatile DAC register value is updated.

The $\overline{\text{LAT}}$ pin allows the DAC wiper to be updated to an external event and have multiple DAC channels/devices updating at a common event.



$\overline{\text{LAT}}$	SYNC	Transfer Data	Comment
1	1	0	No Transfer
1	0	0	No Transfer
0	1	1	Vol. DAC Register n → DAC Wiper n
0	0	0	No Transfer

FIGURE 5-9: *$\overline{\text{LAT}}$ and DAC Interaction.*

Since the DAC wiper n is updated from the volatile DAC register n, all DACs that are associated with a given $\overline{\text{LAT}}$ pin can be updated synchronously.

If the application does not require synchronization, then this signal should be tied low.

Figure 5-10 shows two examples of using the $\overline{\text{LAT}}$ pin to control when the wiper register is updated relative to the value of a sine wave signal.

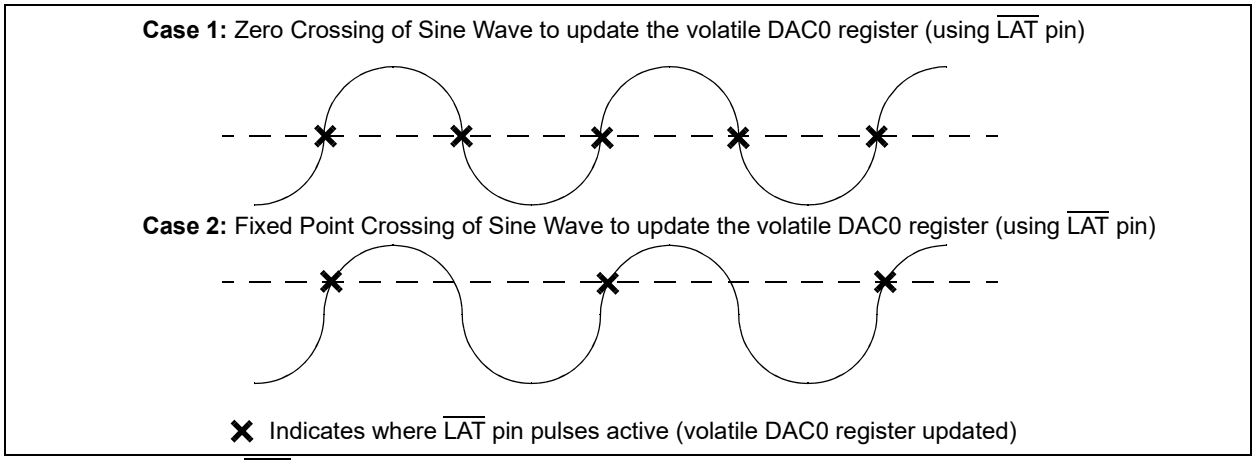


FIGURE 5-10: *$\overline{\text{LAT}}$ Pin Operation Example.*

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TABLE 5-5: DAC INPUT CODE VS. CALCULATED ANALOG OUTPUT (V_{OUT}) (V_{DD} = 5.0V)

Device	Volatile DAC Register Value	V_{RL}(1)	LSb		Gain Selection(2)	V_{OUT}(3)	
			Equation	µV		Equation	V
MCP47FXB2X (12-bit)	1111 1111 1111	5.0V	5.0V/4096	1,220.7	1x	V_{RL} ∗ (4095/4096) ∗ 1	4.998779
		2.5V	2.5V/4096	610.4	1x	V_{RL} ∗ (4095/4096) ∗ 1	2.499390
					2x(2)	V_{RL} ∗ (4095/4096) ∗ 2)	4.998779
	0111 1111 1111	5.0V	5.0V/4096	1,220.7	1x	V_{RL} ∗ (2047/4096) ∗ 1)	2.498779
		2.5V	2.5V/4096	610.4	1x	V_{RL} ∗ (2047/4096) ∗ 1)	1.249390
					2x(2)	V_{RL} ∗ (2047/4096) ∗ 2)	2.498779
	0011 1111 1111	5.0V	5.0V/4096	1,220.7	1x	V_{RL} ∗ (1023/4096) ∗ 1)	1.248779
		2.5V	2.5V/4096	610.4	1x	V_{RL} ∗ (1023/4096) ∗ 1)	0.624390
					2x(2)	V_{RL} ∗ (1023/4096) ∗ 2)	1.248779
	0000 0000 0000	5.0V	5.0V/4096	1,220.7	1x	V_{RL} ∗ (0/4096) * 1)	0
		2.5V	2.5V/4096	610.4	1x	V_{RL} ∗ (0/4096) * 1)	0
					2x(2)	V_{RL} ∗ (0/4096) * 2)	0
MCP47FEB1X (10-bit)	11 1111 1111	5.0V	5.0V/1024	4,882.8	1x	V_{RL} ∗ (1023/1024) ∗ 1	4.995117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} ∗ (1023/1024) ∗ 1	2.497559
					2x(2)	V_{RL} ∗ (1023/1024) ∗ 2	4.995117
	01 1111 1111	5.0V	5.0V/1024	4,882.8	1x	V_{RL} ∗ (511/1024) ∗ 1	2.495117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} ∗ (511/1024) ∗ 1	1.247559
					2x(2)	V_{RL} ∗ (511/1024) ∗ 2	2.495117
	00 1111 1111	5.0V	5.0V/1024	4,882.8	1x	V_{RL} ∗ (255/1024) ∗ 1	1.245117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} ∗ (255/1024) ∗ 1	0.622559
					2x(2)	V_{RL} ∗ (255/1024) ∗ 2	1.245117
	00 0000 0000	5.0V	5.0V/1024	4,882.8	1x	V_{RL} ∗ (0/1024) ∗ 1	0
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} ∗ (0/1024) ∗ 1	0
					2x(2)	V_{RL} ∗ (0/1024) ∗ 1	0
MCP47FXB0X (8-bit)	1111 1111	5.0V	5.0V/256	19,531.3	1x	V_{RL} ∗ (255/256) ∗ 1	4.980469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} ∗ (255/256) ∗ 1	2.490234
					2x(2)	V_{RL} ∗ (255/256) ∗ 2	4.980469
	0111 1111	5.0V	5.0V/256	19,531.3	1x	V_{RL} ∗ (127/256) ∗ 1	2.480469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} ∗ (127/256) ∗ 1	1.240234
					2x(2)	V_{RL} ∗ (127/256) ∗ 2	2.480469
	0011 1111	5.0V	5.0V/256	19,531.3	1x	V_{RL} ∗ (63/256) ∗ 1	1.230469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} ∗ (63/256) ∗ 1	0.615234
					2x(2)	V_{RL} ∗ (63/256) ∗ 2	1.230469
	0000 0000	5.0V	5.0V/256	19,531.3	1x	V_{RL} ∗ (0/256) ∗ 1	0
		2.5V	2.5V/256	9,765.6	1x	V_{RL} ∗ (0/256) ∗ 1	0
					2x(2)	V_{RL} ∗ (0/256) ∗ 2	0

Note 1: V_{RL} is the resistor ladder's reference voltage. It is independent of the VRnB:VRnA selection.

2: Gain selection of 2x (Gx = '1') requires the voltage reference source to come from the V_{REF} pin (VRnB:VRnA = '10' or '11') and requires a V_{REF} pin voltage (or V_{RL}) ≤ V_{DD}/2, or from the internal band gap (VRnB:VRnA = '01').

3: These theoretical calculations do not take into account the offset, gain and nonlinearity errors.

NOTES:

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6.0 I²C SERIAL INTERFACE MODULE

The MCP47FXBX4/8's I²C serial interface module supports the I²C serial protocol specification. This I²C interface is a two-wire interface (clock and data). Figure 6-1 shows a typical I²C interface connection.

The I²C specification only defines the field types, field lengths, timings, etc., of a frame. The frame content defines the behavior of the device. The frame content (commands) for the MCP47FXBX4/8 is defined in **Section 7.0 "I2C Device Commands"**.

An overview of the I²C protocol is available in **Section Appendix B: "I²C Serial Interface"**.

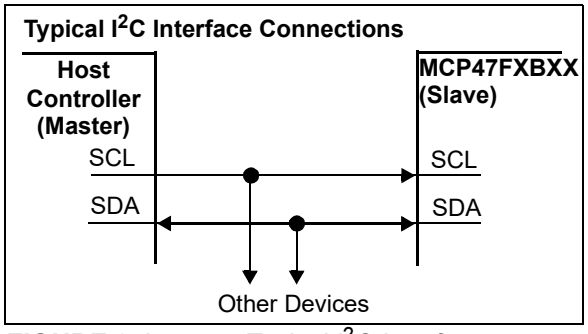


FIGURE 6-1: *Typical I²C Interface.*

6.1 Overview

This section discusses some of the specific characteristics of the MCP47FXBX4/8's I²C serial interface module. This is to assist in the development of your application.

The following sections discuss some of these device-specific characteristics:

- **Interface Pins (SCL and SDA)**
- **Communication Data Rates**
- **POR/BOR**
- **Device Memory Address**
- **General Call Commands**
- **Device I²C Slave Addressing**
- **Entering High-Speed (HS) Mode**

6.2 Interface Pins (SCL and SDA)

The MCP47FXBX4/8 I²C module SCL pin does not generate the serial clock since the device operates in Slave mode. Also, the MCP47FXBX4/8 will not stretch the clock signal (SCL) since memory read access occurs fast enough.

The MCP47FXBX4/8 I²C module implements slope control on the SDA pin output driver.

6.3 Communication Data Rates

The I²C interface specifies different communication bit rates. These are referred to as Standard, Fast or High-Speed modes. The MCP47FXBX4/8 supports these three modes. The clock rates (bit rate) of these modes are:

- Standard mode: up to 100 kHz (kbit/s)
- Fast mode: up to 400 kHz (kbit/s)
- High-Speed mode (HS mode): up to 3.4 MHz (Mbit/s)

A description on how to enter High-Speed mode is provided in **Section 6.9 "Entering High-Speed (HS) Mode"**.

6.4 POR/BOR

On a POR/BOR event, the I²C Serial Interface Module state machine is reset and the device's memory address pointer is forced to 00h.

6.5 Device Memory Address

The memory address is the 5-bit value that provides the location in the device's memory that the specified command will operate on.

On a POR/BOR event, the device's memory address pointer is forced to 00h.

The MCP47FXBX4/8 retains the last "Device Memory Address" received. That is, the MCP47FXBX4/8 does not "corrupt" the "Device Memory Address" after repeated Start or Stop conditions.

6.6 General Call Commands

The General Call commands utilize the I²C specification reserved General Call command address and command codes. The MCP47FXBX4/8 also implements a nonstandard General Call command.

The General Call commands are:

- **General Call Reset**
- **General Call Wake-up** (MCP47FXBX4/8 defined)

The General Call Wake-up command will cause all the MCP47FXBX4/8 devices to exit their Power-Down state.

6.7 Multi-Master Systems

The MCP47FXBX4/8 is not a master device (one that generates the interface clock), but can be used in Multi-Master applications.

6.8 Device I²C Slave Addressing

The MCP47FXBX4/8 implements 7-bit Slave addressing. The address byte is the first byte received following the Start condition from the master device (see Figure 6-2).

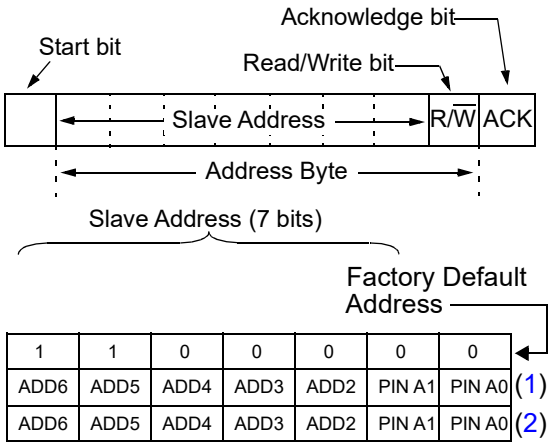
> **Note:** The I²C 10-bit Addressing mode is not supported.

For volatile devices (MCP47FVBX4/8), the I²C Slave address bits ADD6:ADD2 are fixed ('`110 0000`'). The user still has Slave address programmability with the A1:A0 address pins.

For nonvolatile devices, the Slave address is implemented in a nonvolatile register (Register 4-5) which is protected from accidental register writes via the Slave Address Lock (SALCK) Configuration bit. The SALCK Configuration bit requires a high voltage (V_{IHH}) to be modified. The SALCK Configuration bit must be disabled (see **Section 7.4.3 "Disable Configuration Bit (High-Voltage)"**) before a write to the nonvolatile Slave addresses register can modify the value.

> **Note:** After modifying the nonvolatile Slave address value (Register 4-5), it is strongly recommended that the SALCK Configuration bit be enabled (see **Section 7.4.2 "Enable Configuration Bit (High-Voltage)"**).

Figure 6-2 shows the I²C Slave address byte format, which contains the seven address bits and a Read/Write (R/W) bit.



Note 1: Address Bits (ADD6:ADD2) can be reprogrammed by the customer (nonvolatile device), but a High-Voltage command must be used to unlock the Slave Address Lock bit.

2: The state of the A1:A0 pins creates the 7-bit I²C Address.

FIGURE 6-2: *Slave Address Bits in the I²C Control Byte.*

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6.9 Entering High-Speed (HS) Mode

The I²C specification requires that a High-Speed mode device be activated to operate in High-Speed (3.4 Mbit/s) mode. This is accomplished by the master sending a special address byte following the Start bit. This byte is referred to as the High-Speed Master Mode Code (HSMMC).

The device can now communicate at up to 3.4 Mbit/s on SDA and SCL lines. The device will switch out of the HS mode on the next Stop condition.

The master code is sent as follows:

1. Start condition (S)
2. High-Speed Master Mode Code ('`0000 1XXX`'), The `XXX` bits are unique to the HS master mode.
3. No Acknowledge ($\overline{A}$)

After switching to the HS mode, the next transferred byte is the I²C control byte, which specifies the device to communicate with and any number of data bytes plus acknowledgments. The master device can then either issue a repeated Start bit to address a different device (at high-speed) or a Stop bit to return to the fast/standard bus speed. After the Stop bit, any other master device (in a Multi-Master system) can arbitrate for the I²C bus.

The MCP47FXBX4/8 devices do not acknowledge the HS Select byte. However, upon receiving this command, the device switches to HS mode.

Figure 6-3 illustrates the HS mode command sequence.

For more information on the HS mode, or other I²C modes, refer to the "*NXP I²C Specification*".

6.9.1 SLOPE CONTROL

The slope control on the SDA output for the Fast/Standard Speed is different from the one of the High-Speed clock modes of the interface.

6.9.2 PULSE GOBBLER

The pulse gobbler on the SCL pin is automatically adjusted to suppress spikes < 10 ns during HS mode.

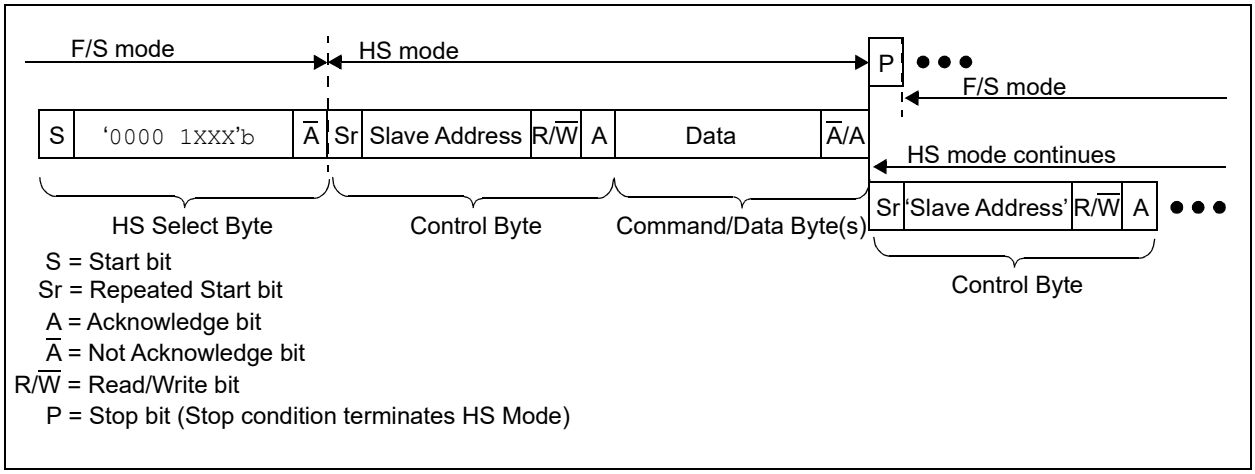

FIGURE 6-3: *HS Mode Sequence.*

NOTES:

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7.0 I²C DEVICE COMMANDS

This section documents the commands supported by the device.

The commands can be grouped into the following categories:

- WRITE command (normal and high-voltage) (C1:C0 = '00')
- READ command (normal and high-voltage) (C1:C0 = '11')
- General Call commands
- Modify Device Configuration Bit command (HVC = V_{IHH})
  - Enable Configuration bit (C1:C0 = '10')
  - Disable Configuration bit (C1:C0 = '01')

The supported commands are shown in Table 7-1. These commands allow both single or continuous data operation. Continuous data operation means that the I²C master does not generate a Stop bit but repeats the required data/clocks. This allows faster updates since the overhead of the I²C control byte is removed. Table 7-1 also shows the required number of bit clocks for each command's different mode of operation.

7.0.1 ABORTING A TRANSMISSION

A Restart or Stop condition in an expected data bit position will abort the current command sequence. If the command was a write, that data word will not be written to the MCP47FXBX4/8. Also, the I²C state machine will be reset.

If the condition is a Restart (Start), then the following byte will be expected to be the Slave Address byte.

If the condition is a Stop, the device will monitor for the Start condition.

TABLE 7-1: DEVICE COMMANDS – NUMBER OF CLOCKS

Command					# of Bit Clocks (1)	Data Update Rate (8-bit/10-bit/12-bit) (Data Words/Second)			Comments
Operation	Code		HV	Mode(6)					
	C1	C0				100 kHz	400 kHz	3.4 MHz (5)	
Write Command (Normal and High-Voltage)	0	0	3	Single	38	2,632	10,526	89,474	
	0	0	3	Continuous	27n + 11	3,559	14,235	120,996	For 10 data words
READ Command (Normal and High-Voltage) (2)	1	1	3	Random	48	2,083	8,333	70,833	
	1	1	3	Continuous	18n + 11	4,762	19,048	161,905	For 10 data words
	1	1	3	Last Address	29	3,448	13,793	117,241	
General Call Reset Command	—	—	3	Single	20	5,000	20,000	170,000	Note 4
General Call Wake-up Command	—	—	3	Single	20	5,000	20,000	170,000	Note 4
Enable Configuration Bit (High-Voltage) Command	1	0	Yes	Single	20	5,000	20,000	170,000	
	1	0	Yes	Continuous	9n + 11	9,901	39,604	336,634	For 10 data words
Disable Configuration Bit (High-Voltage) Command	0	1	Yes	Single	20	5,000	20,000	170,000	
	0	1	Yes	Continuous	9n + 11	9,901	39,604	336,634	For 10 data words

Note 1: "n" indicates the number of times the command operation is to be repeated.
2: This command is useful to determine when an EEPROM programming cycle has completed.
3: This command can be either normal voltage or high voltage.
4: Determined by the General Call Command byte after the I²C General Call address.
5: There is a minimal overhead to enter into 3.4 MHz mode.
6: Nonvolatile registers can only use the Single mode.

7.1 Write Command (Normal and High-Voltage)

WRITE commands are used to transfer data to the desired memory location (from the host controller). The WRITE command can be issued to both volatile and nonvolatile memory locations.

WRITE commands can be structured as either single or continuous. The continuous format allows the fastest data update rate for the device's memory locations, but it is not supported for nonvolatile memory locations.

The format of the command is shown in Figure 7-1 (single) and Figure 7-3 (continuous). For the ACK/NACK behavior, see Figure 7-2.

A WRITE command to a volatile memory location changes that location after a properly formatted WRITE command and the A/$\overline{A}$ clock has been received.

A WRITE command to a nonvolatile memory location starts an EEPROM write cycle only after a properly formatted WRITE command has been received and the Stop condition has occurred.

Note 1: Writes to certain memory locations depend on the state of the WiperLock™ Technology status bits.

2: During device communication, if the device address/command combination is invalid or an unimplemented device address is specified, the MCP47FXBX4/8 will NACK that byte. To reset the I^{2}C state machine, the I^{2}C communication must detect a Start bit.

7.1.1 SINGLE WRITE TO VOLATILE MEMORY

For volatile memory locations, data are written to the MCP47FXBX4/8 after every data word transfer (during the Acknowledge). If a Stop or Restart condition is generated during a data transfer (before the A), the data will not be written to the MCP47FXBX4/8. After the A bit, the master can initiate the next sequence with a Stop or Restart condition.

Refer to Figure 7-1 for the byte write sequence.

7.1.2 SINGLE WRITE TO NONVOLATILE MEMORY

The sequence to write to a single nonvolatile memory location is the same as a single write to a volatile memory with the exception that the EEPROM write cycle (t_{WC}) is started after a properly formatted command, including the Stop bit, if received. After the Stop condition occurs, the serial interface may immediately be re-enabled by initiating a Start condition.

During an EEPROM write cycle, access to the volatile memory is allowed when using the appropriate command sequence. Commands that address nonvolatile memory are ignored until the EEPROM write cycle (t_{wc}) completes. This allows the host controller to operate on the volatile DAC registers.

Note: The EEWA status bit indicates if an EEPROM write cycle is active (see Register 4-4).

Figure 7-1 shows the command format for a single write to volatile or nonvolatile memory location.

7.1.3 CONTINUOUS WRITES TO VOLATILE MEMORY

A Continuous Write mode of operation is possible when writing to the device's volatile memory registers (see Table 7-2). This Continuous Write mode allows writes without a Stop or Restart condition or repeated transmissions of the I^{2}C Control Byte. Figure 7-3 shows the sequence for three continuous writes. The writes do not need to be to the same volatile memory address. The sequence ends with the Master sending a Stop or Restart condition.

TABLE 7-2: VOLATILE MEMORY ADDRESSES

Address	Quad-Channel	Octal-Channel
00h-03h	Yes	Yes
04h-07h	**No**	Yes
08h	Yes	Yes
09h	Yes	Yes
0Ah	Yes	Yes

7.1.4 CONTINUOUS WRITES TO NONVOLATILE MEMORY

If a continuous write is attempted on a nonvolatile memory, the missing Stop condition will cause the command to be an error condition ($\overline{A}$). A Start bit is required to reset the command state machine.

7.1.5 HIGH-VOLTAGE COMMAND (HVC) SIGNAL

The High-Voltage command (HVC) signal is used to indicate that the command or sequence of commands are in the high-voltage operational state. HVC commands allow the device's WiperLock Technology and write protect features to be enabled and disabled.

Note: Writes to a volatile DAC register will not transfer to the output register until the $\overline{LAT}$ (HVC) pin is transitioned from the V_{IHHEN} voltage to a V_{IL} voltage.

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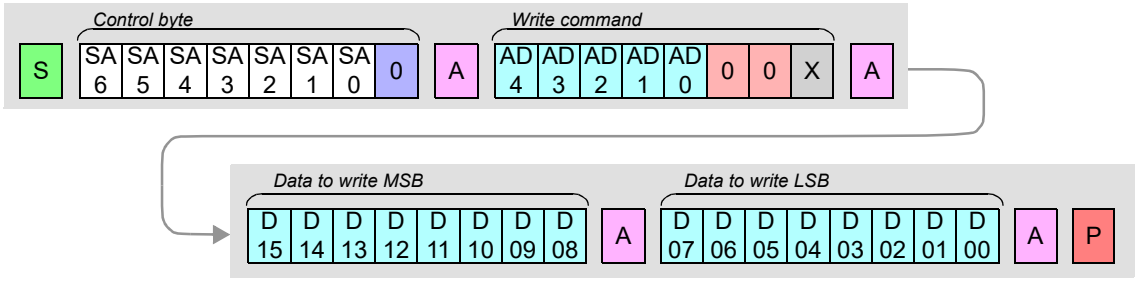


Legend:

S	I²C Start bit	A	I²C ACK bit(1)	X	Reserved, should be set to '0'
SA *n*	I²C Slave Address	AD *n*	Memory Address	D *nn*	Register data (to be written)(2)
0	I²C Write bit	0 0	Write command	P	I²C Stop bit(3)

Note 1: The Acknowledge bit is generated by the MCP47FXBX4/8.

2: At the falling edge of the SCL pin for the `WRITE` command ACK bit, the MCP47FXBX4/8 device updates the value of the specified device register.

3: This command sequence does not need to terminate (using the Stop bit) and the `WRITE` command can be repeated.

FIGURE 7-1: *Write Random Address Command (Volatile and Nonvolatile Memory).*

Write 1 Word Command

	S	Slave Address							R/W	ACK	Command								ACK	Data Byte								ACK	Data Byte								ACK	P
Master	S	SA6	SA5	SA4	SA3	SA2	SA1	SA0	0	A/A	AD4	AD3	AD2	AD1	AD0	C1	C0	x	A/A	D15	D14	D13	D12	D11	D10	D09	D08	A/A	D07	D06	D05	D04	D03	D02	D01	D00	A/A	P

Example 1 (No Command Error)

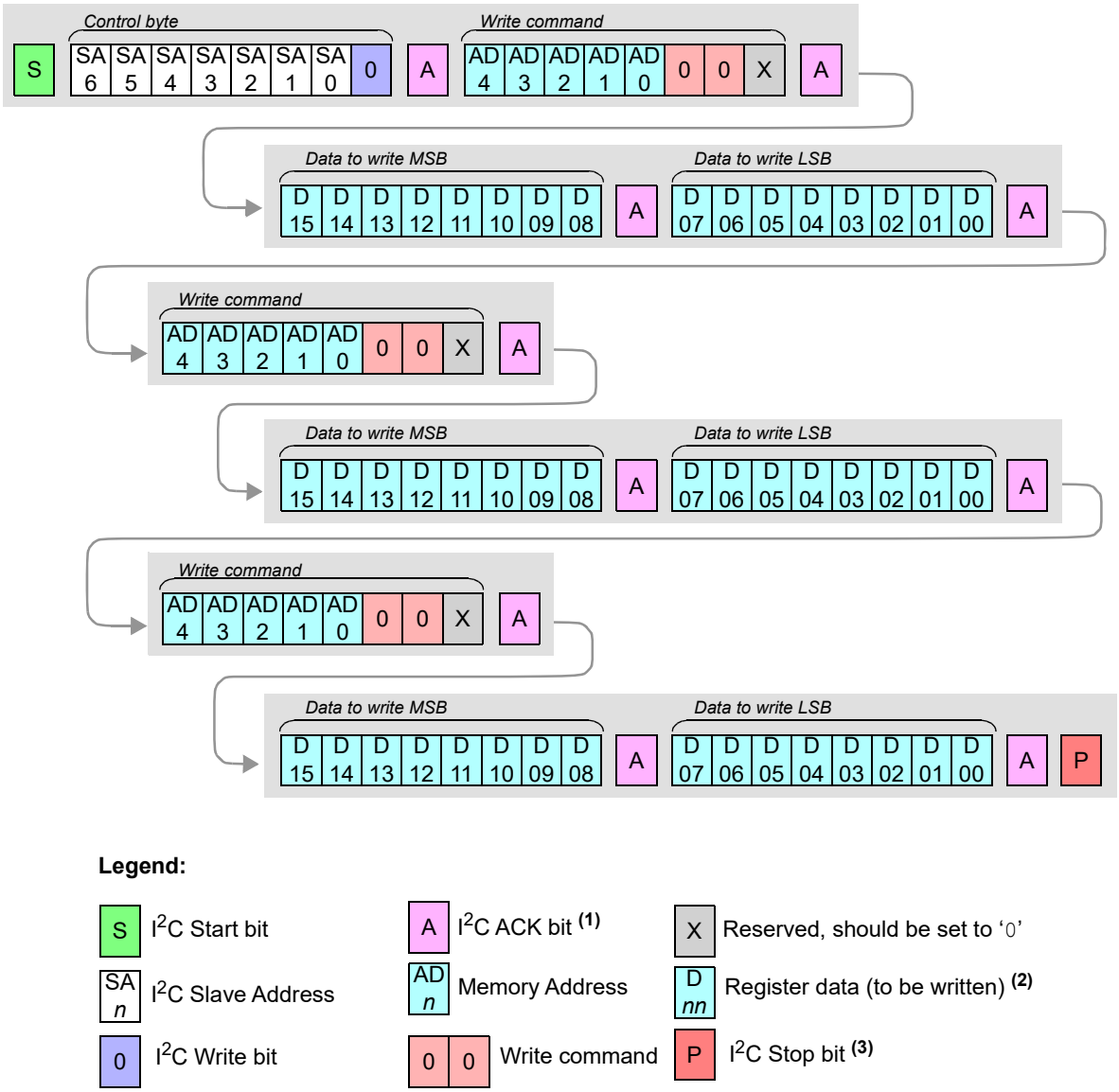
Master	S	1	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	x	1	d	d	d	d	d	d	d	d	1	d	d	d	d	d	d	d	d	1	P
MCP47FXBX4/8										0									0									0									0	
I²C Bus	S	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	x	0	d	d	d	d	d	d	d	d	0	d	d	d	d	d	d	d	d	0	P

Example 2 (Command Error)

Master	S	1	1	0	0	0	0	0	0	1	0	1	1	1	1	0	0	x	1	d	d	d	d	d	d	d	d	1	d	d	d	d	d	d	d	d	1	P
MCP47FXBX4/8										0									1									1									1	
I²C Bus	S	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	x	0	d	d	d	d	d	d	d	d	1	d	d	d	d	d	d	d	d	1	P

Note: Once a command error occurs (example 2), the device will NACK until a Start condition occurs.

FIGURE 7-2: *I²C ACK/NACK Behavior (Write Command Example).*



Note 1: The Acknowledge bit is generated by the MCP47FXBX4/8.

2: At the falling edge of the SCL pin for the `WRITE` command ACK bit, the MCP47FXBX4/8 device updates the value of the specified device register.

3: This command sequence does not need to terminate (using the Stop bit) and the `WRITE` command can be repeated.

FIGURE 7-3: *Continuous `WRITE` Commands (Volatile Memory Only).*

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7.2 READ Command (Normal and High-Voltage)

READ commands are used to transfer data from the specified memory location to the host controller. The READ command can be issued to both volatile and nonvolatile memory locations.

During an EEPROM write cycle (write to nonvolatile memory location or Enable/Disable Configuration Bit command) the READ command can only read the volatile memory locations. By reading the STATUS register (0Ah), the host controller can determine when the write cycle has been completed (via the state of the EEWA bit).

The READ command formats include:

- **Single Read**
  - **Single Memory Address**
  - **Last Memory Address Accessed**
- **Continuous Reads**

The MCP47FXBX4/8 retains the last device memory address received. That is the MCP47FXBX4/8 does not corrupt the device memory address after repeated Start or Stop conditions.

If the address pointer is for a nonvolatile memory location during a nonvolatile write cycle (t_{WC}), the MCP47FXBX4/8 will respond with an $\overline{A}$ bit.

Note 1:	During device communication, if the device address/command combination is invalid or an unimplemented address is specified, then the MCP47FXBX4/8 will NACK that byte. To reset the I²C state machine, the I²C communication must detect a Start bit.
2:	If the $\overline{LAT}$ pin is high (V_{IH}), reads of the volatile DAC register read the output value, not the internal register.
3:	READ commands operate the same regardless of the state of the High-Voltage command signal.

7.2.1 SINGLE READ

The READ command format writes two bytes, the Control byte and the READ command byte (desired memory address and the READ command), and then has a Restart condition. Then, a 2nd Control byte is transmitted, but this control byte indicates an I²C read operation (R/W bit = '1').

7.2.1.1 Single Memory Address

Figure 7-4 shows the sequence for reading a specified memory address.

7.2.1.2 Last Memory Address Accessed

Figure 7-5 shows the waveforms for a single read of the last memory location accessed.

This command allows faster communication when checking the status of the EEPROM Write Active (EEWA) bit (see Register 4-4), as long as the register address of the device's last command is 0Ah.

7.2.2 CONTINUOUS READS

Continuous reads allow the device's memory to be read quickly. Continuous reads are possible to all memory locations. If a nonvolatile memory write cycle occurs, then READ commands may only access the volatile memory locations.

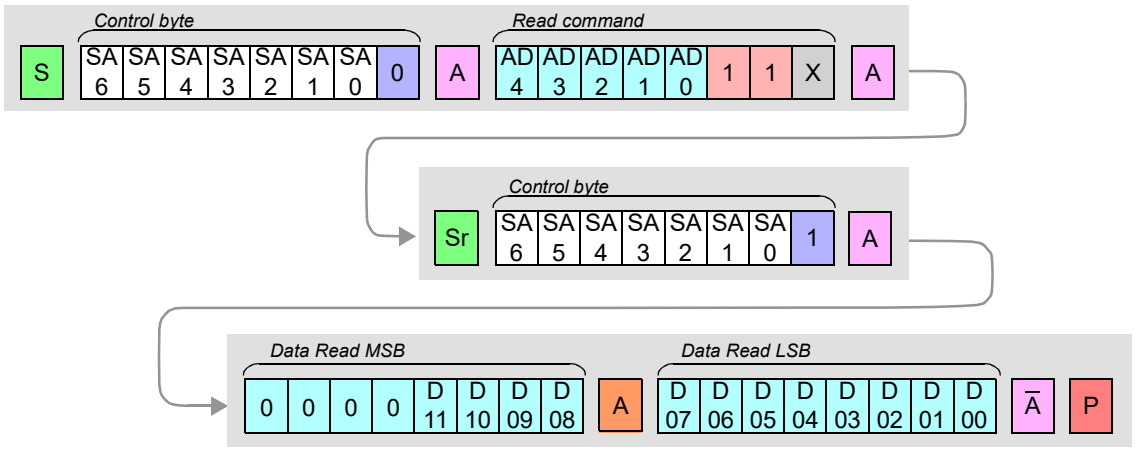
Figure 7-7 shows the sequence for three continuous reads.

For continuous reads, instead of transmitting a Stop or Restart condition after the data transfer, the master continually reads the data byte. The sequence ends with the master Not Acknowledging and then sending a Stop or Restart.

This is useful in reading the System STATUS register (0Ah) to determine if an EEPROM write cycle has been completed (EEWA bit).

7.2.3 IGNORING AN I²C TRANSMISSION AND "FALLING OFF" THE BUS

The MCP47FXBX4/8 expects to receive complete, valid I²C commands and will assume any command not defined as a valid command. This is due to a bus corruption, thus entering a passive High condition on the SDA signal. All signals will be ignored until the next valid Start condition and Control byte are received.



Legend:

S	I²C Start bit	AD *n*	Memory Address(5)	1	I²C Read bit	P	I2C Stop bit(4, 5)
SA *n*	I²C Slave Address	1 1	Read command	D *nn*	Data (read from memory)		
0	I²C Write bit	X	Reserved, set to '0'	A	I²C ACK bit(2)		
A	I²C ACK bit(1)	Sr	I²C Start bit, repeated	Ā	I²C NACK bit(3)		

Note 1: The Acknowledge bit is generated by the MCP47FXBX4/8.

2: The master device is responsible for the A/Ā signal. If an Ā signal occurs, the MCP47FXBX4/8 will abort this transfer and release the bus.

3: The master device will Not Acknowledge, and the MCP47FXBX4/8 will release the bus so the master device can generate a Stop or repeated Start condition.

4: At the falling edge of the SCL pin for the `READ` command ACK bit, the MCP47FXBX4/8 device updates the value of the specified device Register.

5: This command sequence does not need to terminate (using the Stop bit) and the `READ` command can be repeated (see continuous read format, **Section 7.2.2 "Continuous Reads"**).

FIGURE 7-4: *`READ` Command – Single Memory Address.*

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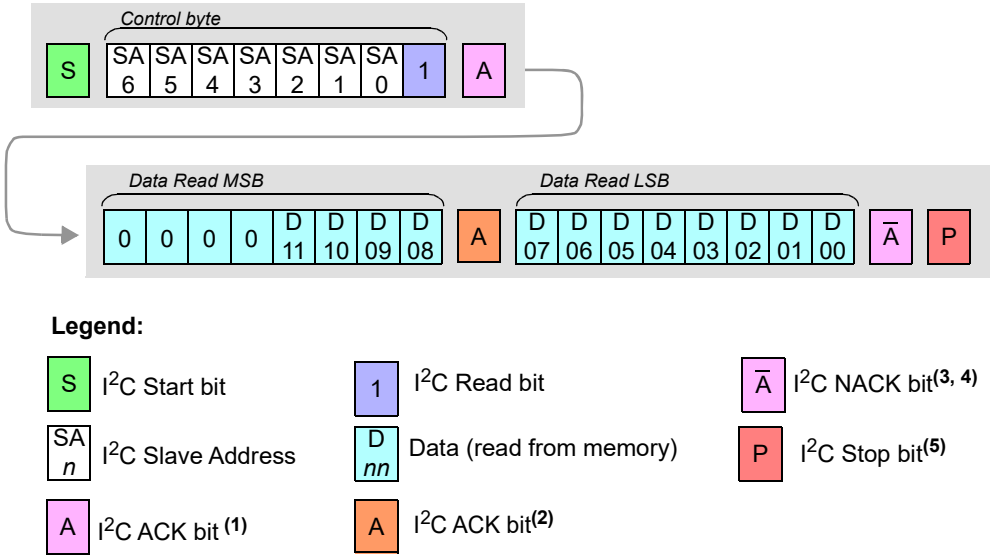

Legend:

S	I²C Start bit	1	I²C Read bit	Ā	I²C NACK bit(3, 4)
SA *n*	I²C Slave Address	D *nn*	Data (read from memory)	P	I²C Stop bit(5)
A	I²C ACK bit (1)	A	I²C ACK bit(2)		

Note 1: The Acknowledge bit is generated by the MCP47FXBX4/8.

2: The master device is responsible for the A/Ā signal. If an Ā signal occurs, the MCP47FXBX4/8 will abort this transfer and release the bus.

3: The master device will Not Acknowledge, and the MCP47FXBX4/8 will release the bus so the master device can generate a Stop or repeated Start condition.

4: At the falling edge of the SCL pin for the `READ` command ACK bit, the MCP47FXBX4/8 device updates the value of the specified device register.

5: This command sequence does not need to terminate (using the Stop bit) and the `READ` command can be repeated (see continuous read format, **Section 7.2.2 "Continuous Reads"**).

FIGURE 7-5: *`READ` Command – Last Memory Address Accessed.*

Read 1 Word Command

	S	Slave Address							R/W	ACK	Command								ACK
Master	S	SA6	SA5	SA4	SA3	SA2	SA1	SA0	0	1	AD4	AD3	AD2	AD1	AD0	C1	C0	x	1

	Sr	Slave Address							R/W	ACK	Data Byte								ACK	Data Byte								ACK	P
Master (Continued)	Sr	SA6	SA5	SA4	SA3	SA2	SA1	SA0	1	1	D15	D14	D13	D12	D11	D10	D09	D08	1	D07	D06	D05	D04	D03	D02	D01	D00	1	P

Ex.1 (No Command Error)

Master	S	1	1	0	0	0	0	0	0	1	0	0	0	0	1	1	1	x	1
MCP47FXBXXA0										0									0
I²C Bus	S	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	x	0

Master (Continued)	S	0	0	0	0	1	0	0	1	1									1									1	P
MCP47FXBXXA0 (Continued)										0	d	d	d	d	d	d	d	d	0	d	d	d	d	d	d	d	d	0	
I²C Bus (Continued)	S	0	0	0	0	0	0	0	1	0	d	d	d	d	d	d	d	d	0	d	d	d	d	d	d	d	d	0	P

Ex.2 (With Command Error)

Master	S	1	1	0	0	0	0	0	0	1	0	1	1	1	1	0	0	x	1
MCP47FXBXXA0										0									1
I²C Bus	S	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	x	1

Master (Continued)	S	1	1	0	0	0	0	0	1	1									1									1	P
MCP47FXBXXA0 (Continued)										0	?	?	?	?	?	?	?	?	0	?	?	?	?	?	?	?	?	1	
I²C Bus (Continued)	S	1	1	0	0	0	0	0	1	0	?	?	?	?	?	?	?	?	0	?	?	?	?	?	?	?	?	1	P

Note 1: Once a command error occurs (example 2), the MCP47FXBX4/8 will NACK until a Start condition occurs.

2: For the command error case (Example 2), the data read are from the register of the last valid address loaded into the device.

FIGURE 7-6: *I²C ACK/NACK Behavior (`READ` Command Example).*

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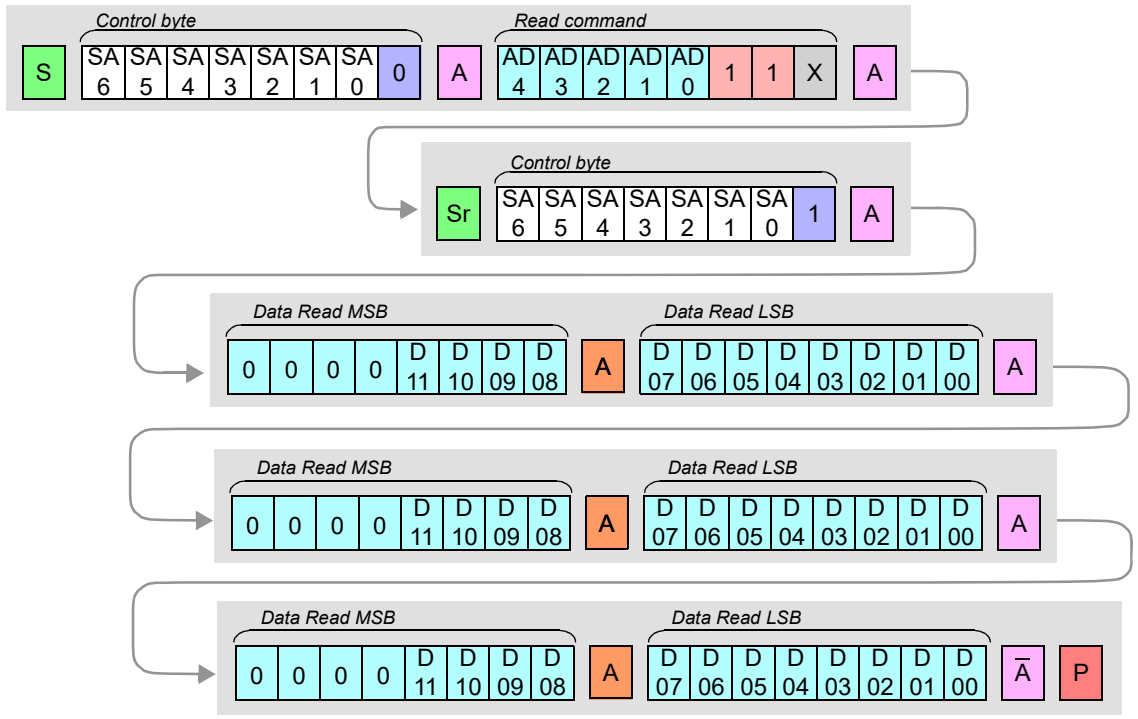


Legend:

S	I²C Start bit	AD *n*	Memory Address	1	I²C Read bit	P	I²C Stop bit(4)
SA *n*	I²C Slave Address	1 1	Read command	D *nn*	Data (read from memory)		
0	I²C Write bit	X	Reserved, set to '0'	A	I²C ACK bit(2)		
A	I²C ACK bit(1)	Sr	I²C Start bit, repeated	Ā	I²C NACK bit(3)		

Note 1: The Acknowledge bit is generated by the MCP47FXBX4/8.

2: The master device is responsible for A/Ā signal. If an Ā signal occurs, the MCP47FXBX4/8 will abort this transfer and release the bus.

3: The master device will Not Acknowledge and the MCP47FXBX4/8 will release the bus so the master device can generate a Stop or repeated Start condition.

4: At the falling edge of the SCL pin for the `READ` command ACK bit, the MCP47FXBX4/8 updates the value of the specified device register.

FIGURE 7-7: *Continuous `READ` Command of Specified Address.*

7.3 General Call Commands

The MCP47FXBX4/8 acknowledges the General Call Address command (00h in the first byte). General Call commands can be used to communicate to all devices on the I²C bus (at the same time) that understand the General Call command. The meaning of the general call address is always specified in the second byte (see Figure 7-8).

If the second byte has a '1' in the LSb, the specification intends this to indicate a "Hardware General Call". The MCP47FXBX4/8 will ignore this byte and all following bytes (and $\overline{A}$), until a Stop bit (P) is encountered.

The MCP47FXBX4/8 devices support the following I²C General Call commands:

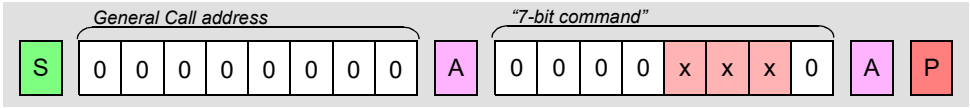
- **General Call Reset** (06h)
- **General Call Wake-up** (0Ah)

The General Call Reset command format is specified by the I²C specification. The General Call Wake-Up command is a Microchip-defined format. The General Call Wake-Up command will have all devices wake up (that is, exit the Power-Down mode).

The other two I²C specification command codes (04h and 00h) are not supported. Therefore those commands are Not Acknowledged.

If these 7-bit commands conflict with other I²C devices on the bus, then the customer will need two I²C buses and ensure that the devices are on the correct bus for their desired application functionality.

Note: Refer to the NXP specification #UM10204, Rev. 03 19 June 2007 document for more details on the General Call specifications. The I²C specification does not allow '00000000' (00h) in the second byte.



Legend:

S I²C Start bit | A I²C ACK bit(1) | x x x GC command | P I²C Stop bit(2,3)

Note 1: The Acknowledge bit is generated by the MCP47FXBX4/8.

2: This command sequence does not need to terminate (using the Stop bit) and the General Call command can be repeated, or another General Call command can be sent. Only the first command will be accepted by the MCP47FXBX4/8.

FIGURE 7-8: *General Call Format.*

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7.3.1 GENERAL CALL RESET

The I²C General Call Reset command forces a reset event. This is similar to the Power-on Reset, except that the reset delay timer is not started. This command allows multiple MCP47FXBX4/8 devices to be reset synchronously.

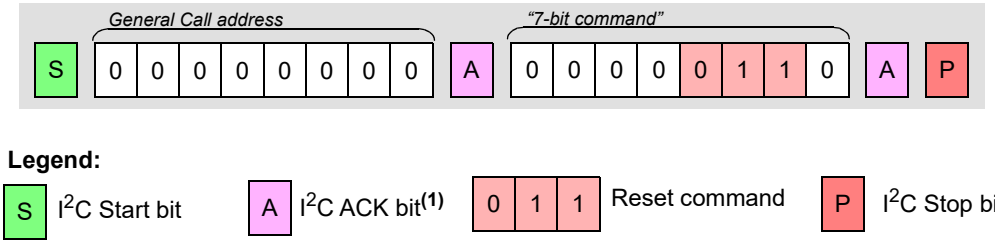
The device performs a General Call Reset if the second byte is '00000110' (06h). At the acknowledgment of this byte, the device will abort the current conversion and perform the following tasks:

- Internal reset similar to a POR. The contents of the EEPROM are loaded into the DAC registers and the analog output is available immediately (following the acknowledgment pulse).
- The V_{OUT} will be available immediately, but after a short time delay following the acknowledgment pulse. The V_{OUT} value is determined by the EEPROM contents.

7.3.2 GENERAL CALL WAKE-UP

The I²C General Call Wake-up command forces the device to exit its Power-Down state (forces the PDnB:PDnA bits to '00'). This command allows multiple MCP47FXBX4/8 devices to wake up synchronously.

The device performs General Call Wake-up if the second byte (after the General Call Address) is '00001010' (0Ah). At the acknowledgment of this byte, the device will perform the following task: the device's volatile Power-Down bits (PDnB:PDnA) are forced to '00'. The nonvolatile (EEPROM) Power-Down bit values are not affected by this command.

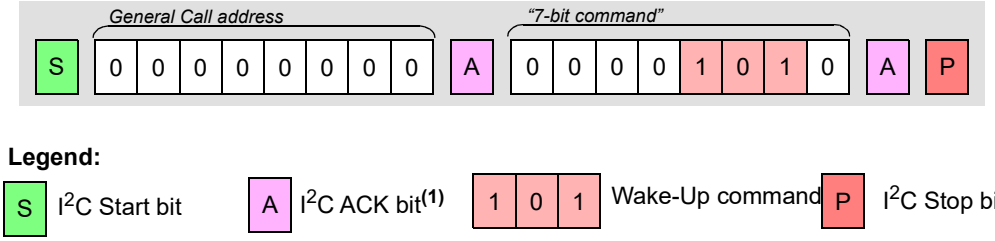


Note 1: The Acknowledge bit is generated by the MCP47FXBX4/8.

2: At the falling edge of the SCL pin for the General Call Reset command $\overline{ACK}$ bit, the MCP47FXBX4/8 device is reset.

3: This command sequence does not need to terminate (using the Stop bit) and the General Call Reset command can be repeated, or the General Call Wake-Up command can be sent. Only the first command will be accepted by the MCP47FXBX4/8.

FIGURE 7-9: *General Call Reset Command.*



Note 1: The Acknowledge bit is generated by the MCP47FXBX4/8.

2: At the rising edge of the last data bit for the General Call Wake-Up command, the volatile Power-Down bits (PDnB:PDnA) are forced to '00'.

3: This command sequence does not need to terminate (using the Stop bit) and the General Call Wake-Up command can be repeated, or the General Call Reset command can be sent.

FIGURE 7-10: *General Call Wake-Up Command.*

7.4 Modify Device Configuration Bit Commands

These commands are used to program the device Configuration bits. These commands require a high voltage (V_{IHH}) on the HVC pin.

The MCP47FXBX4/8 devices support the following Modify Device Configuration Bit commands:

- **Enable Configuration Bit (High-Voltage)**
- **Disable Configuration Bit (High-Voltage)**

These Configuration bits are used to inhibit the DAC values from inadvertent modification.

7.4.1 THE HIGH-VOLTAGE COMMAND (HVC) SIGNAL

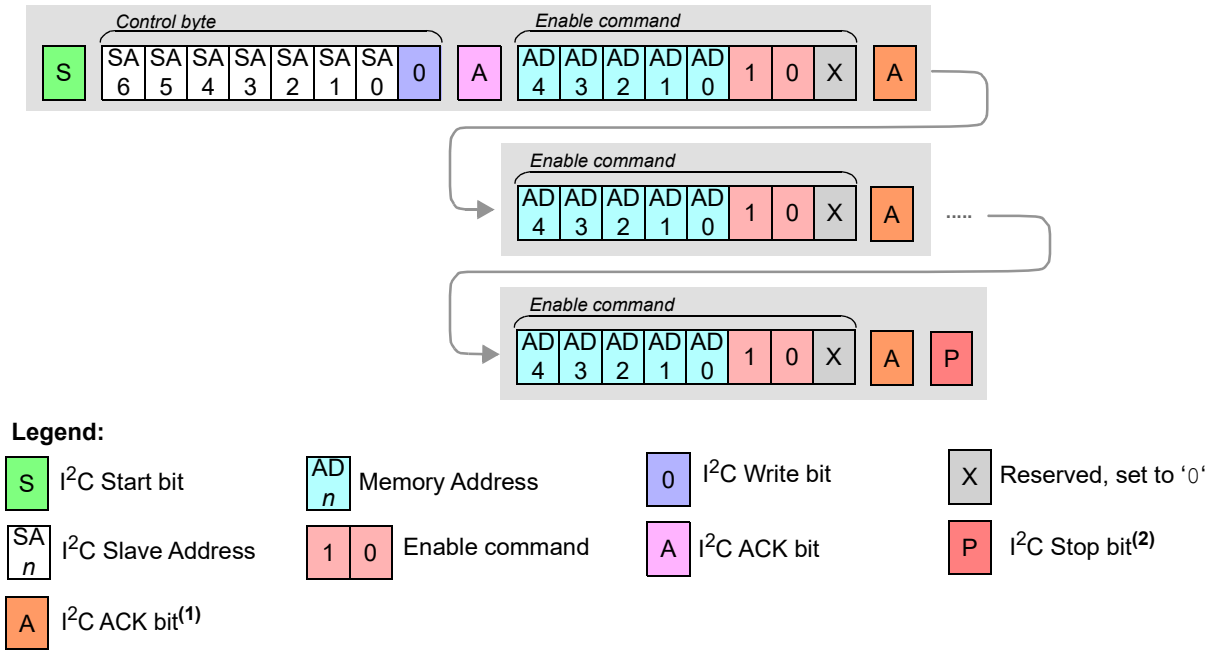
The High-Voltage command signal is used to indicate that the command, or sequence of commands, are in the High-Voltage mode. Signals > V_{IHH} (~9.0V) on the HVC pin put the device into High-Voltage mode. High-Voltage commands allow the device's WiperLock Technology and write-protect features to be enabled and disabled.

> **Note 1:** There is a required delay after the HVC pin is driven to the V_{IHH} level to the 1st edge of the SCL pin.
>
> **2:** Issuing an enable or disable command to a nonvolatile location will cause an error condition ($\overline{A}$ will be generated).

7.4.2 ENABLE CONFIGURATION BIT (HIGH-VOLTAGE)

Figure 7-11 shows the formats for a single Modify Write Protect or WiperLock Technology command.

A Modify Write Protect or WiperLock Technology command will only start an EEPROM write cycle (t_{wc}) after a properly formatted command has been received and the Stop condition occurs. During an EEPROM write cycle, only serial commands to volatile memory are accepted. All other serial commands are ignored until the EEPROM write cycle (t_{wc}) completes. This allows the host controller to operate on the volatile DAC, the volatile V_{REF}, Power-Down, Gain, Status, and WiperLock technology STATUS registers. The EEWA bit in the STATUS register indicates the status of an EEPROM write cycle.



Note 1: This command sequence does not need to terminate (using the Stop bit) and can change to any other desired command sequence (Enable, read or write).

2: This command byte is not required and the Stop bit may occur immediately after the 2nd ACK bit in this sequence.

FIGURE 7-11: *I^2C Enable Command Sequence.*

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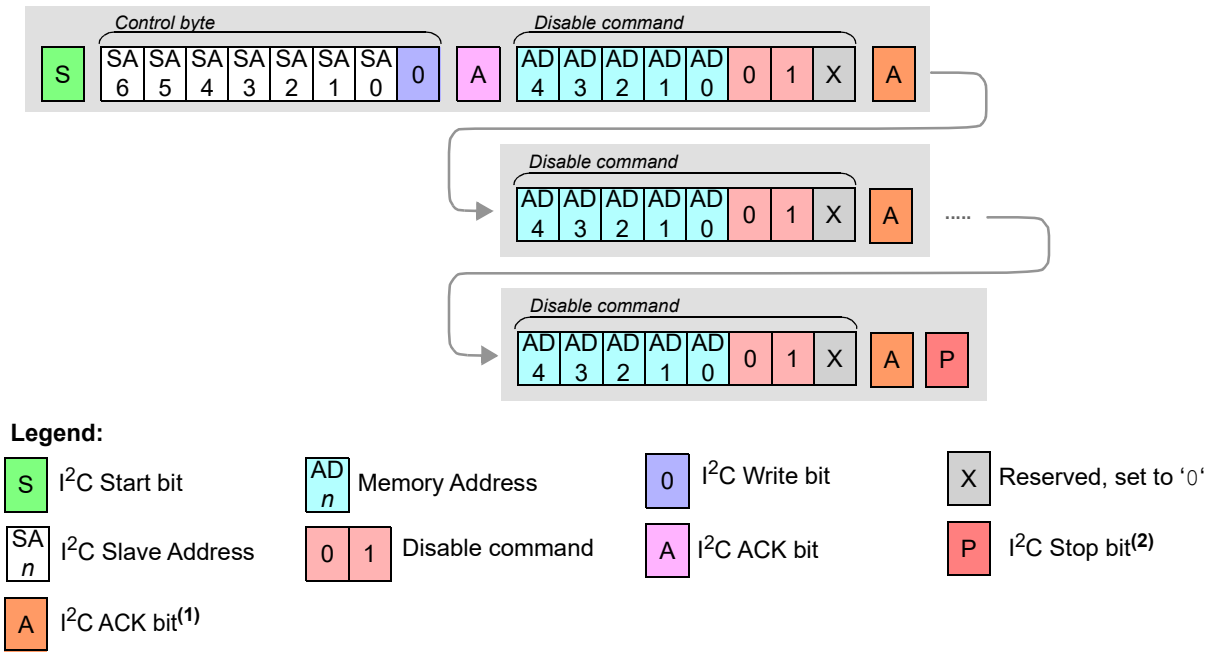
7.4.3 DISABLE CONFIGURATION BIT (HIGH-VOLTAGE)

Figure 7-12 shows the formats for a single Modify Write Protect or WiperLock Technology command.

A Modify Write Protect or WiperLock Technology command will only start an EEPROM write cycle (t_{wc}) after a properly formatted command has been received and the Stop condition occurs.

During an EEPROM write cycle, only serial commands to volatile memory are accepted. All other serial commands are ignored until the EEPROM write cycle (t_{wc}) completes. This allows the host controller to operate on the volatile DAC, the volatile V_{REF}, Power-Down, Gain, Status, and WiperLock Technology STATUS registers. The EEWA bit in the STATUS register indicates the status of an EEPROM write cycle.



Legend:

S	I²C Start bit	AD *n*	Memory Address	0	I²C Write bit	X	Reserved, set to '0'
SA *n*	I²C Slave Address	0 1	Disable command	A	I²C ACK bit	P	I²C Stop bit(2)
A	I²C ACK bit(1)						

Note 1: This command sequence does not need to terminate (using the Stop bit) and can change to any other desired command sequence (Enable, read or write).

2: This command byte is not required and the Stop bit may occur immediately after the 2nd ACK bit in this sequence.

FIGURE 7-12: *I²C Disable Command Sequence.*

NOTES:

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8.0 APPLICATIONS INFORMATION

The MCP47FXBX4/8 devices are general purpose, quad/octal-channel voltage output DACs for various applications where a precision operation with low-power and nonvolatile EEPROM memory is needed.

Since the devices include a nonvolatile EEPROM memory, the user can utilize these devices for applications that require the output to return to the previous set-up value on subsequent power-ups.

8.1 I²C Bus Connection Considerations

8.1.1 CONNECTING TO THE I²C BUS USING PULL-UP RESISTORS

The SCL and SDA pins of the MCP47FXBX4/8 devices are open-drain configurations. These pins require a pull-up resistor, as shown in Figure 8-3.

The pull-up resistor values (R_1 and R_2) for SCL and SDA pins depend on the operating speed (standard, fast and high speed) and loading capacitance of the I²C bus line. A higher value of the pull-up resistor consumes less power, but increases the signal transition time (higher RC time constant) on the bus line. Therefore, it can limit the bus operating speed. The lower resistor value, on the other hand, consumes higher power, but allows higher operating speed. If the bus line has higher capacitance due to long metal traces or multiple device connections to the bus line, a smaller pull-up resistor is needed to compensate the long RC time constant. The pull-up resistor is typically chosen between 1 kΩ and 10 kΩ ranges for Standard and Fast modes, and less than 1 kΩ for High-Speed mode.

8.1.2 DEVICE CONNECTION TEST

The user can test the presence of the device on the I²C bus line by using a simple I²C command. This test can be achieved by checking an acknowledge response from the device after sending a `READ` or `WRITE` command. Figure 8-1 shows an example with a `READ` command. The steps are:

1. Set the R/$\overline{W}$ bit "High" in the device's address byte.
2. Check the ACK bit of the address byte.
   If the device acknowledges (ACK = `0`) the command, then the device is connected. Otherwise, it is not connected.
3. Send Stop bit.

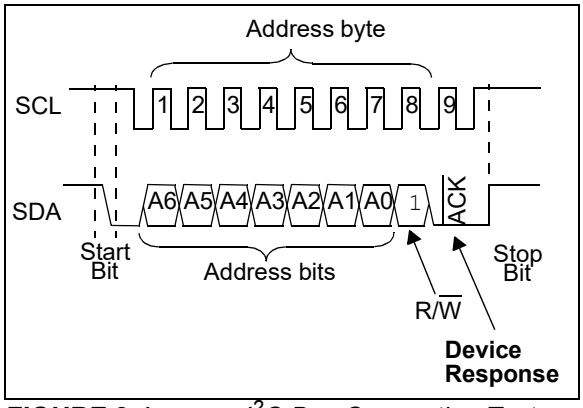


FIGURE 8-1: *I²C Bus Connection Test.*

8.1.3 SOFTWARE I²C INTERFACE RESET SEQUENCE

Note:	This technique is documented in AN1028.

At times, it may become necessary to perform a Software Reset Sequence to ensure the MCP47FXBX4/8 devices are in a correct and known I²C interface state. This technique only resets the I²C state machine.

This is useful if the MCP47FXBX4/8 devices power-up in an incorrect state (due to excessive bus noise, etc), or if the master device is reset during communication. Figure 8-2 shows the communication sequence to software reset the device.

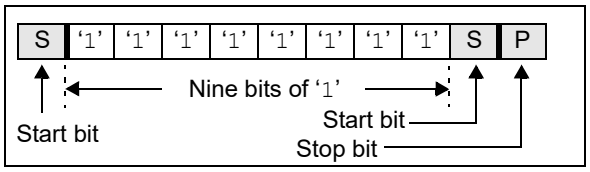


FIGURE 8-2: *Software Reset Sequence Format.*

The 1st Start bit will cause the device to reset from a state in which expects to receive data from the master device. In this mode, the device monitors the data bus in Receive mode and can detect if the Start bit forces an internal reset.

The nine bits of '`1`' are used to force a reset of those devices that could not be reset by the previous Start bit. This occurs only if the MCP47FXBX4/8 devices drive an A bit on the I²C bus, or are in Output mode (from a `READ` command) and are driving a data bit of '`0`' onto the I²C bus. In both of these cases, the previous Start bit could not be generated due to the MCP47FXBX4/8 holding the bus low. By sending out nine '`1`' bits, it is ensured that the device will see an $\overline{A}$ bit (the master device does not drive the I²C bus low to acknowledge the data sent by the MCP47FXBX4/8), which also forces the MCP47FXBX4/8 to reset.

The second Start bit is sent to address the rare possibility of an erroneous write. This could occur if the master device was reset while sending a `WRITE` command to the MCP47FXBX4/8, and then as the master device returns to normal operation and issues a Start condition, while the MCP47FXBX4/8 devices issue an acknowledge. In this case, if the second Start bit is not sent (and the Stop bit was sent) the MCP47FXBX4/8 could initiate a write cycle.

Note:	The potential for this erroneous write ONLY occurs if the master device is reset while sending a `WRITE` command to the MCP47FEBXX.

The Stop bit terminates the current I^2C bus activity. The MCP47FXBX4/8 waits to detect the next Start condition.

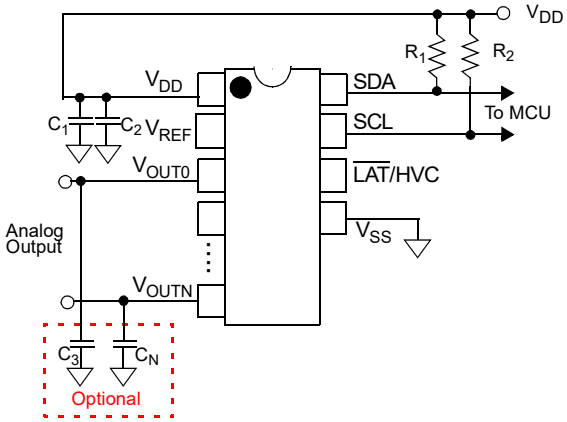
This sequence does not affect any other I^2C devices which may be on the bus, as they should disregard this for being an invalid command.

8.2 Power Supply Considerations

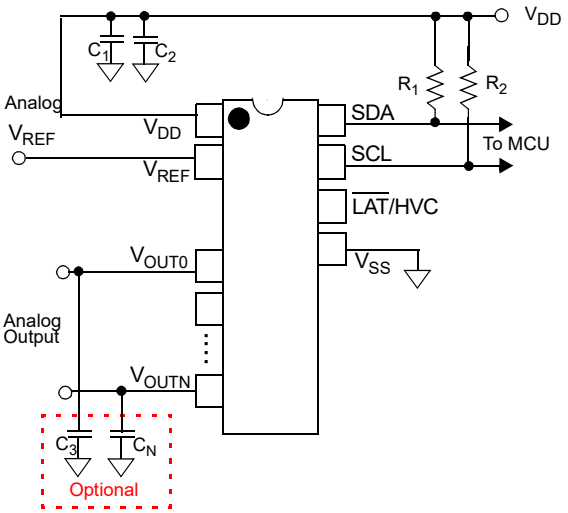
The power source should be as clean as possible. The power supply to the device is also used for the DAC voltage reference internally if the internal V_{DD} is selected as the resistor ladder's reference voltage (VRnB:VRnA = '`00`').

Any noise induced on the V_{DD} line can affect the DAC performance. Typical applications will require a bypass capacitor in order to filter out high-frequency noise on the V_{DD} line. The noise can be induced onto the power supply's traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-3 shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) in parallel on the V_{DD} line. These capacitors should be placed as close to the V_{DD} pin as possible (within 4 mm). If the application circuit has separate digital and analog power supplies, the V_{DD} and V_{SS} pins of the device should reside on the analog plane.

When setting the part voltage reference to Band Gap mode, the use of the V_{REF} pin decoupling capacitors is not recommended.



(a) Circuit when V_{DD} is selected as reference.
(**Note:** V_{DD} is connected to the reference circuit internally.)



(b) Circuit when external reference is used.

R_1 and R_2 are I^2C pull-up resistors:

R_1 and R_2:		=	
5 kΩ - 10 kΩ for f_{SCL}		=	100 kHz to 400 kHz
~700Ω for f_{SCL}		=	3.4 MHz
C_1:	0.1 µF capacitor	=	Ceramic
C_2:	10 µF capacitor	=	Tantalum
C_3:	~ 0.1 µF	=	Optional to reduce noise in V_{OUT} pin
C_4:	0.1 µF capacitor	=	Ceramic
C_5:	10 µF capacitor	=	Tantalum
C_6:	0.1 µF capacitor	=	Ceramic

FIGURE 8-3: *Circuit Example.*

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8.3 Layout Considerations

Several layout considerations may be applicable to your application. These may include:

- **Noise**
- **PCB Area Requirements**

8.3.1 NOISE

Particularly harsh environments may require shielding of critical signals. Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP47FXBX4/8's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR).

Multi-layer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable to provide.

Separate digital and analog ground planes are recommended. In this case, the V_{SS} pin and the ground pins of the V_{DD} capacitors should be terminated to the analog ground plane.

Note:	Breadboards and wire-wrapped boards are not recommended.

8.3.2 PCB AREA REQUIREMENTS

In some applications, PCB area is a criteria for device selection. Table 8-1 shows the typical package dimensions and area for the different package options.

TABLE 8-1: PACKAGE FOOTPRINT(1)

Package			Package Footprint		
Pins	Type	Code	Dimensions (mm)		Area (mm^2)
			Length	Width	
20	TSSOP	ST	3.00	4.90	14.70
20	VQFN	MQ	5	5	25

Note 1: Does not include recommended land pattern dimensions. Dimensions are typical values.

NOTES:

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9.0 DEVELOPMENT SUPPORT

Development support can be classified into two groups. These are:

- **Development Tools**
- **Technical Documentation**

9.1 Development Tools

Several development tools are available to assist in your design and evaluation of the MCP47FXBX4/8 devices. The currently available tools are shown in Table 9-1.

Figure 9-1 shows how the TSSOP20EV bond-out PCB can be populated to easily evaluate the MCP47FXBX4/8 devices. The PICkit™ Serial Analyzer can be used to control the DAC output registers and state of the configuration, control and STATUS register.

The TSSOP20EV boards may be purchased directly from the Microchip website at www.microchip.com.

9.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs, and Design Guides. Table 9-2 shows some of these documents.

TABLE 9-1: DEVELOPMENT TOOLS (Note 1)

Board Name	Part #	Comment
20-Pin TSSOP and SSOP Evaluation Board	TSSOP20EV	Most Flexible option - Recommended Bond-out PCB

Note 1: Supports the PICkit™ Serial Analyzer. See the User's Guide for additional information and requirements.

TABLE 9-2: TECHNICAL DOCUMENTATION

Application Note Number	Title	Literature #
AN1326	Using the MCP4728 12-Bit DAC for LDMOS Amplifier Bias Control Applications	DS01326
—	Signal Chain Design Guide	DS21825
—	Analog Solutions for Automotive Applications Design Guide	DS01005

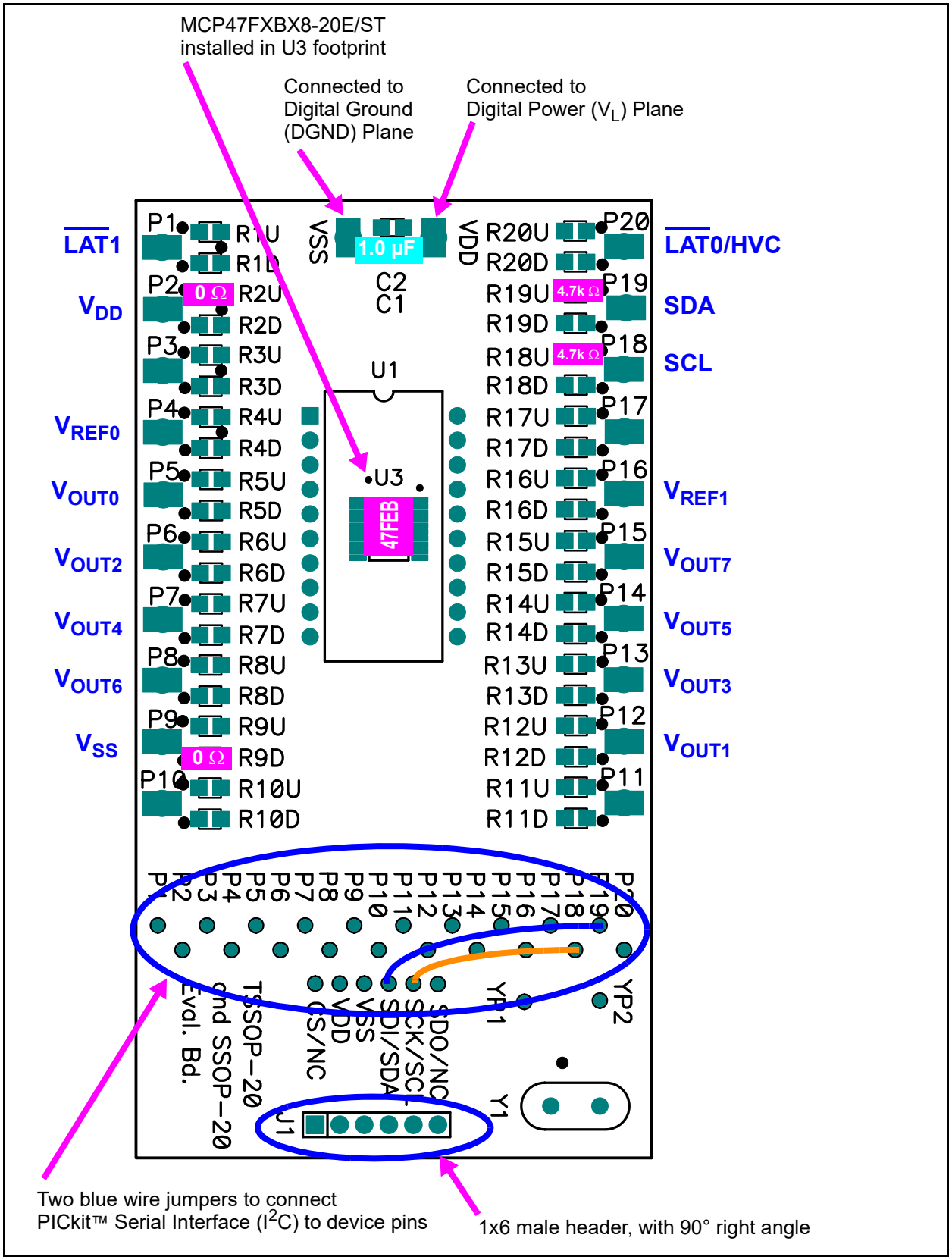

FIGURE 9-1: *MCP47FXBX4/8 Evaluation Board Circuit Using TSSOP20EV.*

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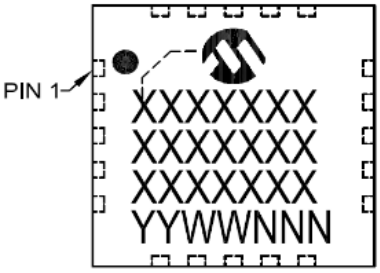
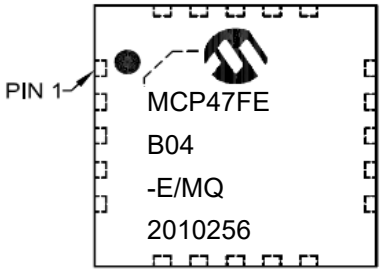
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

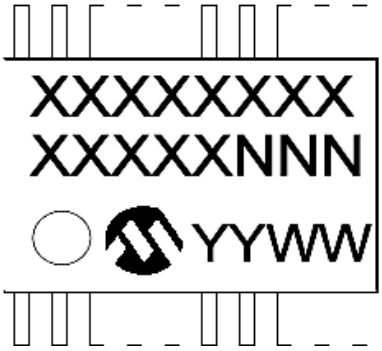
20-Lead 5 x 5 mm VQFN



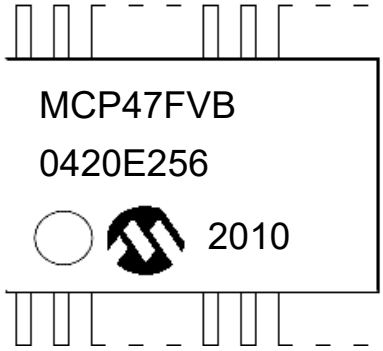
Example



20-Lead TSSOP



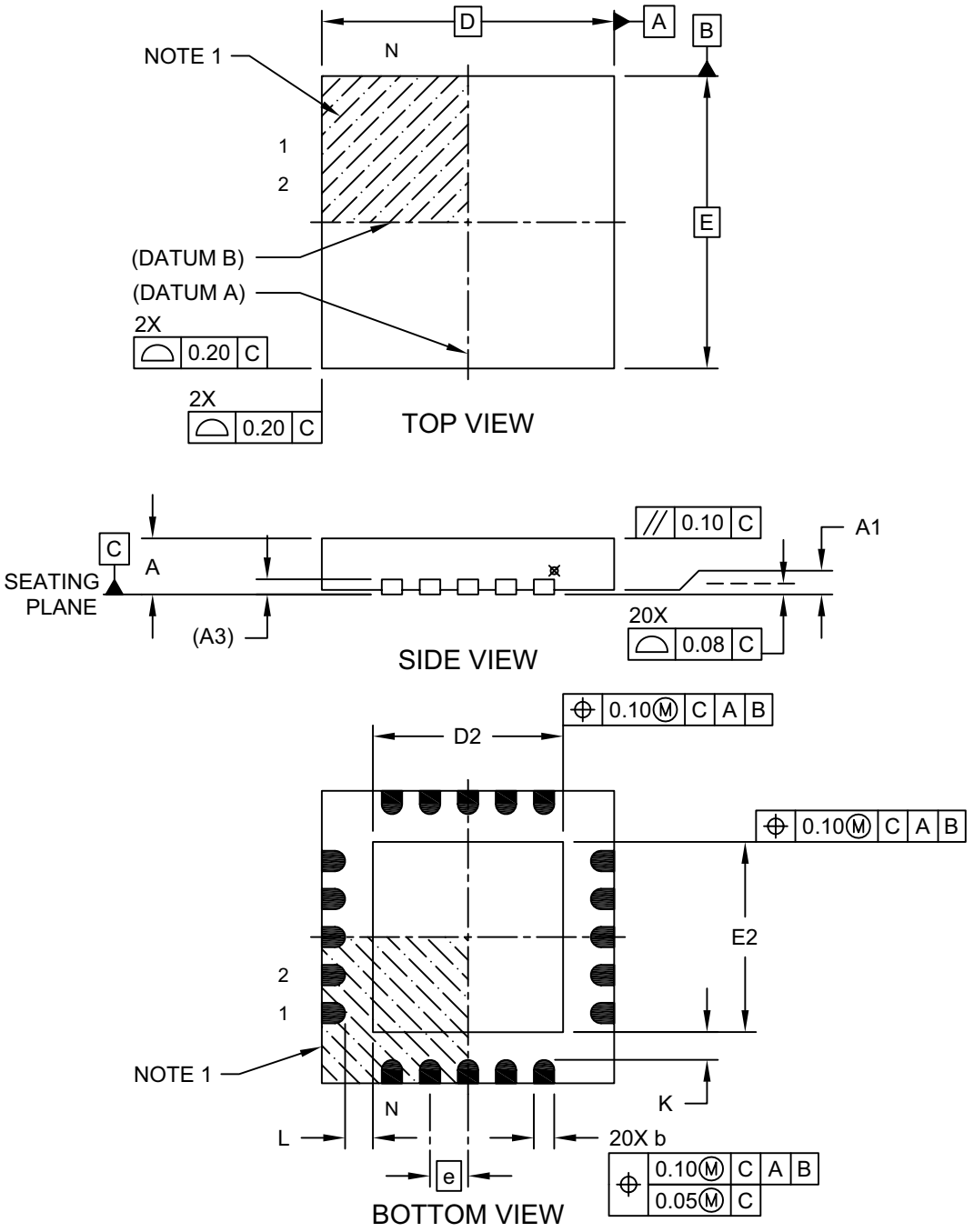
Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

20-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x1.0 mm Body [VQFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-139C (MQ) Sheet 1 of 2

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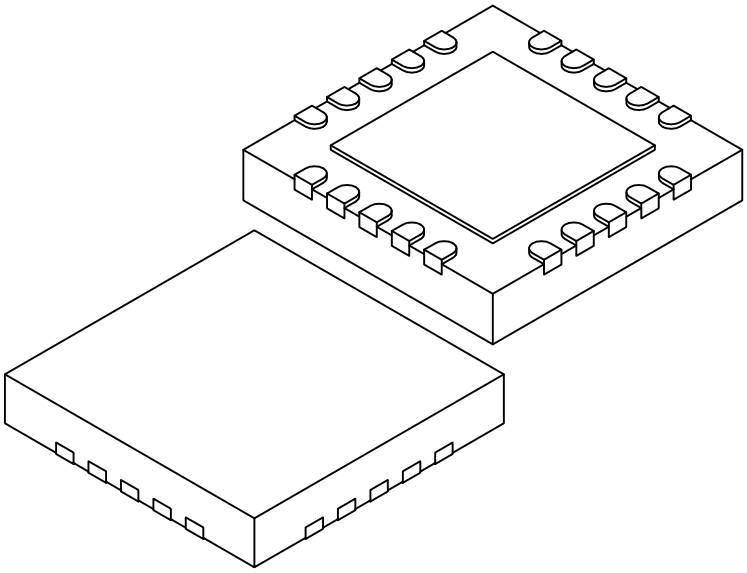
20-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x1.0 mm Body [VQFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	20		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	(A3)	0.20 REF		
Overall Length	D	5.00 BSC		
Exposed Pad Length	D2	3.15	3.25	3.35
Overall Width	E	5.00 BSC		
Exposed Pad Width	E2	3.15	3.25	3.35
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.35	0.40	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

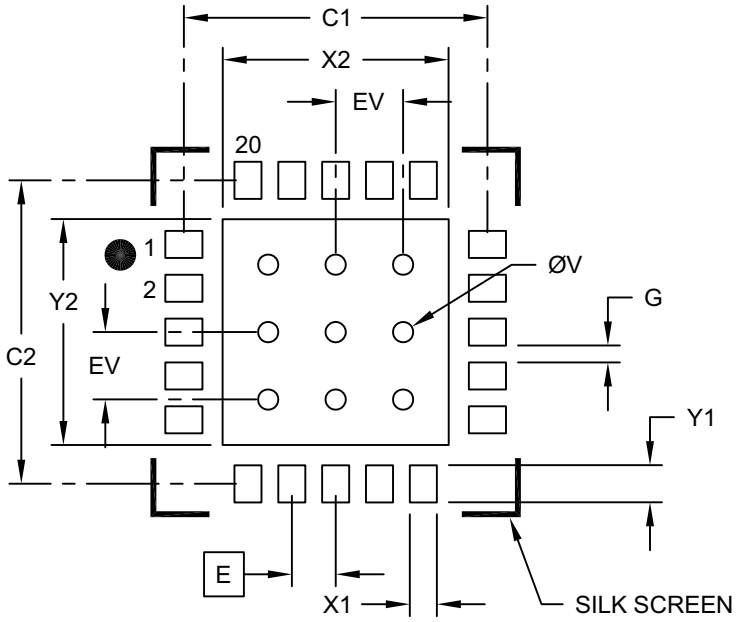
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-139C (MQ) Sheet 2 of 2

20-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x1.0 mm Body [VQFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			3.35
Optional Center Pad Length	T2			3.35
Contact Pad Spacing	C1		4.50	
Contact Pad Spacing	C2		4.50	
Contact Pad Width (X20)	X1			0.40
Contact Pad Length (X20)	Y1			0.55
Distance Between Pads	G	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2139B (MQ)

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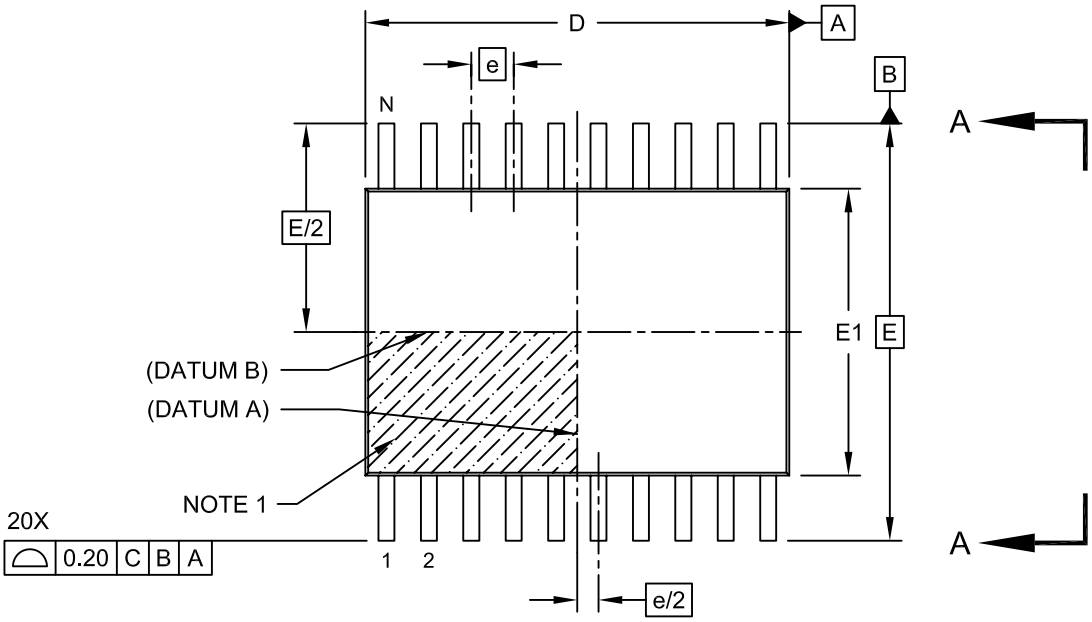
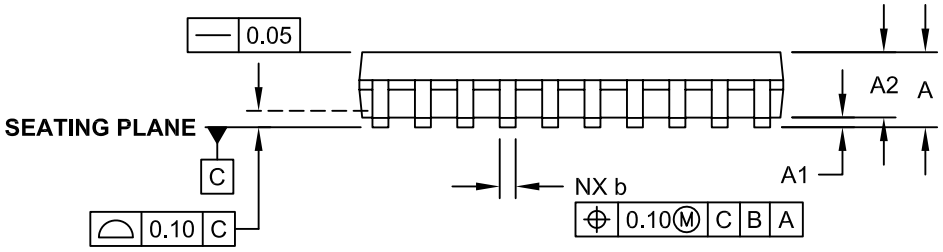
20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

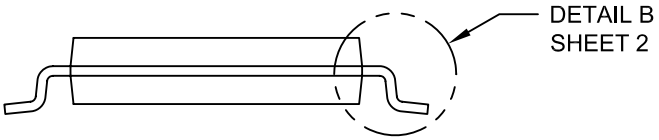
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

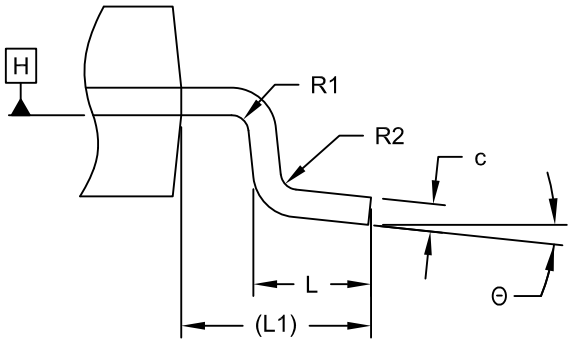


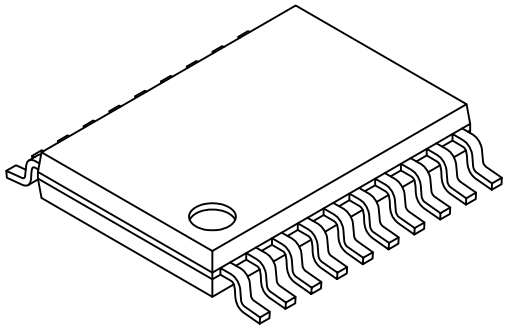
VIEW A—A

Microchip Technology Drawing C04-088C Sheet 1 of 2

20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	6.40	6.50	6.60
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	Θ	0°	-	8°
Lead Width	b	0.19	-	0.30
Lead Thickness	c	0.09	-	0.20
Bend Radius	R1	0.09	-	-
Bend Radius	R2	0.09	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-088C Sheet 2 of 2

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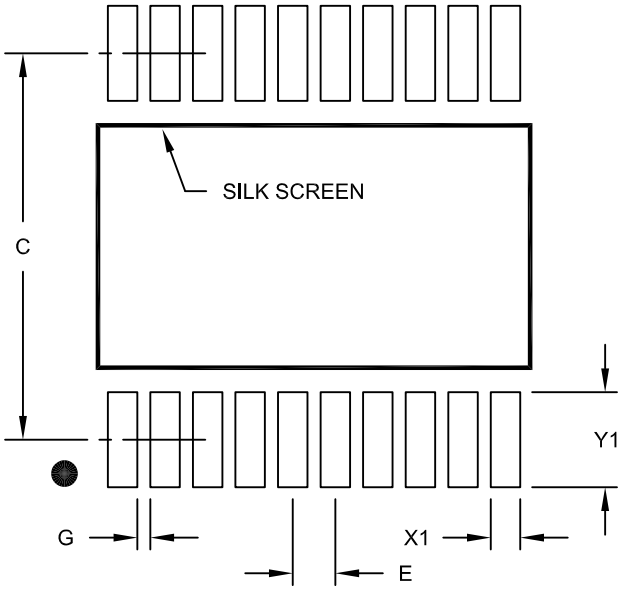
20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		5.90	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2088A

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (June 2020)

- Original release of this document.

NOTES:

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APPENDIX B: I²C SERIAL INTERFACE

This I²C interface is a two-wire interface that allows multiple devices to be connected to this two-wire bus. Figure B-1 shows a typical I²C interface connection.

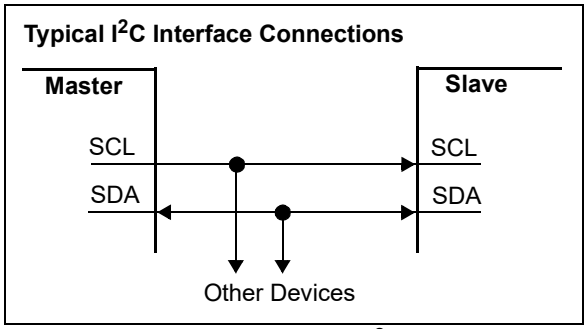

FIGURE B-1: TYPICAL I²C INTERFACE.

B.1 Overview

A device that sends data onto the bus is defined as transmitter, and a device receiving data is defined as receiver. The bus must be controlled by a master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions. Devices that do not generate a serial clock work as slave devices. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. Communication is initiated by the master (micro-controller), which sends the Start bit followed by the slave address byte. The first byte transmitted is always the slave address byte, which contains the device code, the address bits and the R/$\overline{W}$ bit.

The I²C interface specifies different communication bit rates. These are referred to as Standard, Fast or High-Speed modes. The MCP47FXBX4/8 supports these three modes. The clock rates (bit rate) of these modes are:

- Standard mode: up to 100 kHz (kbit/s)
- Fast mode: up to 400 kHz (kbit/s)
- High-Speed mode (HS mode): up to 3.4 MHz (Mbit/s)

The I²C protocol supports two addressing modes:

- 7-bit slave addressing
- 10-bit slave addressing (allows more devices on the I²C bus)

Only 7-bit slave addressing will be discussed in this section.

The I²C serial protocol allows multiple master devices on the I²C bus. This is referred to as Multi-master. For this, all master devices must support Multi-master operation. In this configuration, all master devices monitor their communication. If they detect that they wish to transmit a bit that is a logic high but is detected as a logic low (some other master device driving), they “get off” the bus. That is, they stop their communication and continue to listen to determine if the communication is directed towards them.

The I²C serial protocol only defines the field types, field lengths, timings, etc. of a frame. The frame content defines the behavior of the device. For details on the frame content (commands/data), refer to **Section 7.0 “I2C Device Commands”**.

The I²C serial protocol defines some commands called “General Call Addressing”, which allows the master device to communicate to all slave devices on the I²C bus.

Note:	Refer to the NXP Specification #UM10204, Rev. 03 19 June 2007 document for more details on the I²C specifications.

B.2 Signal Descriptions

The I²C interface uses two pins (signals). These are:

- SDA (Serial Data)
- SCL (Serial Clock)

B.2.1 SERIAL DATA (SDA)

The Serial Data (SDA) signal is the data signal of the device. The value on this pin is latched on the rising edge of the SCL signal when the signal is an input.

With the exception of the Start (Restart) and Stop conditions, the High or Low state of the SDA pin can only change when the clock signal on the SCL pin is low. During the high period of the clock, the SDA pin's value (high or low) must be stable. Changes in the SDA pin's value while the SCL pin is high will be interpreted as a Start or a Stop condition.

B.2.2 SERIAL CLOCK (SCL)

The Serial Clock (SCL) signal is the clock signal of the device. The rising edge of the SCL signal latches the value on the SDA pin.

Depending on the Clock Rate mode, the interface will display different characteristics.

B.3 I²C Operation

B.3.1 I²C BIT STATES AND SEQUENCE

Figure B-8 shows the I²C transfer sequence, while Figure B-7 shows the bit definitions. The Serial Clock is generated by the master. The following definitions are used for the bit states:

- Start bit (S)
- Data bit
- Acknowledge (A) bit (driven low)/
  No Acknowledge ($\overline{A}$) bit (not driven low)
- Repeated Start bit (Sr)
- Stop bit (P)

B.3.1.1 Start Bit

The Start bit (see Figure B-2) indicates the beginning of a data transfer sequence. The Start bit is defined as the SDA signal falling when the SCL signal is high.

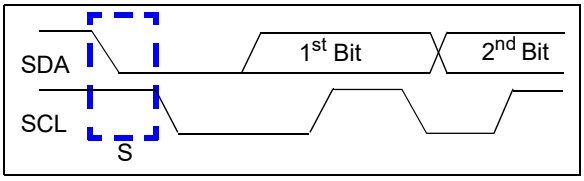

FIGURE B-2: START BIT.

B.3.1.2 Data Bit

The SDA signal may change state while the SCL signal is low. While the SCL signal is high, the SDA signal MUST be stable (see Figure B-3).

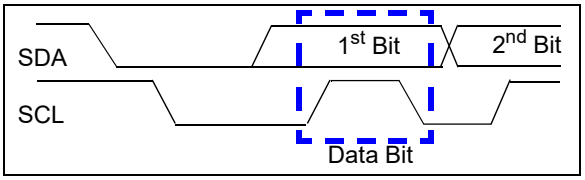

FIGURE B-3: DATA BIT.

B.3.1.3 Acknowledge (A) Bit

The A bit (see Figure B-4) is typically a response from the receiving device to the transmitting device. Depending on the context of the transfer sequence, the A bit may indicate different things. Typically, the slave device will supply an A response after the Start bit and eight data bits have been received. An A bit has the SDA signal low, while the $\overline{A}$ bit has the SDA signal high.

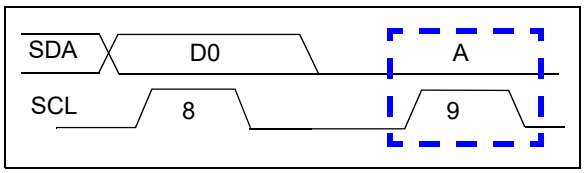

FIGURE B-4: ACKNOWLEDGE WAVEFORM.

Table B-1 shows some of the conditions where the slave device issues the A or Not A ($\overline{A}$).

If an error condition occurs (such as an $\overline{A}$ instead of A), then a Start bit must be issued to reset the command state machine.

TABLE B-1: MCP47FXBX4/8 A/$\overline{A}$ RESPONSES

Event	Acknowledge Bit Response	Comment
General Call	A	
Slave Address Valid	A	
Slave Address Not Valid	$\overline{A}$	
Communication during EEPROM Write Cycle	A	After the device has received address and command, and valid conditions for EEPROM write
Bus Collision	N/A	I²C module resets, or a "Don't Care" if the collision occurs on the master's Start bit

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B.3.1.4 Repeated Start Bit

The Repeated Start bit (see Figure B-5) indicates that the current master device wishes to continue communicating with the current slave device without releasing the I²C bus. The Repeated Start condition is the same as the Start condition, except that the Repeated Start bit follows a Start bit (with the Data bits + A bit) and not a Stop bit.

The Start bit is the beginning of a data transfer sequence and is defined as the SDA signal falling when the SCL signal is high.

> **Note 1:** A bus collision during the Repeated Start condition occurs if:
>
> •SDA is sampled low when SCL goes from low to high.
>
> •SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

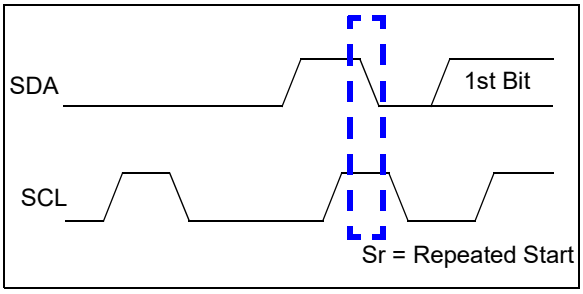

FIGURE B-5: REPEAT START CONDITION WAVEFORM.

B.3.1.5 Stop Bit

The Stop bit (see Figure B-6) Indicates the end of the I²C data transfer sequence. The Stop bit is defined as the SDA signal rising when the SCL signal is high.

A Stop bit should reset the I²C interface of the slave device.

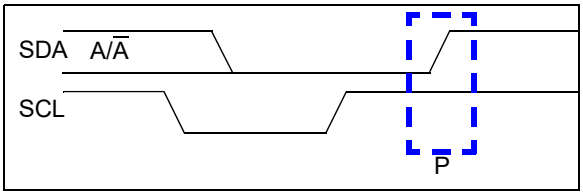

FIGURE B-6: STOP CONDITION RECEIVE OR TRANSMIT MODE.

B.3.2 CLOCK STRETCHING

Clock Stretching is something that the receiving device can do, to allow additional time to respond to the data that have been received.

B.3.3 ABORTING A TRANSMISSION

If any part of the I²C transmission does not meet the command format, it is aborted. This can be intentionally accomplished with a Start or Stop condition. This is done so that noisy transmissions (usually an extra Start or Stop condition) are aborted before they corrupt the device.

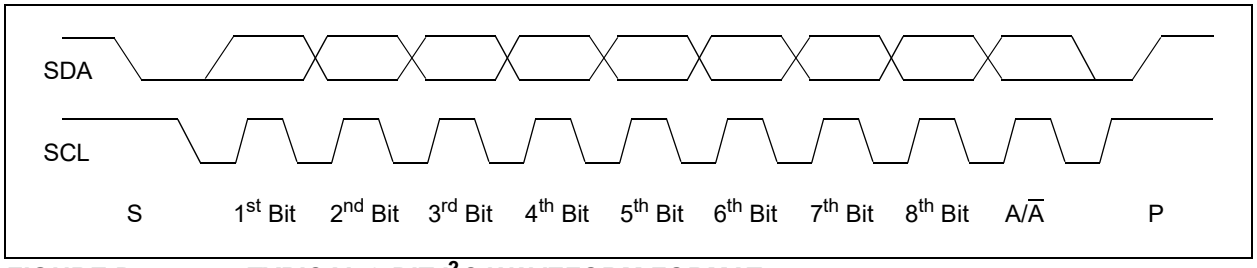

FIGURE B-7: TYPICAL 8-BIT I²C WAVEFORM FORMAT.

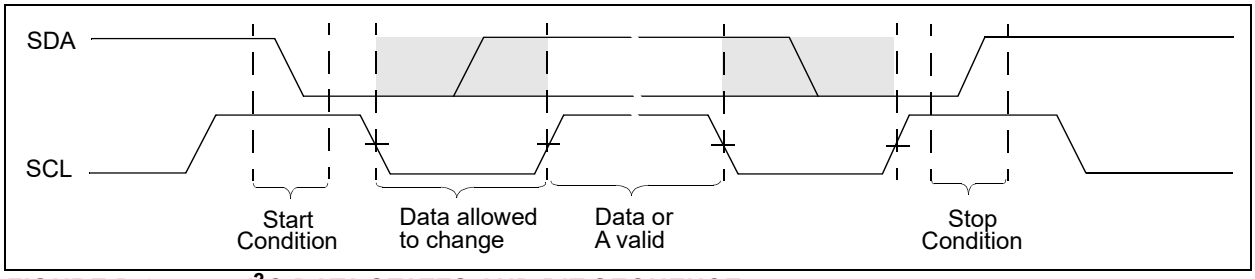

FIGURE B-8: I²C DATA STATES AND BIT SEQUENCE.

B.3.4 SLOPE CONTROL

As the device transitions from HS mode to FS mode, the slope control parameter changes from the HS specification to the FS specification.

For FS and HS modes, the device has a spike suppression and a Schmitt Trigger at SDA and SCL inputs.

B.3.5 DEVICE ADDRESSING

The I²C slave address control byte is the first byte received following the Start condition from the master device. This byte has seven bits to specify the slave address and the Read/Write control bit.

Figure B-9 shows the I²C slave address byte format, which contains the seven address bits and a Read/Write (R/$\overline{W}$) bit.

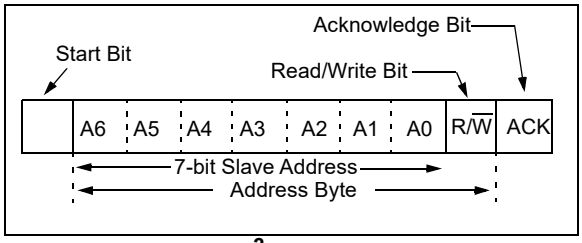

FIGURE B-9: I²C SLAVE ADDRESS CONTROL BYTE.

B.3.6 HS MODE

The I²C specification requires that a High-Speed mode device be activated to operate in HS (3.4 Mbit/s) mode. This is done by the master sending a special address byte following the Start bit. This byte is referred to as the High-Speed Master Mode Code (HSMMC).

The device can now communicate at up to 3.4 Mbit/s on SDA and SCL lines. The device will switch out of the HS mode on the next Stop condition.

The master code is sent as follows:

1. Start condition (S)
2. High-Speed Master Mode Code (`0000 1XXX`), The `XXX` bits are unique to the HS mode master.
3. No Acknowledge ($\overline{A}$)

After switching to the HS mode, the next transferred byte is the I²C control byte, which specifies the device to communicate with and any number of data bytes plus acknowledgments. The master device can then either issue a Repeated Start bit to address a different device (at high speed) or a Stop bit to return to fast/standard bus speed. After the Stop bit, any other master device (in a Multi-master system) can arbitrate for the I²C bus.

See Figure B-10 for an illustration of the HS mode command sequence.

For more information on the HS mode, or other I²C modes, refer to the "*NXP I²C Specification*".

B.3.6.1 Slope Control

The slope control on the SDA output is different between the Fast/Standard Speed and the High-Speed clock modes of the interface.

B.3.6.2 Pulse Gobbler

The pulse gobbler on the SCL pin is automatically adjusted to suppress spikes < 10 ns during HS mode.

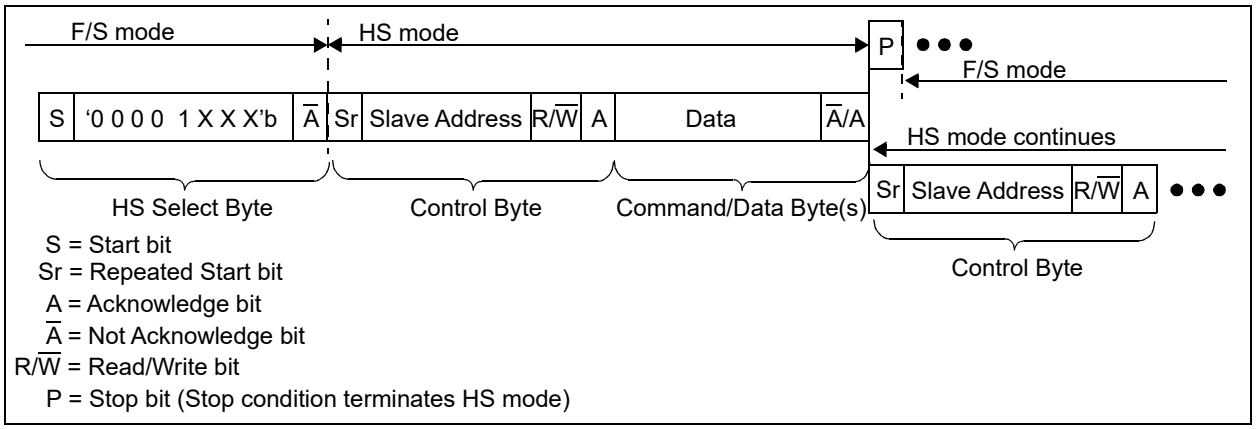

FIGURE B-10: HS MODE SEQUENCE.

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B.3.7 GENERAL CALL

The General Call is a method used by the master device to communicate with all other slave devices. In a Multi-master application, the other master devices operate in Slave mode. The General Call address has two documented formats. These are shown in Figure B-11.

The I²C specification documents three 7-bit command bytes.

The I²C specification does not allow '00000000' (00h) in the second byte. Also, '00000100' and '00000110' functionality is defined by the specification. Lastly, a data byte with a '1' in the LSb indicates a Hardware General Call.

For details on the operation of the MCP47FXBX4/8's General Call commands, see **Section 7.3 "General Call Commands"**.

> **Note:** Only one General Call command per issue of the General Call control byte. Any additional General Call commands are ignored and Not Acknowledged.

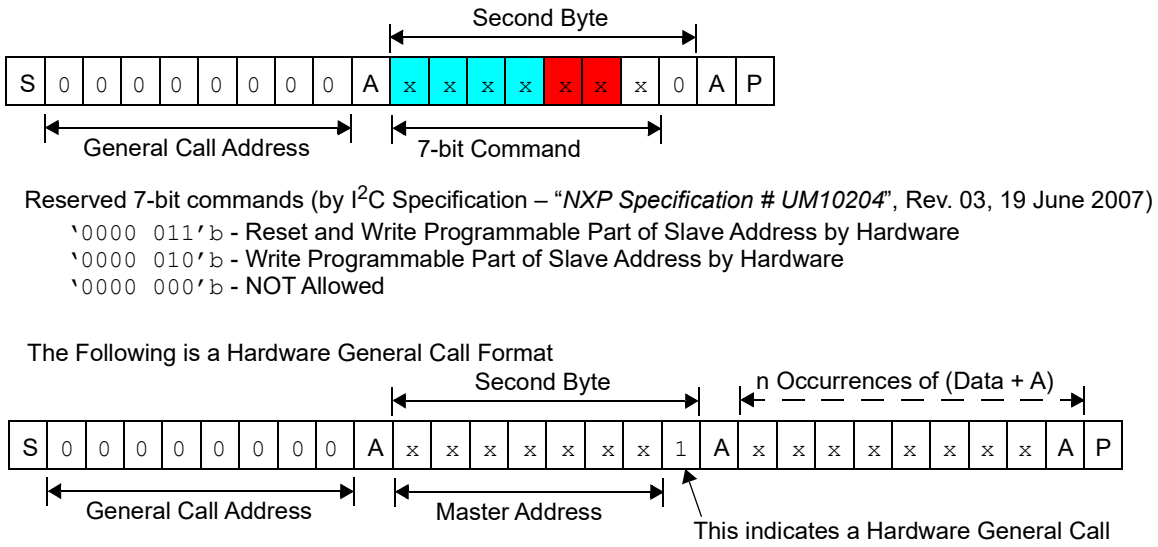

FIGURE B-11: GENERAL CALL FORMATS.

NOTES:

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APPENDIX C: TERMINOLOGY

C.1 Resolution

The resolution is the number of DAC output states that divide the Full-Scale Range (FSR). For the 12-bit DAC, the resolution is 2^{12}, meaning the DAC code ranges from 0 to 4095.

Note:	When there are 2^N resistors in the resistor ladder and 2^N tap points, the full-scale DAC register code is the resistor element (1 LSb) from the source reference voltage (V_{DD} or V_{REF}).

C.2 Least Significant Bit (LSb)

This is the voltage difference between two successive codes. For a given output voltage range, it is divided by the resolution of the device (Equation C-1). The range may be V_{DD} (or V_{REF}) to V_{SS} (ideal), the DAC register codes across the linear range of the output driver (Measured 1), or full scale to zero scale (Measured 2).

EQUATION C-1: LSb VOLTAGE CALCULATION

Ideal

$$V_{LSb(IDEAL)} = \frac{V_{DD}}{2^N} \quad \text{or} \quad \frac{V_{REF}}{2^N}$$

Measured 1

$$V_{LSb(Measured)} = \frac{V_{OUT(@4000)} - V_{OUT(@100)}}{(4000 - 100)}$$

Measured 2

$$V_{LSb} = \frac{V_{OUT(@FS)} - V_{OUT(@ZS)}}{2^N - 1}$$

2^N = 4096 (MCP47FEB2X)
= 1024 (MCP47FEB1X)
= 256 (MCP47FEB0X)

C.3 Monotonic Operation

Monotonic operation means that the device's output voltage (V_{OUT}) increases with every one code step (LSb) increment (from V_{SS} to the DAC's reference voltage (V_{DD} or V_{REF})).

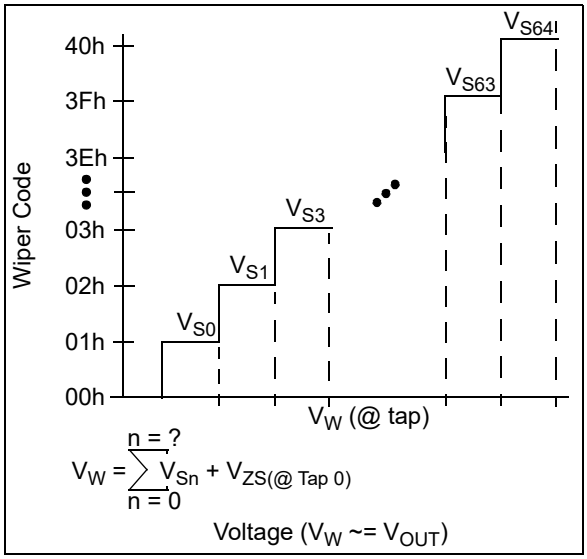

FIGURE C-1: V_W (V_{OUT}).

C.4 Full-Scale Error (E_{FS})

The Full-Scale error (see Figure C-3) is the error on the V_{OUT} pin relative to the expected V_{OUT} voltage (theoretical) for the maximum device DAC register code (code FFFh for 12-bit, code 3FFh for 10-bit, and code FFh for 8-bit), see Equation C-2. The error depends on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{SS}) greater than specified, the Full-Scale error will be greater.

The error in bits is determined by the theoretical voltage step size to give an error in LSb.

EQUATION C-2: FULL-SCALE ERROR

$$E_{FS} = \frac{V_{OUT(@FS)} - V_{IDEAL(@FS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{FS} is expressed in LSb.

$V_{OUT(@FS)}$ is the V_{OUT} voltage when the DAC register code is at full scale.

$V_{IDEAL(@FS)}$ is the ideal output voltage when the DAC register code is at full scale.

$V_{LSb(IDEAL)}$ is the theoretical voltage step size.

C.5 Zero-Scale Error (E_{ZS})

The Zero-Scale error (see Figure C-2) is the difference between the ideal and the measured V_{OUT} voltage with the DAC register code equal to 000h (Equation C-3). The error depends on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{DD}) greater than specified, the Zero-Scale error will be greater.

The error in bits is determined by the theoretical voltage step size to give an error in LSb.

EQUATION C-3: ZERO SCALE ERROR

$$E_{ZS} = \frac{V_{OUT(@ZS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{FS} is expressed in LSb.

$V_{OUT(@ZS)}$ is the V_{OUT} voltage when the DAC register code is at zero scale.

$V_{LSb(IDEAL)}$ is the theoretical voltage step size.

C.6 Total Unadjusted Error (E_T)

The Total Unadjusted error (E_T) is the difference between the ideal and measured V_{OUT} voltage. Typically, calibration of the output voltage is implemented to improve system's performance.

The error in bits is determined by the theoretical voltage step size to give an error in LSb.

Equation C-4 shows the Total Unadjusted error calculation:

EQUATION C-4: TOTAL UNADJUSTED ERROR CALCULATION

$$E_T = \frac{(V_{OUT\_Actual(@Code)} - V_{OUT\_Ideal(@Code)})}{V_{LSb(Ideal)}}$$

Where:

E_T is expressed in LSb.

$V_{OUT\_Actual(@Code)}$ = The measured DAC output voltage at the specified code

$V_{OUT\_Ideal(@Code)}$ = The calculated DAC output voltage at the specified code (code × $V_{LSb(Ideal)}$)

$V_{LSb(Ideal)}$ = V_{REF}/# Steps
12-bit = V_{REF}/4096
10-bit = V_{REF}/1024
8-bit = V_{REF}/256

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C.7 Offset Error (E_{OS})

The Offset error is the delta voltage of the V_{OUT} voltage from the ideal output voltage at the specified code. This code is specified where the output amplifier is in the linear operating range; for the MCP47FXBX4/8, we specify code 100 (decimal). Offset error does not include Gain error, see Figure C-2.

This error is expressed in mV. Offset error can be negative or positive. The Offset error can be calibrated by software in application circuits.

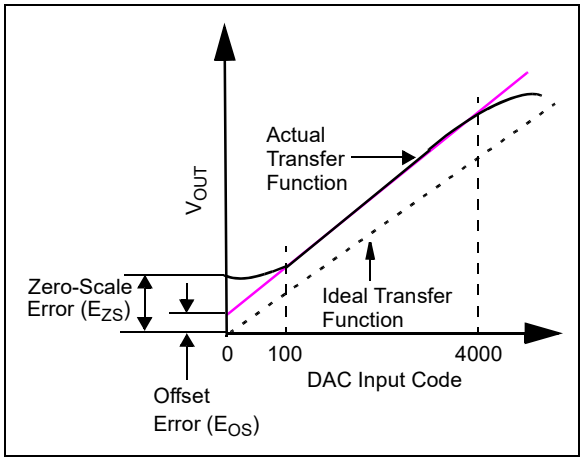

FIGURE C-2: OFFSET ERROR (ZERO GAIN ERROR).

C.8 Offset Error Drift (E_{OSD})

The Offset Error Drift is the variation in Offset error due to a change in ambient temperature. The Offset Error Drift is typically expressed in ppm/°C or µV/°C.

C.9 Gain Error (E_G)

Gain error is a calculation based on the ideal slope using the voltage boundaries for the linear range of the output driver (code 100 and code 4000) (see Figure C-3). The Gain error calculation nullifies the device's Offset error.

The Gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The gain error is usually expressed as a percent of Full-Scale Range (% of FSR) or in LSb. FSR is the ideal full-scale voltage of the DAC (see Equation C-5).

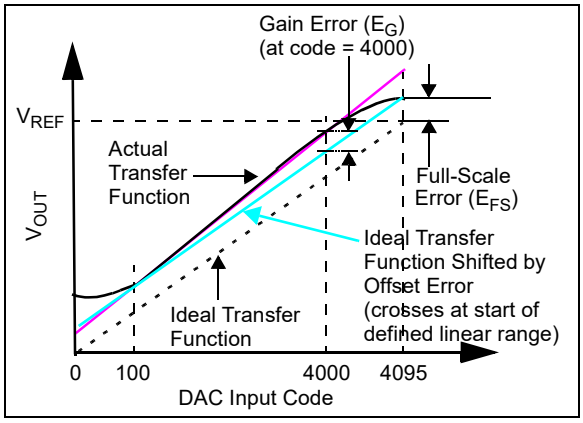

FIGURE C-3: GAIN ERROR AND FULL-SCALE ERROR EXAMPLE.

EQUATION C-5: EXAMPLE GAIN ERROR

$$E_G = \frac{(V_{OUT(@4000)} - V_{OS} - V_{OUT\_Ideal(@4000)})}{V_{Full\text{-}Scale\ Range}} \cdot 100$$

Where:

E_G is expressed in % of FSR.

$V_{OUT(@4000)}$	=	The measured DAC output voltage at the specified code
$V_{OUT\_Ideal(@4000)}$	=	The calculated DAC output voltage at the specified code ($4000 \times V_{LSb(Ideal)}$)
V_{OS}	=	Measured offset voltage
$V_{Full\text{-}Scale\ Range}$	=	Expected full-scale output value (such as the V_{REF} voltage)

C.10 Gain Error Drift (E_{GD})

The Gain Error Drift is the variation in Gain error due to a change in ambient temperature. The Gain Error Drift is typically expressed in ppm/°C (of FSR).

C.11 Integral Nonlinearity (INL)

The Integral Nonlinearity (INL) error is the maximum deviation of an actual transfer function from an ideal transfer function (straight line) passing through the defined end points of the DAC transfer function (after Offset and Gain errors have been removed).

For the MCP47FXBX4/8, INL is calculated using the defined end points, DAC code 100 and code 4000. INL can be expressed as a percentage of FSR or in LSb. INL is also called Relative Accuracy. Equation C-6 shows how to calculate the INL error in LSb and Figure C-4 shows an example of INL accuracy.

Positive INL means V_{OUT} voltage higher than the ideal one. Negative INL means V_{OUT} voltage lower than the ideal one.

EQUATION C-6: INL ERROR

$$E_{INL} = \frac{(V_{OUT} - V_{Calc\_Ideal})}{V_{LSb(Measured)}}$$

Where:

INL is expressed in LSb.

V_{Calc_Ideal} = Code × $V_{LSb(Measured)}$ + V_{OS}

$V_{OUT(Code = n)}$ = The measured DAC output voltage with a given DAC register code

$V_{LSb(Measured)}$ = For Measured: $(V_{OUT(4000)} - V_{OUT(100)})/3900$

V_{OS} = Measured offset voltage

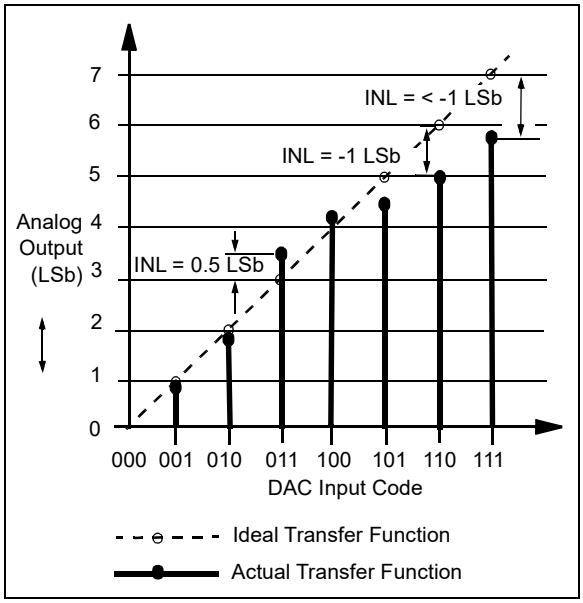

FIGURE C-4: INL ACCURACY.

C.12 Differential Nonlinearity (DNL)

The Differential Nonlinearity (DNL) error (see Figure C-5) is the measure of step-size between codes in an actual transfer function. The ideal step-size between codes is 1 LSb. A DNL error of zero would imply that every code is exactly 1 LSb wide. If the DNL error is less than 1 LSb, the DAC guarantees monotonic output and no missing codes. Equation C-7 shows how to calculate the DNL error between any two adjacent codes in LSb.

EQUATION C-7: DNL ERROR

$$E_{DNL} = \frac{(V_{OUT(code = n+1)} - V_{OUT(code = n)})}{V_{LSb(Measured)}} - 1$$

Where:

DNL is expressed in LSb.

$V_{OUT(code = n)}$ = The measured DAC output voltage with a given DAC register code.

$V_{LSb(Measured)}$ = For Measured: $(V_{OUT(4000)} - V_{OUT(100)})/3900$

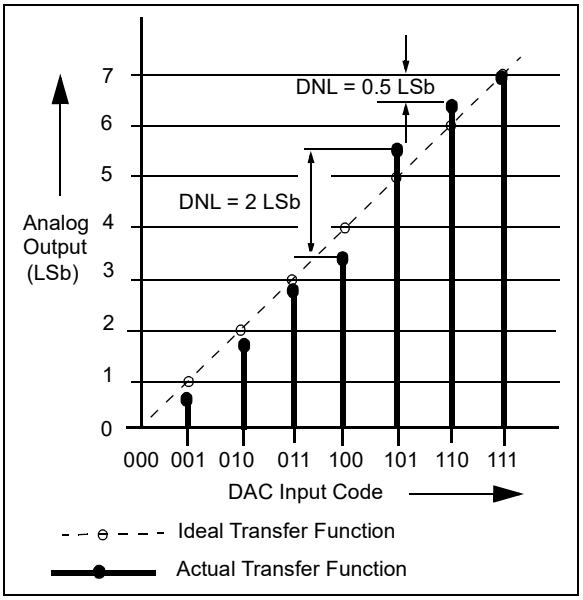

FIGURE C-5: DNL ACCURACY.

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C.13 Settling Time

The settling time is the time delay required for the V_{OUT} voltage to settle into its new output value. This time is measured from the start of code transition to when the V_{OUT} voltage is within the specified accuracy.

For the MCP47FXBX4/8, the settling time is a measurement of the time delay until the V_{OUT} voltage reaches within 0.5 LSb of its final value, when the volatile DAC register changes from 1/4 to 3/4 of the FSR (12-bit device: 400h to C00h).

C.14 Major Code Transition Glitch

Major code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes the state. It is normally specified as the area of the glitch in nV-Sec and is measured when the digital code is changed by 1 LSb at the major carry transition (Example: `011...111` to `100... 000`, or `100... 000` to `011 ... 111`).

C.15 Digital Feed-through

The digital feed-through is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. The area of the glitch is expressed in nV-Sec and is measured with a full-scale change (Example: all '`0`'s to all '`1`'s and vice versa) on the digital input pins. The digital feed-through is measured when the DAC is not written to the output register.

C.16 -3 dB Bandwidth

This is the frequency of the signal at the V_{REF} pin that causes the voltage at the V_{OUT} pin to fall -3 dB from a static value on the V_{REF} pin. The output decreases due to the RC characteristics of the resistor ladder and the characteristics of the output buffer.

C.17 Power-Supply Sensitivity (PSS)

PSS indicates how the output of the DAC is affected by changes in the supply voltage. PSS is the ratio of the change in V_{OUT} to a change in V_{DD} for mid-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied from 5.5V to 2.7V as a step (V_{REF} voltage held constant), and expressed in %/%, which is the % change of the DAC output voltage with respect to the % change of the V_{DD} voltage.

EQUATION C-8: PSS CALCULATION

$$PSS = \frac{(V_{OUT(@5.5V)} - V_{OUT(@2.7V)}) / V_{OUT(@5.5V)}}{(5.5V - 2.7V) / (5.5V)}$$

Where:

PSS is expressed in % / %.

$V_{OUT(@5.5V)}$ = The measured DAC output voltage with V_{DD} = 5.5V

$V_{OUT(@2.7V)}$ = The measured DAC output voltage with V_{DD} = 2.7V

C.18 Power-Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied ±10% (V_{REF} voltage held constant) and expressed in dB or µV/V.

C.19 V_{OUT} Temperature Coefficient

The V_{OUT} temperature coefficient quantifies the error in the resistor ladder's resistance ratio (DAC register code value) and output buffer due to temperature drift.

C.20 Absolute Temperature Coefficient

The absolute temperature coefficient quantifies the error in the end-to-end output voltage (nominal output voltage V_{OUT}) due to temperature drift. For a DAC, this error is typically not an issue due to the ratiometric aspect of the output.

C.21 Noise Spectral Density

The noise spectral density is a measurement of the device's internally generated random noise and is characterized as a spectral density (voltage per √Hz). It is measured by loading the DAC to the mid-scale value and measuring the noise at the V_{OUT} pin. It is measured in nV/√Hz.

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NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	— XX	X	/XX
Device	Tape and Reel	Pin Count	Temperature Range	Package

Device:	MCP47FXB0X:	Quad/Octal-Channel, 8-Bit DAC with I^2C Interface
	MCP47FXB1X:	Quad/Octal-Channel, 10-Bit DAC with I^2C Interface
	MCP47FXB2X:	Quad/Octal-Channel, 12-Bit DAC with I^2C Interface
Tape and Reel:	T =	Tape and Reel
	Blank =	Tube
Pin Count:	20-Lead	
Temperature Range:	E =	-40°C to +125°C (Extended)
Package:	MQ =	Plastic Quad Flat, No Lead Package (VQFN), 5 x 5 mm, 20-Lead
	ST =	Plastic Thin Shrink Small Outline Package (TSSOP), 20-Lead

Examples:

a) MCP47FEB04-E/MQ: Quad-Channel, 8-Bit Nonvolatile DAC, Extended Temperature, 20LD VQFN.

b) MCP47FEB08T-E/MQ: Octal-Channel, 8-Bit Nonvolatile DAC, Tape and Reel, Extended Temperature, 20LD VQFN.

c) MCP47FEB18-20E/ST: Octal-Channel, 10-Bit Nonvolatile DAC, Extended Temperature, 20LD TSSOP.

d) MCP47FEB18T-20E/ST: Octal-Channel, 10-Bit Nonvolatile DAC, Tape and Reel, Extended Temperature, 20LD TSSOP.

e) MCP47FVB28-E/MQ: Octal-Channel, 12-Bit Volatile DAC, Extended Temperature, 20LD VQFN.

f) MCP47FVB28T-E/MQ: Octal-Channel, 12-Bit Volatile DAC, Tape and Reel, Extended Temperature, 20LD VQFN.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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