

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: XMC4700E196F2048AAXQMA1

Manufacturer: Infineon Technologies

Package: 196-LFBGA

Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/infineon-technologies-xmc4700e196f2048aaxqma1.html>

Request a Quote:

[Submit RFQ for this part](#)



Scan for product page

Contact Information

Email: info@antrexco.com

WhatsApp: +86-186-8066-5326

Website: <https://antrexco.com>

Quality & Trust

New & Original Components

Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

Secure sourcing support for OEM / EMS projects

Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

XMC4700/XMC4800

Microcontroller Series for Industrial Applications

ARM® Cortex® -M4
32-bit processor core

About this Document

This datasheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4[78]00 series devices.

The document describes the characteristics of a superset of the XMC4[78]00 series devices. For simplicity, the various device types are referred to by the collective term XMC4[78]00 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
 - describes the functionality of the superset of devices.
- **Datasheets**
 - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
 - list deviations from the specifications given in the related Reference Manual or Datasheets. Errata Sheets are provided for the superset of devices.

Attention: *Please consult all parts of the documentation set to attain consolidated knowledge about your device.*

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to <http://www.infineon.com/xmc4000> to get access to the latest versions of those documents.

Table of contents

	About this Document	1
	Table of contents	2
1	Summary of Features	4
1.1	Ordering Information	6
1.2	Device Types	6
1.3	Device Type Features	7
1.4	Definition of Feature Variants	9
1.5	Identification Registers	10
2	General Device Information	11
2.1	Logic Symbols	11
2.2	Pin Configuration and Definition	14
2.2.1	Package Pin Summary	16
2.2.2	Port I/O Functions	25
2.2.2.1	Port I/O Function Table	26
2.3	Power Connection Scheme	47
3	Electrical Parameters	48
3.1	General Parameters	48
3.1.1	Parameter Interpretation	48
3.1.2	Absolute Maximum Ratings	48
3.1.3	Pin Reliability in Overload	50
3.1.4	Pad Driver and Pad Classes Summary	52
3.1.5	Operating Conditions	53
3.2	DC Parameters	54
3.2.1	Input/Output Pins	54
3.2.2	Analog to Digital Converters (VADC)	60
3.2.3	Digital to Analog Converters (DAC)	64
3.2.4	Out-of-Range Comparator (ORC)	67
3.2.5	Die Temperature Sensor	68
3.2.6	USB OTG Interface DC Characteristics	69
3.2.7	Oscillator Pins	71
3.2.8	Power Supply Current	73
3.2.9	Flash Memory Parameters	77
3.3	AC Parameters	78
3.3.1	Testing Waveforms	78
3.3.2	Power-Up and Supply Monitoring	79
3.3.3	Power Sequencing	80
3.3.4	Phase Locked Loop (PLL) Characteristics	81
3.3.5	Internal Clock Source Characteristics	82

Table of contents

3.3.6	JTAG Interface Timing	83
3.3.7	Serial Wire Debug Port (SW-DP) Timing	84
3.3.8	Embedded Trace Macro Cell (ETM) Timing	85
3.3.9	Peripheral Timing	86
3.3.9.1	Delta-Sigma Demodulator Digital Interface Timing	86
3.3.9.2	Synchronous Serial Interface (USIC SSC) Timing	87
3.3.9.3	Inter-IC (IIC) Interface Timing	89
3.3.9.4	Inter-IC Sound (IIS) Interface Timing	91
3.3.9.5	SDMMC Interface Timing	92
3.3.10	EBU Timing	100
3.3.10.1	EBU Asynchronous Timing	100
3.3.10.2	EBU Burst Mode Access Timing	106
3.3.10.3	EBU Arbitration Signal Timing	108
3.3.10.4	EBU SDRAM Access Timing	109
3.3.11	USB Interface Characteristics	113
3.3.12	Ethernet Interface (ETH) Characteristics	113
3.3.12.1	ETH Measurement Reference Points	113
3.3.12.2	ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)	114
3.3.12.3	ETH MII Parameters	115
3.3.12.4	ETH RMII Parameters	116
3.3.13	EtherCAT (ECAT) Characteristics	117
3.3.13.1	ECAT Measurement Reference Points	117
3.3.13.2	ETH Management Signal Parameters (MCLK, MDIO)	117
3.3.13.3	MII Timing TX Characteristics	118
3.3.13.4	MII Timing RX Characteristics	119
3.3.13.5	Sync/Latch Timings	120
4	Package and Reliability	121
4.1	Package Parameters	121
4.1.1	Thermal Considerations	122
4.2	Package Outlines	123
5	Quality Declarations	127
	Revision history	128
	Disclaimer	129

1 Summary of Features

1 Summary of Features

The XMC4[78]00 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

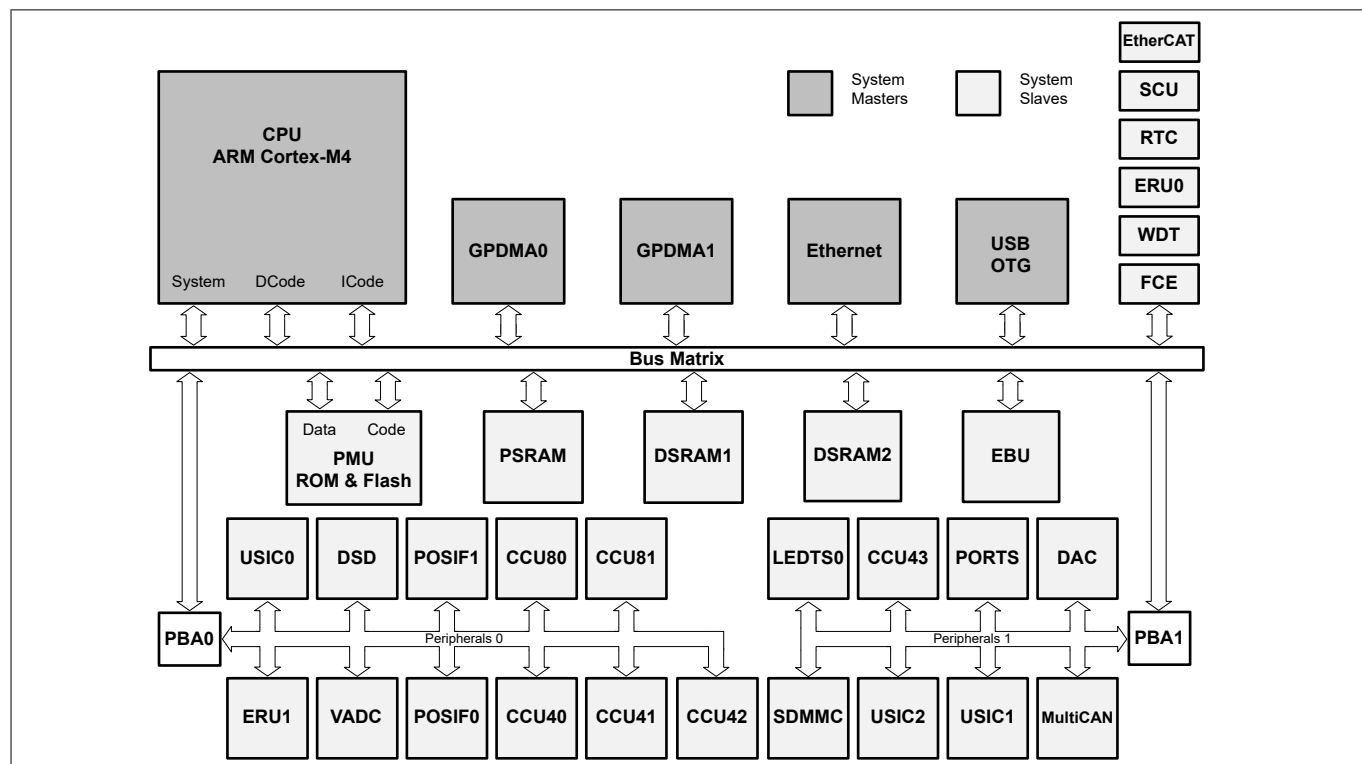


Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
 - High performance 32-bit ARM Cortex-M4 CPU
 - 16-bit and 32-bit Thumb2 instruction set
 - DSP/MAC instructions
 - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- General Purpose DMA with up-to 12 channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

On-Chip Memories

- 16 KB on-chip boot ROM
- 96 KB on-chip high-speed program memory
- 128 KB on-chip high speed data memory
- 128 KB on-chip high-speed communication memory
- 2,048 KB on-chip Flash Memory with 8 KB instruction cache

1 Summary of Features

Communication Peripherals

- Ethernet MAC module capable of 10/100 Mbit/s transfer rates
- EtherCATSlave interface (ECAT) capable of 100 Mbit/s transfer rates with 2 MII ports, 8 Fieldbus Memory Management Units (FMMU), 8 Sync Manager, 64 bit distributed clocks
- Universal Serial Bus, USB 2.0 host, Full-Speed OTG, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with 6 nodes, 256 message objects (MO), data rate up to 1 Mbaud
- Six Universal Serial Interface Channels (USIC), providing 6 serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface
- SD and Multi-Media Card interface (SDMMC) for data storage memory cards
- External Bus Interface Unit (EBU) enabling communication with external memories and off-chip peripherals

Analog Frontend Peripherals

- Four Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Delta Sigma Demodulator with four channels, digital input stage for A/D signal conversion
- Digital-Analog Converter (DAC) with two channels of 12-bit resolution

Industrial Control Peripherals

- Two Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Two Position Interfaces (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

On-Chip Debug Support

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

1 Summary of Features

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC4<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
 - E: LFBGA
 - F: LQFP
 - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
 - F: -40°C to 85°C
 - K: -40°C to 125°C
- <FFFF> the Flash memory size

For ordering codes for the XMC4[78]00 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4[78]00 series, some descriptions may not apply to a specific product. Please see [Table 1](#).

For simplicity the term **XMC4[78]00** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 1 Synopsis of XMC4[78]00 Device Types

Derivative ¹⁾	Package	Flash Kbytes	SRAM Kbytes
XMC4700-E196x2048	PG-LFBGA-196	2048	352
XMC4700-F144x2048	PG-LQFP-144	2048	352
XMC4700-F100x2048	PG-LQFP-100	2048	352
XMC4700-E196x1536	PG-LFBGA-196	1536	276
XMC4700-F144x1536	PG-LQFP-144	1536	276
XMC4700-F100x1536	PG-LQFP-100	1536	276
XMC4800-E196x2048	PG-LFBGA-196	2048	352
XMC4800-F144x2048	PG-LQFP-144	2048	352
XMC4800-F100x2048	PG-LQFP-100	2048	352
XMC4800-E196x1536	PG-LFBGA-196	1536	276
XMC4800-F144x1536	PG-LQFP-144	1536	276
XMC4800-F100x1536	PG-LQFP-100	1536	276
XMC4800-E196x1024	PG-LFBGA-196	1024	200
XMC4800-F144x1024	PG-LQFP-144	1024	200
XMC4800-F100x1024	PG-LQFP-100	1024	200

1) x is a placeholder for the supported temperature range.

1 Summary of Features

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC4[78]00 Device Types

Derivative ¹⁾	LEDTS Intf.	SD MMC Intf.	EBU Intf. ²⁾	ETH Intf. ³⁾	ECAT Slave Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4700-E196x2048	1	1	SDM	MR	–	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F144x2048	1	1	SDM	MR	–	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F100x2048	1	1	M16	R	–	1	3 x 2	N[0..5] MO[0..255]
XMC4700-E196x1536	1	1	SDM	MR	–	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F144x1536	1	1	SDM	MR	–	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F100x1536	1	1	M16	R	–	1	3 x 2	N[0..5] MO[0..255]
XMC4800-E196x2048	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F144x2048	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F100x2048	1	1	M16	R	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-E196x1536	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F144x1536	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F100x1536	1	1	M16	R	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-E196x1024	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F144x1024	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F100x1024	1	1	M16	R	2 x MII	1	3 x 2	N[0..5] MO[0..255]

1) x is a placeholder for the supported temperature range.

2) Memory types supported S=SDRAM, D=DEMUX, M=MUX 16-bit and 32-bit, M16=MUX 16-bit.

3) Supported interfaces, M=MII, R=RMII.

1 Summary of Features

Table 3 **Features of XMC4[78]00 Device Types**

Derivative¹⁾	ADC Chan.	DSD Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice	POSIF Intf.
XMC4700-E196x2048	32	4	2	4 x 4	2 x 4	2
XMC4700-F144x2048	32	4	2	4 x 4	2 x 4	2
XMC4700-F100x2048	24	4	2	4 x 4	2 x 4	2
XMC4700-E196x1536	32	4	2	4 x 4	2 x 4	2
XMC4700-F144x1536	32	4	2	4 x 4	2 x 4	2
XMC4700-F100x1536	24	4	2	4 x 4	2 x 4	2
XMC4800-E196x2048	32	4	2	4 x 4	2 x 4	2
XMC4800-F144x2048	32	4	2	4 x 4	2 x 4	2
XMC4800-F100x2048	24	4	2	4 x 4	2 x 4	2
XMC4800-E196x1536	32	4	2	4 x 4	2 x 4	2
XMC4800-F144x1536	32	4	2	4 x 4	2 x 4	2
XMC4800-F100x1536	24	4	2	4 x 4	2 x 4	2
XMC4800-E196x1024	32	4	2	4 x 4	2 x 4	2
XMC4800-F144x1024	32	4	2	4 x 4	2 x 4	2
XMC4800-F100x1024	24	4	2	4 x 4	2 x 4	2

1) x is a placeholder for the supported temperature range.

1 Summary of Features

1.4 Definition of Feature Variants

The XMC4[78]00 types are offered with several memory sizes and number of available VADC channels. [Table 4](#) describes the location of the available Flash memory, [Table 5](#) describes the location of the available SRAMs, [Table 6](#) the available VADC channels.

Table 4 Flash Memory Ranges

Total Flash Size	Cached Range	Uncached Range
1,024 Kbytes	0800 0000 _H – 080F FFFF _H	0C00 0000 _H – 0C0F FFFF _H
1,536 Kbytes	0800 0000 _H – 0817 FFFF _H	0C00 0000 _H – 0C17 FFFF _H
2,048 Kbytes	0800 0000 _H – 081F FFFF _H	0C00 0000 _H – 0C1F FFFF _H

Table 5 SRAM Memory Ranges

Total SRAM Size	Program SRAM	System Data SRAM	Communication Data SRAM
200 Kbytes	1FFE E000 _H – 1FFF FFFF _H	2000 0000 _H – 2001 FFFF _H	–
276 Kbytes	1FFE 8000 _H – 1FFF FFFF _H	2000 0000 _H – 2001 FFFF _H	2002 0000 _H – 2002 CFFF _H
352 Kbytes	1FFE 8000 _H – 1FFF FFFF _H	2000 0000 _H – 2001 FFFF _H	2002 0000 _H – 2003 FFFF _H

Table 6 ADC Channels¹⁾

Package	VADC G0	VADC G1	VADC G2	VADC G3
PG-LQFP-144	CH0..CH7	CH0..CH7	CH0..CH7	CH0..CH7
PG-LFBGA-196				
PG-LQFP-100	CH0..CH7	CH0..CH7	CH0..CH3	CH0..CH3

¹⁾ Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1 Summary of Features

1.5 Identification Registers

The identification registers allow software to identify the marking.

Table 7 XMC4700 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 7001 _H	EES-AA, ES-AA, AA
JTAG IDCODE	101D F083 _H	EES-AA, ES-AA, AA

Table 8 XMC4800 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 8001 _H	EES-AA, ES-AA, AA
JTAG IDCODE	101D F083 _H	EES-AA, ES-AA, AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

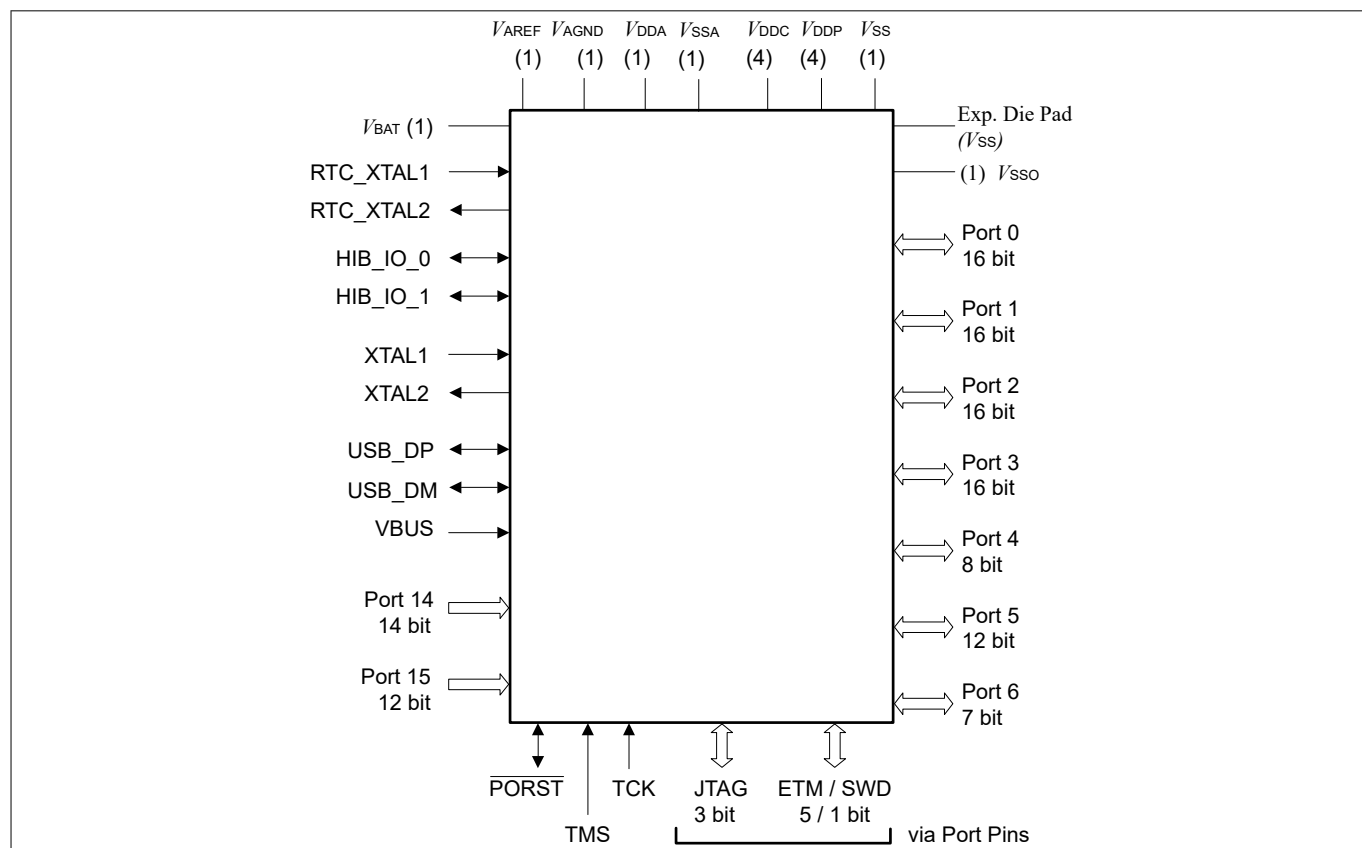


Figure 2 **XMC4[78]00 Logic Symbol PG-LQFP-144**

2 General Device Information

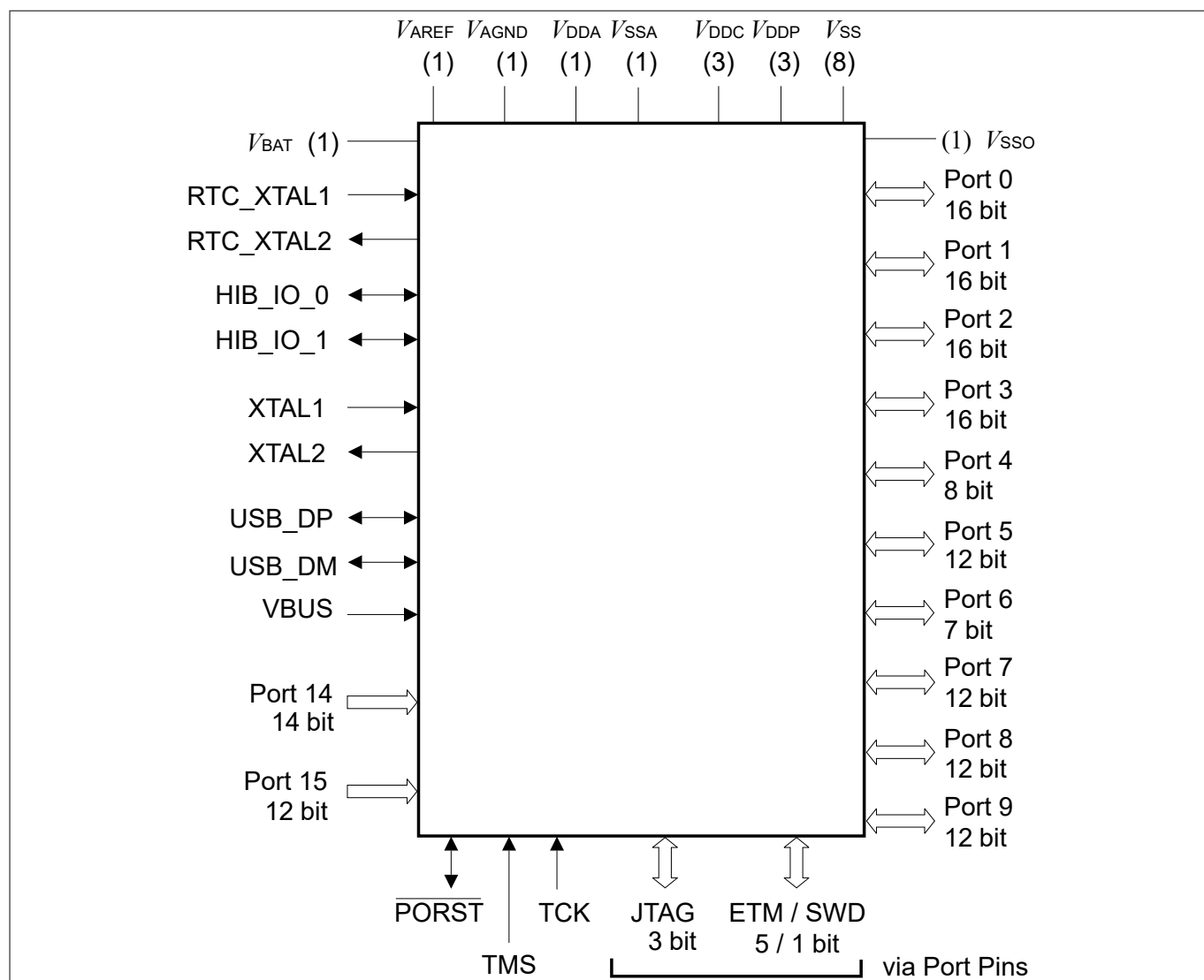


Figure 3 XMC4[78]00 Logic Symbol PG-LFBGA-196

2 General Device Information

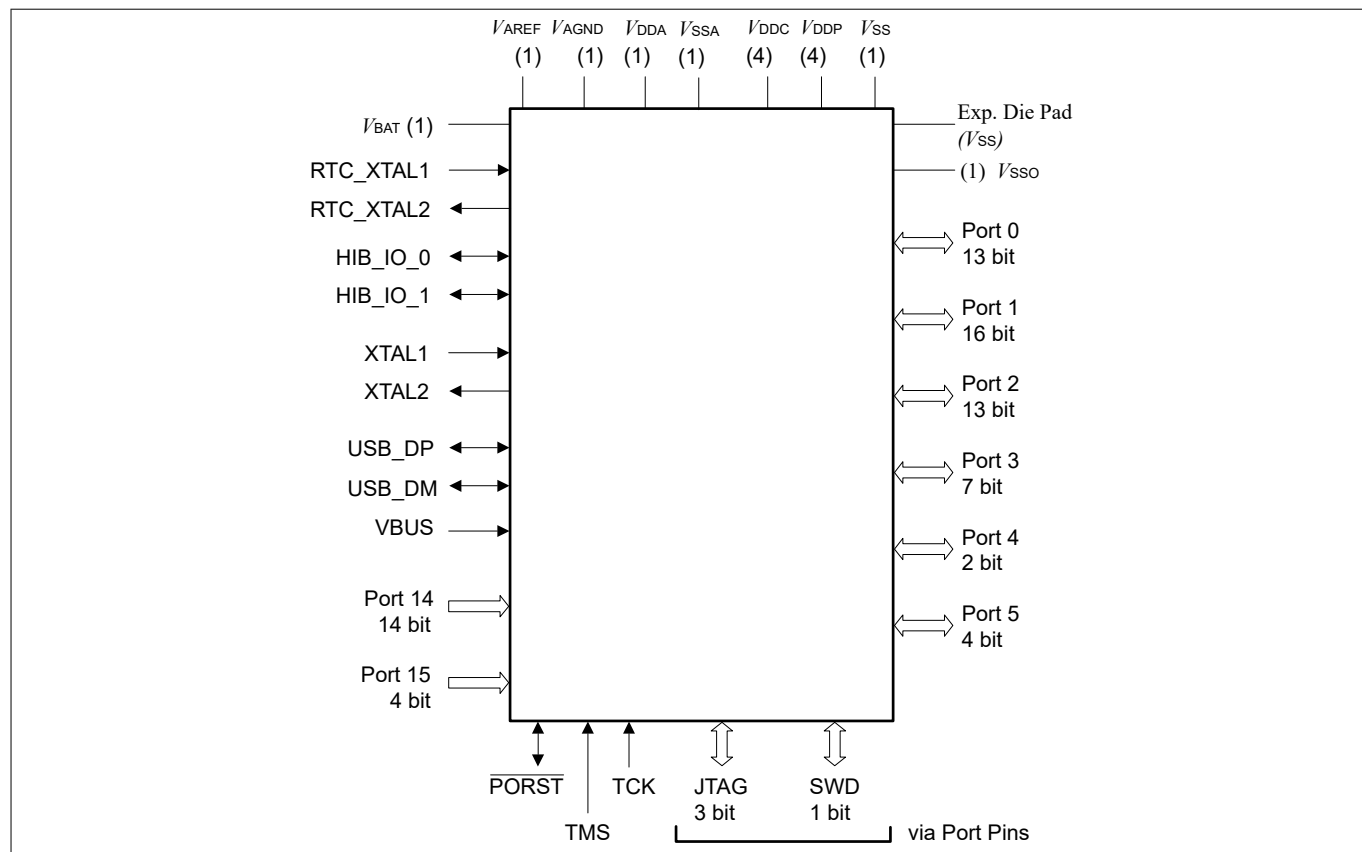


Figure 4 XMC4[78]00 Logic Symbol PG-LQFP-100

2 General Device Information

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the four sides of the different packages.

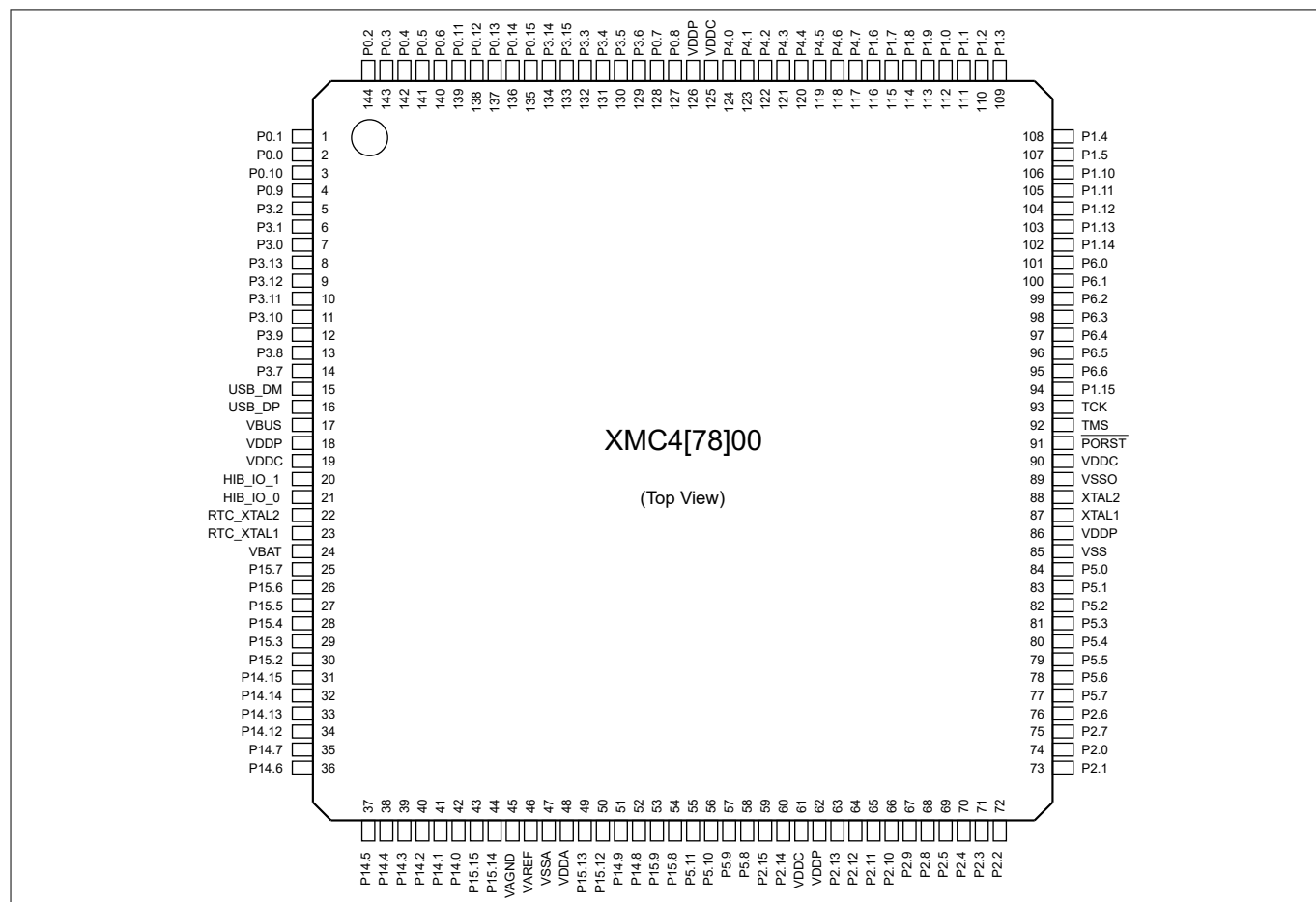


Figure 5 XMC4[78]00 PG-LQFP-144 Pin Configuration (top view)

2 General Device Information

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	P8.6	P8.8	P8.10	P8.9	P8.11	P8.1	P9.8	P9.7	P9.9	P9.5	P9.4	n.c.	VSS	A
B	n.c.	P8.3	P8.2	P8.7	P8.5	P8.4	P8.0	P9.10	P9.11	n.c.	P9.6	n.c.	VSS	n.c.	B
C	VSS	VDDC	P0.2	P0.3	P0.5	P0.6	P3.6	P0.8	P4.1	P1.8	VDDP	VSS	n.c.	n.c.	C
D	VDDP	P3.1	P3.2	P0.10	P0.4	P3.5	P0.7	P4.0	P1.6	P1.7	P1.9	VDDC	P9.3	P9.2	D
E	P3.0	P3.13	P0.1	P0.0	P0.13	P0.15	P4.4	P4.6	P4.7	P1.4	P1.2	P1.3	n.c.	P9.1	E
F	USB_DM	P3.12	P3.11	P0.9	P0.12	P3.14	P3.15	P4.5	P1.0	P1.5	P1.11	P1.10	P9.0	P7.11	F
G	USB_DP	VBUS	P3.8	P3.7	P0.11	P0.14	P3.4	P4.2	P1.1	P1.14	P1.12	P1.13	P7.9	P7.10	G
H	RTC_XTAL1	RTC_XTAL2	HIB_IO_1	HIB_IO_0	P3.9	P3.10	P3.3	P4.3	P6.1	P6.4	P6.5	P6.6	n.c.	P7.8	H
J	VBAT	P15.3	P15.5	P15.4	P15.6	P15.7	TMS	TCK	P6.3	P6.0	PORST	P1.15	n.c.	P7.7	J
K	P15.2	P14.15	P14.14	P14.13	P5.10	P5.8	P5.2	P5.1	P5.0	P6.2	XTAL1	XTAL2	n.c.	P7.6	K
L	P14.12	P14.7	P14.6	P14.3	P5.11	P2.15	P5.7	P5.5	P2.6	P5.3	P2.0	VSSO	P7.0	P7.5	L
M	P14.4	P14.5	P14.2	P15.15	P15.12	P5.9	P2.14	P5.6	P2.7	P5.4	P2.2	P2.1	P7.1	P7.3	M
N	VDDA	P14.1	P14.0	P15.14	P14.9	P15.9	P2.12	P2.10	P2.8	P2.4	P2.3	VDDP	P7.2	P7.4	N
P	VSSA	VAGND	VAREF	P15.13	P14.8	P15.8	P2.13	P2.11	P2.9	P2.5	VDDC	VSS	n.c.	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

XMC4[78]00 -(top view)

Figure 6 XMC4[78]00 PG-LFBGA-196 Pin Configuration (top view)

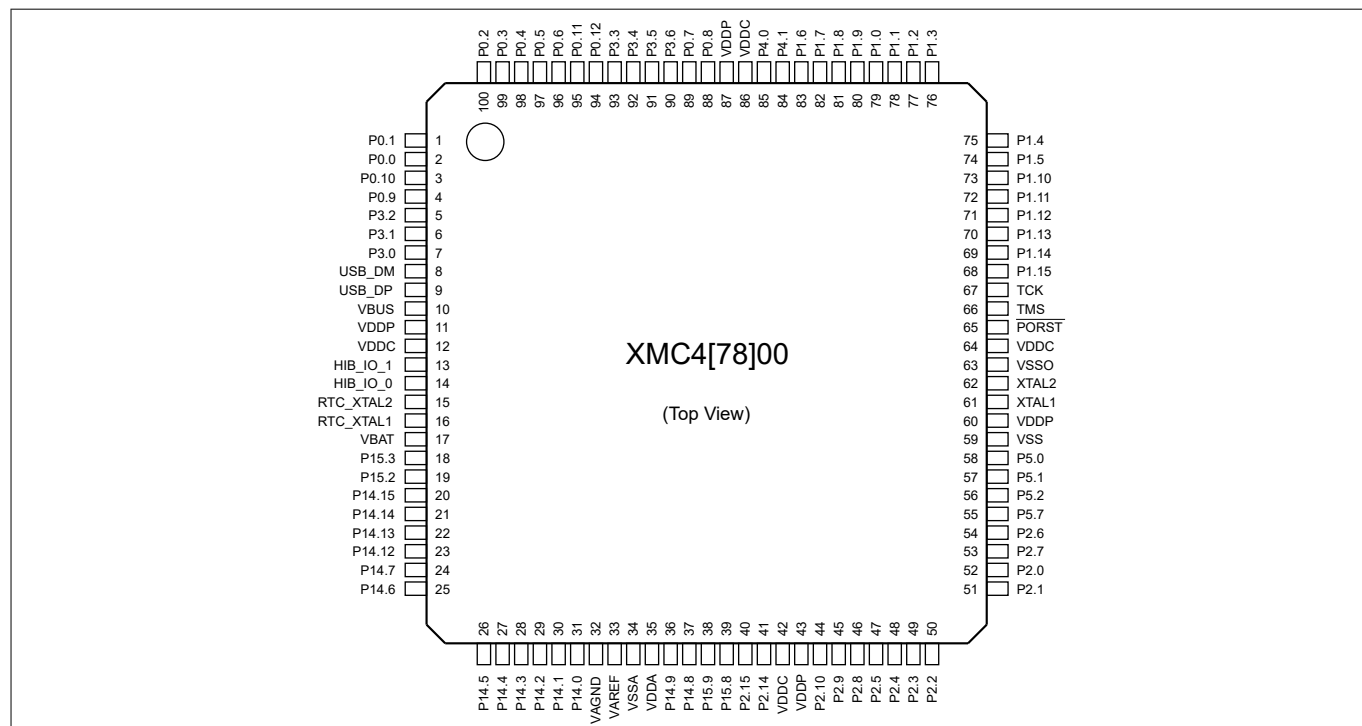


Figure 7 XMC4[78]00 PG-LQFP-100 Pin Configuration (top view)

2 General Device Information

2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

Table 9 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A2	–

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. $\overline{\text{PORST}}$) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, A2, special=special pad, In=input pad, AN/DIG_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, that is deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

Table 10 Package Pin Mapping

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P0.0	E4	2	2	A1+	–
P0.1	E3	1	1	A1+	–
P0.2	C3	144	100	A2	–
P0.3	C4	143	99	A2	–
P0.4	D5	142	98	A2	–
P0.5	C5	141	97	A2	–
P0.6	C6	140	96	A2	–
P0.7	D7	128	89	A2	After a system reset, via HWSEL this pin selects the DB.TDI function.
P0.8	C8	127	88	A2	After a system reset, via HWSEL this pin selects the $\overline{\text{DB.TRST}}$ function, with a weak pull-down active.
P0.9	F4	4	4	A2	–
P0.10	D4	3	3	A1+	–
P0.11	G5	139	95	A1+	–
P0.12	F5	138	94	A1+	–

(table continues...)

2 General Device Information

Table 10 (continued) Package Pin Mapping

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P0.13	E5	137	–	A1+	–
P0.14	G6	136	–	A1+	–
P0.15	E6	135	–	A1+	–
P1.0	F9	112	79	A1+	–
P1.1	G9	111	78	A1+	–
P1.2	E11	110	77	A2	–
P1.3	E12	109	76	A2	–
P1.4	E10	108	75	A1+	–
P1.5	F10	107	74	A1+	–
P1.6	D9	116	83	A2	–
P1.7	D10	115	82	A2	–
P1.8	C10	114	81	A2	–
P1.9	D11	113	80	A2	–
P1.10	F12	106	73	A1+	–
P1.11	F11	105	72	A1+	–
P1.12	G11	104	71	A2	–
P1.13	G12	103	70	A2	–
P1.14	G10	102	69	A2	–
P1.15	J12	94	68	A2	–
P2.0	L11	74	52	A2	–
P2.1	M12	73	51	A2	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	M11	72	50	A2	–
P2.3	N11	71	49	A2	–
P2.4	N10	70	48	A2	–
P2.5	P10	69	47	A2	–
P2.6	L9	76	54	A1+	–
P2.7	M9	75	53	A1+	–
P2.8	N9	68	46	A2	–
P2.9	P9	67	45	A2	–
P2.10	N8	66	44	A2	–
P2.11	P8	65	–	A2	–

(table continues...)

2 General Device Information

Table 10 (continued) Package Pin Mapping

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P2.12	N7	64	–	A2	–
P2.13	P7	63	–	A2	–
P2.14	M7	60	41	A2	–
P2.15	L6	59	40	A2	–
P3.0	E1	7	7	A2	–
P3.1	D2	6	6	A2	–
P3.2	D3	5	5	A2	–
P3.3	H7	132	93	A1+	–
P3.4	G7	131	92	A1+	–
P3.5	D6	130	91	A2	–
P3.6	C7	129	90	A2	–
P3.7	G4	14	–	A1+	–
P3.8	G3	13	–	A1+	–
P3.9	H5	12	–	A1+	–
P3.10	H6	11	–	A1+	–
P3.11	F3	10	–	A1+	–
P3.12	F2	9	–	A2	–
P3.13	E2	8	–	A2	–
P3.14	F6	134	–	A1+	–
P3.15	F7	133	–	A1+	–
P4.0	D8	124	85	A2	–
P4.1	C9	123	84	A2	–
P4.2	G8	122	–	A1+	–
P4.3	H8	121	–	A1+	–
P4.4	E7	120	–	A1+	–
P4.5	F8	119	–	A1+	–
P4.6	E8	118	–	A1+	–
P4.7	E9	117	–	A1+	–
P5.0	K9	84	58	A1+	–
P5.1	K8	83	57	A1+	–
P5.2	K7	82	56	A1+	–
P5.3	L10	81	–	A2	–
P5.4	M10	80	–	A2	–

(table continues...)

2 General Device Information

Table 10 (continued) Package Pin Mapping

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P5.5	L8	79	–	A2	–
P5.6	M8	78	–	A2	–
P5.7	L7	77	55	A1+	–
P5.8	K6	58	–	A2	–
P5.9	M6	57	–	A2	–
P5.10	K5	56	–	A1+	–
P5.11	L5	55	–	A1+	–
P6.0	J10	101	–	A2	–
P6.1	H9	100	–	A2	–
P6.2	K10	99	–	A2	–
P6.3	J9	98	–	A1+	–
P6.4	H10	97	–	A2	–
P6.5	H11	96	–	A2	–
P6.6	H12	95	–	A2	–
P7.0	L13	–	–	A2	–
P7.1	M13	–	–	A2	–
P7.2	N13	–	–	A2	–
P7.3	M14	–	–	A2	–
P7.4	N14	–	–	A1+	–
P7.5	L14	–	–	A1+	–
P7.6	K14	–	–	A1+	–
P7.7	J14	–	–	A1+	–
P7.8	H14	–	–	A2	–
P7.9	G13	–	–	A1+	–
P7.10	G14	–	–	A1+	–
P7.11	F14	–	–	A1+	–
P8.0	B7	–	–	A2	–
P8.1	A7	–	–	A2	–
P8.2	B3	–	–	A2	–
P8.3	B2	–	–	A2	–
P8.4	B6	–	–	A1+	–
P8.5	B5	–	–	A1+	–
P8.6	A2	–	–	A1+	–

(table continues...)

2 General Device Information

Table 10 (continued) Package Pin Mapping

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P8.7	B4	–	–	A1+	–
P8.8	A3	–	–	A2	–
P8.9	A5	–	–	A1+	–
P8.10	A4	–	–	A1+	–
P8.11	A6	–	–	A1+	–
P9.0	F13	–	–	A2	–
P9.1	E14	–	–	A2	–
P9.2	D14	–	–	A1+	–
P9.3	D13	–	–	A2	–
P9.4	A12	–	–	A1+	–
P9.5	A11	–	–	A1+	–
P9.6	B11	–	–	A1+	–
P9.7	A9	–	–	A1+	–
P9.8	A8	–	–	A1+	–
P9.9	A10	–	–	A1+	–
P9.10	B8	–	–	A1+	–
P9.11	B9	–	–	A1+	–
P14.0	N3	42	31	AN/DIG_IN	–
P14.1	N2	41	30	AN/DIG_IN	–
P14.2	M3	40	29	AN/DIG_IN	–
P14.3	L4	39	28	AN/DIG_IN	–
P14.4	M1	38	27	AN/DIG_IN	–
P14.5	M2	37	26	AN/DIG_IN	–
P14.6	L3	36	25	AN/DIG_IN	–
P14.7	L2	35	24	AN/DIG_IN	–
P14.8	P5	52	37	AN/DAC/DIG_IN	–
P14.9	N5	51	36	AN/DAC/DIG_IN	–
P14.12	L1	34	23	AN/DIG_IN	–
P14.13	K4	33	22	AN/DIG_IN	–
P14.14	K3	32	21	AN/DIG_IN	–
P14.15	K2	31	20	AN/DIG_IN	–
P15.2	K1	30	19	AN/DIG_IN	–
P15.3	J2	29	18	AN/DIG_IN	–

(table continues...)

2 General Device Information

Table 10 (continued) Package Pin Mapping

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P15.4	J4	28	–	AN/DIG_IN	–
P15.5	J3	27	–	AN/DIG_IN	–
P15.6	J5	26	–	AN/DIG_IN	–
P15.7	J6	25	–	AN/DIG_IN	–
P15.8	P6	54	39	AN/DIG_IN	–
P15.9	N6	53	38	AN/DIG_IN	–
P15.12	M5	50	–	AN/DIG_IN	–
P15.13	P4	49	–	AN/DIG_IN	–
P15.14	N4	44	–	AN/DIG_IN	–
P15.15	M4	43	–	AN/DIG_IN	–
USB_DP	G1	16	9	special	–
USB_DM	F1	15	8	special	–
HIB_IO_0	H4	21	14	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0". As output the medium driver mode is active.
HIB_IO_1	H3	20	13	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as input with no pull device active. As output the medium driver mode is active.
TCK	J8	93	67	A1	Weak pull-down active.

(table continues...)

2 General Device Information

Table 10 (continued) Package Pin Mapping

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
TMS	J7	92	66	A1+	Weak pull-up active. As output the strong-soft driver mode is active.
$\overline{\text{PORST}}$	J11	91	65	special	Weak pull-up permanently active, strong pull-down controlled by EVR.
XTAL1	K11	87	61	clock_IN	–
XTAL2	K12	88	62	clock_O	–
RTC_XTAL1	H1	23	16	clock_IN	–
RTC_XTAL2	H2	22	15	clock_O	–
VBAT	J1	24	17	Power	When VDDP is supplied VBAT has to be supplied as well.
VBUS	G2	17	10	special	–
VAREF	P3	46	33	AN_Ref	–
VAGND	P2	45	32	AN_Ref	–
VDDA	N1	48	35	AN_Power	–
VSSA	P1	47	34	AN_Power	–
VDDC	–	19	12	Power	–
VDDC	–	61	42	Power	–
VDDC	–	90	64	Power	–
VDDC	–	125	86	Power	–
VDDC	C2	–	–	Power	–
VDDC	D12	–	–	Power	–
VDDC	P11	–	–	Power	–
VDDP	–	18	11	Power	–
VDDP	–	62	43	Power	–
VDDP	–	86	60	Power	–
VDDP	–	126	87	Power	–
VDDP	C11	–	–	Power	–

(table continues...)

2 General Device Information

Table 10 (continued) Package Pin Mapping

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
VDDP	D1	–	–	Power	–
VDDP	N12	–	–	Power	–
VSS	–	85	59	Power	–
VSS	A1	–	–	Power	–
VSS	A14	–	–	Power	–
VSS	B13	–	–	Power	–
VSS	C1	–	–	Power	–
VSS	C12	–	–	Power	–
VSS	P12	–	–	Power	–
VSS	P14	–	–	Power	–
VSSO	L12	89	63	Power	–
VSS	–	Exp. Pad	Exp. Pad	Power	Exposed Die Pad The exposed die pad is connected internally to VSS. For proper operation, it is mandatory to connect the exposed pad directly to the common ground on the board. For thermal aspects, please refer to the Datasheet. Board layout examples are given in an application note.
n.c.	A13	–	–	Power	–
n.c.	B1	–	–	Power	–
n.c.	B10	–	–	Power	–
n.c.	B12	–	–	Power	–
n.c.	B14	–	–	Power	–
n.c.	C13	–	–	Power	–
n.c.	C14	–	–	Power	–

(table continues...)

2 General Device Information

Table 10 (continued) Package Pin Mapping

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
n.c.	E13	–	–	Power	–
n.c.	H13	–	–	Power	–
n.c.	J13	–	–	Power	–
n.c.	K13	–	–	Power	–
n.c.	P13	–	–	Power	–

2 General Device Information

2.2.2 Port I/O Functions

The following general scheme is used to describe each Port pin:

Table 11 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

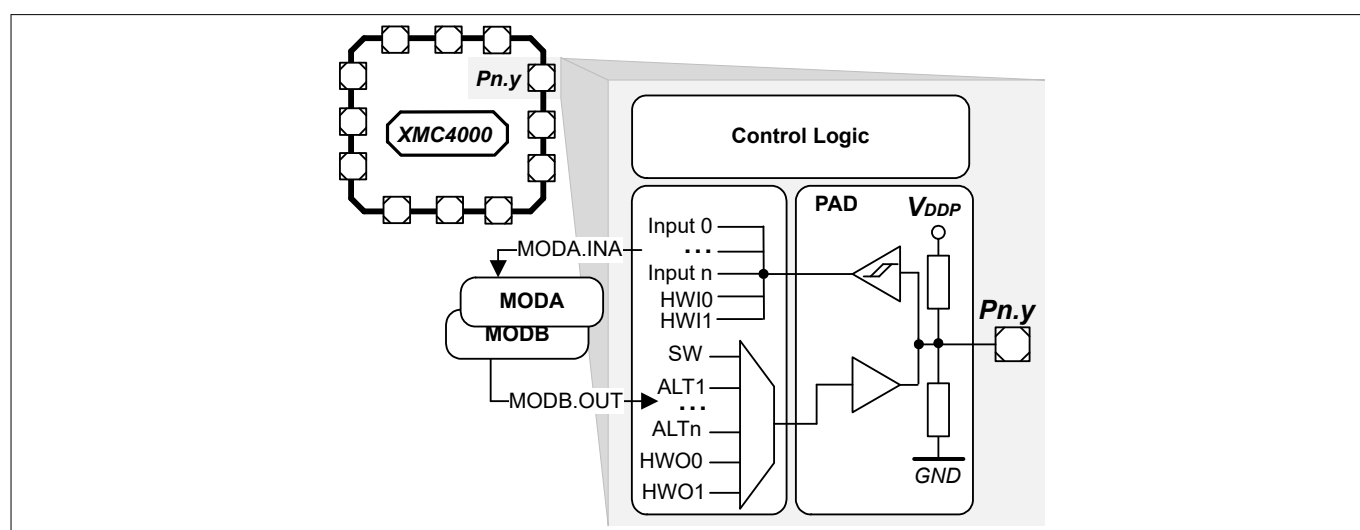


Figure 8 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn_IOC.R.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware “masters” (HWO0/HWI0). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

2 General Device Information

2.2.2.1 Port I/O Function Table

Table 12 Port I/O Functions

Function	Outputs					Inputs						
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input
P0.0	ECAT0. PHY_R ST	CAN. N0_TX D	CCU80 OUT21	LEDTS 0. COL2					U1C1. DX0D	ETH0. CLK_R MIIB	ERU0. 0B0	ETH0. CLKRX B
P0.1	USB. DRIVE VBUS	U1C1. DOUT 0	CCU80 OUT11	LEDTS 0. COL3						ETH0. CRS_D VB	ERU0. 0A0	ETH0. RXDVB
P0.2	ECAT0. P1_TX D2	U1C1. SELO1	CCU80 OUT01		U1C0. DOUT 3	EBU. AD0	U1C0. HWIN3	EBU. D0	ETH0. RXD0B		ERU0. 3B3	ECAT0. P1_RX _CLKA
P0.3	ECAT0. P1_TX D3		CCU80 OUT20		U1C0. DOUT 2	EBU. AD1	U1C0. HWIN2	EBU. D1	ETH0. RXD1B		ERU1. 3B0	
P0.4	ETH0. TX_EN		CCU80 OUT10		U1C0. DOUT 1	EBU. AD2	U1C0. HWIN1	EBU. D2		U1C0. DX0A	ERU0. 2B3	ECAT0. P1_RX D3A
P0.5	ETH0. TXD0	U1C0. DOUT 0	CCU80 OUT00		U1C0. DOUT 0	EBU. AD3	U1C0. HWIN0	EBU. D3		U1C0. DX0B	ERU1. 3A0	ECAT0. P1_RX D2A
P0.6	ETH0. TXD1	U1C0. SELO0	CCU80 OUT30			EBU. ADV				U1C0. DX2A	ERU0. 3B2	ECAT0. P1_RX D1A

(table continues...)

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs						
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWIO	HWI1	Input	Input	Input	Input	Input
P0.7	WWDVT. SERVI CE_O UT	U0C0. SELO0	ECAT0. LED_E RR			EBU. AD6	DB. TDI	EBU. D6	U0C0. DX2B	DSD. DIN1A	ERU0. 2B1	CCU80 IN0A	CCU80 IN1A IN3A
P0.8	SCU. EXTCL K	U0C0. SCLKO UT	ECAT0. LED_R UN			EBU. AD7	$\overline{\text{DB.}}$ $\overline{\text{TRST}}$	EBU. D7	U0C0. DX1B	DSD. DIN0A	ERU0. 2A1	CCU80 IN1B	
P0.9		U1C1. SELO0	CCU80 OUT12	LEDTS O. COL0	ETH0. MDO	$\overline{\text{EBU.}}$ $\overline{\text{CS1}}$	ETH0. MDIA		U1C1. DX2A	USB. ID	ERU0. 1B0		ECAT0. P1_RX _DVA
P0.10	ETH0. MDC	U1C1. SCLKO UT	CCU80 OUT02	LEDTS O. COL1					U1C1. DX1A		ERU0. 1A0		ECAT0. P1_TX _CLKA
P0.11	ECAT0. P1_LI NK_AC T	U1C0. SCLKO UT	CCU80 OUT31		$\overline{\text{SDMMC.}}$ $\overline{\text{BREQ}}$ $\overline{\text{RST}}$	$\overline{\text{EBU.}}$			ETH0. RXERB	U1C0. DX1A	ERU0. 3A2		ECAT0. P1_RX D0A
P0.12		U1C1. SELO0	CCU40 OUT3		ECAT0. MDO	$\overline{\text{EBU.}}$ $\overline{\text{HLDA}}$	ECAT0. MDIA	$\overline{\text{EBU.}}$ $\overline{\text{HLDA}}$		U1C1. DX2B	ERU0. 2B2		
P0.13		U1C1. SCLKO UT	CCU40 OUT2							U1C1. DX1B	ERU0. 2A2		
P0.14		U1C0. SELO1	CCU40 OUT1		U1C1. DOUT 3		U1C1. HWIN3					CCU42 IN3C	

(table continues...)

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs					
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWIO	HWI1	Input	Input	Input	Input
P0.15		U1C0. SELO2	CCU40 OUT0		U1C1. DOUT 2		U1C1. HWIN2			CCU42 IN2C		
P1.0	DSD. CGPW MN	U0C0. SELO0	CCU40 OUT3	ERU1. PDOU T3				U0C0. DX2A	ERU0. 3B0	CCU40 IN3A		ECAT0. P0_TX _CLKA
P1.1	DSD. CGPW MP	U0C0. SCLKO UT	CCU40 OUT2	ERU1. PDOU T2			SDMM C. SDWC	U0C0. DX1A	POSIF 0. IN2A	CCU40 IN2A		ECAT0. P0_RX _CLKA
P1.2	ECAT0. P0_TX D3		CCU40 OUT1	ERU1. PDOU T1	U0C0. DOUT 3	EBU. AD14	U0C0. HWIN3	EBU. D14	POSIF 0. IN1A	ERU1. 2B0 IN1A		
P1.3	ECAT0. P0_TX _ENA	U0C0. MCLK OUT	CCU40 OUT0	ERU1. PDOU T0	U0C0. DOUT 2	EBU. AD15	U0C0. HWIN2	EBU. D15	POSIF 0. IN0A	ERU1. 2A0 IN0A		
P1.4	WWDT. SERVI CE_O UT	CAN. N0_TX D	CCU80 OUT33	CCU81 OUT20	U0C0. DOUT 1		U0C0. HWIN1		CAN. N1_RX DD	CCU41 IN0C		ECAT0. P0_RX D0A
P1.5	CAN. N1_TX D	U0C0. DOUT 0	CCU80 OUT23	CCU81 OUT10	U0C0. DOUT 0		U0C0. HWIN0		CAN. N0_RX DA	CCU41 IN1C	DSD. DIN2B	ECAT0. P0_RX D1A
P1.6	ECAT0. P0_TX D0	U0C0. SCLKO UT			SDMM C. DATA1 _OUT	EBU. AD10	SDMM C. DATA1 _IN	EBU. D10	DSD. DIN2A			

(table continues...)

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs						
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWIO	HWI1	Input	Input	Input	Input	Input
P1.7	ECAT0. P0_TX D1	U0C0. DOUT 0	DSD. MCLK2	U1C1. SELO2	SDMM C. DATA2 _OUT	EBU. AD11	SDMM C. DATA2 _IN	EBU. D11	DSD. MCLK2 A			DSD. MCLK0 C	
P1.8	ECAT0. P0_TX D2	U0C0. SELO1	DSD. MCLK1	U1C1. SCLK0 UT	SDMM C. DATA4 _OUT	EBU. AD12	SDMM C. DATA4 _IN	EBU. D12	CAN. N2_RX DA	DSD. MCLK1 A	DSD. MCLK2 D	DSD. MCLK0 D	DSD. MCLK3 D
P1.9	U0C0. SCLK0 UT	CAN. N2_TX D	DSD. MCLK0	U1C1. DOUT 0	SDMM C. DATA5 _OUT	EBU. AD13	SDMM C. DATA5 _IN	EBU. D13	DSD. MCLK0 A		DSD. MCLK1 C	DSD. MCLK2 C	DSD. MCLK3 C
P1.10	ETH0. MDC	U0C0. SCLK0 UT	CCU81 OUT21	ECAT0. LED_E RR		EBU. AD13	SDMM C. DATA5 _IN	EBU. D13				CCU41 IN2C	ECAT0. P0_RX D2A
P1.11	ECAT0. LED_S TATE_ RUN	U0C0. SELO0	CCU81 OUT11	ECAT0. LED_R UN	ETH0. MDO		ETH0. MDIC					CCU41 IN3C	ECAT0. P0_RX D3A
P1.12	ETH0. TX_EN	CAN. N1_TX D	CCU81 OUT01	ECAT0. P0_LI NK_AC T	SDMM C. DATA6 _OUT	EBU. AD16	SDMM C. DATA6 _IN	EBU. D16					

(table continues...)

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs					
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWIO	HWI1	Input	Input	Input	Input
P1.13	ETH0. TXD0	U0C1. SELO3	CCU81 OUT20	ECAT0. PHY_C LK25	SDMM C. DATA7 _OUT	EBU. AD17	SDMM C. DATA7 _IN	EBU. D17	CAN. N1_RX DC			
P1.14	ETH0. TXD1	U0C1. SELO2	CCU81 OUT10	ECAT0. SYNC0		EBU. AD18		EBU. D18	U1C0. DX0E			
P1.15	SCU. EXTCLK	DSD. MCLK2	CCU81 OUT00	U1C0. DOUT0		EBU. AD19		EBU. D19	DSD. MCLK2 B	ERU1. 1A0		ECAT0. P0_LI NKB
P2.0	CAN. N0_TXD	CCU81 OUT21	DSD. CGPW MN	LEDTS O. COL1	ETH0. MDO	EBU. AD20	ETH0. MDIB	EBU. D20		ERU0. 0B3	CCU40 IN1C	
P2.1	CAN. N5_TXD	CCU81 OUT11	DSD. CGPW MP	LEDTS O. COL0	DB.TD O/ TRACE SWO	EBU. AD21		EBU. D21	ETH0. CLK_R M1A	ERU1. 0B0	CCU40 IN0C	ETH0. CLKRX A
P2.2	VADC. EMUX00	CCU81 OUT01	CCU41 OUT3	LEDTS O. LINE0	LEDTS O. EXTEN DED0	EBU. AD22	LEDTS O. TSIN0 A	EBU. D22	ETH0. RXD0A	ERU0. 1B2	CCU41 IN3A	
P2.3	VADC. EMUX01	U0C1. SELO0	CCU41 OUT2	LEDTS O. LINE1	LEDTS O. EXTEN DED1	EBU. AD23	LEDTS O. TSIN1 A	EBU. D23	ETH0. RXD1A	ERU0. 1A2	CCU41 IN2A	

(table continues...)

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs					Inputs								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWIO	HWI1	Input	Input	Input	Input	Input	Input
P2.4	VADC. EMUX 02	U0C1. SCLKO UT	CCU41 OUT1	LEDTS 0. LINE2	LEDTS 0. EXTEN DED2	EBU. AD24	LEDTS 0. TSIN2 A	EBU. D24	ETH0. RXERA	U0C1. DX1A	ERU0. 0B2	POSIF 1. IN1A	CCU41 IN1A	
P2.5	ETH0. TX_EN	U0C1. DOUT 0	CCU41 OUT0	LEDTS 0. LINE3	LEDTS 0. EXTEN DED3	EBU. AD25	LEDTS 0. TSIN3 A	EBU. D25	ETH0. RXDVA	U0C1. DX0B	ERU0. 0A2	POSIF 1. IN0A	CCU41 IN0A	ETH0. CRS_D VA
P2.6	U2C0. SELO4	ERU1. PDOU T3	CCU80 OUT13	LEDTS 0. COL3	U2C0. DOUT 3		U2C0. HWIN3		DSD. DIN1B	CAN. N1_RX DA	ERU0. 1B3	CAN. N5_RX DB	CCU40 IN3C	ECAT0. P0_RX _ERRB
P2.7	ETH0. MDC	CAN. N1_TX D	CCU80 OUT03	LEDTS 0. COL2					DSD. DIN0B			ERU1. 1B0	CCU40 IN2C	
P2.8	ETH0. TXD0	ERU1. PDOU T1	CCU80 OUT32	LEDTS 0. LINE4	LEDTS 0. EXTEN DED4	EBU. AD26	LEDTS 0. TSIN4 A	EBU. D26	DAC. TRIGG ER5				CCU40 IN0B	CCU40 IN1B
													CCU40 IN2B	CCU40 IN3B
P2.9	ETH0. TXD1	ERU1. PDOU T2	CCU80 OUT22	LEDTS 0. LINE5	LEDTS 0. EXTEN DED5	EBU. AD27	LEDTS 0. TSIN5 A	EBU. D27	DAC. TRIGG ER4				CCU41 IN0B	CCU41 IN1B
													CCU41 IN2B	CCU41 IN3B
P2.10	VADC. EMUX 10	ERU1. PDOU T0	ECAT0. PHY_R ST	ECAT0. SYNC1	DB. ETM_T RACED ATA3	EBU. AD28		EBU. D28						

(table continues...)

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs					
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input
P2.11	ETH0. TXER	ECAT0. P1_TX D0	CCU80 OUT22		DB. ETM_T RACED ATA2	EBU. AD29		EBU. D29				
P2.12	ETH0. TXD2	ECAT0. P1_TX D1	CCU81 OUT33	ETH0. TXD0	DB. ETM_T RACED ATA1	EBU. AD30		EBU. D30	CCU43 IN3C			
P2.13	ETH0. TXD3	ECAT0. P1_TX D2		ETH0. TXD1	DB. ETM_T RACED ATA0	EBU. AD31		EBU. D31	CCU43 IN2C			
P2.14	VADC. EMUX 11	U1C0. DOUT 0	CCU80 OUT21	CAN. N4_TX D	DB. ETM_T RACEC LK	EBU. BC0.			U1C0. DX0D	CCU43 IN0B	CCU43 IN1B	CCU43 IN2B IN3B
P2.15	VADC. EMUX 12	ECAT0. P1_TX D3	CCU80 OUT11	LEDTS 0. LINE6	LEDTS 0. EXTEN DED6	EBU. BC1.	LEDTS 0. TSING A		ETH0. COLA	U1C0. DX0C	CCU42 IN0B	CCU42 IN1B IN2B IN3B
P3.0	U2C1. SELO0	U0C1. SCLKO UT	CCU42 OUT0	ECAT0. P1_TX _ENA		EBU. RD			U0C1. DX1B	CCU80 IN2C	CCU81 IN0C	
P3.1		U0C1. SELO0	ECAT0. P1_TX D0			EBU. RD_WR			U0C1. DX2B	CCU80 IN1C	ERU0. OB1	
(table continues...)												

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs					
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input
P3.2	USB. DRIVE VBUS	CAN. N0_TX D	ECAT0. P1_TX D1	LEDTS 0. COLA		$\overline{\text{EBU.}}$ $\overline{\text{CS0}}$			ERU0. 0A1	CCU80 . IN0C		
P3.3		U1C1. SELO1	CCU42 . OUT3	ECAT0. MCLK 0.	SDMM C. LED			$\overline{\text{EBU.}}$ $\overline{\text{WAIT}}$	DSD. DIN3B	CCU42 . IN3A	CCU80 . IN3B	
P3.4	U2C1. MCLK OUT	U1C1. SELO2	CCU42 . OUT2	DSD. MCLK3 0.	SDMM C. BUS_P OWER			$\overline{\text{EBU.}}$ $\overline{\text{HOLD}}$	U2C1. DX0B	CCU42 . IN2A	CCU80 . IN0B	ECAT0. P1_LI NKA
P3.5	U2C1. DOUT 0	U1C1. SELO3	CCU42 . OUT1	U0C1. DOUT 0	SDMM C. CMD_ OUT	EBU. AD4	SDMM C. CMD_I N	EBU. D4	ERU0. 3B1	CCU42 . IN1A		ECAT0. P1_RX _ERRA
P3.6	U2C1. SCLK0 UT	U1C1. SELO4	CCU42 . OUT0	U0C1. SCLK0 UT	SDMM C. CLK_O UT	EBU. AD5	SDMM C. CLK_I N	EBU. D5	ERU0. 3A1	CCU42 . IN0A		
P3.7	ECAT0. SYNC0	CAN. N2_TX D	CCU41 . OUT3	LEDTS 0. LINE0								
P3.8	U2C0. DOUT 0	U0C1. SELO3	CCU41 . OUT2	LEDTS 0. LINE1						POSIF 1. IN2B		

(table continues...)

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs						
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input
P3.9	U2C0. SCLKO UT	CAN. N1_TX D	CCU41 OUT1	LEDTS 0. LINE2							POSIF 1. IN1B		
P3.10	U2C0. SELO0	CAN. N0_TX D	CCU41 OUT0	LEDTS 0. LINE3	U0C1. DOUT 3		U0C1. HWIN3				POSIF 1. IN0B		
P3.11	U2C1. DOUT 0	U0C1. SELO2	CCU42 OUT3	LEDTS 0. LINE4	U0C1. DOUT 2		U0C1. HWIN2		CAN. N1_RX DB			CCU81 IN3C	
P3.12	ECAT0. P1_LI NK_AC T	U0C1. SELO1	CCU42 OUT2	LEDTS 0. LINE5	U0C1. DOUT 1		U0C1. HWIN1		CAN. N0_RX DC	U2C1. DX0D		CCU81 IN2C	
P3.13	U2C1. SCLKO UT	U0C1. DOUT 0	CCU42 OUT1	LEDTS 0. LINE6	U0C1. DOUT 0		U0C1. HWIN0		U0C1. DX0D			CCU81 IN1C	
P3.14		U1C0. SELO3			U1C1. DOUT 1		U1C1. HWIN1			U1C1. DX0B			
P3.15		U1C1. DOUT 0			U1C1. DOUT 0		U1C1. HWIN0			U1C1. DX0A			
P4.0	CAN. N3_TX D	ECAT0. PHY_C LK25	DSD. MCLK1	U1C0. SCLKO UT	SDMM C. DATA0 _OUT	EBU. AD8	SDMM C. DATA0 _IN	EBU. D8	U1C1. DX1C	DSD. MCLK1 B	U0C1. DX0E	U2C1. DX0C	ECAT0. P0_RX _ERRA

(table continues...)

2 General Device Information

Table 12
(continued) Port I/O Functions

Function	Outputs					Inputs										
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	
P4.1	U2C1. SELO0	U1C1. MCLK OUT	DSD. MCLK0	U0C1. SELO0	SDMM C. DATA3 _OUT	EBU. AD9	SDMM C. DATA3 _IN	EBU. D9	U2C1. DX2B	DSD. MCLK0 B		U2C1. DX2A	DSD. MCLK1 D		ECAT0. P0_LI NKA	
P4.2	U2C1. SELO1	U1C1. DOU T0		U2C1. SCLK0 UT	ECAT0. MDO		ECAT0. MDIB		U1C1. DX0C			U2C1. DX1A	CCU43 . IN1C			
P4.3	U2C1. SELO2	U0C0. SELO5	CCU43 . OUT3	ECAT0. MCLK									CCU43 . IN3A			
P4.4		U0C0. SELO4	CCU43 . OUT2		U2C1. DOUT 3		U2C1. HWIN3						CCU43 . IN2A			
P4.5		U0C0. SELO3	CCU43 . OUT1		U2C1. DOUT 2		U2C1. HWIN2						CCU43 . IN1A			
P4.6		U0C0. SELO2	CCU43 . OUT0		U2C1. DOUT 1		U2C1. HWIN1	CAN. N2_RX DC				U2C1. DX0E	CCU43 . IN0A			
P4.7	U2C1. DOUT 0	CAN. N2_TX D			U2C1. DOUT 0		U2C1. HWIN0		U0C0. DX0C				CCU43 . IN0C			
P5.0	U2C0. DOUT 0	DSD. CGPW MN	CCU81 . OUT33	ERU1. PDOU T0	U2C0. DOUT 0		U2C0. HWIN0		U2C0. DX0B	ETH0. RXD0D	U0C0. DX0D	ECAT0. P0_RX D0B	CCU81 . IN0A	CCU81 . IN1A	CCU81 . IN2A	CCU81 . IN3A

(table continues...)

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs					
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input
P5.1	U0C0. DOUT 0	DSD. CGPW MP	CCU81 OUT32	ERU1. PDOU T1	U2C0. DOUT 1		U2C0. HWIN1		U2C0. DX0A	ETH0. RXD1D	ECAT0. P0_RX D1B	CCU81 IN0B
P5.2	U2C0. SCLKO UT	ECAT0. P0_LI NK_AC T	CCU81 OUT23	ERU1. PDOU T2					U2C0. DX1A	ETH0. CRS_D VD	ECAT0. P0_RX D2B	CCU81 IN1B
P5.3	U2C0. SELO0		CCU81 OUT22	ERU1. PDOU T3	EBU. CKE	EBU. A20			U2C0. DX2A	ETH0. RXERD		CCU81 IN2B
P5.4	U2C0. SELO1		CCU81 OUT13		$\overline{\text{EBU.}} \text{RAS}$	EBU. A21				ETH0. CRSD		CCU81 IN3B
P5.5	U2C0. SELO2		CCU81 OUT12		$\overline{\text{EBU.}} \text{CAS}$	EBU. A22				ETH0. COLD		
P5.6	U2C0. SELO3		CCU81 OUT03		EBU. BFCLK O	EBU. A23			EBU. BFCLK I			
P5.7	ECAT0. SYNC0		CCU81 OUT02	LEDTS 0. COLA	U2C0. DOUT 2		U2C0. HWIN2				ECAT0. P0_RX D3B	
P5.8	ECAT0. P1_TX _ENA	U1C0. SCLKO UT	CCU80 OUT01	CAN. N4_TX D	EBU. SDCLK O	$\overline{\text{EBU.}} \text{CS2.}$			ETH0. RXD2A	U1C0. DX1B		
(table continues...)												

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs				
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input
P5.9		U1C0. SELO0	CCU80 OUT20	ETH0. TX_EN	EBU. BFCLK O	EBU. CS3.			ETH0. RXD3A	U1C0. DX2B	ECAT0. P1_TX _CLKB
P5.10		U1C0. MCLK OUT	CCU80 OUT10	LEDTS 0. LINE7	LEDTS 0. EXTEN DED7		LEDTS 0. TSIN7 A		ETH0. CLK_T XA	CAN. N5_RX DA	
P5.11		U1C0. SELO1	CCU80 OUT00	CAN. N5_TX D					ETH0. CRSA		
P6.0	ETH0. TXD2	U0C1. SELO1	CCU81 OUT31	ECAT0. PHY_C LK25	DB. ETM_T RACEC LK	EBU. A16					
P6.1	ETH0. TXD3	U0C1. SELO0	CCU81 OUT30	ECAT0. P0_TX _ENA	DB. ETM_T RACED ATA3	EBU. A17			U0C1. DX2C		
P6.2	ETH0. TXER	U0C1. SCLKO UT	CCU43 OUT3	ECAT0. P0_TX D0	DB. ETM_T RACED ATA2	EBU. A18			U0C1. DX1C		
P6.3			CCU43 OUT2	ECAT0. P0_LI NK_AC T					U0C1. DX0C	ETH0. RXD3B	

(table continues...)

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs					
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input
P6.4		U0C1. DOUT 0	CCU43 OUT1	ECAT0. P0_TX D1	EBU. SDCLK O	EBU. A19			EBU. SDCLK I	ETH0. RXD2B		
P6.5	CAN. N3_TX D	U0C1. MCLK OUT	CCU43 OUT0	ECAT0. P0_TX D2	DB. ETM_T RACED ATA1	EBU. BC2			DSD. DIN3A	ETH0. CLK_R MIID	U2C0. DX0D	ETH0. CLKRX D
P6.6	U2C0. DOUT 0		DSD. MCLK3	ECAT0. P0_TX D3	DB. ETM_T RACED ATA0	EBU. BC3			DSD. MCLK3 A	ETH0. CLK_T XB	CAN. N3_RX DB	
P7.0		CAN. N3_TX D		ECAT0. P0_TX D0	EBU. A19							
P7.1				ECAT0. P0_TX D1	EBU. A20					CAN. N3_RX DC		
P7.2		CAN. N4_TX D		ECAT0. P0_TX D2	EBU. A21							
P7.3				ECAT0. P0_TX D3	EBU. A22					CAN. N4_RX DC		
P7.4			CCU42 OUT0						ECAT0. P0_RX D0C			

(table continues...)

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs					
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input
P7.5			CCU42 OUT1						ECAT0. P0_RX D1C			
P7.6			CCU42 OUT2						ECAT0. P0_RX D2C			
P7.7			CCU42 OUT3						ECAT0. P0_RX D3C			
P7.8		CAN. N5_TX D		ECAT0. P0_TX _ENA	DB. ETM_T RACEC LK							
P7.9			CCU80 OUT22						ECAT0. P0_RX _ERRC			
P7.10			CCU80 OUT32						ECAT0. P0_RX _CLKC			
P7.11			CCU80 OUT33						ECAT0. P0_RX _DVC			
P8.0				ECAT0. P1_TX D0	DB. ETM_T RACED ATA0				CAN. N5_RX DC			

(table continues...)

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs					
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input
P8.1				ECAT0. P1_TX D1	DB. ETM_T RACED ATA1				U0C0. DX2C			
P8.2				ECAT0. P1_TX D2	DB. ETM_T RACED ATA2							
P8.3				ECAT0. P1_TX D3	DB. ETM_T RACED ATA3				U0C0. DX1C			
P8.4		U0C0. SELO1							ECAT0. P1_RX D0C			
P8.5		U0C0. SCLKO UT							ECAT0. P1_RX D1C			
P8.6		U0C0. SELO0							ECAT0. P1_RX D2C			
P8.7		U0C0. DOUT 0							ECAT0. P1_RX D3C			
(table continues...)												

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs					Inputs					Input	Input	Input	Input	Input	Input
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input						
P8.8				ECAT0. P1_TX _ENA							U0C0. DX0E					
P8.9			CCU81 . OUT33						ECAT0. P1_RX _ERRC							
P8.10			CCU81 . OUT21						ECAT0. P1_RX _CLKC							
P8.11			CCU81 . OUT11						ECAT0. P1_RX _DVC							
P9.0		U2C0. SELO0		ECAT0. SYNC0					ECAT0. LATCH 0B	U2C0. DX2C	ECAT0. P1_TX _CLKC					
P9.1		U2C0. SCLKO UT		ECAT0. SYNC1					ECAT0. LATCH 1B	U2C0. DX1C	ECAT0. P0_TX _CLKC					
P9.2		U2C0. SELO1		ECAT0. PHY_R ST					ETH0. COLC							
P9.3		U2C0. DOUT 0		ECAT0. PHY_C LK25					ETH0. CRSC							
(table continues...)																

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs					
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input
P9.4	ECAT0. LED_S TATE_ RUN			ECAT0. LED_R UN					U2C0. DX0E			
P9.5		U2C0. SELO2		ECAT0. LED_E RR					ETH0. RXD2C			
P9.6		U2C0. SELO3		ECAT0. MCLK					ETH0. RXD3C			
P9.7		U2C0. SELO4			ECAT0. MDO		ECAT0. MDIC		ETH0. RXERC			
P9.8				ECAT0. P0_LI NK_AC T					U2C1. DX2C			
P9.9				ECAT0. P1_LI NK_AC T					U2C1. DX1C			
P9.10		U2C1. DOUT 0							ECAT0. P0_LI NKC			
P9.11		U2C1. SELO3							ECAT0. P1_LI NKC			
(table continues...)												

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs					Inputs						
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input
P14.0									VADC. G0CH0			
P14.1									VADC. G0CH1			
P14.2									VADC. G0CH2	VADC. G1CH2		
P14.3									VADC. G0CH3	VADC. G1CH3	CAN. N0_RX DB	
P14.4									VADC. G0CH4	VADC. G2CH0	CAN. N4_RX DB	ECAT0. LATCH 1A
P14.5									VADC. G0CH5	VADC. G2CH1	POSIF 0. IN2B	ECAT0. LATCH 0A
P14.6									VADC. G0CH6		POSIF 0. IN1B	ECAT0. P1_RX _CLKB
P14.7									VADC. G0CH7		POSIF 0. IN0B	ECAT0. P1_RX D0B
P14.8					DAC. OUT_0					VADC. G1CH0	VADC. G3CH2	ETH0. RXD0C
(table continues...)												

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs					
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input
P14.9					DAC. OUT_1				VADC. G1CH1	VADC. G3CH3	ETH0. RXD1C	
P14.12									VADC. G1CH4			ECAT0. P1_RX D1B
P14.13									VADC. G1CH5			ECAT0. P1_RX D2B
P14.14									VADC. G1CH6		G1OR C6	ECAT0. P1_RX D3B
P14.15									VADC. G1CH7		G1OR C7	ECAT0. P1_RX _DVB
P15.2										VADC. G2CH2		ECAT0. P1_RX _ERRB
P15.3										VADC. G2CH3		ECAT0. P1_LI NKB
P15.4										VADC. G2CH4		
P15.5										VADC. G2CH5		
(table continues...)												

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs						
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWIO	HWI1	Input	Input	Input	Input	Input
P15.6										VADC. G2CH6			
P15.7										VADC. G2CH7			
P15.8										VADC. G3CH0	ETH0. CLK_R MIIC		ETH0. CLKRX C
P15.9										VADC. G3CH1	ETH0. CRS_D VC		ETH0. RXDVC
P15.12										VADC. G3CH4			
P15.13										VADC. G3CH5			
P15.14										VADC. G3CH6			
P15.15										VADC. G3CH7			
HIB_IO _0	HIBOU T	WWDT. SERVI CE_O UT							WAKE UPA				

(table continues...)

2 General Device Information

Table 12 (continued) Port I/O Functions

Function	Outputs						Inputs					
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWIO	HWI1	Input	Input	Input	Input
HIB_IO_1	HIBOUT	WWDT. SERVI CE_O UT							WAKE UPB			
USB_DP												
USB_DM												
TCK							DB.TC K/ SWCL K					
TMS					DB.TM S/ SWDIO							
$\overline{\text{PORST}}$												
XTAL1									U0C0. DX0F	U0C1. DX0F	U1C0. DX0F	U1C1. DX0F
XTAL2												
RTC_XTAL1										ERU0. 1B1		
RTC_XTAL2												

2 General Device Information

2.3 Power Connection Scheme

Figure 9 shows a reference power connection scheme for the XMC4[78]00.

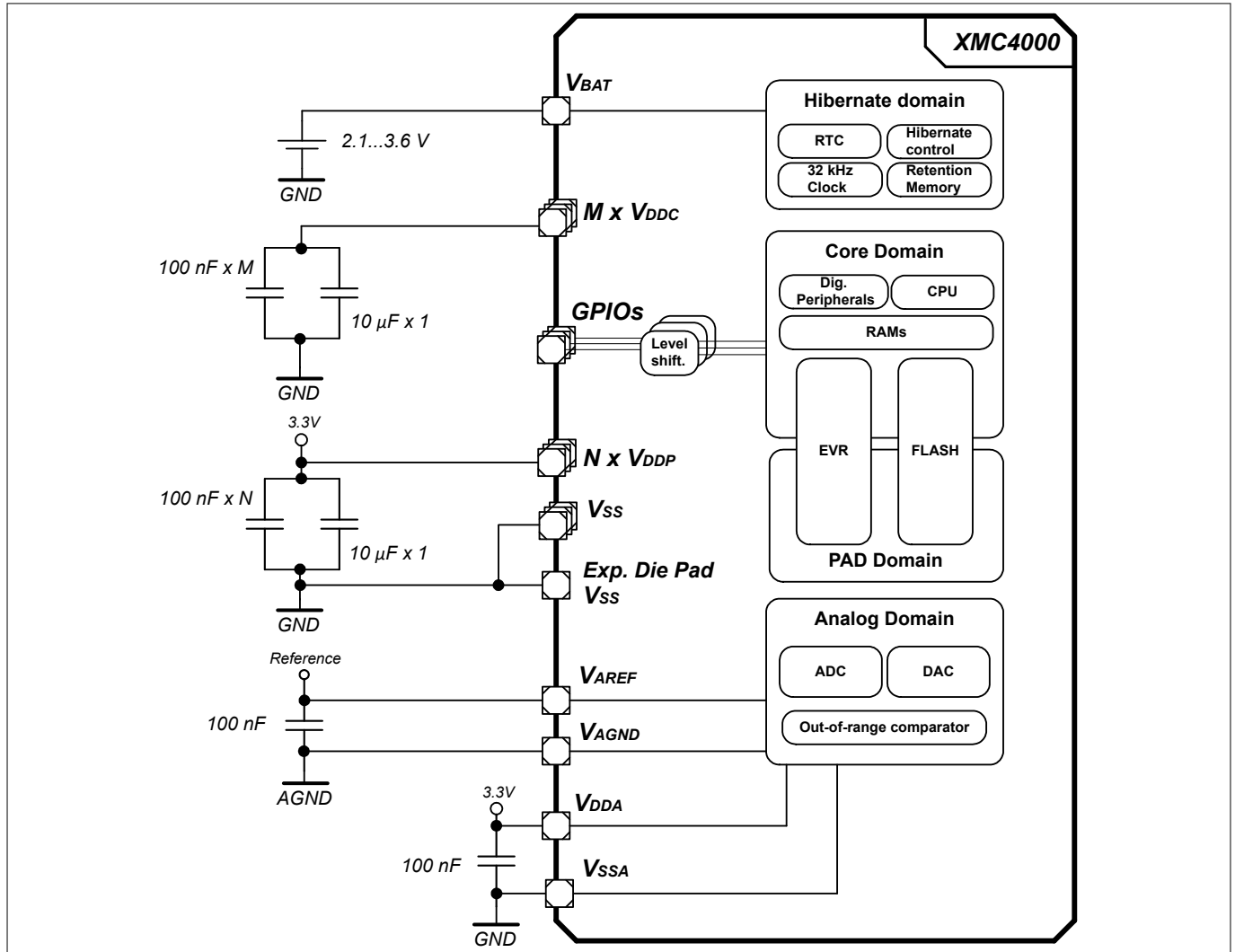


Figure 9 Power Connection Scheme

Every power supply pin needs to be connected. Different pins of the same supply need also to be externally connected. As example, all V_{DDP} pins must be connected externally to one V_{DDP} net. In this reference scheme one 100 nF capacitor is connected at each supply pin against V_{SS} . An additional 10 μ F capacitor is connected to the V_{DDP} nets and an additional 10 μ F capacitor to the V_{DDC} nets.

The XMC4[78]00 has a common ground concept, all V_{SS} , V_{SSA} and V_{SSO} pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.

V_{AGND} is the low potential to the analog reference V_{AREF} . Depending on the application it can share the common ground or have a different potential. In devices with shared V_{DDA}/V_{AREF} and V_{SSA}/V_{AGND} pins the reference is tied to the supply. Some analog channels can optionally serve as "Alternate Reference"; further details on this operating mode are described in the Reference Manual.

When V_{DDP} is supplied, V_{BAT} must be supplied as well. If no other supply source (e.g. battery) is connected to V_{BAT} , the V_{BAT} pin can also be connected directly to V_{DDP} .

3 Electrical Parameters

3 Electrical Parameters

Attention: *All parameters in this chapter are preliminary target values and may change based on characterization results.*

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the XMC4[78]00 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with a two-letter abbreviation in column “Symbol”:

- **CC**
Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4[78]00 and must be regarded for system design
- **SR**
Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4[78]00 is designed in

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 13 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Storage temperature	T_{ST} SR	-65	–	150	°C	–
Junction temperature	T_J SR	-40	–	150	°C	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP} SR	–	–	4.3	V	–
Voltage on any Class A and dedicated input pin with respect to V_{SS}	V_{IN} SR	-1.0	–	$V_{DDP} + 1.0$ or max. 4.3	V	whichever is lower
Voltage on any analog input pin with respect to V_{AGND}	V_{AIN} V_{AREF} SR	-1.0	–	$V_{DDP} + 1.0$ or max. 4.3	V	whichever is lower
Input current on any pin during overload condition	I_{IN} SR	-10	–	+10	mA	–
Absolute maximum sum of all input circuit currents for one port group during overload condition ¹⁾	ΣI_{IN} SR	-25	–	+25	mA	–

(table continues...)

3 Electrical Parameters

Table 13 (continued) **Absolute Maximum Rating Parameters**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{IN} SR	-100	–	+100	mA	–

1) The port groups are defined in [Pin Reliability in Overload](#).

Figure 10 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP} . The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP} . For the range up to $V_{DDP} + 1.0$ V also see the definition of the overload conditions in [Section 3.1.3](#).

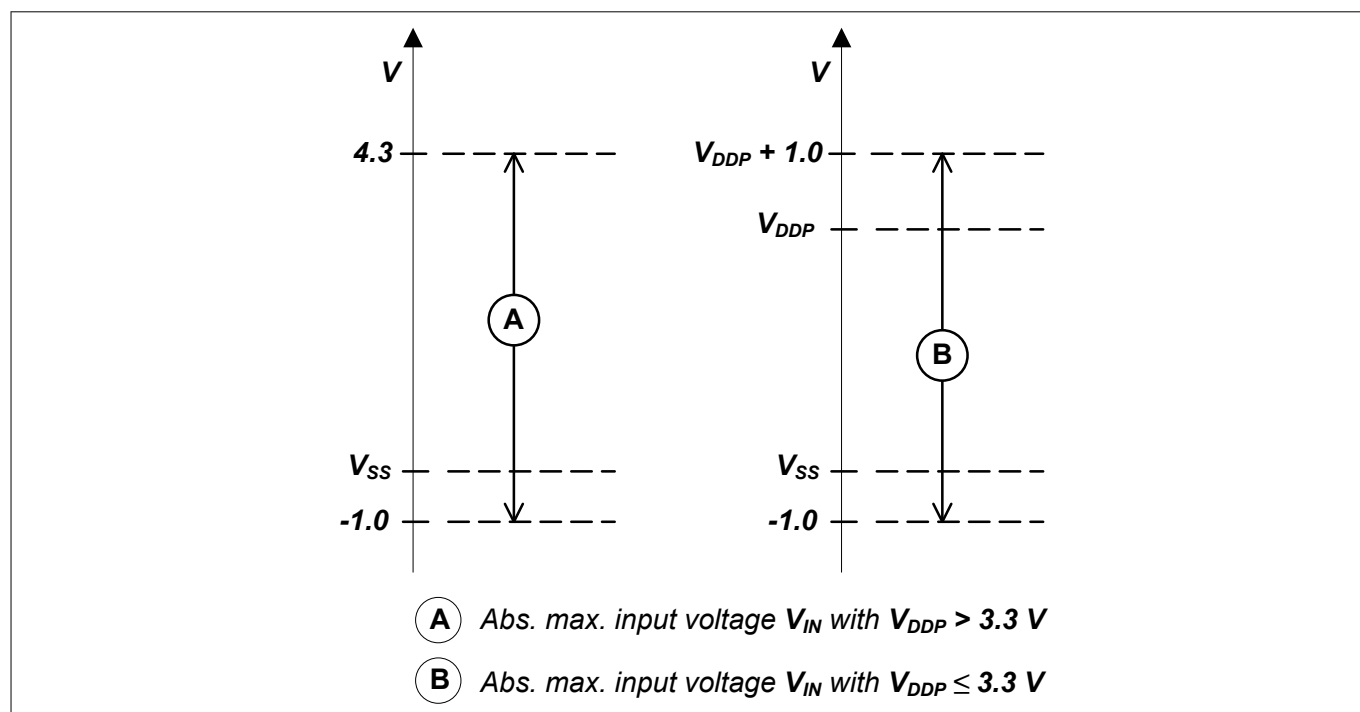


Figure 10 **Absolute Maximum Input Voltage Ranges**

3 Electrical Parameters

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 14 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
 - pad supply levels (V_{DDP} or V_{DDA})
 - temperature

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 14 Overload Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	–
Absolute sum of all input circuit currents for one port group during overload condition ¹⁾	I_{OVG} SR	–	–	20	mA	$\sum I_{OVx} $, for all $I_{OVx} < 0$ mA
		–	–	20	mA	$\sum I_{OVx} $, for all $I_{OVx} > 0$ mA
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	80	mA	$\sum I_{OVG}$

1) The port groups are defined in Table 17.

Figure 11 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

3 Electrical Parameters

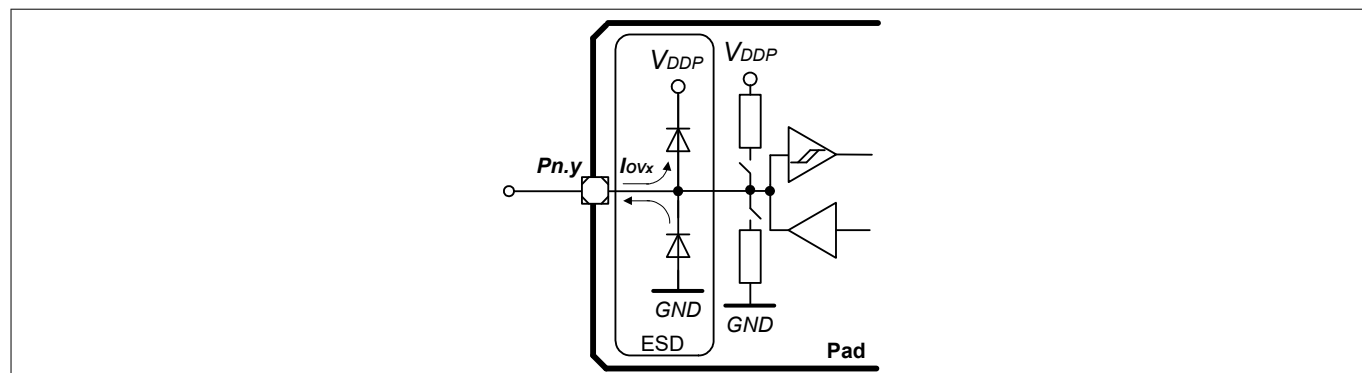


Figure 11 Input Overload Current via ESD structures

Table 15 and Table 16 list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the [Absolute Maximum Ratings](#) must not be exceeded during overload.

Table 15 PN-Junction Characteristics for positive Overload

Pad Type	$I_{OV} = 5 \text{ mA}, T_J = -40^\circ\text{C}$	$I_{OV} = 5 \text{ mA}, T_J = 150^\circ\text{C}$
A1/A1+	$V_{IN} = V_{DDP} + 1.0 \text{ V}$	$V_{IN} = V_{DDP} + 0.75 \text{ V}$
A2	$V_{IN} = V_{DDP} + 0.7 \text{ V}$	$V_{IN} = V_{DDP} + 0.6 \text{ V}$
AN/DIG_IN	$V_{IN} = V_{DDP} + 1.0 \text{ V}$	$V_{IN} = V_{DDP} + 0.75 \text{ V}$

Table 16 PN-Junction Characteristics for negative Overload

Pad Type	$I_{OV} = 5 \text{ mA}, T_J = -40^\circ\text{C}$	$I_{OV} = 5 \text{ mA}, T_J = 150^\circ\text{C}$
A1/A1+	$V_{IN} = V_{SS} - 1.0 \text{ V}$	$V_{IN} = V_{SS} - 0.75 \text{ V}$
A2	$V_{IN} = V_{SS} - 0.7 \text{ V}$	$V_{IN} = V_{SS} - 0.6 \text{ V}$
AN/DIG_IN	$V_{IN} = V_{DDP} - 1.0 \text{ V}$	$V_{IN} = V_{DDP} - 0.75 \text{ V}$

Table 17 Port Groups for Overload and Short-Circuit Current Sum Parameters

Group	Pins
1	P0.[15:0], P3.[15:0], P8.[11:0]
2	P14.[15:0], P15.[15:0]
3	P2.[15:0], P5.[11:0], P7.[11:0]
4	P1.[15:0], P4.[7:0], P6.[6:0], P9.[11:0]

3 Electrical Parameters

3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and their basic characteristics.

Table 18 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub-Class	Speed Grade	Load	Termination
A	3.3 V	LVTTTL I/O	A1 (e.g. GPIO)	6 MHz	100 pF	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	Series termination recommended
			A2 (e.g. ext. Bus)	80 MHz	15 pF	Series termination recommended

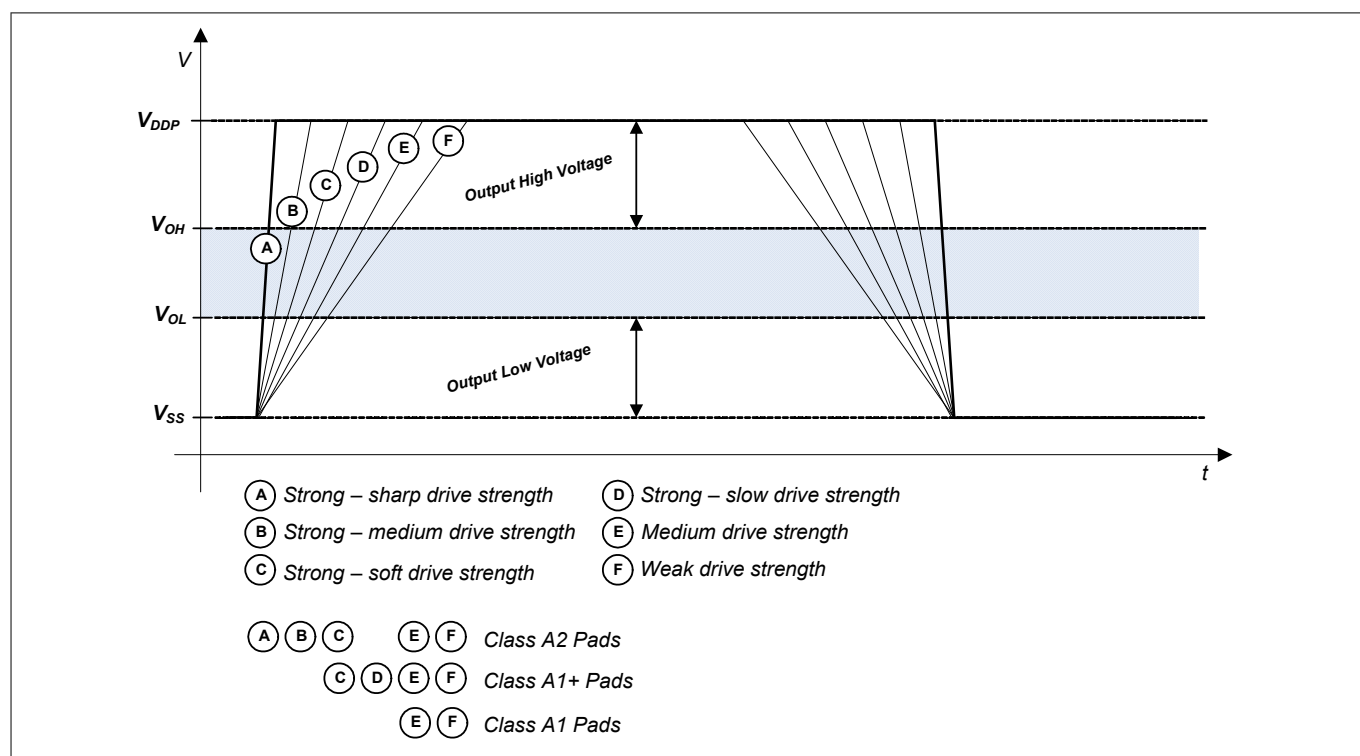


Figure 12 Output Slopes with different Pad Driver Modes

Figure 12 is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in [Section 3.2.1](#).

3 Electrical Parameters

3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4[78]00. All parameters specified in the following sections refer to these operating conditions, unless noted otherwise.

Table 19 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	125	°C	Temp. Range K
Digital supply voltage	V_{DDP} SR	3.13 ¹⁾	3.3	3.63 ²⁾	V	
Core Supply Voltage	V_{DDC} CC	– ¹⁾	1.3	–	V	Generated internally
Digital ground voltage	V_{SS} SR	0	–	–	V	
ADC analog supply voltage	V_{DDA} SR	3.0	3.3	3.6 ²⁾	V	
Analog ground voltage for V_{DDA}	V_{SSA} SR	-0.1	0	0.1	V	
Battery Supply Voltage for Hibernate Domain	V_{BAT} SR	1.95 ³⁾	–	3.63	V	When V_{DDP} is supplied V_{BAT} has to be supplied as well.
System Frequency	f_{SYS} SR	–	–	144	MHz	
Short circuit current of digital outputs	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents per pin group ⁴⁾	ΣI_{SC_PG} SR	–	–	20	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} SR	–	–	100	mA	

1) See also the Supply Monitoring thresholds, [Section 3.3.2](#).

2) Voltage overshoot to 4.0 V is permissible at Power-Up and $\overline{PORST}$ low, provided the pulse duration is less than 100 μ s and the cumulated sum of the pulses does not exceed 1 h over lifetime.

3) To start the hibernate domain it is required that $V_{BAT} \geq 2.1$ V, for a reliable start of the oscillation of RTC_XTAL in crystal mode it is required that $V_{BAT} \geq 3.0$ V.

4) The port groups are defined in [Table 17](#).

3 Electrical Parameters

3.2 DC Parameters

3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.

The Pull-up on the $\overline{\text{PORST}}$ pin is identical to the Pull-up on the standard digital input/output pins.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Standard Pad Parameters

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Pin capacitance (digital inputs/ outputs)	C_{IO} CC	–	10	pF	–
Pull-down current	$ I_{PDL} $ SR	150	–	μA	¹⁾ $V_{IN} \geq 0.6 \times V_{DDP}$
		–	10	μA	²⁾ $V_{IN} \leq 0.36 \times V_{DDP}$
Pull-up current	$ I_{PUH} $ SR	–	10	μA	²⁾ $V_{IN} \geq 0.6 \times V_{DDP}$
		100	–	μA	¹⁾ $V_{IN} \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes ³⁾	H_YSA CC	$0.1 \times V_{DDP}$	–	V	–
$\overline{\text{PORST}}$ spike filter always blocked pulse duration	t_{SF1} CC	–	10	ns	–
$\overline{\text{PORST}}$ spike filter pass-through pulse duration	t_{SF2} CC	100	–	ns	–
$\overline{\text{PORST}}$ pull-down current	$ I_{PPD} $ CC	13	–	mA	$V_{IN} = 1.0 \text{ V}$

- 1) Current required to override the pull device with the opposite logic level (“force current”). With active pull device, at load currents between force and keep current the input state is undefined.
- 2) Load current at which the pull device still maintains the valid logic level (“keep current”). With active pull device, at load currents between force and keep current the input state is undefined.
- 3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3 Electrical Parameters

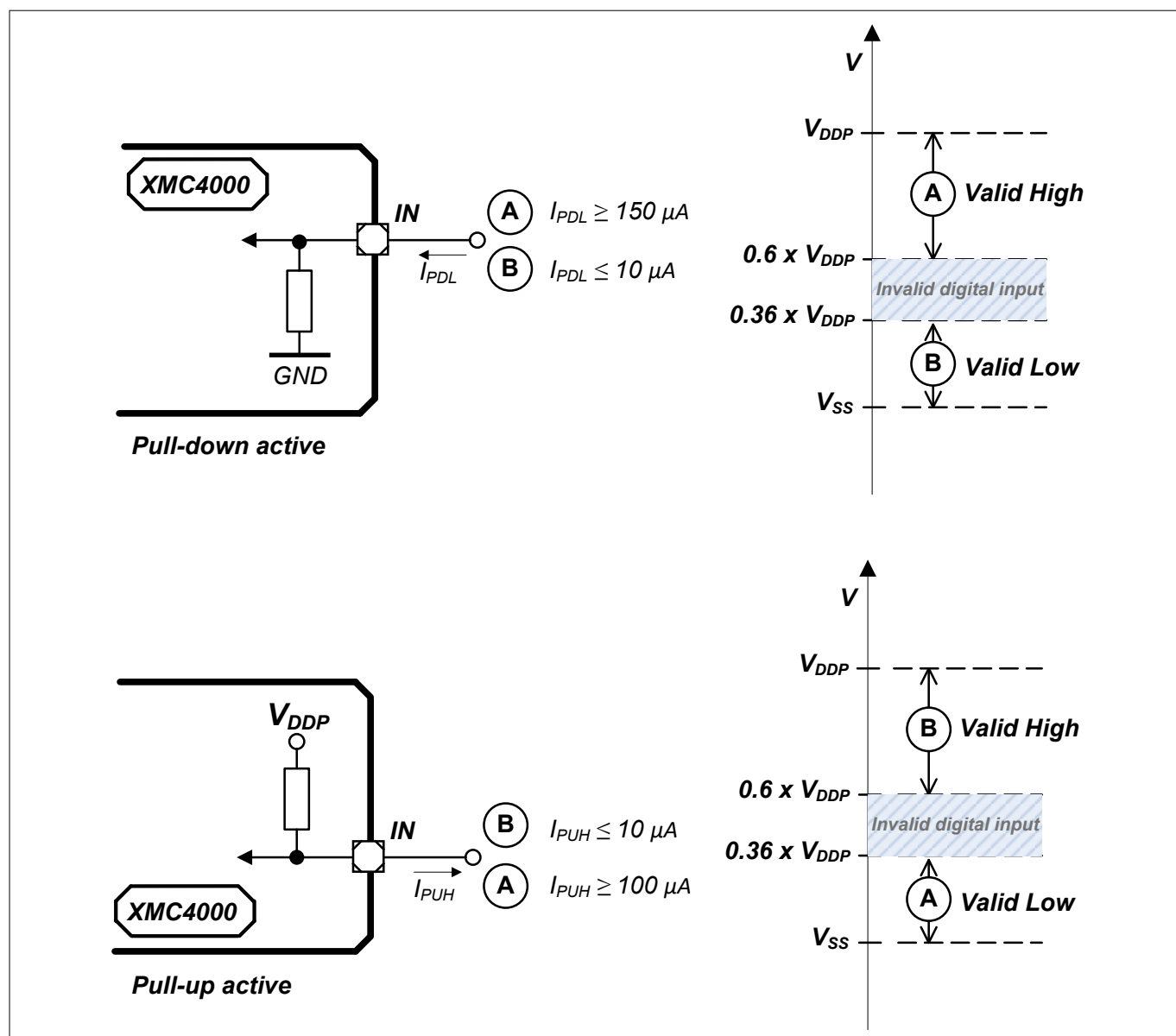


Figure 13 Pull Device Input Characteristics

Figure 13 visualizes the input characteristics with an active internal pull device:

- in the cases “A” the internal pull device is overridden by a strong external driver;
- in the cases “B” the internal pull device defines the input logical state against a weak external load

Table 21 Standard Pads Class_A1

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Input leakage current	I_{OZA1} CC	-500	500	nA	$0\text{ V} \leq V_{IN} \leq V_{DDP}$
Input high voltage	V_{IHA1} SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILA1} SR	-0.3	$0.36 \times V_{DDP}$	V	–
Output high voltage, POD ¹⁾ = weak	V_{OHA1} CC	$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -400\text{ }\mu\text{A}$
		2.4	–	V	$I_{OH} \geq -500\text{ }\mu\text{A}$

(table continues...)

3 Electrical Parameters

Table 21 (continued) **Standard Pads Class_A1**

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Output high voltage, POD ¹⁾ = medium		$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -1.4 \text{ mA}$
		2.4	–	V	$I_{OH} \geq -2 \text{ mA}$
Output low voltage	V_{OLA1} CC	–	0.4	V	$I_{OL} \leq 500 \mu\text{A}$; POD ¹⁾ = weak
		–	0.4	V	$I_{OL} \leq 2 \text{ mA}$; POD ¹⁾ = medium
Fall time	t_{FA1} CC	–	150	ns	$C_L = 20 \text{ pF}$; POD ¹⁾ = weak
		–	50	ns	$C_L = 50 \text{ pF}$; POD ¹⁾ = medium
Rise time	t_{RA1} CC	–	150	ns	$C_L = 20 \text{ pF}$; POD ¹⁾ = weak
		–	50	ns	$C_L = 50 \text{ pF}$; POD ¹⁾ = medium

1) POD = Pin Out Driver.

Table 22 **Standard Pads Class_A1+**

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Input leakage current	I_{OZA1+} CC	-1	1	μA	$0\text{ V} \leq V_{IN} \leq V_{DDP}$
Input high voltage	V_{IHA1+} SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILA1+} SR	-0.3	$0.36 \times V_{DDP}$	V	–
Output high voltage, POD ¹⁾ = weak	V_{OHA1+} CC	$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -400\text{ }\mu\text{A}$
		2.4	–	V	$I_{OH} \geq -500\text{ }\mu\text{A}$
Output high voltage, POD ¹⁾ = medium		$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -1.4\text{ mA}$
		2.4	–	V	$I_{OH} \geq -2\text{ mA}$
Output high voltage, POD ¹⁾ = strong		$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -1.4\text{ mA}$
		2.4	–	V	$I_{OH} \geq -2\text{ mA}$
Output low voltage	V_{OLA1+} CC	–	0.4	V	$I_{OL} \leq 500\text{ }\mu\text{A}$; POD ¹⁾ = weak
		–	0.4	V	$I_{OL} \leq 2\text{ mA}$; POD ¹⁾ = medium
		–	0.4	V	$I_{OL} \leq 2\text{ mA}$; POD ¹⁾ = strong

(table continues...)

3 Electrical Parameters

Table 22 (continued) **Standard Pads Class_A1+**

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Fall time	$t_{FA1+ CC}$	–	150	ns	$C_L = 20 \text{ pF}$; POD ¹⁾ = weak
		–	50	ns	$C_L = 50 \text{ pF}$; POD ¹⁾ = medium
		–	28	ns	$C_L = 50 \text{ pF}$; POD ¹⁾ = strong; edge = slow
		–	16	ns	$C_L = 50 \text{ pF}$; POD ¹⁾ = strong; edge = soft
Rise time	$t_{RA1+ CC}$	–	150	ns	$C_L = 20 \text{ pF}$; POD ¹⁾ = weak
		–	50	ns	$C_L = 50 \text{ pF}$; POD ¹⁾ = medium
		–	28	ns	$C_L = 50 \text{ pF}$; POD ¹⁾ = strong; edge = slow
		–	16	ns	$C_L = 50 \text{ pF}$; POD ¹⁾ = strong; edge = soft

1) POD = Pin Out Driver.

3 Electrical Parameters

Table 23 **Standard Pads Class_A2**

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Input Leakage current	I_{OZA2} CC	-6	6	μA	$0\text{ V} \leq V_{\text{IN}} < 0.5 \cdot V_{\text{DDP}} - 1\text{ V}$; $0.5 \cdot V_{\text{DDP}} + 1\text{ V} < V_{\text{IN}} \leq V_{\text{DDP}}$
		-3	3	μA	$0.5 \cdot V_{\text{DDP}} - 1\text{ V} < V_{\text{IN}} < 0.5 \cdot V_{\text{DDP}} + 1\text{ V}$
Input high voltage	V_{IHA2} SR	$0.6 \times V_{\text{DDP}}$	$V_{\text{DDP}} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILA2} SR	-0.3	$0.36 \times V_{\text{DDP}}$	V	–
Output high voltage, POD = weak	V_{OHA2} CC	$V_{\text{DDP}} - 0.4$	–	V	$I_{\text{OH}} \geq -400\text{ }\mu\text{A}$
		2.4	–	V	$I_{\text{OH}} \geq -500\text{ }\mu\text{A}$
Output high voltage, POD = medium		$V_{\text{DDP}} - 0.4$	–	V	$I_{\text{OH}} \geq -1.4\text{ mA}$
		2.4	–	V	$I_{\text{OH}} \geq -2\text{ mA}$
Output high voltage, POD = strong		$V_{\text{DDP}} - 0.4$	–	V	$I_{\text{OH}} \geq -1.4\text{ mA}$
		2.4	–	V	$I_{\text{OH}} \geq -2\text{ mA}$
Output low voltage, POD = weak	V_{OLA2} CC	–	0.4	V	$I_{\text{OL}} \leq 500\text{ }\mu\text{A}$
Output low voltage, POD = medium		–	0.4	V	$I_{\text{OL}} \leq 2\text{ mA}$
Output low voltage, POD = strong		–	0.4	V	$I_{\text{OL}} \leq 2\text{ mA}$
Fall time	t_{FA2} CC	–	150	ns	$C_{\text{L}} = 20\text{ pF}$; POD = weak
		–	50	ns	$C_{\text{L}} = 50\text{ pF}$; POD = medium
		–	3.7	ns	$C_{\text{L}} = 50\text{ pF}$; POD = strong; edge = sharp
		–	7	ns	$C_{\text{L}} = 50\text{ pF}$; POD = strong; edge = medium
		–	16	ns	$C_{\text{L}} = 50\text{ pF}$; POD = strong; edge = soft
Rise time	t_{RA2} CC	–	150	ns	$C_{\text{L}} = 20\text{ pF}$; POD = weak
		–	50	ns	$C_{\text{L}} = 50\text{ pF}$; POD = medium

(table continues...)

3 Electrical Parameters

Table 23 (continued) **Standard Pads Class_A2**

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
		–	3.7	ns	$C_L = 50 \text{ pF}$; POD = strong; edge = sharp
		–	7.0	ns	$C_L = 50 \text{ pF}$; POD = strong; edge = medium
		–	16	ns	$C_L = 50 \text{ pF}$; POD = strong; edge = soft

Table 24 **HIB_IO Class_A1 special Pads**

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Input leakage current	$I_{OZHIB \text{ CC}}$	-500	500	nA	$0 \text{ V} \leq V_{IN} \leq V_{BAT}$
Input high voltage	$V_{IHIB \text{ SR}}$	$0.6 \times V_{BAT}$	$V_{BAT} + 0.3$	V	max. 3.6 V
Input low voltage	$V_{ILIB \text{ SR}}$	-0.3	$0.36 \times V_{BAT}$	V	–
Input Hysteresis for HIB_IO pins ¹⁾	$HYSHIB \text{ CC}$	$0.1 \times V_{BAT}$	–	V	$V_{BAT} \geq 3.13 \text{ V}$
		$0.06 \times V_{BAT}$	–	V	$V_{BAT} < 3.13 \text{ V}$
Output high voltage, POD ¹⁾ = medium	$V_{OHIB \text{ CC}}$	$V_{BAT} - 0.4$	–	V	$I_{OH} \geq -1.4 \text{ mA}$
Output low voltage	$V_{OLIB \text{ CC}}$	–	0.4	V	$I_{OL} \leq 2 \text{ mA}$
Fall time	$t_{FHIB \text{ CC}}$	–	50	ns	$V_{BAT} \geq 3.13 \text{ V}$ $C_L = 50 \text{ pF}$
		–	100	ns	$V_{BAT} < 3.13 \text{ V}$ $C_L = 50 \text{ pF}$
Rise time	$t_{RHIB \text{ CC}}$	–	50	ns	$V_{BAT} \geq 3.13 \text{ V}$ $C_L = 50 \text{ pF}$
		–	100	ns	$V_{BAT} < 3.13 \text{ V}$ $C_L = 50 \text{ pF}$

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3 Electrical Parameters

3.2.2 Analog to Digital Converters (VADC)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 VADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Analog reference voltage ¹⁾	V_{AREF} SR	$V_{AGND} + 1$	–	$V_{DDA} + 0.05^{2)}$	V	–
Analog reference ground ¹⁾	V_{AGND} SR	$V_{SSM} - 0.05$	–	$V_{AREF} - 1$	V	–
Analog reference voltage range ^{1) 3)}	$V_{AREF} - V_{AGND}$ SR	1	–	$V_{DDA} + 0.1$	V	–
Analog input voltage	V_{AIN} SR	V_{AGND}	–	V_{DDA}	V	–
Input leakage at analog inputs ⁴⁾	I_{OZ1} CC	–100	–	200	nA	$0.03 \times V_{DDA} < V_{AIN} < 0.97 \times V_{DDA}$
		–500	–	100	nA	$0 \text{ V} \leq V_{AIN} \leq 0.03 \times V_{DDA}$
		–100	–	500	nA	$0.97 \times V_{DDA} \leq V_{AIN} \leq V_{DDA}$
Input leakage current at V_{AREF}	I_{OZ2} CC	–1	–	1	μA	$0 \text{ V} \leq V_{AREF} \leq V_{DDA}$
Input leakage current at V_{AGND}	I_{OZ3} CC	–1	–	1	μA	$0 \text{ V} \leq V_{AGND} \leq V_{DDA}$
Internal ADC clock	f_{ADCI} CC	2	–	36	MHz	$V_{DDA} = 3.3 \text{ V}$
Switched capacitance at the analog voltage inputs ⁵⁾	C_{AINSW} CC	–	4	6.5	pF	–
Total capacitance of an analog input	C_{AINTOT} CC	–	12	20	pF	–
Switched capacitance at the positive reference voltage input ^{1) 6)}	C_{AREFSW} CC	–	15	30	pF	–
Total capacitance of the voltage reference inputs ¹⁾	$C_{AREFTOT}$ CC	–	20	40	pF	–
Total Unadjusted Error	TUE CC	–4	–	4	LSB	12-bit resolution; $V_{DDA} = 3.3 \text{ V}$; $V_{AREF} = V_{DDA}$ ⁷⁾
Differential Non-Linearity Error ⁸⁾	EA_{DNL} CC	–3	–	3	LSB	
Gain Error ⁸⁾	EA_{GAIN} CC	–4	–	4	LSB	
Integral Non-Linearity ⁸⁾	EA_{INL} CC	–3	–	3	LSB	
Offset Error ⁸⁾	EA_{OFF} CC	–4	–	4	LSB	

(table continues...)

3 Electrical Parameters

Table 25 (continued) VADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
RMS Noise ⁹⁾	EN_{RMS} CC	–	1	2 ^{10) 11)}	LSB	–
Worst case ADC V_{DDA} power supply current per active converter	I_{DDAA} CC	–	1.5	2	mA	during conversion $V_{DDP} = 3.6$ V, $T_J = 150^{\circ}\text{C}$
Charge consumption on V_{AREF} per conversion ¹⁾	Q_{CONV} CC	–	30	–	pC	$0\text{ V} \leq V_{AREF} \leq V_{DDA}$ ¹²⁾
ON resistance of the analog input path	R_{AIN} CC	–	600	1200	Ohm	–
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	–
Resistance of the reference voltage input path	R_{AREF} CC	–	700	1700	Ohm	–

- 1) Applies to AINx, when used as alternate reference input.
- 2) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).
- 3) If the analog reference voltage is below V_{DDA} , then the ADC converter errors increase. If the reference voltage is reduced by the factor k ($k < 1$), TUE, DNL, INL, Gain, and Offset errors increase also by the factor $1/k$.
- 4) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see Figure 16).
- 5) The sampling capacity of the conversion C-network is pre-charged to $V_{AREF}/2$ before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from $V_{AREF}/2$.
- 6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.
- 7) For 10-bit conversions, the errors are reduced to $1/4$; for 8-bit conversions, the errors are reduced to $1/16$. Never less than ± 1 LSB.
- 8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.
- 9) This parameter is valid for soldered devices and requires careful analog board design.
- 10) Resulting worst case combined error is arithmetic combination of TUE and EN_{RMS} .
- 11) Value is defined for one sigma Gauss distribution.
- 12) The resulting current for a conversion can be calculated with $I_{AREF} = Q_{CONV} / t_c$.
The fastest 12-bit post-calibrated conversion of $t_c = 459$ ns results in a typical average current of $I_{AREF} = 65.4$ μA .

3 Electrical Parameters

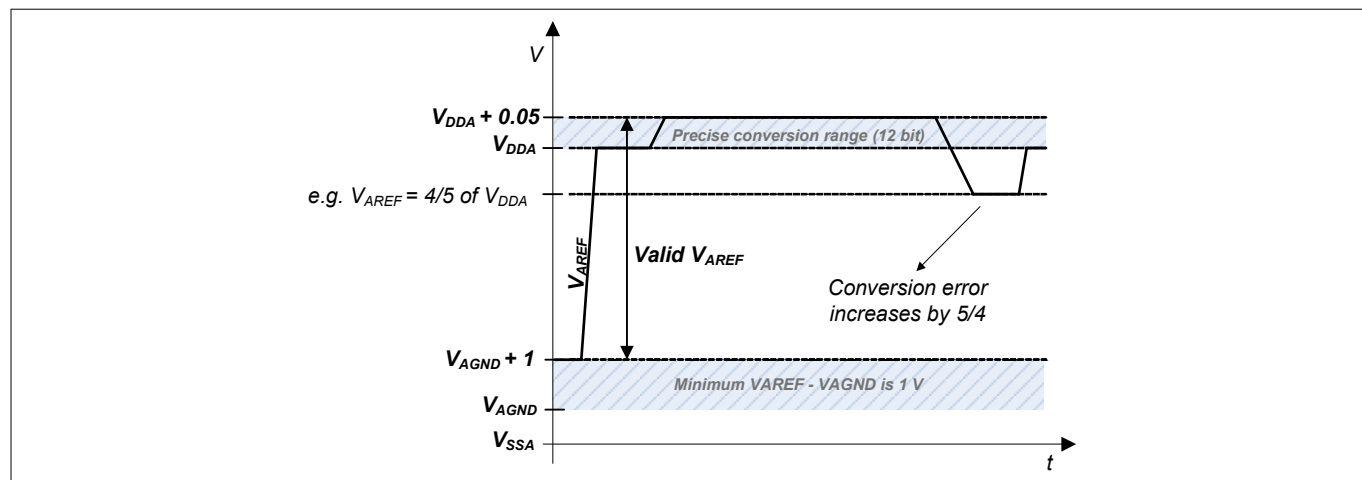


Figure 14 VADC Reference Voltage Range

The power-up calibration of the VADC requires a maximum number of $4352 f_{\text{ADCI}}$ cycles.

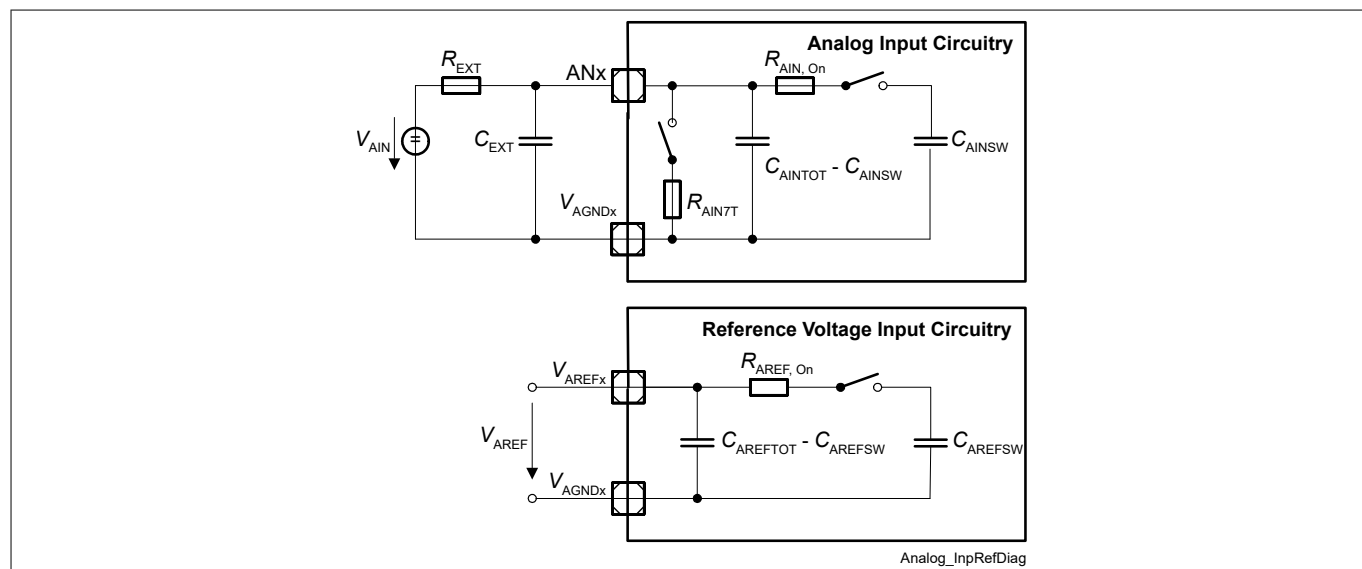


Figure 15 VADC Input Circuits

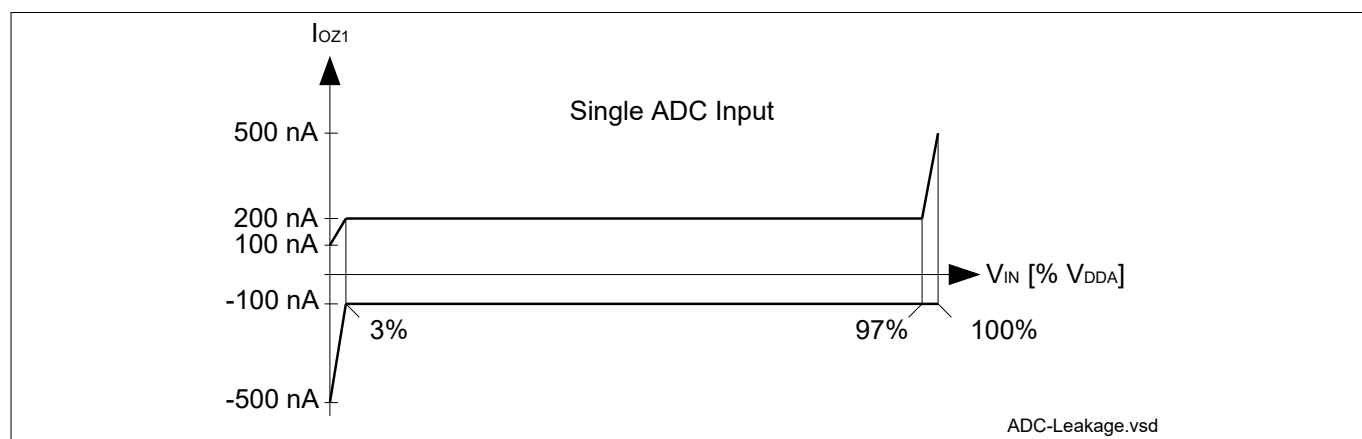


Figure 16 VADC Analog Input Leakage Current

3 Electrical Parameters

Conversion Time

Table 26 Conversion Time (Operating Conditions apply)

Parameter	Symbol	Values	Unit	Note
Conversion time	t_C CC	$2 \times T_{ADC} + (2 + N + STC + PC + DM) \times T_{ADCI}$	μs	N = 8, 10, 12 for N-bit conversion $T_{ADC} = 1/f_{PERIPH}$ $T_{ADCI} = 1/f_{ADCI}$

- STC defines additional clock cycles to extend the sample time
- PC adds two cycles if post-calibration is enabled
- DM adds one cycle for an extended conversion time of the MSB

Conversion Time Examples

System assumptions:

$f_{ADC} = 144$ MHz that is $t_{ADC} = 6.9$ ns, DIVA = 3, $f_{ADCI} = 36$ MHz that is $t_{ADCI} = 27.8$ ns

According to the given formulas the following minimum conversion times can be achieved (STC = 0, DM = 0):

12-bit post-calibrated conversion (PC = 2):

$$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 27.8 \text{ ns} + 2 \times 6.9 \text{ ns} = 459 \text{ ns}$$

12-bit uncalibrated conversion:

$$t_{CN12} = (2 + 12) \times t_{ADCI} + 2 \times t_{ADC} = 14 \times 27.8 \text{ ns} + 2 \times 6.9 \text{ ns} = 403 \text{ ns}$$

10-bit uncalibrated conversion:

$$t_{CN10} = (2 + 10) \times t_{ADCI} + 2 \times t_{ADC} = 12 \times 27.8 \text{ ns} + 2 \times 6.9 \text{ ns} = 348 \text{ ns}$$

8-bit uncalibrated:

$$t_{CN8} = (2 + 8) \times t_{ADCI} + 2 \times t_{ADC} = 10 \times 27.8 \text{ ns} + 2 \times 6.9 \text{ ns} = 292 \text{ ns}$$

3 Electrical Parameters

3.2.3 Digital to Analog Converters (DAC)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 27 DAC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
RMS supply current	$I_{DD\ CC}$	–	2.5	4	mA	per active DAC channel, without load currents of DAC outputs
Resolution	$RES\ CC$	–	12	–	Bit	–
Update rate	$f_{URATE_A\ CC}$	–		2	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 1 LSB accuracy
Update rate	$f_{URATE_F\ CC}$	–		5	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 4 LSB accuracy
Settling time	$t_{SETTLE\ CC}$	–	1	2	μs	at full scale jump, output voltage reaches target value ± 20 LSB
Slew rate	$SR\ CC$	2	5	–	V/ μs	–
Minimum output voltage	$V_{OUT_MIN\ CC}$	–	0.3	–	V	code value unsigned: 000 _H ; signed: 800 _H
Maximum output voltage	$V_{OUT_MAX\ CC}$	–	2.5	–	V	code value unsigned: FFF _H ; signed: 7FF _H
Integral non-linearity	$INL\ CC$	-5.5	± 2.5	5.5	LSB	$R_L \geq 5\ k\Omega$, $C_L \leq 50\ pF$
Differential non-linearity	$DNL\ CC$	-2	± 1	2	LSB	$R_L \geq 5\ k\Omega$, $C_L \leq 50\ pF$
Offset error	$ED_{OFF\ CC}$		± 20		mV	–
Gain error	$ED_{G_IN\ CC}$	-6.5	-1.5	3	%	–
Startup time	$t_{STARTUP\ CC}$	–	15	30	μs	time from output enabling till code valid ± 16 LSB
3dB Bandwidth of Output Buffer	$f_{C1\ CC}$	2.5	5	–	MHz	verified by design

(table continues...)

3 Electrical Parameters

Table 27 (continued) **DAC Parameters (Operating Conditions apply)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Output sourcing current	$I_{OUT_SOURCE\ CC}$	–	-30	–	mA	–
Output sinking current	$I_{OUT_SINK\ CC}$	–	0.6	–	mA	–
Output resistance	$R_{OUT\ CC}$	–	50	–	Ohm	–
Load resistance	$R_L\ SR$	5	–	–	kOhm	–
Load capacitance	$C_L\ SR$	–	–	50	pF	–
Signal-to-Noise Ratio	$SNR\ CC$	–	70	–	dB	examination bandwidth < 25 kHz
Total Harmonic Distortion	$THD\ CC$	–	70	–	dB	examination bandwidth < 25 kHz
Power Supply Rejection Ratio	$PSRR\ CC$	–	56	–	dB	to V_{DDA} verified by design

Conversion Calculation

Unsigned:

$$DACxDATA = 4095 \times (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN})$$

Signed:

$$DACxDATA = 4095 \times (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN}) - 2048$$

3 Electrical Parameters

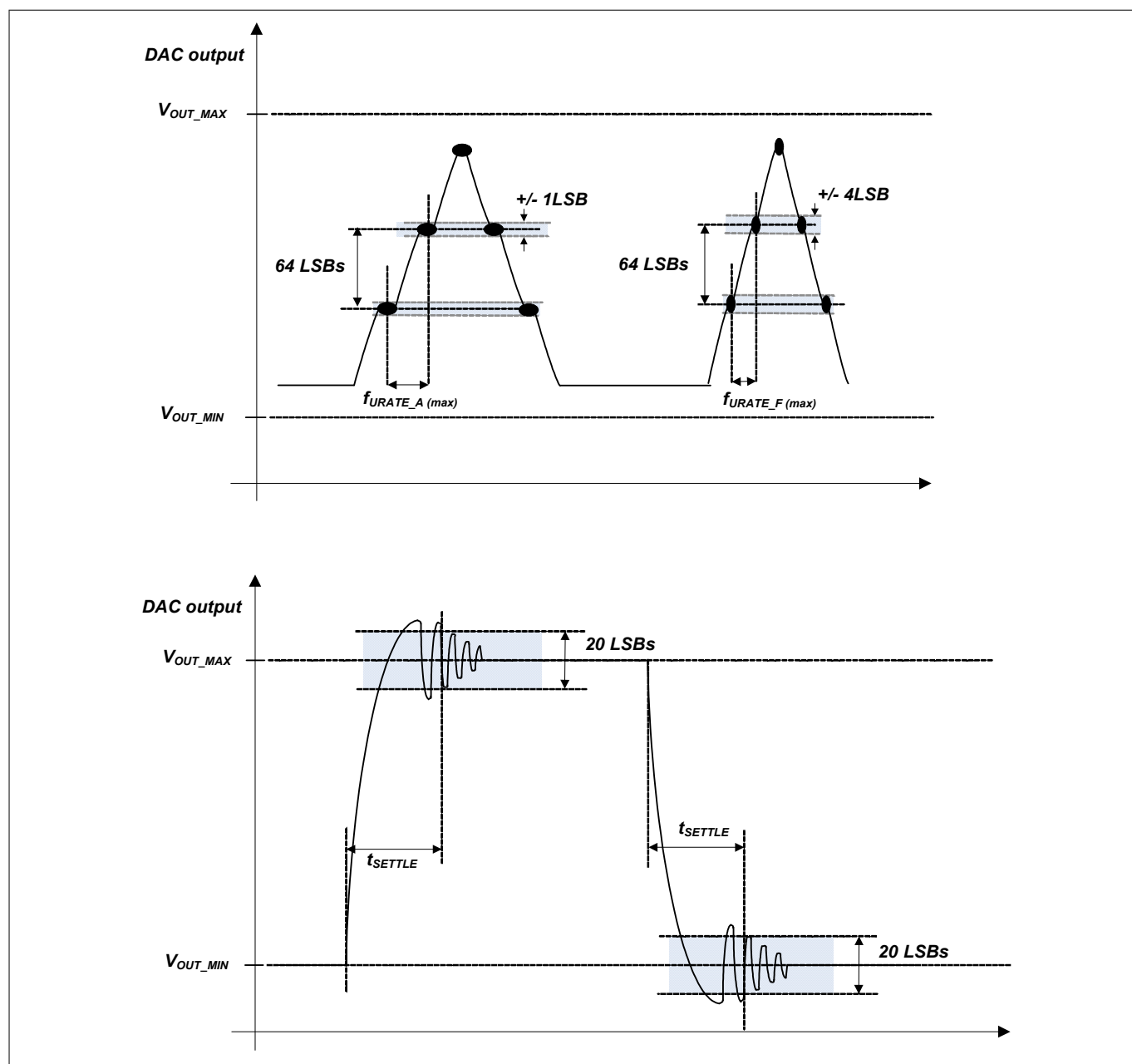


Figure 17 **DAC Conversion Examples**

3 Electrical Parameters

3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the analog reference¹⁾ (V_{AREF}) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The parameters in Table 28 apply for the maximum reference voltage $V_{AREF} = V_{DDA} + 50 \text{ mV}$.

Table 28 ORC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
DC Switching Level	$V_{ODC} \text{ CC}$	100	125	210	mV	$V_{AIN} \geq V_{AREF} + V_{ODC}$
Hysteresis	$V_{OHYS} \text{ CC}$	50	–	V_{ODC}	mV	
Detection Delay of a persistent Overvoltage	$t_{ODD} \text{ CC}$	50	–	450	ns	$V_{AIN} \geq V_{AREF} + 210 \text{ mV}$
		45	–	105	ns	$V_{AIN} \geq V_{AREF} + 400 \text{ mV}$
Always detected Overvoltage Pulse	$t_{OPDD} \text{ CC}$	440	–	–	ns	$V_{AIN} \geq V_{AREF} + 210 \text{ mV}$
		90	–	–	ns	$V_{AIN} \geq V_{AREF} + 400 \text{ mV}$
Never detected Overvoltage Pulse	$t_{OPDN} \text{ CC}$	–	–	45	ns	$V_{AIN} \geq V_{AREF} + 210 \text{ mV}$
		–	–	30	ns	$V_{AIN} \geq V_{AREF} + 400 \text{ mV}$
Release Delay	$t_{ORD} \text{ CC}$	65	–	105	ns	$V_{AIN} \leq V_{AREF}$
Enable Delay	$t_{OED} \text{ CC}$	–	100	200	ns	

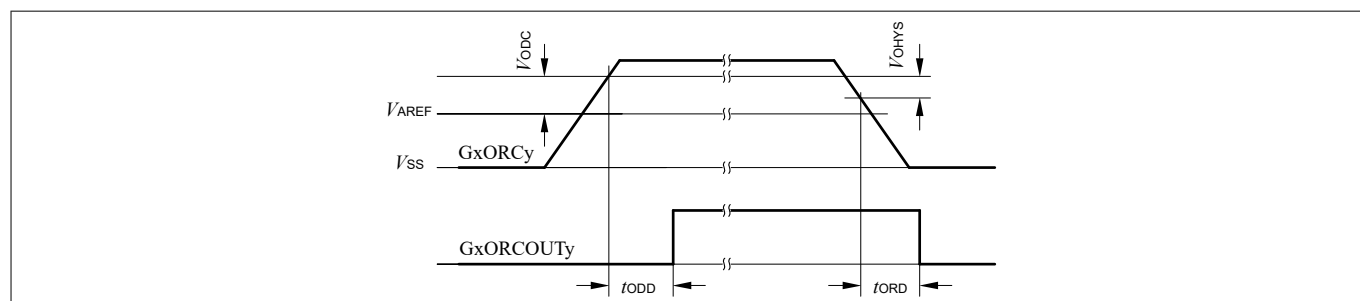


Figure 18 GxORCOUTy Trigger Generation

¹ Always the standard VADC reference, alternate references do not apply to the ORC.

3 Electrical Parameters

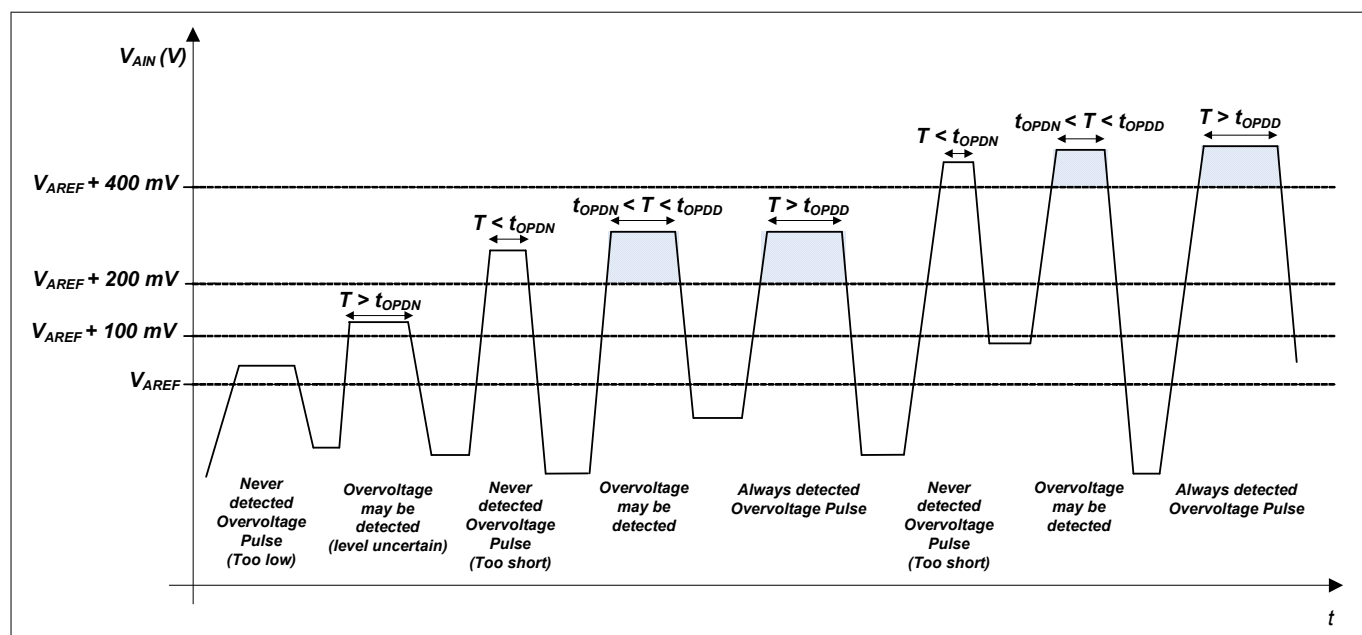


Figure 19 ORC Detection Ranges

3.2.5 Die Temperature Sensor

The Die Temperature Sensor (DTS) measures the junction temperature T_J .

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 29 Die Temperature Sensor Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Temperature sensor range	T_{SR} SR	-40	–	150	°C	–
Linearity Error (to the below defined formula)	ΔT_{LE} CC	–	±1	–	°C	per $\Delta T_J \leq 30^\circ\text{C}$
Offset Error	ΔT_{OE} CC	–	±6	–	°C	$\Delta T_{OE} = T_J - T_{DTS}$ $V_{DDP} \leq 3.3 \text{ V}^{1)}$
Measurement time	t_M CC	–	–	100	µs	–
Start-up time after reset inactive	t_{TSST} SR	–	–	10	µs	–

1) At $V_{DDP_max} = 3.63 \text{ V}$ the typical offset error increases by an additional $\Delta T_{OE} = \pm 1^\circ\text{C}$.

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

Temperature $T_{DTS} = (\text{RESULT} - 605)/2.05$ [°C]

This formula and the values defined in Table 29 apply with the following calibration values:

- DTSCON.BGTRIM = 8_H
- DTSCON.REFTRIM = 4_H

3 Electrical Parameters

3.2.6 USB OTG Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 30 USB OTG VBUS and ID Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
VBUS input voltage range	$V_{IN\ CC}$	0.0	–	5.25	V	–
A-device VBUS valid threshold	$V_{B1\ CC}$	4.4	–	–	V	–
A-device session valid threshold	$V_{B2\ CC}$	0.8	–	2.0	V	–
B-device session valid threshold	$V_{B3\ CC}$	0.8	–	4.0	V	–
B-device session end threshold	$V_{B4\ CC}$	0.2	–	0.8	V	–
VBUS input resistance to ground	$R_{VBUS_IN\ CC}$	40	–	100	kOhm	–
B-device VBUS pull-up resistor	$R_{VBUS_PU\ CC}$	281	–	–	Ohm	Pull-up voltage = 3.0 V
B-device VBUS pull-down resistor	$R_{VBUS_PD\ CC}$	656	–	–	Ohm	–
USB.ID pull-up resistor	$R_{UID_PU\ CC}$	14	–	25	kOhm	–
VBUS input current	$I_{VBUS_IN\ CC}$	–	–	150	μA	$0\ V \leq V_{IN} \leq 5.25\ V$: $T_{AVG} = 1\ ms$

3 Electrical Parameters

Table 31 **USB OTG Data Line (USB_DP, USB_DM) Parameters (Operating Conditions apply)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input low voltage	V_{IL} SR	–	–	0.8	V	–
Input high voltage (driven)	V_{IH} SR	2.0	–	–	V	–
Input high voltage (floating) ¹⁾	V_{IHZ} SR	2.7	–	3.6	V	–
Differential input sensitivity	V_{DIS} CC	0.2	–	–	V	–
Differential common mode range	V_{CM} CC	0.8	–	2.5	V	–
Output low voltage	V_{OL} CC	0.0	–	0.3	V	1.5 kOhm pull-up to 3.6 V
Output high voltage	V_{OH} CC	2.8	–	3.6	V	15 kOhm pull-down to 0 V
DP pull-up resistor (idle bus)	R_{PUI} CC	900	–	1575	Ohm	–
DP pull-up resistor (upstream port receiving)	R_{PUA} CC	1425	–	3090	Ohm	–
DP, DM pull-down resistor	R_{PD} CC	14.25	–	24.8	kOhm	–
Input impedance DP, DM	Z_{INP} CC	300	–	–	kOhm	$0\text{ V} \leq V_{IN} \leq V_{DDP}$
Driver output resistance DP, DM	Z_{DRV} CC	28	–	44	Ohm	–

1) Measured at A-connector with $1.5\text{ kOhm} \pm 5\%$ to $3.3\text{ V} \pm 0.3\text{ V}$ connected to USB_DP or USB_DM and at B-connector with $15\text{ kOhm} \pm 5\%$ to ground connected to USB_DP and USB_DM.

3 Electrical Parameters

3.2.7 Oscillator Pins

Note: *It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.*

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

The oscillator pins can be operated with an external crystal (see [Figure 20](#)) or in direct input mode (see [Figure 21](#)).

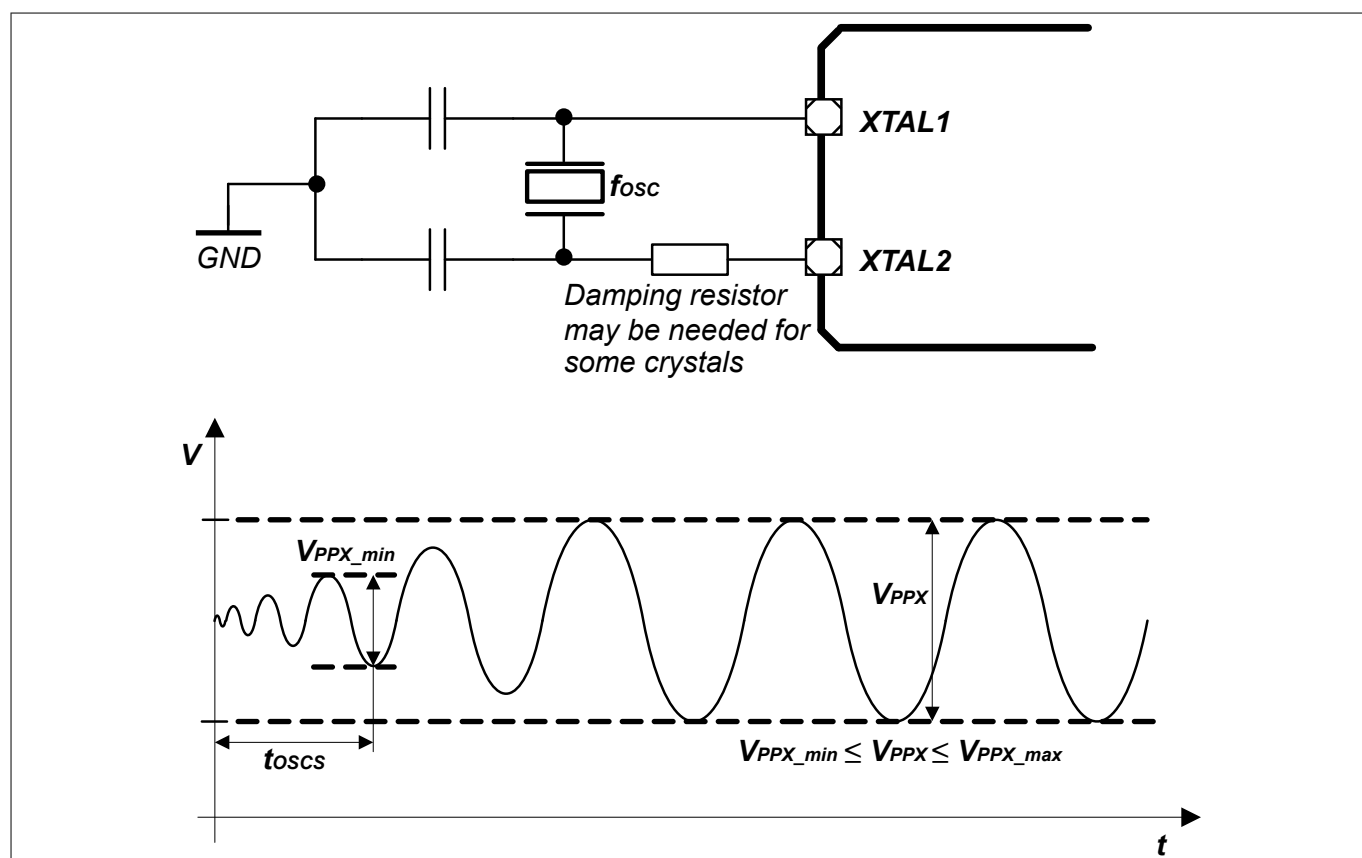


Figure 20 **Oscillator in Crystal Mode**

3 Electrical Parameters

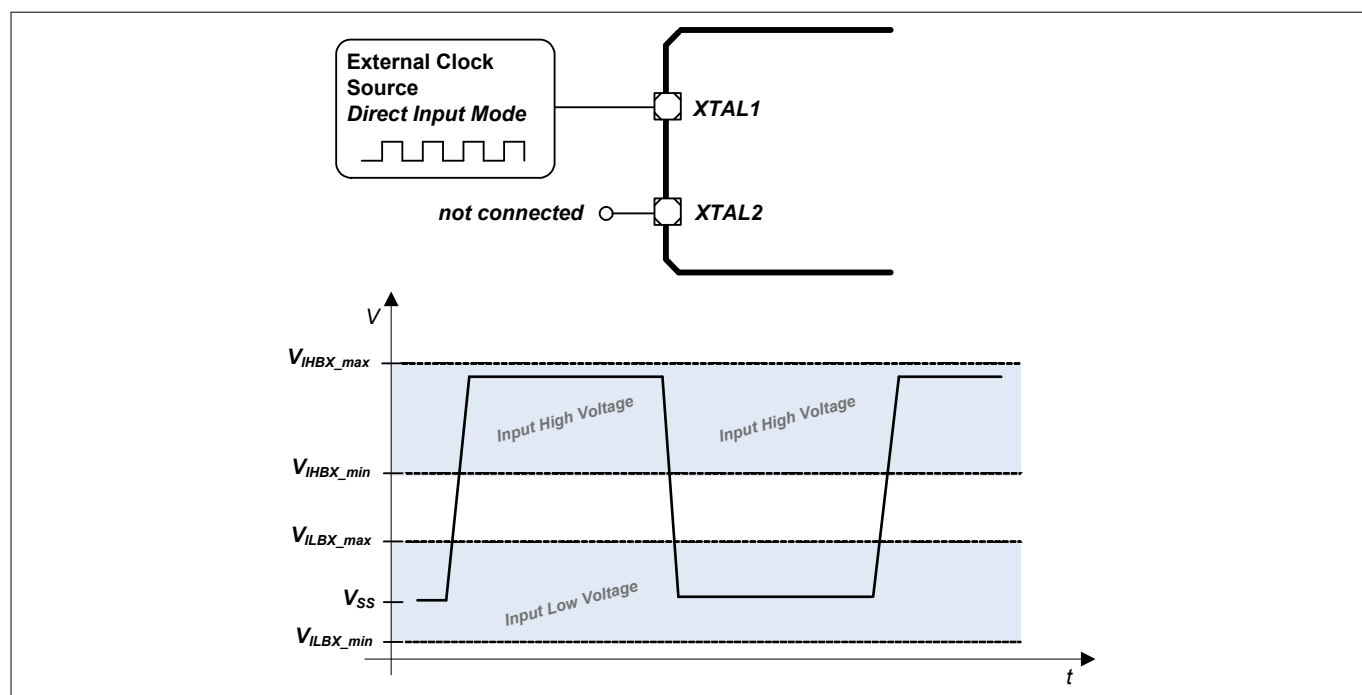


Figure 21 Oscillator in Direct Input Mode

Table 32 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	4	–	40	MHz	Direct Input Mode selected
		4	–	25	MHz	External Crystal Mode selected
Oscillator start-up time ^{1) 2)}	t_{OSCS} CC	–	–	10	ms	–
Input voltage at XTAL1	V_{IX} SR	-0.5	–	$V_{\text{DDP}} + 0.5$	V	–
Input amplitude (peak-to-peak) at XTAL1 ^{2) 3)}	V_{PPX} SR	$0.4 \times V_{\text{DDP}}$	–	$V_{\text{DDP}} + 1.0$	V	–
Input high voltage at XTAL1 ⁴⁾	V_{IHBX} SR	1.0	–	$V_{\text{DDP}} + 0.5$	V	–
Input low voltage at XTAL1 ⁴⁾	V_{ILBX} SR	-0.5	–	0.4	V	–
Input leakage current at XTAL1	I_{LX1} CC	-100	–	100	nA	Oscillator power down $0 \text{ V} \leq V_{\text{IX}} \leq V_{\text{DDP}}$

- 1) t_{OSCS} is defined from the moment the oscillator is enabled with SCU_OSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of $0.4 \times V_{\text{DDP}}$.
- 2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.
- 3) If the shaper unit is enabled and not bypassed.
- 4) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

3 Electrical Parameters

Table 33 **RTC_XTAL Parameters**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	–	32.768	–	kHz	–
Oscillator start-up time ^{1) 2) 3)}	t_{OSCS} CC	–	–	5	s	–
Input voltage at RTC_XTAL1	V_{IX} SR	-0.3	–	$V_{BAT} + 0.3$	V	–
Input amplitude (peak-to-peak) at RTC_XTAL1 ^{2) 4)}	V_{PPX} SR	0.4	–	–	V	–
Input high voltage at RTC_XTAL1 ⁵⁾	V_{IHBX} SR	$0.6 \times V_{BAT}$	–	$V_{BAT} + 0.3$	V	–
Input low voltage at RTC_XTAL1 ⁵⁾	V_{ILBX} SR	-0.3	–	$0.36 \times V_{BAT}$	V	–
Input Hysteresis for RTC_XTAL1 ^{5) 6)}	V_{HYSX} CC	$0.1 \times V_{BAT}$	–	–	V	$3.0 \text{ V} \leq V_{BAT} < 3.6 \text{ V}$
		$0.03 \times V_{BAT}$	–	–	V	$V_{BAT} < 3.0 \text{ V}$
Input leakage current at RTC_XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down $0 \text{ V} \leq V_{IX} \leq V_{BAT}$

- 1) t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_OSCULCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of 400 mV.
- 2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.
- 3) For a reliable start of the oscillation in crystal mode it is required that $V_{BAT} \geq 3.0 \text{ V}$. A running oscillation is maintained across the full V_{BAT} voltage range.
- 4) If the shaper unit is enabled and not bypassed.
- 5) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.
- 6) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.2.8 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

If not stated otherwise, the operating conditions for the parameters in the following table are:

$$V_{DDP} = 3.3 \text{ V}, T_A = 25^\circ\text{C}$$

Table 34 **Power Supply Parameters**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Active supply current ^{1) 2)} Peripherals enabled	I_{DDPA} CC	–	135	–	mA	144/144/144

(table continues...)

3 Electrical Parameters

Table 34 (continued) **Power Supply Parameters**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Frequency: $f_{\text{CPU}} / f_{\text{PERIPH}} / f_{\text{CCU}}$ in MHz		–	125	–		144/72/72
		–	97	–		72/72/144
		–	80	–		24/24/24
		–	68	–		1/1/1
Active supply current Code execution from RAM Flash in Sleep mode	$I_{\text{DDPA CC}}$	–	108	–	mA	144/144/144
		–	98	–		144/72/72
Active supply current ³⁾ Peripherals disabled Frequency: $f_{\text{CPU}} / f_{\text{PERIPH}} / f_{\text{CCU}}$ in MHz	$I_{\text{DDPA CC}}$	–	86	–	mA	144/144/144
		–	85	–		144/72/72
		–	70	–		72/72/144
		–	55	–		24/24/24
		–	50	–		1/1/1
Sleep supply current ⁴⁾ Peripherals enabled Frequency: $f_{\text{CPU}} / f_{\text{PERIPH}} / f_{\text{CCU}}$ in MHz	$I_{\text{DDPS CC}}$	–	127	–	mA	144/144/144
		–	115	–		144/72/72
		–	93	–		72/72/144
		–	57	–		24/24/24
		–	47	–		1/1/1
$f_{\text{CPU}} / f_{\text{PERIPH}} / f_{\text{CCU}}$ in kHz		–	48	–		100/100/100
Sleep supply current ⁵⁾ Peripherals disabled Frequency: $f_{\text{CPU}} / f_{\text{PERIPH}} / f_{\text{CCU}}$ in MHz	$I_{\text{DDPS CC}}$	–	77	–	mA	144/144/144
		–	76	–		144/72/72
		–	65	–		72/72/144
		–	53	–		24/24/24
		–	46	–		1/1/1
$f_{\text{CPU}} / f_{\text{PERIPH}} / f_{\text{CCU}}$ in kHz		–	47	–		100/100/100
Deep Sleep supply current ⁶⁾ Flash in Sleep mode Frequency: $f_{\text{CPU}} / f_{\text{PERIPH}} / f_{\text{CCU}}$ in MHz	$I_{\text{DDPD CC}}$	–	11	–	mA	24/24/24
		–	7.0	–		4/4/4
		–	6.6	–		1/1/1
$f_{\text{CPU}} / f_{\text{PERIPH}} / f_{\text{CCU}}$ in kHz		–	7.6	–		100/100/100 ⁷⁾
Hibernate supply current RTC on ⁸⁾	$I_{\text{DDPH CC}}$	–	8.7	–	μA	$V_{\text{BAT}} = 3.3 \text{ V}$
		–	6.5	–		$V_{\text{BAT}} = 2.4 \text{ V}$
		–	5.7	–		$V_{\text{BAT}} = 2.0 \text{ V}$

(table continues...)

3 Electrical Parameters

Table 34 (continued) Power Supply Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Hibernate supply current RTC off ⁹⁾	$I_{DDPH\ CC}$	–	8.0	–	μA	$V_{BAT} = 3.3\ V$
		–	6.0	–		$V_{BAT} = 2.4\ V$
		–	5.0	–		$V_{BAT} = 2.0\ V$
Hibernate off ¹⁰⁾	$I_{DDPH\ CC}$	–	4.4	–	μA	$V_{BAT} = 3.3\ V$
		–	3.5	–		$V_{BAT} = 2.4\ V$
		–	3.1	–		$V_{BAT} = 2.0\ V$
Worst case active supply current ¹¹⁾	$I_{DDPA\ CC}$	–	–	250 ²⁾	mA	$V_{DDP} = 3.6\ V$, $T_J = 150^\circ C$
V_{DDA} power supply current	$I_{DDA\ CC}$	–	–	–	mA	–
I_{DDP} current at $\overline{PORST}$ Low	$I_{DDP_PORST\ CC}$	–	5	10	mA	$V_{DDP} = 3.3\ V$, $T_J = 25^\circ C$
		–	13	55	mA	$V_{DDP} = 3.6\ V$, $T_J = 150^\circ C$
Power Dissipation	$P_{DISS\ CC}$	–	–	1.4	W	$V_{DDP} = 3.6\ V$, $T_J = 150^\circ C$
Wake-up time from Sleep to Active mode	$t_{SSA\ CC}$	–	6	–	cycles	–
Wake-up time from Deep Sleep to Active mode		–	–	–	ms	Defined by the wake-up of the Flash module, see Section 3.2.9
Wake-up time from Hibernate mode		–	–	–	ms	Wake-up via power-on reset event, see Section 3.3.2

1) CPU executing code from Flash, all peripherals idle.

2) I_{DDP} decreases typically by approximately 5 mA when f_{SYS} decreases by 10 MHz, at constant T_J .

3) CPU executing code from Flash.

4) CPU in sleep, all peripherals idle, Flash in Active mode.

5) CPU in sleep, Flash in Active mode.

6) CPU in sleep, peripherals disabled, after wake-up code execution from RAM.

7) To wake-up the Flash from its Sleep mode, $f_{CPU} \geq 1\ MHz$ is required.

8) OSC_ULP operating with external crystal on RTC_XTAL.

9) OSC_ULP off, Hibernate domain operating with OSC_SI clock.

10) V_{BAT} supplied, but Hibernate domain not started; for example state after factory assembly.

11) Test Power Loop: $f_{SYS} = 144\ MHz$, CPU executing benchmark code from Flash, all CCUs in 100 kHz timer mode, all ADC groups in continuous conversion mode, USICs as SPI in internal loop-back mode, CAN in 500 kHz internal loop-back mode, interrupt triggered DMA block transfers to parity protected RAMs and FCE, DTS measurements and FPU calculations.

The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.

3 Electrical Parameters

Peripheral Idle Currents

Default test conditions:

- f_{sys} and derived clocks at 144 MHz
- $V_{\text{DDP}} = 3.3 \text{ V}$, $T_a = 25^\circ\text{C}$
- all peripherals are held in reset (see the PRSTAT registers in the Reset Control Unit of the SCU)
- the peripheral clocks are disabled (see CGATSTAT registers in the Clock Control Unit of the SCU)
- no I/O activity

The given values are a result of differential measurements with asserted and deasserted peripheral reset as well as disabled and enabled clock of the peripheral under test.

The tested peripheral is left in the state after the peripheral reset is deasserted, no further initialisation or configuration is done. For example no timer is running in the CCUs, no communication active in the USICs, etc.

Table 35 **Peripheral Idle Currents**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
PORTS FCE WDT POSIFx ¹⁾	$I_{\text{PER CC}}$	–	≤ 0.3	–	mA	–
MultiCAN ERU LEDTSCU0 ETH CCU4x ¹⁾ , CCU8x ¹⁾		–	≤ 1.0	–		–
DAC (digital) ²⁾		–	1.3	–		–
USICx DMA1 SDMMC		–	3.0	–		–
DSD, EBU, VADC (digital) ²⁾		–	4.5	–		–
DMA0, USB, EtherCAT		–	6.0	–		–

- 1) Enabling the f_{CCU} clock for the POSIFx/CCU4x/CCU8x modules adds approximately $I_{\text{PER}} = 4.8 \text{ mA}$, disregarding which and how many of those peripherals are enabled.
- 2) The current consumption of the analog components are given in the dedicated Datasheet sections of the respective peripheral.

3 Electrical Parameters

3.2.9 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 36 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Erase Time per 256 Kbyte Sector	$t_{\text{ERP CC}}$	–	5	5.5	s	–
Erase Time per 64 Kbyte Sector	$t_{\text{ERP CC}}$	–	1.2	1.4	s	–
Erase Time per 16 Kbyte Logical Sector	$t_{\text{ERP CC}}$	–	0.3	0.4	s	–
Program time per page ¹⁾	$t_{\text{PRP CC}}$	–	5.5	11	ms	–
Erase suspend delay	$t_{\text{FL_ErSusp CC}}$	–	–	15	ms	–
Wait time after margin change	$t_{\text{FL_MarginDel CC}}$	10	–	–	μs	–
Wake-up time	$t_{\text{WU CC}}$	–	–	270	μs	–
Read access time	$t_{\text{a CC}}$	22	–	–	ns	For operation with $1/f_{\text{CPU}} < t_{\text{a}}$ wait states must be configured ²⁾
Data Retention Time, Physical Sector ^{3) 4)}	$t_{\text{RET CC}}$	20	–	–	years	Max. 1000 erase/program cycles
Data Retention Time, Logical Sector ^{3) 4)}	$t_{\text{RETL CC}}$	20	–	–	years	Max. 100 erase/program cycles
Data Retention Time, User Configuration Block (UCB) ^{3) 4)}	$t_{\text{RTU CC}}$	20	–	–	years	Max. 4 erase/program cycles per UCB
Endurance on 64 Kbyte Physical Sector PS4	$N_{\text{EPS4 CC}}$	10000	–	–	cycles	Cycling distributed over life time ⁵⁾

- 1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.
- 2) The following formula applies to the wait state configuration: $\text{FCON.WSPFLASH} \times (1/f_{\text{CPU}}) \geq t_{\text{a}}$.
- 3) Storage and inactive time included.
- 4) Values given are valid for an average weighted junction temperature of $T_{\text{J}} = 110^{\circ}\text{C}$.
- 5) Only valid with robust EEPROM emulation algorithm, equally cycling the logical sectors. For more details see the Reference Manual.

3 Electrical Parameters

3.3 AC Parameters

3.3.1 Testing Waveforms

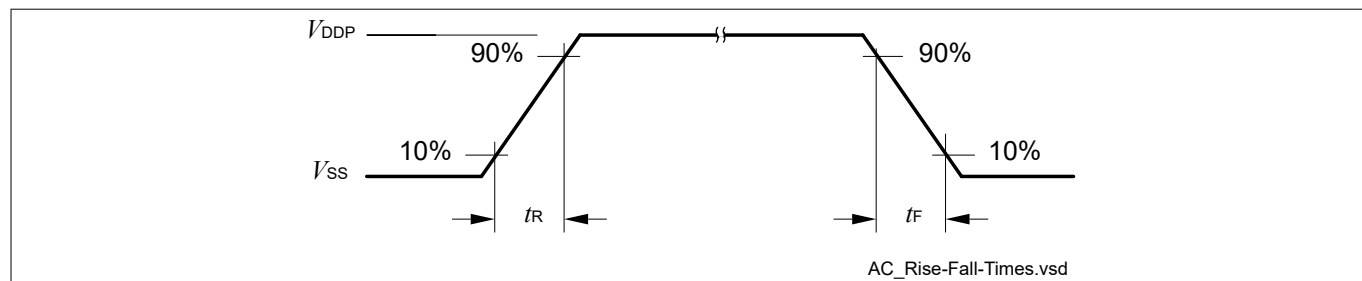


Figure 22 Rise/Fall Time Parameters

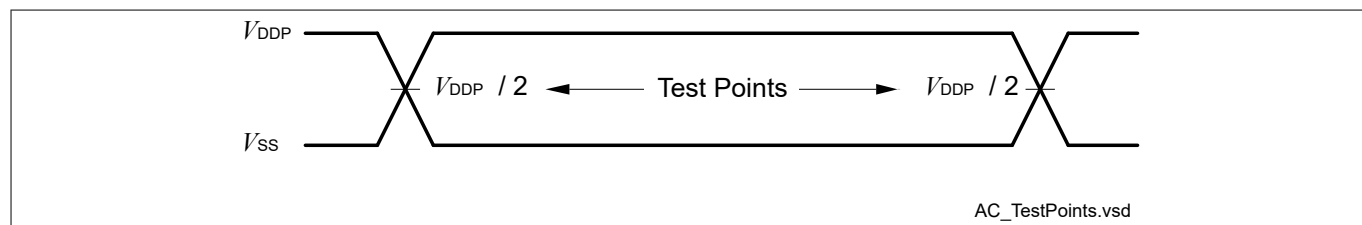


Figure 23 Testing Waveform, Output Delay

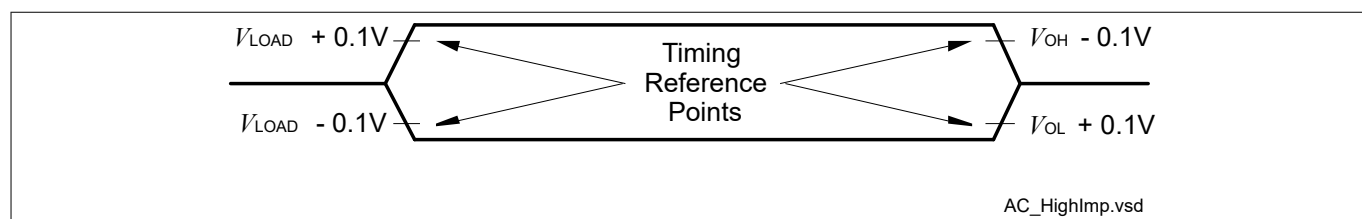


Figure 24 Testing Waveform, Output High Impedance

3 Electrical Parameters

3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when V_{DDP} and/or V_{DDC} violate the respective thresholds.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

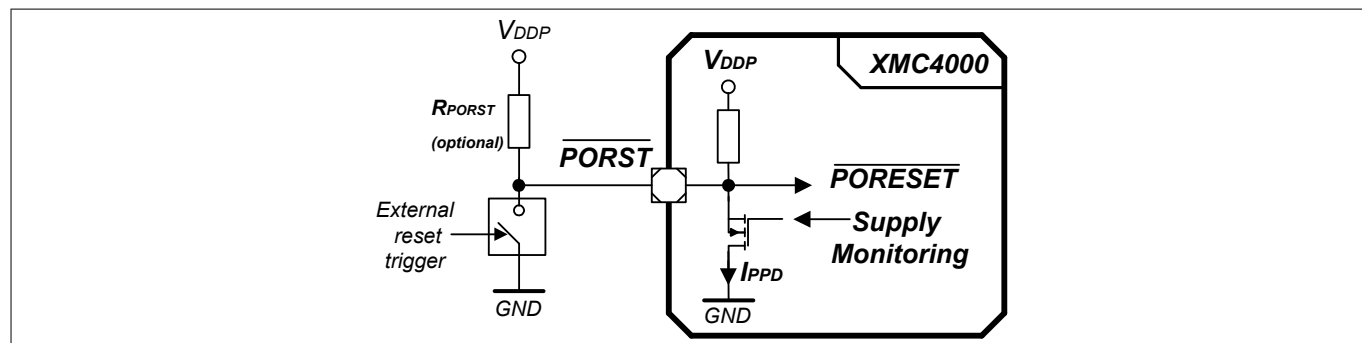


Figure 25 $\overline{\text{PORST}}$ Circuit

Table 37 Supply Monitoring Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Digital supply voltage reset threshold	$V_{\text{POR CC}}$	2.79 ¹⁾	–	3.05 ²⁾	V	³⁾
Core supply voltage reset threshold	$V_{\text{PV CC}}$	–	–	1.17	V	–
V_{DDP} voltage to ensure defined pad states	$V_{\text{DDPPA CC}}$	–	1.0	–	V	–
$\overline{\text{PORST}}$ rise time	$t_{\text{PR SR}}$	–	–	2	μs	⁴⁾
Startup time from power-on reset with code execution from Flash	$t_{\text{SSW CC}}$	–	2.5	3.5	ms	Time to the first user code instruction
V_{DDC} ramp up time	$t_{\text{VCR CC}}$	–	550	–	μs	Ramp up after power-on or after a reset triggered by a violation of V_{POR} or V_{PV}

1) Minimum threshold for reset assertion.

2) Maximum threshold for reset deassertion.

3) The V_{DDP} monitoring has a typical hysteresis of $V_{\text{PORHYS}} = 180 \text{ mV}$.

4) If t_{PR} is not met, low spikes on $\overline{\text{PORST}}$ may be seen during start up (e.g. reset pulses generated by the supply monitoring due to a slow ramping V_{DDP}).

3 Electrical Parameters

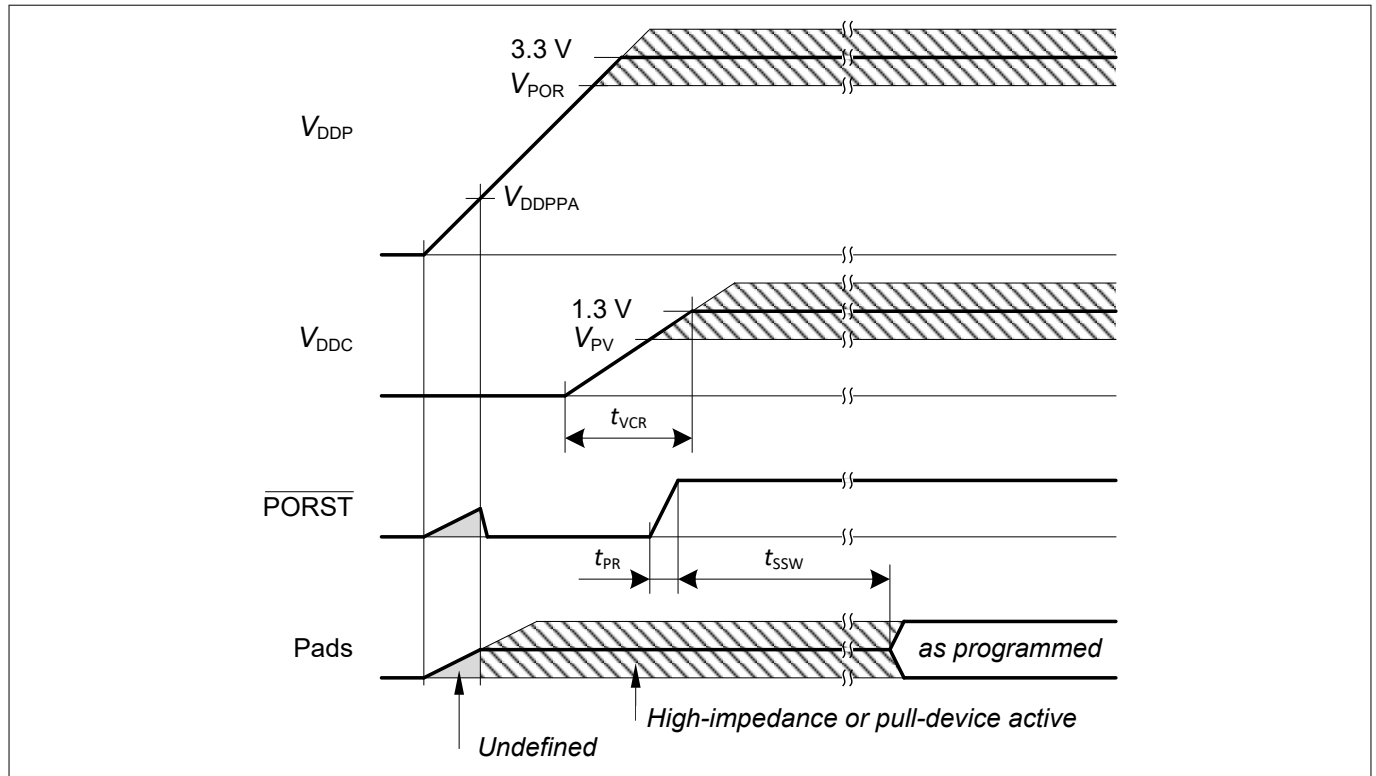


Figure 26 Power-Up Behavior

3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency f_{CPU} . Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 38 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	–	–	50	mA	Load increase on V_{DDP} $\Delta t \leq 10$ ns
Negative Load Step Current	ΔI_{NLS} SR	–	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq 10$ ns
V_{DDC} Voltage Over-/Undershoot from Load Step	ΔV_{LS} CC	–	–	± 100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	–	μs	–

(table continues...)

3 Electrical Parameters

Table 38 (continued) **Power Sequencing Parameters**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Negative Load Step Settling Time	t_{NLSS} SR	100	–	–	μs	–
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	–	10	–	μF	In addition $C = 100$ nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:

$f_{CPU} = f_{SYS}$, target frequency $f_{CPU} = 144$ MHz, main PLL $f_{VCO} = 288$ MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 72 MHz - 96 MHz - 144 MHz (K2 steps 12 - 6 - 4 - 3 - 2)

24 MHz - 48 MHz - 96 MHz - 144 MHz (K2 steps 12 - 6 - 3 - 2)

24 MHz - 72 MHz - 144 MHz (K2 steps 12 - 4 - 2)

3.3.4 Phase Locked Loop (PLL) Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Main and USB PLL

Table 39 **PLL Parameters**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	D_P CC	–	–	± 5	ns	accumulated over 300 cycles $f_{SYS} = 144$ MHz
Duty Cycle ¹⁾	D_{DC} CC	46	50	54	%	Low pulse to total period, assuming an ideal input clock source
PLL base frequency	$f_{PLLBASE}$ CC	30	–	140	MHz	–
VCO input frequency	f_{REF} CC	4	–	16	MHz	–
VCO frequency range	f_{VCO} CC	260	–	520	MHz	–
PLL lock-in time	t_L CC	–	–	400	μs	–

1) 50% for even K2 divider values, $50 \pm (10/K2)$ for odd K2 divider values.

3 Electrical Parameters

3.3.5 Internal Clock Source Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Fast Internal Clock Source

Table 40 Fast Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Nominal frequency	$f_{\text{OFINC CC}}$	–	36.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	$\Delta f_{\text{OFI CC}}$	-0.5	–	0.5	%	automatic calibration ^{1) 2)}
		-15	–	15	%	factory calibration, $V_{\text{DDP}} = 3.3 \text{ V}$
		-25	–	25	%	no calibration, $V_{\text{DDP}} = 3.3 \text{ V}$
		-7	–	7	%	Variation over voltage range ³⁾ $3.13 \text{ V} \leq V_{\text{DDP}} \leq 3.63 \text{ V}$
Start-up time	$t_{\text{OFIS CC}}$	–	50	–	μs	–

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the V_{DDP} supply voltage.

3) Deviations from the nominal V_{DDP} voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

Slow Internal Clock Source

Table 41 Slow Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Nominal frequency	$f_{\text{OSI CC}}$	–	32.768	–	kHz	–
Accuracy	$\Delta f_{\text{OSI CC}}$	-4	–	4	%	$V_{\text{BAT}} = \text{const.}$ $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$
		-5	–	5	%	$V_{\text{BAT}} = \text{const.}$ $T_A < 0^\circ\text{C}$ or $T_A > 85^\circ\text{C}$
		-5	–	5	%	$2.4 \text{ V} \leq V_{\text{BAT}},$ $T_A = 25^\circ\text{C}$
		-10	–	10	%	$1.95 \text{ V} \leq V_{\text{BAT}} < 2.4 \text{ V},$ $T_A = 25^\circ\text{C}$
Start-up time	$t_{\text{OSIS CC}}$	–	50	–	μs	–

3 Electrical Parameters

3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 42 JTAG Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	25	–	–	ns	–
TCK high time	t_2 SR	10	–	–	ns	–
TCK low time	t_3 SR	10	–	–	ns	–
TCK clock rise time	t_4 SR	–	–	4	ns	–
TCK clock fall time	t_5 SR	–	–	4	ns	–
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	–
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	–
TDO valid after TCK falling edge ¹⁾ (propagation delay)	t_8 CC	–	–	13	ns	$C_L = 50$ pF
		3	–	–	ns	$C_L = 20$ pF
TDO hold after TCK falling edge ¹⁾	t_{18} CC	2	–	–	ns	–
TDO high impeded. to valid from TCK falling edge ^{1) 2)}	t_9 CC	–	–	14	ns	$C_L = 50$ pF
TDO valid to high impeded. from TCK falling edge ¹⁾	t_{10} CC	–	–	13.5	ns	$C_L = 50$ pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

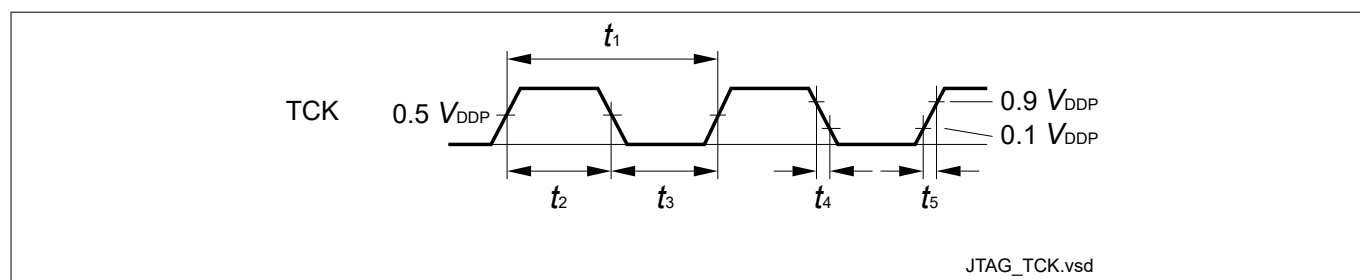


Figure 27 Test Clock Timing (TCK)

3 Electrical Parameters

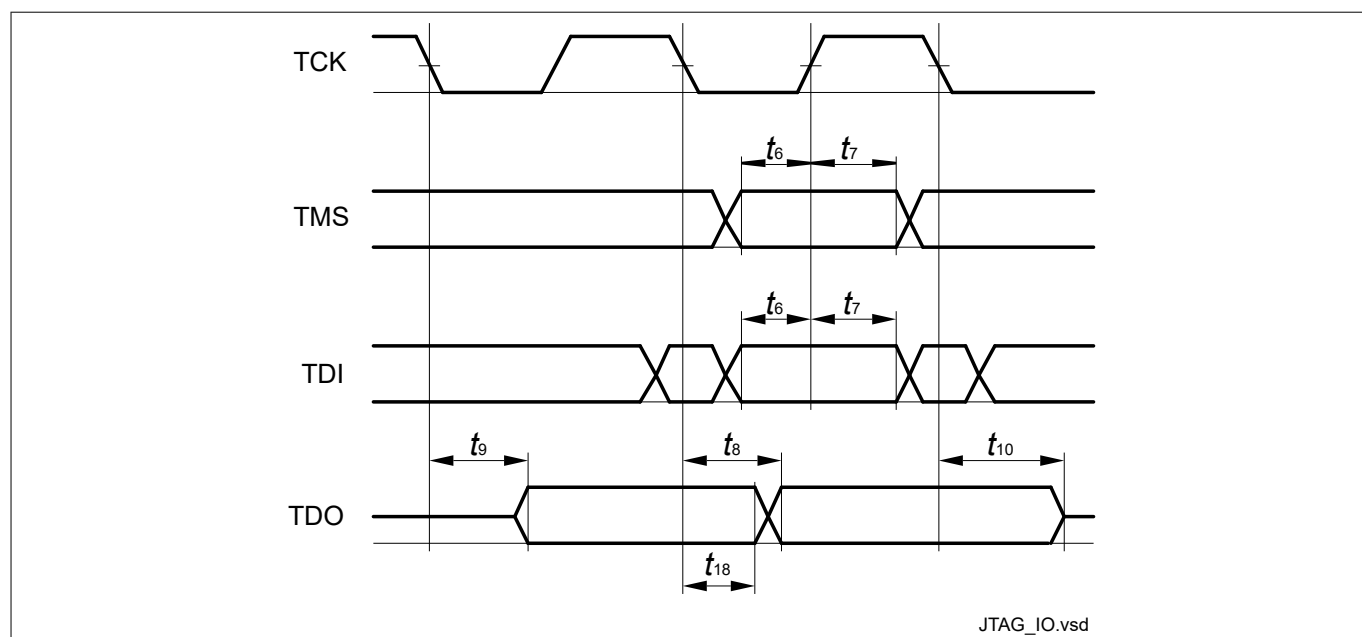


Figure 28 JTAG Timing

3.3.7 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 43 SWD Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
SWDCLK clock period	t_{SC} SR	25	–	–	ns	$C_L = 30$ pF
		40	–	–	ns	$C_L = 50$ pF
SWDCLK high time	t_1 SR	10	–	500000	ns	–
SWDCLK low time	t_2 SR	10	–	500000	ns	–
SWDIO input setup to SWDCLK rising edge	t_3 SR	6	–	–	ns	–
SWDIO input hold after SWDCLK rising edge	t_4 SR	6	–	–	ns	–
SWDIO output valid time after SWDCLK rising edge	t_5 CC	–	–	17	ns	$C_L = 50$ pF
		–	–	13	ns	$C_L = 30$ pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	3	–	–	ns	–

3 Electrical Parameters

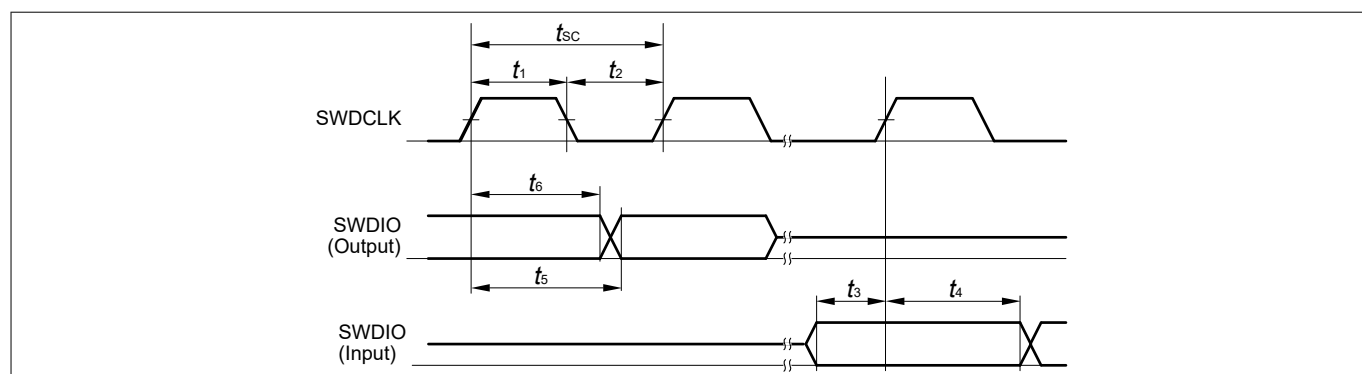


Figure 29 SWD Timing

3.3.8 Embedded Trace Macro Cell (ETM) Timing

The data timing refers to the active clock edge. The XMC4[78]00 ETM uses the half-rate clocking mode. In this mode both, the rising and falling clock edges are active clock edges.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply, with $C_L \leq 15 \text{ pF}$.

Table 44 ETM Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
TRACECLK period	t_1 CC	13.8	–	–	ns	–
TRACECLK high time	t_2 CC	2	–	–	ns	–
TRACECLK low time	t_3 CC	2	–	–	ns	–
TRACECLK and TRACEDATA rise time	t_4 CC	–	–	3	ns	–
TRACECLK and TRACEDATA fall time	t_5 CC	–	–	3	ns	–
TRACEDATA output valid time	t_6 CC	-2	–	3	ns	–

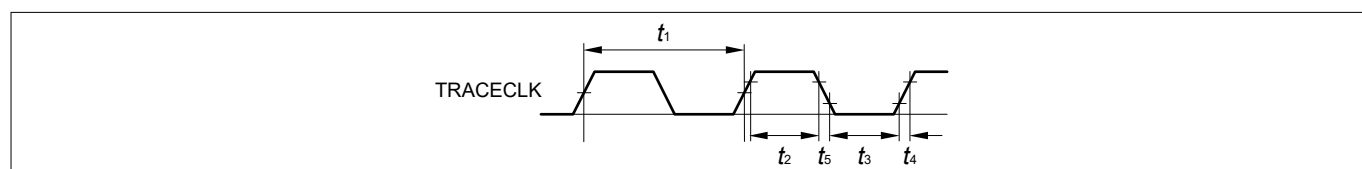


Figure 30 ETM Clock Timing

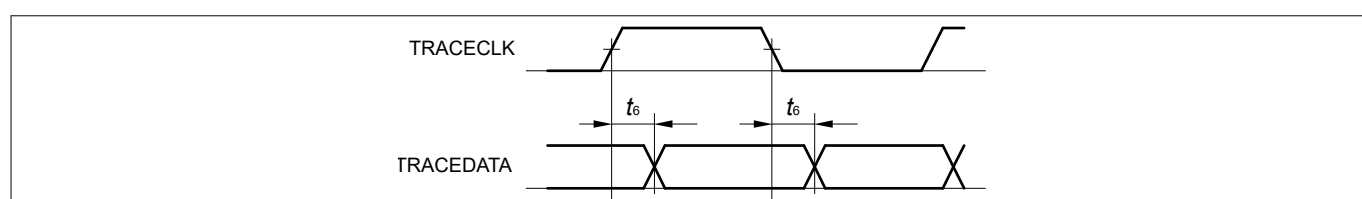


Figure 31 ETM Data Timing

3 Electrical Parameters

3.3.9 Peripheral Timing

3.3.9.1 Delta-Sigma Demodulator Digital Interface Timing

The following parameters are applicable for the digital interface of the Delta-Sigma Demodulator (DSD). The data timing is relative to the active clock edge. Depending on the operation mode of the connected modulator that can be the rising and falling clock edge.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 45 DSD Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
MCLK period in master mode	t_1 CC	33.3	–	–	ns	$t_1 \geq 4 \times t_{\text{PERIPH}}$ ¹⁾
MCLK high time in master mode	t_2 CC	9	–	–	ns	$t_2 > t_{\text{PERIPH}}$ ¹⁾
MCLK low time in master mode	t_3 CC	9	–	–	ns	$t_3 > t_{\text{PERIPH}}$ ¹⁾
MCLK period in slave mode	t_1 SR	33.3	–	–	ns	$t_1 \geq 4 \times t_{\text{PERIPH}}$ ¹⁾
MCLK high time in slave mode	t_2 SR	t_{PERIPH}	–	–	ns	¹⁾
MCLK low time in slave mode	t_3 SR	t_{PERIPH}	–	–	ns	¹⁾
DIN input setup time to the active clock edge	t_4 SR	$t_{\text{PERIPH}} + 4$	–	–	ns	¹⁾
DIN input hold time from the active clock edge	t_5 SR	$t_{\text{PERIPH}} + 3$	–	–	ns	¹⁾

1) $t_{\text{PERIPH}} = 1/f_{\text{PERIPH}}$

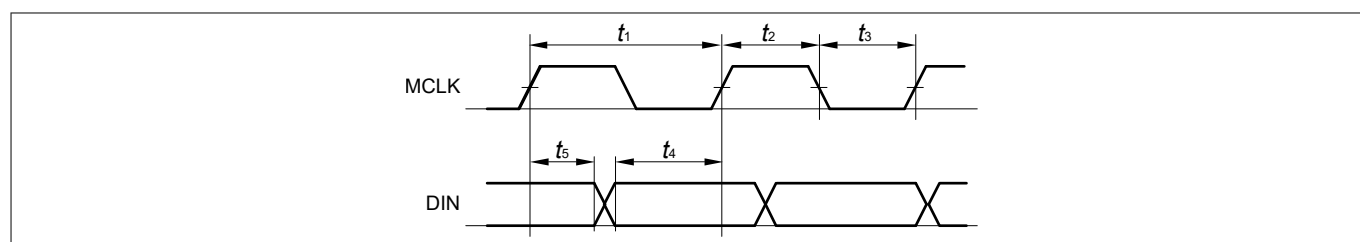


Figure 32 DSD Data Timing

3 Electrical Parameters

3.3.9.2 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 46 USIC SSC Master Mode Timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK} CC	33.3	–	–	ns	–
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	$t_{PB} - 6.5^{1)}$	–	–	ns	–
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	$t_{PB} - 8.5^{1)}$	–	–	ns	–
Data output DOUT[3:0] valid time	t_3 CC	–6	–	8	ns	–
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4 SR	23	–	–	ns	–
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5 SR	1	–	–	ns	–

1) $t_{PB} = 1/f_{PB}$

Table 47 USIC SSC Slave Mode Timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK} SR	66.6	–	–	ns	–
Select input DX2 setup to first clock input DX1 transmit edge ¹⁾	t_{10} SR	3	–	–	ns	–
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	t_{11} SR	4	–	–	ns	–
Receive data input DX0/DX[5:3] setup time to shift clock receive edge ¹⁾	t_{12} SR	6	–	–	ns	–
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge ¹⁾	t_{13} SR	4	–	–	ns	–
Data output DOUT[3:0] valid time	t_{14} CC	0	–	24	ns	–

1) This input timing is valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

3 Electrical Parameters

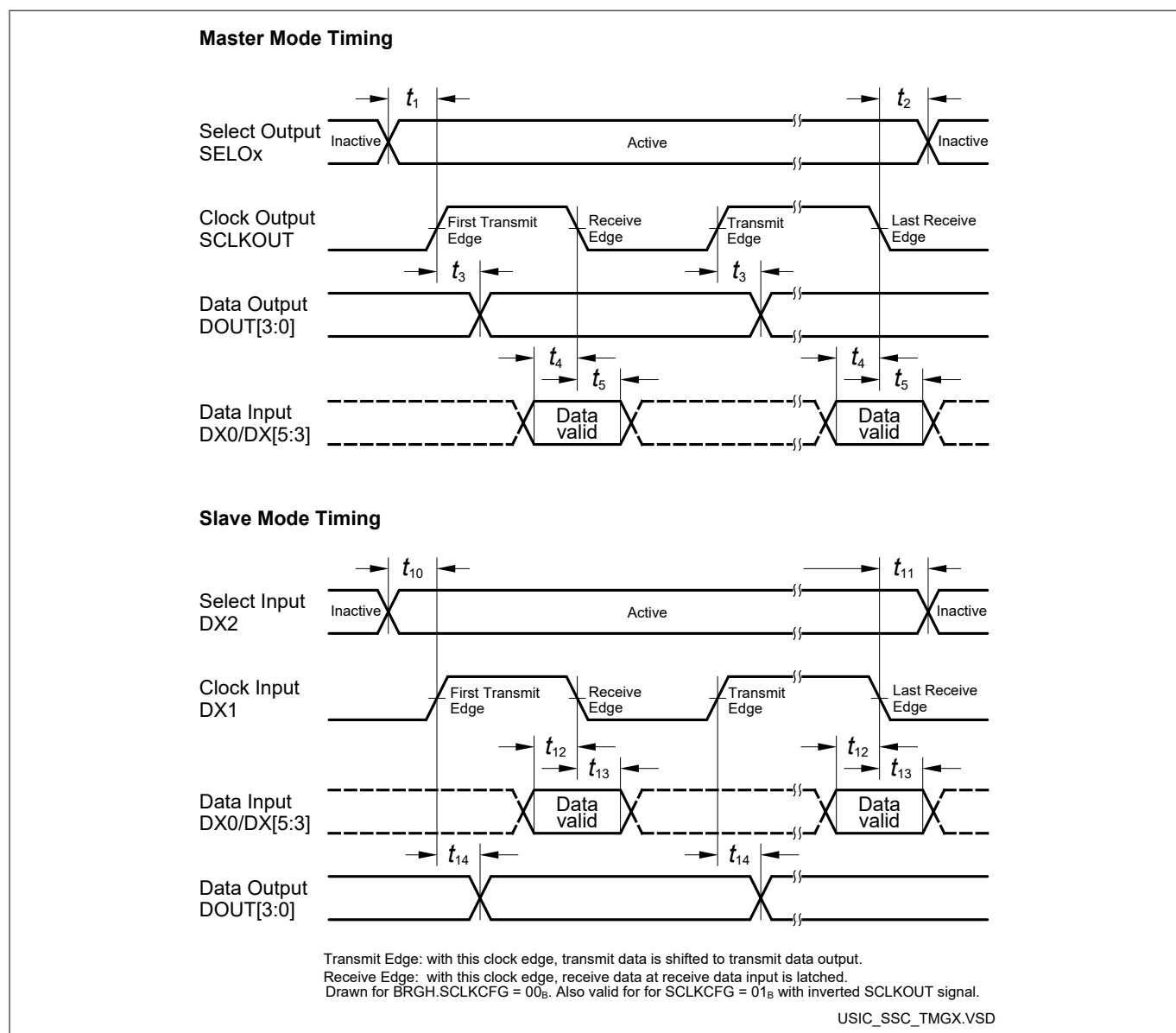


Figure 33 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

3 Electrical Parameters

3.3.9.3 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 48 USIC IIC Standard Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	–	–	300	ns	–
Rise time of both SDA and SCL	t_2 CC/SR	–	–	1000	ns	–
Data hold time	t_3 CC/SR	0	–	–	μs	–
Data set-up time	t_4 CC/SR	250	–	–	ns	–
LOW period of SCL clock	t_5 CC/SR	4.7	–	–	μs	–
HIGH period of SCL clock	t_6 CC/SR	4.0	–	–	μs	–
Hold time for (repeated) START condition	t_7 CC/SR	4.0	–	–	μs	–
Set-up time for repeated START condition	t_8 CC/SR	4.7	–	–	μs	–
Set-up time for STOP condition	t_9 CC/SR	4.0	–	–	μs	–
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	–	–	μs	–
Capacitive load for each bus line	C_b SR	–	–	400	pF	–

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Table 49 USIC IIC Fast Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	$20 + 0.1 \cdot C_b^{2)}$	–	300	ns	–
Rise time of both SDA and SCL	t_2 CC/SR	$20 + 0.1 \cdot C_b^{2)}$	–	300	ns	–
Data hold time	t_3 CC/SR	0	–	–	μs	–
Data set-up time	t_4 CC/SR	100	–	–	ns	–
LOW period of SCL clock	t_5 CC/SR	1.3	–	–	μs	–
HIGH period of SCL clock	t_6 CC/SR	0.6	–	–	μs	–

(table continues...)

3 Electrical Parameters

Table 49 (continued) **USIC IIC Fast Mode Timing¹⁾**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Hold time for (repeated) START condition	t_7 CC/SR	0.6	–	–	μs	–
Set-up time for repeated START condition	t_8 CC/SR	0.6	–	–	μs	–
Set-up time for STOP condition	t_9 CC/SR	0.6	–	–	μs	–
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	–	–	μs	–
Capacitive load for each bus line	C_b SR	–	–	400	pF	–

- 1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.
- 2) C_b refers to the total capacitance of one bus line in pF.

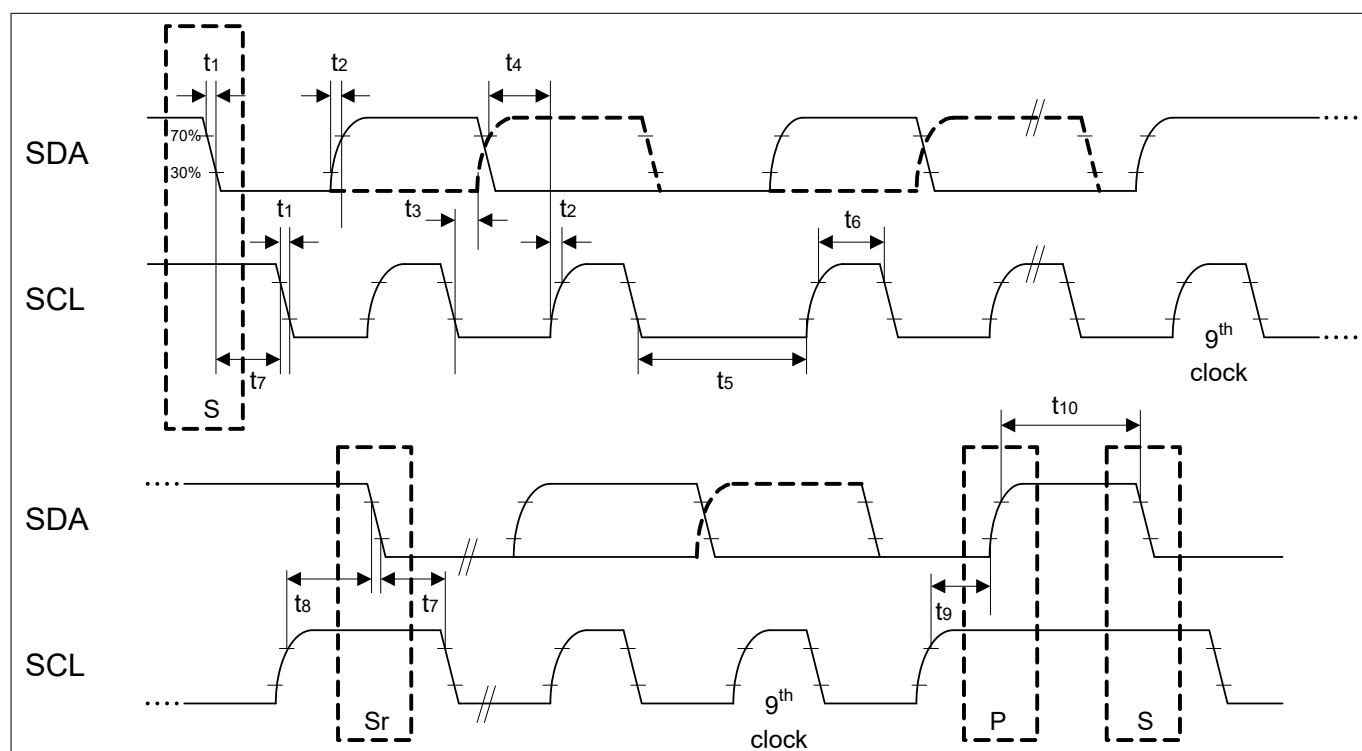


Figure 34 **USIC IIC Stand and Fast Mode Timing**

3 Electrical Parameters

3.3.9.4 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 50 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	33.3	–	–	ns	–
Clock high time	t_2 CC	$0.35 \times t_{1min}$	–	–	ns	–
Clock low time	t_3 CC	$0.35 \times t_{1min}$	–	–	ns	–
Hold time	t_4 CC	0	–	–	ns	–
Clock rise time	t_5 CC	–	–	$0.15 \times t_{1min}$	ns	–

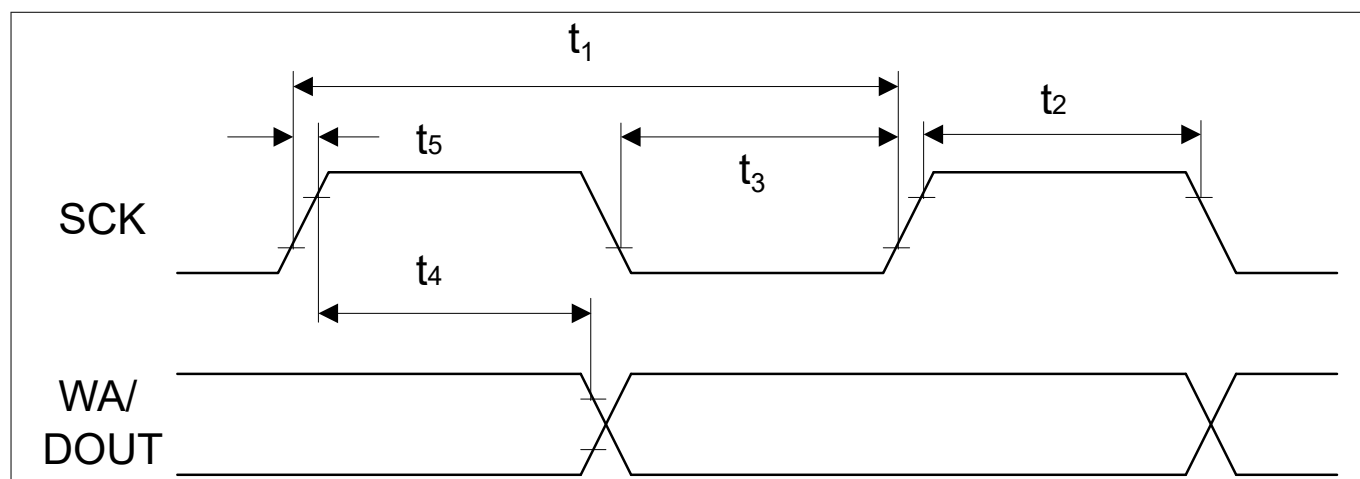


Figure 35 USIC IIS Master Transmitter Timing

Table 51 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	66.6	–	–	ns	–
Clock high time	t_7 SR	$0.35 \times t_{6min}$	–	–	ns	–
Clock low time	t_8 SR	$0.35 \times t_{6min}$	–	–	ns	–
Set-up time	t_9 SR	$0.2 \times t_{6min}$	–	–	ns	–
Hold time	t_{10} SR	0	–	–	ns	–

3 Electrical Parameters

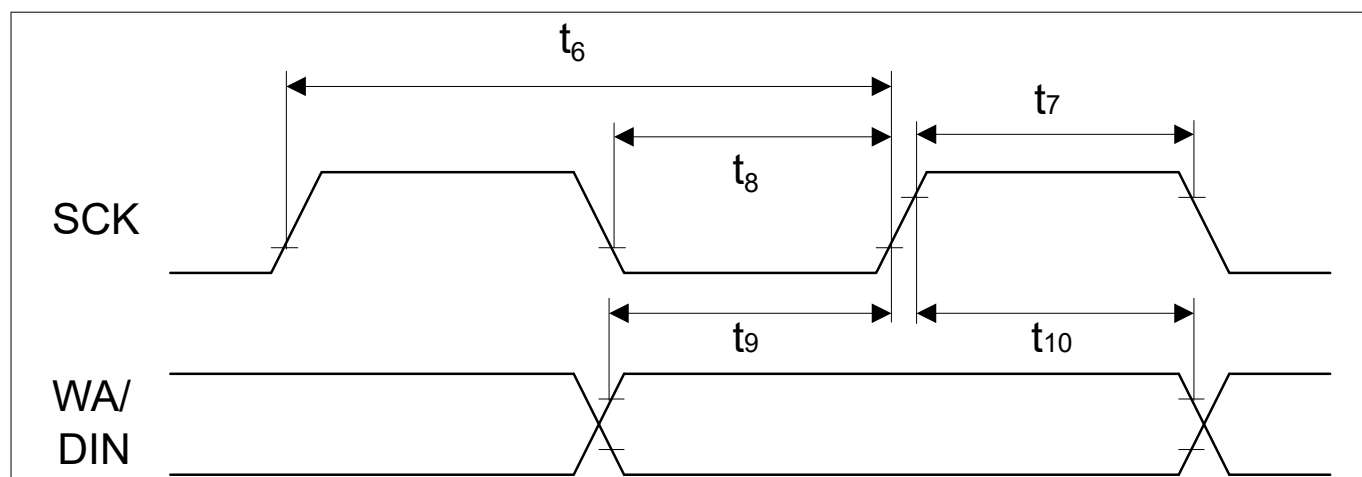


Figure 36 USIC IIS Slave Receiver Timing

3.3.9.5 SDMMC Interface Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, total external capacitive load $C_L = 40 \text{ pF}$.

AC Timing Specifications (Full-Speed Mode)

Table 52 SDMMC Timing for Full-Speed Mode

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Clock frequency in full speed transfer mode ($1/t_{pp}$)	$f_{pp \text{ CC}}$	0	24	MHz	–
Clock cycle in full speed transfer mode	$t_{pp \text{ CC}}$	40	–	ns	–
Clock low time	$t_{WL \text{ CC}}$	10	–	ns	–
Clock high time	$t_{WH \text{ CC}}$	10	–	ns	–
Clock rise time	$t_{TLH \text{ CC}}$	–	10	ns	–
Clock fall time	$t_{THL \text{ CC}}$	–	10	ns	–
Inputs setup to clock rising edge	$t_{ISU_F \text{ SR}}$	2	–	ns	–
Inputs hold after clock rising edge	$t_{IH_F \text{ SR}}$	2	–	ns	–
Outputs valid time in full speed mode	$t_{ODLY_F \text{ CC}}$	–	10	ns	–
Outputs hold time in full speed mode	$t_{OH_F \text{ CC}}$	0	–	ns	–

3 Electrical Parameters

Table 53 SD Card Bus Timing for Full-Speed Mode¹⁾

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
SD card input setup time	t_{ISU}	5	–	ns	–
SD card input hold time	t_{IH}	5	–	ns	–
SD card output valid time	t_{ODLY}	–	14	ns	–
SD card output hold time	t_{OH}	0	–	ns	–

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

Full-Speed Output Path (Write)

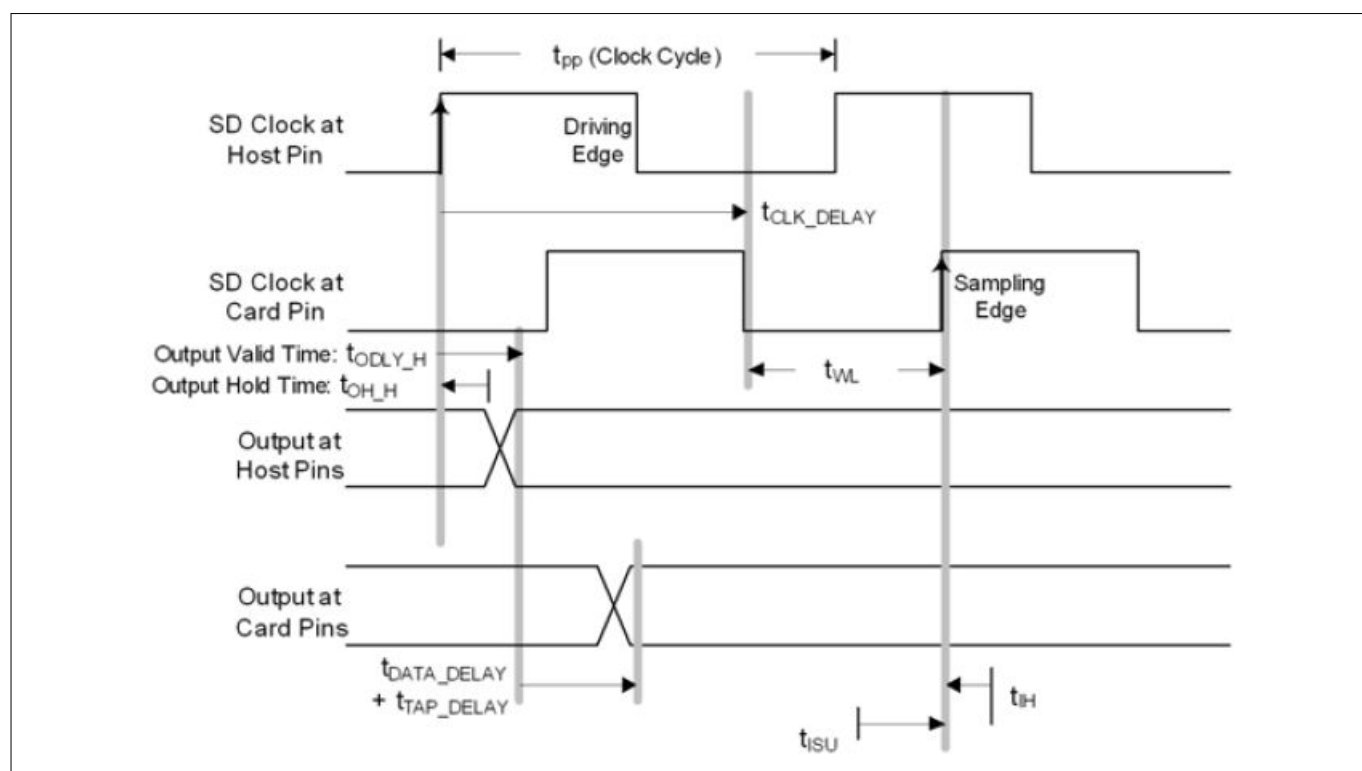


Figure 37 Full-Speed Output Path

Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

$$t_{ODLY_F} + t_{DATA_DELAY} + t_{TAP_DELAY} + t_{ISU} < t_{WL} \quad (1)$$

With clock delay:

$$t_{ODLY_F} + t_{DATA_DELAY} + t_{TAP_DELAY} + t_{ISU} < t_{WL} + t_{CLK_DELAY} \quad (2)$$

3 Electrical Parameters

$$\begin{aligned}
 t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} + t_{\text{WL}} &< t_{\text{PP}} + t_{\text{CLK_DELAY}} - t_{\text{ISU}} - t_{\text{ODLY_F}} \\
 t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} + 20 &< 40 + t_{\text{CLK_DELAY}} - 5 - 10 \\
 t_{\text{DATA_DELAY}} &< 5 + t_{\text{CLK_DELAY}} - t_{\text{TAP_DELAY}}
 \end{aligned}
 \tag{3}$$

The data can be delayed versus clock up to 5 ns in ideal case of $t_{\text{WL}} = 20$ ns.

Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$\begin{aligned}
 t_{\text{CLK_DELAY}} &< t_{\text{WL}} + t_{\text{OH_F}} + t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} - t_{\text{IH}} \\
 t_{\text{CLK_DELAY}} &< 20 + t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} - 5 \\
 t_{\text{DATA_DELAY}} &< 15 + t_{\text{CLK_DELAY}} + t_{\text{TAP_DELAY}}
 \end{aligned}
 \tag{4}$$

The clock can be delayed versus data up to 18.2 ns (external delay line) in ideal case of $t_{\text{WL}} = 20$ ns, with maximum $t_{\text{TAP_DELAY}} = 3.2$ ns programmed.

Full-Speed Input Path (Read)

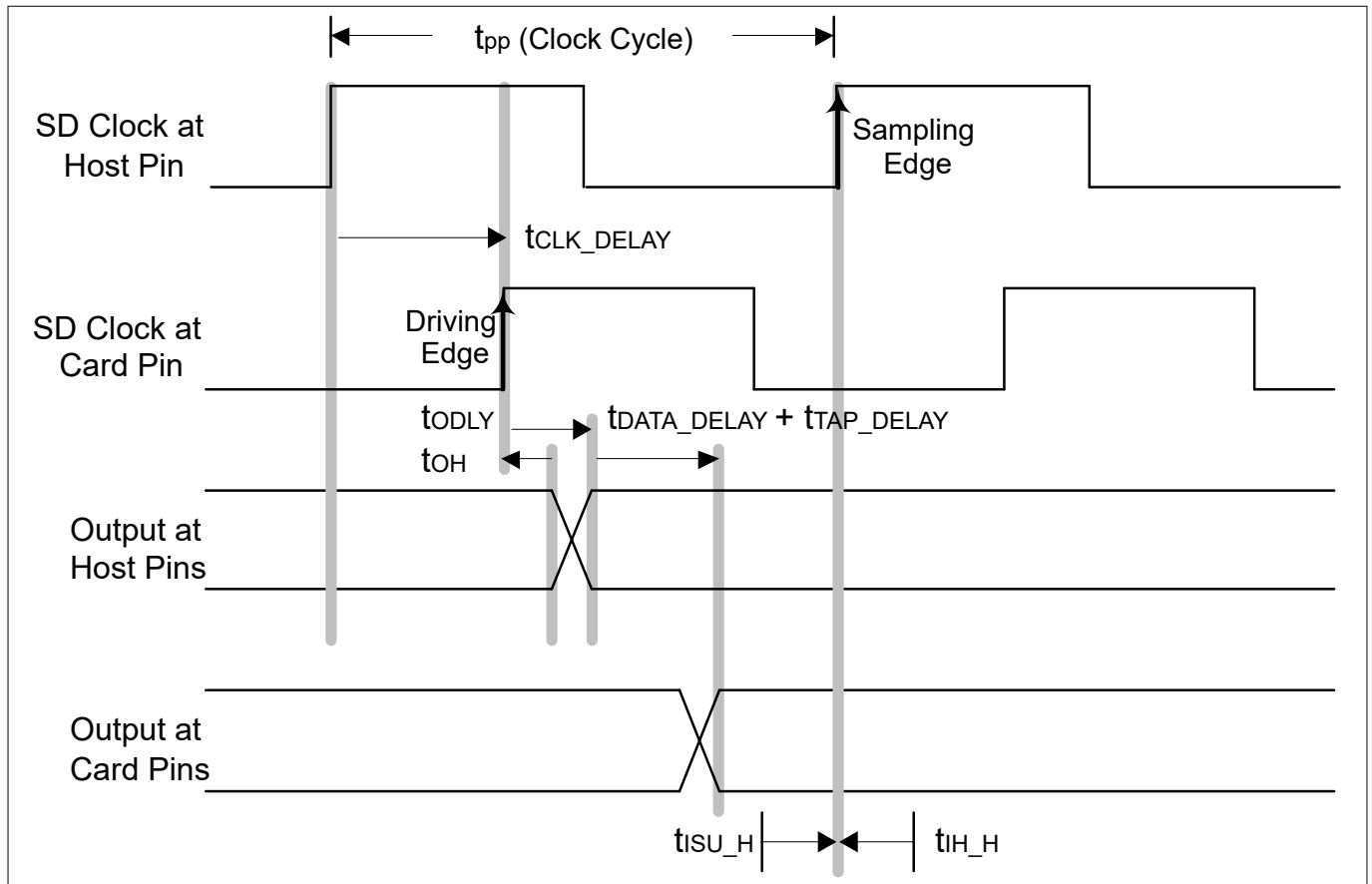


Figure 38 Full-Speed Input Path

3 Electrical Parameters

Full-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$\begin{aligned}
 t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} + t_{\text{ODLY}} + t_{\text{ISU_F}} &< 0.5 \times t_{\text{pp}} \\
 t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} &< 0.5 \times t_{\text{pp}} - t_{\text{ODLY}} - t_{\text{ISU_F}} - t_{\text{TAP_DELAY}} \\
 t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} &< 20 - 14 - 2 - t_{\text{TAP_DELAY}} \\
 t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} &< 4 - t_{\text{TAP_DELAY}}
 \end{aligned}
 \tag{5}$$

The data + clock delay can be up to 4 ns for a 40 ns clock cycle.

Full-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$\begin{aligned}
 t_{\text{CLK_DELAY}} + t_{\text{OH}} + t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} &> t_{\text{IH_F}} \\
 t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} &> t_{\text{IH_F}} - t_{\text{OH}} - t_{\text{TAP_DELAY}} \\
 t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} &> 2 - t_{\text{TAP_DELAY}}
 \end{aligned}
 \tag{6}$$

The data + clock delay must be greater than 2 ns if $t_{\text{TAP_DELAY}}$ is not used.

If the $t_{\text{TAP_DELAY}}$ is programmed to at least 2 ns, the data + clock delay must be greater than 0 ns (or less). This is always fulfilled.

AC Timing Specifications (High-Speed Mode)

Table 54 **SDMMC Timing for High-Speed Mode**

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Clock frequency in high speed transfer mode ($1/t_{\text{pp}}$)	$f_{\text{pp CC}}$	0	48	MHz	–
Clock cycle in high speed transfer mode	$t_{\text{pp CC}}$	20	–	ns	–
Clock low time	$t_{\text{WL CC}}$	7	–	ns	–
Clock high time	$t_{\text{WH CC}}$	7	–	ns	–
Clock rise time	$t_{\text{TLH CC}}$	–	3	ns	–
Clock fall time	$t_{\text{THL CC}}$	–	3	ns	–
Inputs setup to clock rising edge	$t_{\text{ISU_H SR}}$	2	–	ns	–
Inputs hold after clock rising edge	$t_{\text{IH_H SR}}$	2	–	ns	–
Outputs valid time in high speed mode	$t_{\text{ODLY_H CC}}$	–	14	ns	–
Outputs hold time in high speed mode	$t_{\text{OH_H CC}}$	2	–	ns	–

3 Electrical Parameters

Table 55 SD Card Bus Timing for High-Speed Mode¹⁾

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
SD card input setup time	t_{ISU}	6	–	ns	–
SD card input hold time	t_{IH}	2	–	ns	–
SD card output valid time	t_{ODLY}	–	14	ns	–
SD card output hold time	t_{OH}	2.5	–	ns	–

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

High-Speed Output Path (Write)

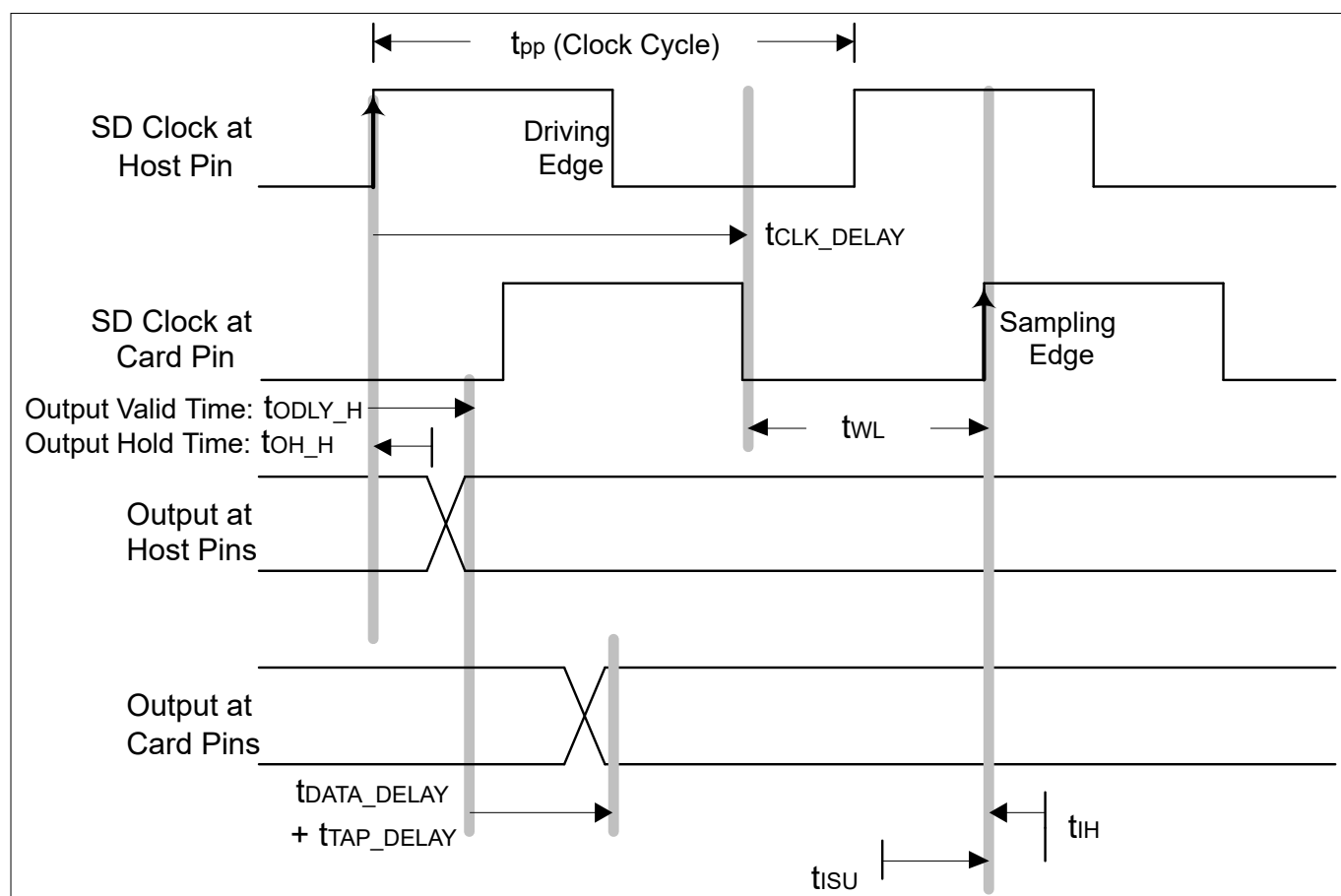


Figure 39 High-Speed Output Path

3 Electrical Parameters

High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

$$t_{\text{ODLY_H}} + t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} + t_{\text{ISU}} < t_{\text{WL}} \quad (7)$$

With clock delay:

$$t_{\text{ODLY_H}} + t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} + t_{\text{ISU}} < t_{\text{WL}} + t_{\text{CLK_DELAY}} \quad (8)$$

$$\begin{aligned} t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} - t_{\text{CLK_DELAY}} &< t_{\text{WL}} - t_{\text{ISU}} - t_{\text{ODLY_H}} \\ t_{\text{DATA_DELAY}} - t_{\text{CLK_DELAY}} &< t_{\text{WL}} - t_{\text{ISU}} - t_{\text{ODLY_H}} - t_{\text{TAP_DELAY}} \\ t_{\text{DATA_DELAY}} - t_{\text{CLK_DELAY}} &< 10 - 6 - 14 - t_{\text{TAP_DELAY}} \\ t_{\text{DATA_DELAY}} - t_{\text{CLK_DELAY}} &< -10 - t_{\text{TAP_DELAY}} \end{aligned} \quad (9)$$

The data delay is less than the clock delay by at least 10 ns in the ideal case where $t_{\text{WL}} = 10$ ns.

High-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$\begin{aligned} t_{\text{CLK_DELAY}} &< t_{\text{WL}} + t_{\text{OH_H}} + t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} - t_{\text{IH}} \\ t_{\text{CLK_DELAY}} - t_{\text{DATA_DELAY}} &< t_{\text{WL}} + t_{\text{OH_H}} + t_{\text{TAP_DELAY}} - t_{\text{IH}} \\ t_{\text{CLK_DELAY}} - t_{\text{DATA_DELAY}} &< 10 + 2 + t_{\text{TAP_DELAY}} - 2 \\ t_{\text{CLK_DELAY}} - t_{\text{DATA_DELAY}} &< 10 + t_{\text{TAP_DELAY}} \end{aligned} \quad (10)$$

The clock can be delayed versus data up to 13.2 ns (external delay line) in ideal case of $t_{\text{WL}} = 10$ ns, with maximum $t_{\text{TAP_DELAY}} = 3.2$ ns programmed.

3 Electrical Parameters

High-Speed Input Path (Read)

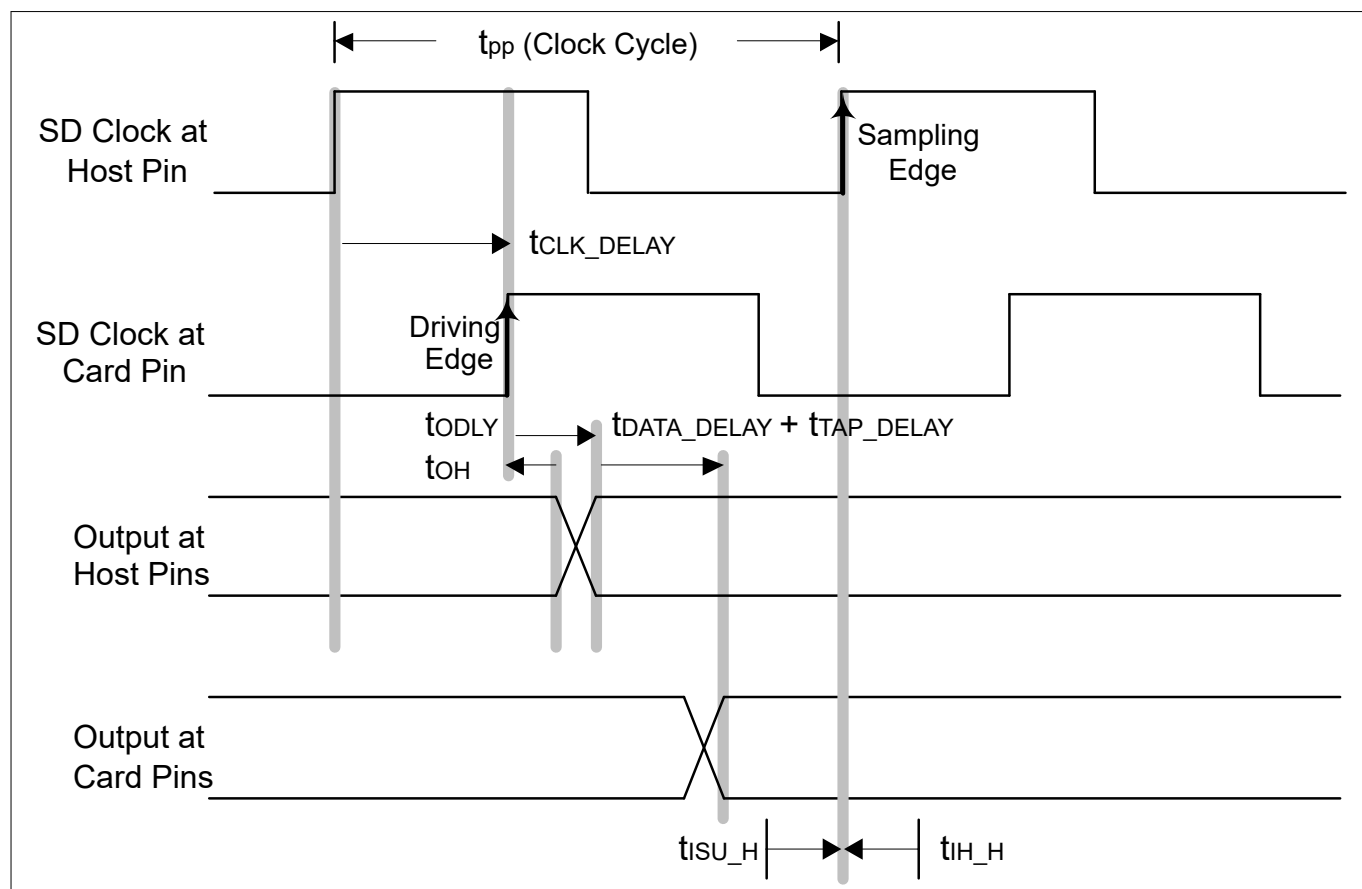


Figure 40 High-Speed Input Path

3 Electrical Parameters

High-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$\begin{aligned}t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} + t_{\text{ODLY}} + t_{\text{ISU_H}} &< t_{\text{pp}} \\t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} &< t_{\text{pp}} - t_{\text{ODLY}} - t_{\text{ISU_H}} - t_{\text{TAP_DELAY}} \\t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} &< 20 - 14 - 2 - t_{\text{TAP_DELAY}} \\t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} &< 4 - t_{\text{TAP_DELAY}}\end{aligned}\tag{11}$$

The data + clock delay can be up to 4 ns for a 20 ns clock cycle.

High-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$\begin{aligned}t_{\text{CLK_DELAY}} + t_{\text{OH}} + t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} &> t_{\text{IH_H}} \\t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} &> t_{\text{IH_H}} - t_{\text{OH}} - t_{\text{TAP_DELAY}} \\t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} &> 2 - 2.5 - t_{\text{TAP_DELAY}} \\t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} &> -0.5 - t_{\text{TAP_DELAY}}\end{aligned}\tag{12}$$

The data + clock delay must be greater than -0.5 ns for a 20 ns clock cycle. This is always fulfilled.

3 Electrical Parameters

3.3.10 EBU Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and $C_L = 16 \text{ pF}$.

3.3.10.1 EBU Asynchronous Timing

Note: For each timing, the accumulated PLL jitter must be added separately.

Table 56 Common Timing Parameters for all Asynchronous Timings

Parameter			Symbol	Limit Values		Unit	Edge Setting
				Min.	Max.		
Pulse width deviation from the ideal programmed width due to the A2 pad asymmetry, strong driver mode, rise delay - fall delay. $C_L = 16 \text{ pF}$.		CC	t_a	-1	1.5	ns	sharp
				-2	1		medium
AD(24:16) output delay	to $\overline{\text{ADV}}$ rising edge, multiplexed read/write	CC	t_{13}	-5.5	2		–
AD(24:16) output delay		CC	t_{14}	-5.5	2		–

Read Timings

Table 57 Asynchronous Read Timing, Multiplexed and Demultiplexed

Parameter			Symbol	Limit Values		Unit
				Min.	Max.	
A(24:16) output delay	to $\overline{\text{RD}}$ rising edge, deviation from the ideal programmed value.	CC	t_0	-2.5	2.5	ns
A(24:16) output delay		CC	t_1	-2.5	2.5	
$\overline{\text{CS}}$ rising edge		CC	t_2	-2	2.5	
$\overline{\text{ADV}}$ rising edge		CC	t_3	-1.5	4.5	
$\overline{\text{BC}}$ rising edge		CC	t_4	-2.5	2.5	
$\overline{\text{WAIT}}$ input setup		SR	t_5	12	–	
$\overline{\text{WAIT}}$ input hold		SR	t_6	0	–	
Data input setup		SR	t_7	12	–	
Data input hold		SR	t_8	0	–	
RD/ $\overline{\text{WR}}$ output delay		CC	t_9	-2.5	1.5	

3 Electrical Parameters

Multiplexed Read Timing

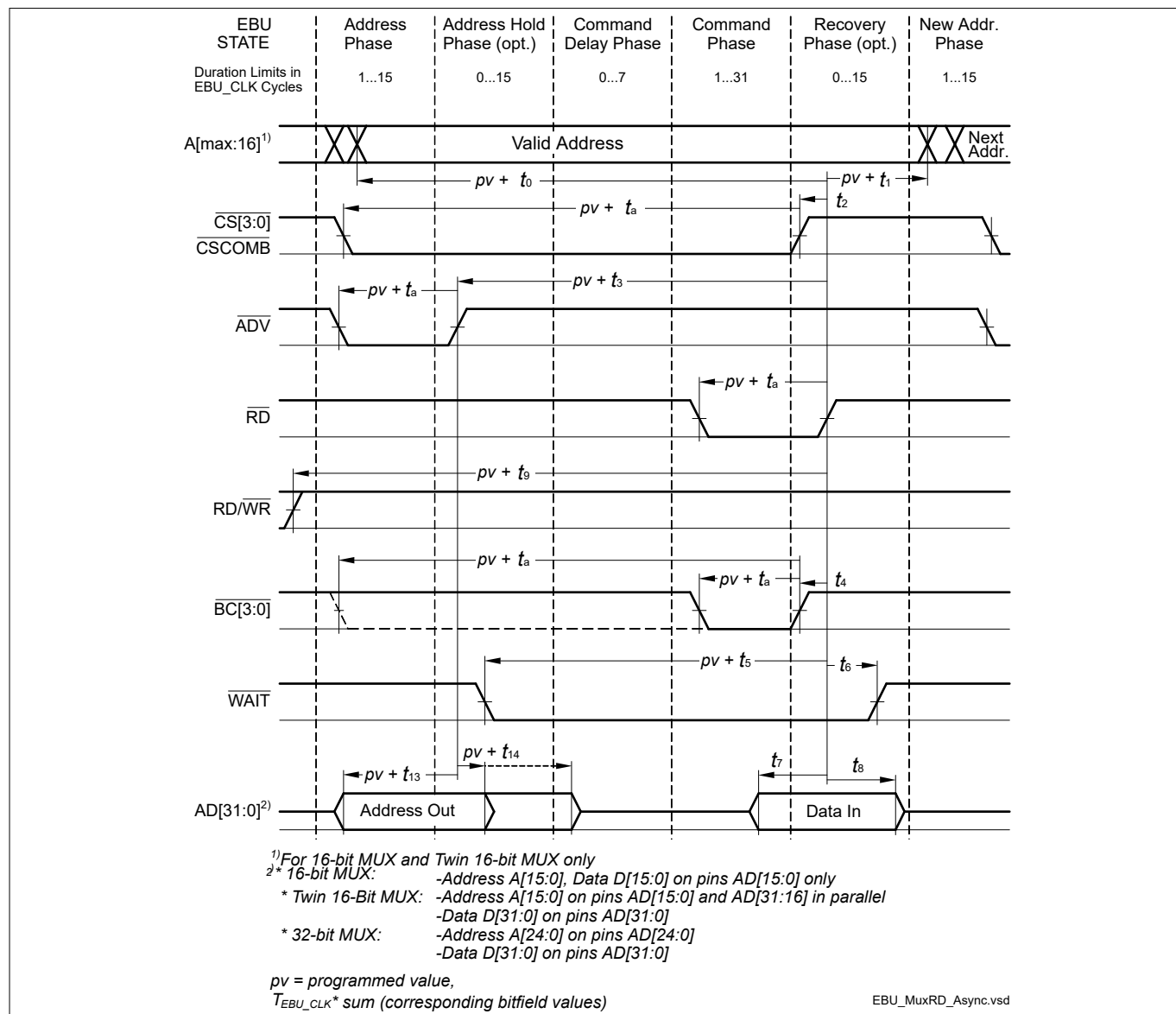


Figure 41 **Multiplexed Read Access**

3 Electrical Parameters

Demultiplexed Read Timing

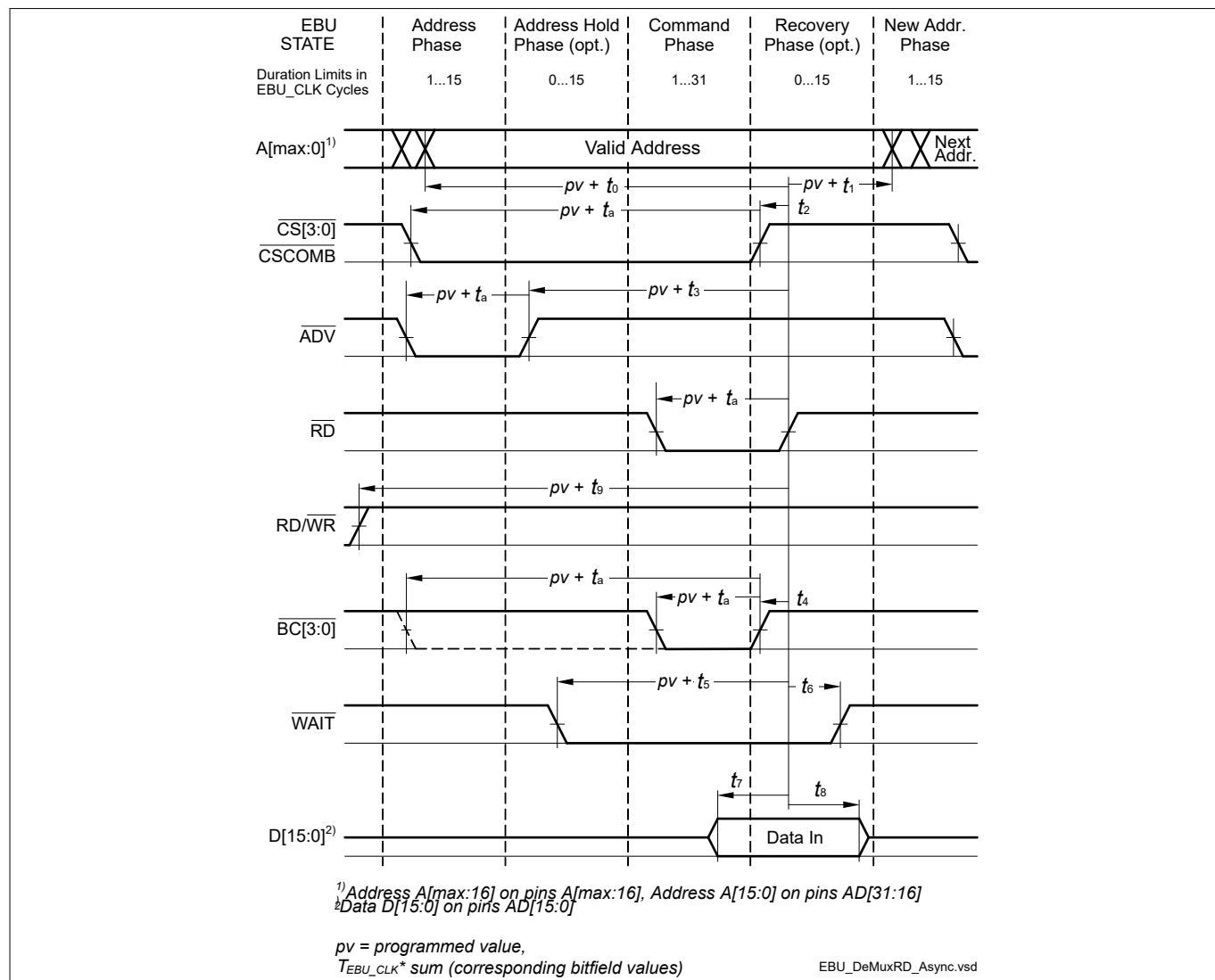


Figure 42 Demultiplexed Read Access

3 Electrical Parameters

Write Timing

Table 58 Asynchronous Write Timing, Multiplexed and Demultiplexed

Parameter			Symbol	Limit Values		Unit
				Min.	Max.	
A(24:0) output delay	to RD/ $\overline{\text{WR}}$ rising edge, deviation from the ideal programmed value.	CC	t_{30}	-2.5	2.5	ns
A(24:0) output delay		CC	t_{31}	-2.5	2.5	
$\overline{\text{CS}}$ rising edge		CC	t_{32}	-2	2	
$\overline{\text{ADV}}$ rising edge		CC	t_{33}	-2	4.5	
$\overline{\text{BC}}$ rising edge		CC	t_{34}	-2.5	2	
$\overline{\text{WAIT}}$ input setup		SR	t_{35}	12	–	
$\overline{\text{WAIT}}$ input hold		SR	t_{36}	0	–	
Data output delay		CC	t_{37}	-5.5	2	
Data output delay		CC	t_{38}	-5.5	2	
RD/ $\overline{\text{WR}}$ output delay		CC	t_{39}	-2.5	1.5	

3 Electrical Parameters

Multiplexed Write Timing

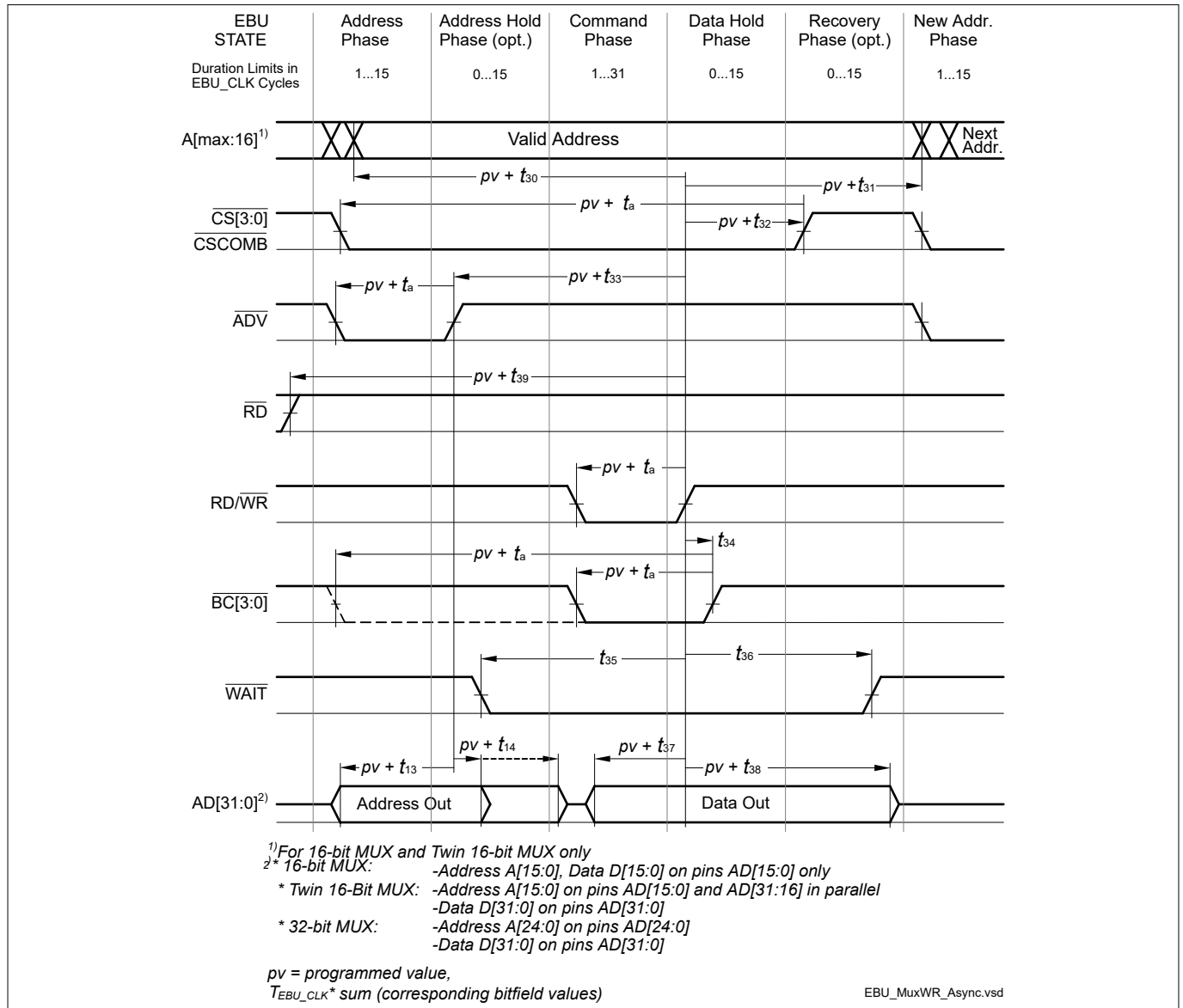


Figure 43 **Multiplexed Write Access**

3 Electrical Parameters

Demultiplexed Write Timing

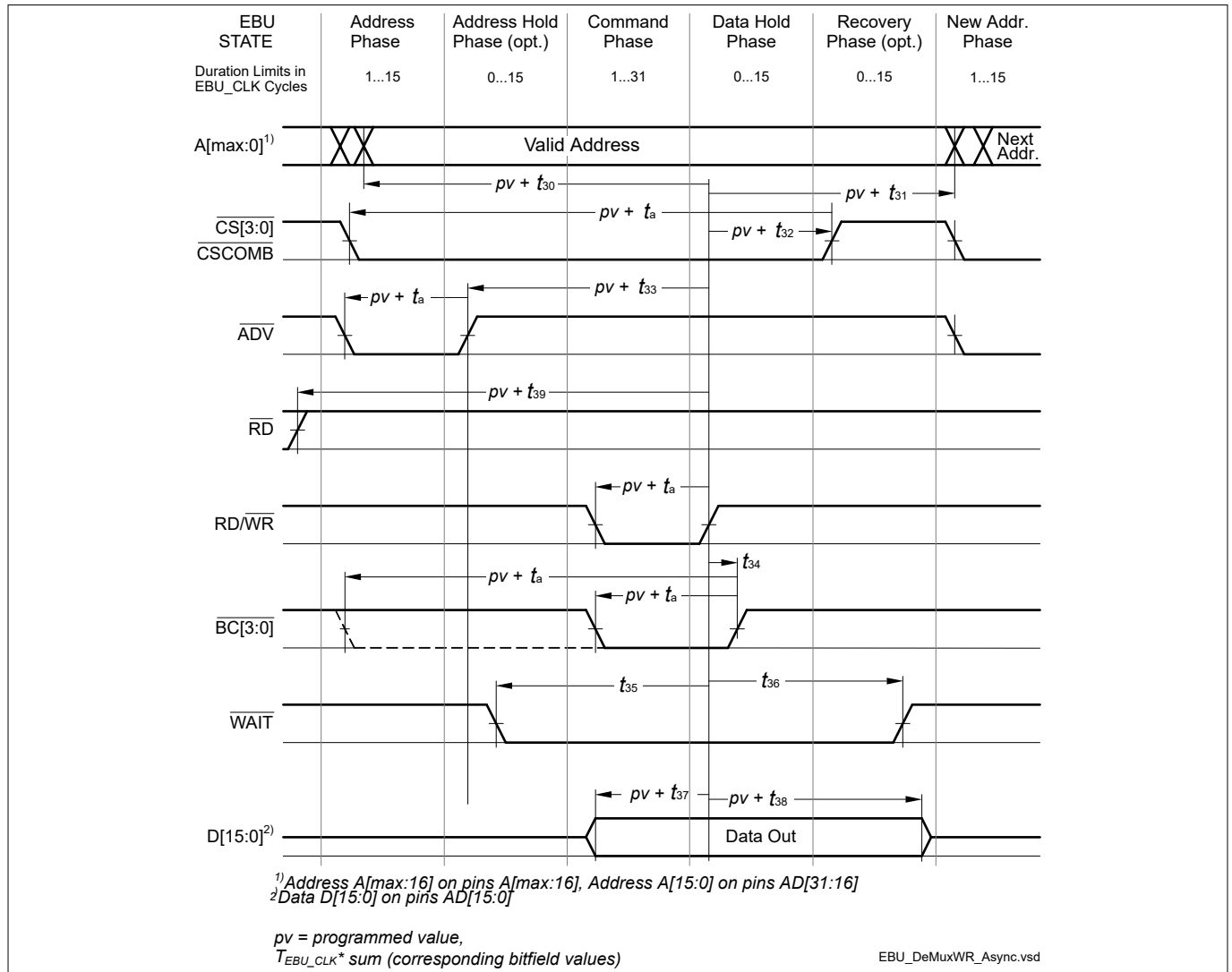


Figure 44 **Demultiplexed Write Access**

3 Electrical Parameters

3.3.10.2 EBU Burst Mode Access Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and $C_L = 16 \text{ pF}$.

Table 59 EBU Burst Mode Read/Write Access Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	$t_{10} \text{ CC}$	-2	–	2	ns	–
$\overline{\text{RD}}$ and $\overline{\text{WR}}$ active/inactive after BFCLKO active edge ¹⁾	$t_{12} \text{ CC}$	-2	–	2	ns	–
$\overline{\text{CSx}}$ output delay from BFCLKO active edge ¹⁾	$t_{21} \text{ CC}$	-2.5	–	1.5	ns	–
$\overline{\text{ADV}}$ active/inactive after BFCLKO active edge ²⁾	$t_{22} \text{ CC}$	-2	–	2	ns	–
$\overline{\text{BAA}}$ active/inactive after BFCLKO active edge ²⁾	$t_{22a} \text{ CC}$	-2.5	–	1.5	ns	–
Data setup to BFCLKI rising edge ³⁾	$t_{23} \text{ SR}$	3	–	–	ns	–
Data hold from BFCLKI rising edge ³⁾	$t_{24} \text{ SR}$	0	–	–	ns	–
$\overline{\text{WAIT}}$ setup (low or high) to BFCLKI rising edge ³⁾	$t_{25} \text{ SR}$	3	–	–	ns	–
$\overline{\text{WAIT}}$ hold (low or high) from BFCLKI rising edge ³⁾	$t_{26} \text{ SR}$	0	–	–	ns	–

- 1) An active edge can be a rising or falling edge, depending on the settings of bits BFCN.EBSE/ECSE and the clock divider ratio. Negative minimum values for these parameters mean that the last data read during a burst may be corrupted. However, with clock feedback enabled, this value is an oversampling not required for the internal bus transaction, and will be discarded.
- 2) This parameter is valid for BUSCONx.EBSE = 1 and BUSAPx.EXTCLK = 00_B.
 For BUSCONx.EBSE = 1 and other values of BUSAPx.EXTCLK, ADV and BAA will be delayed by 1/2 of the internal bus clock period $T_{\text{CPU}} = 1/f_{\text{CPU}}$.
 For BUSCONx. EBSE = 0 and BUSAPx.EXTCLK = 11_B, add 2 internal bus clock periods. For BUSCONx. EBSE = 0 and other values of BUSAPx.EXTCLK, add 1 internal bus clock period.
- 3) If the clock feedback is not enabled, the input signals are latched using the internal clock in the same way as for asynchronous access. Thus, t_5 , t_6 , t_7 and t_8 from the asynchronous timing apply.

3 Electrical Parameters

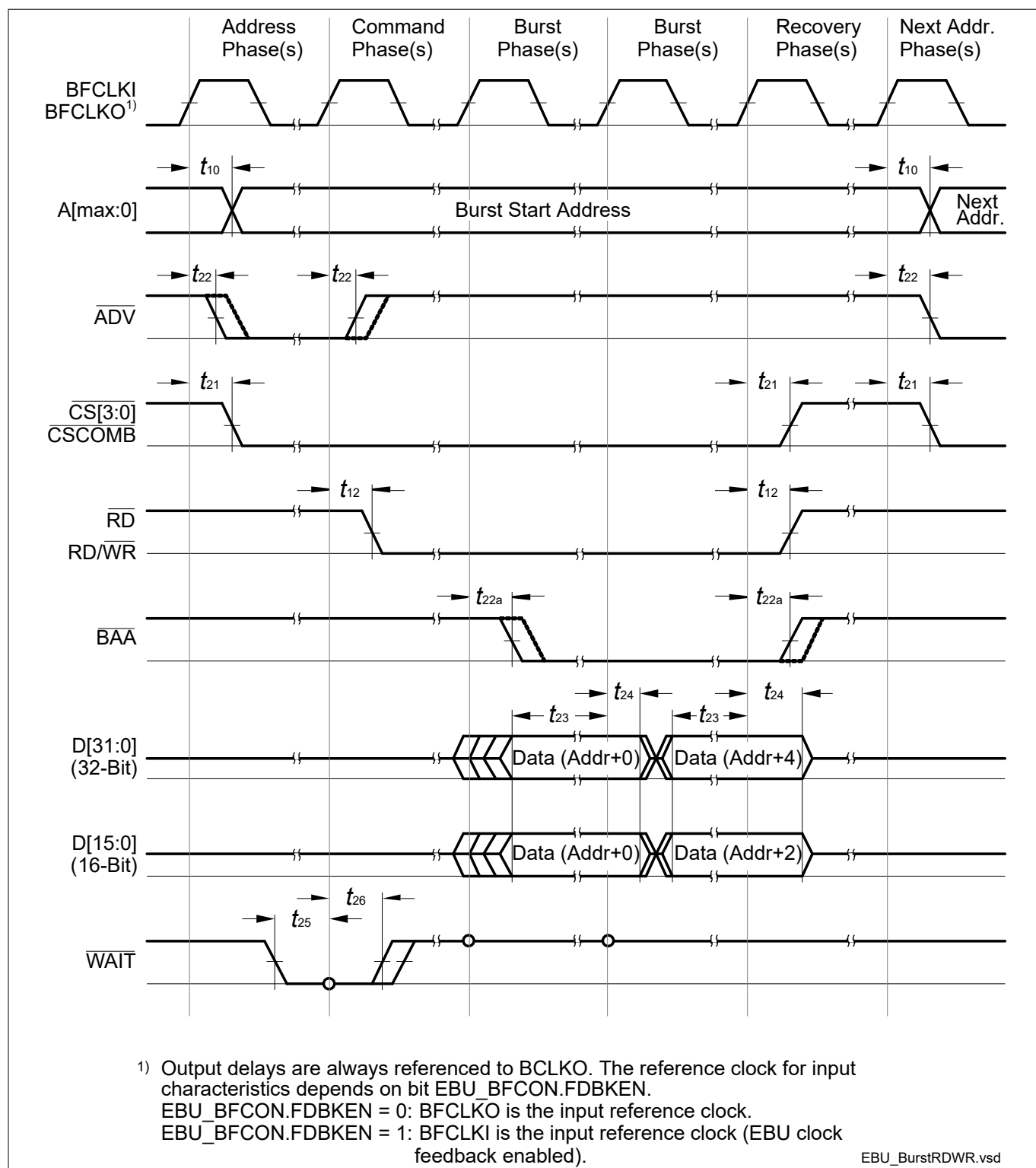


Figure 45 EBU Burst Mode Read/Write Access Timing

3 Electrical Parameters

3.3.10.3 EBU Arbitration Signal Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 60 EBU Arbitration Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	t_1 CC	–	–	16	ns	$C_L = 50$ pF
Data setup to BFCLKO falling edge	t_2 SR	11	–	–	ns	–
Data hold from BFCLKO falling edge	t_3 SR	2	–	–	ns	–

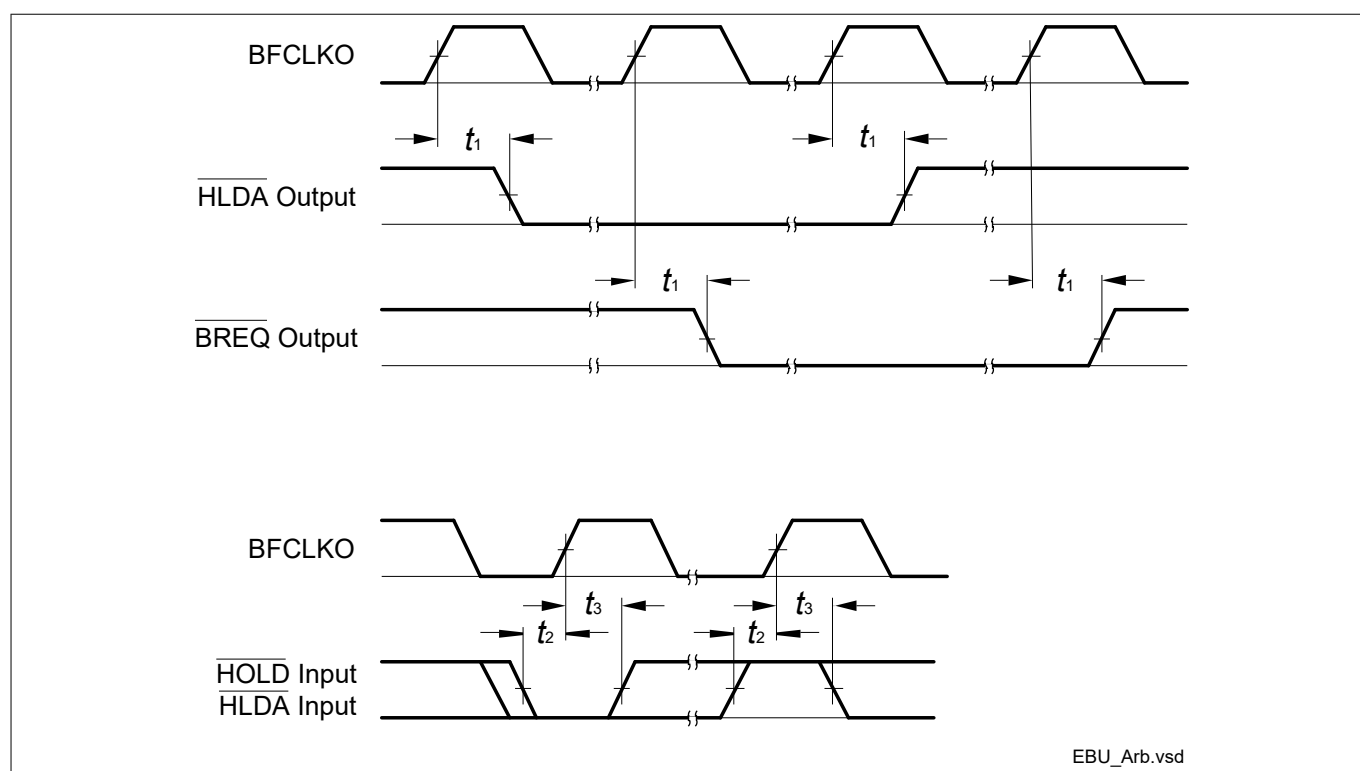


Figure 46 EBU Arbitration Signal Timing

3 Electrical Parameters

3.3.10.4 EBU SDRAM Access Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and $C_L = 16 \text{ pF}$.

Note: With $\text{EBU_CLC.SYNC} = 1_B$ frequency must be limited to $f_{\text{CPU}} = 120 \text{ MHz}$.

Table 61 EBU SDRAM Access SDCLKO Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
SDCLKO period	$t_1 \text{ CC}$	12.5	–	–	ns	–
SDCLKO high time	$t_2 \text{ SR}$	5.5	–	–	ns	–
SDCLKO low time	$t_3 \text{ SR}$	3.75	–	–	ns	–
SDCLKO rise time	$t_4 \text{ SR}$	–	–	3.0	ns	–
SDCLKO fall time	$t_5 \text{ SR}$	–	–	3.0	ns	–

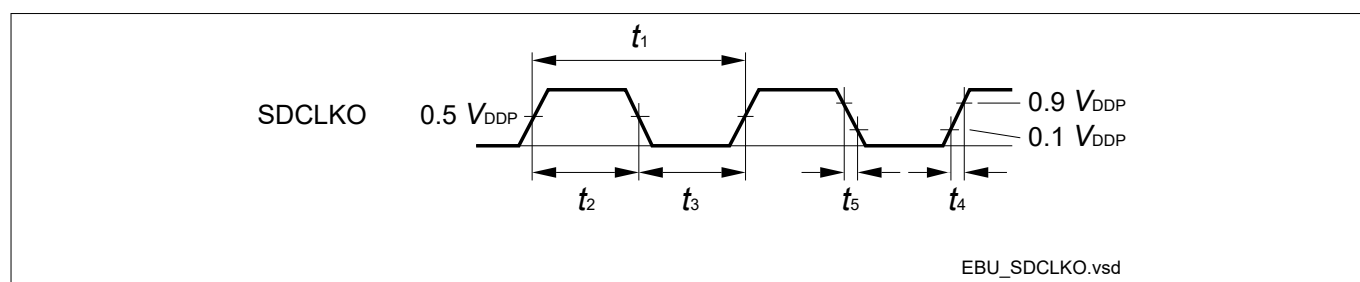


Figure 47 EBU SDRAM Access CLKOUT Timing

3 Electrical Parameters

Table 62 EBU SDRAM Access Signal Timing Parameters

Parameter			Symbol	Limit Values		Unit
				Min.	Max.	
A(15:0) output valid	from SDCLKO low-to-high transition	CC	t_6	–	9	ns
A(15:0) output hold		CC	t_7	3	–	
$\overline{CS}(3:0)$ low		CC	t_8	–	9	
$\overline{CS}(3:0)$ high		CC	t_9	3	–	
$\overline{RAS}$ low		CC	t_{10}	–	9	
$\overline{RAS}$ high		SR	t_{11}	3	–	
$\overline{CAS}$ low		SR	t_{12}	–	9	
$\overline{CAS}$ high		CC	t_{13}	3	–	
RD/ $\overline{WR}$ low		CC	t_{14}	–	9	
RD/ $\overline{WR}$ high		CC	t_{15}	3	–	
$\overline{BC}(3:0)$ low		CC	t_{16}	–	9	
$\overline{BC}(3:0)$ high		CC	t_{17}	3	–	
D(15:0) output valid		CC	t_{18}	–	9	
D(15:0) output hold		CC	t_{19}	3	–	
CKE output valid ¹⁾		CC	t_{22}	–	7	
CKE output hold ¹⁾		CC	t_{23}	2	–	
D(15:0) input hold		SR	t_{21}	3	–	
D(15:0) input setup to SDCLKO low-to-high transition		SR	t_{20}	4	–	

1) Not depicted in the read and write access timing figures below.

3 Electrical Parameters

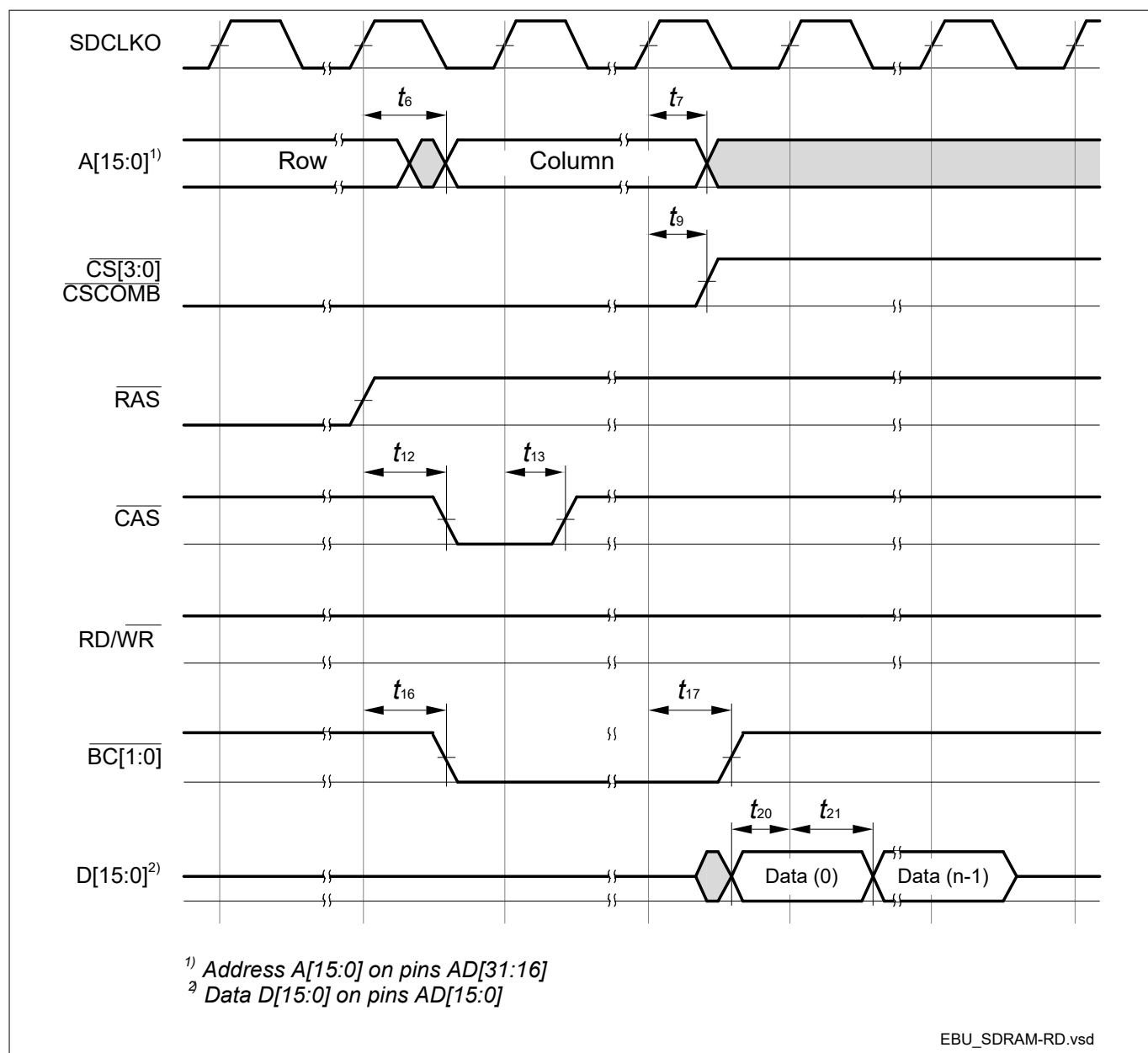


Figure 48 EBU SDRAM Read Access Timing

3 Electrical Parameters

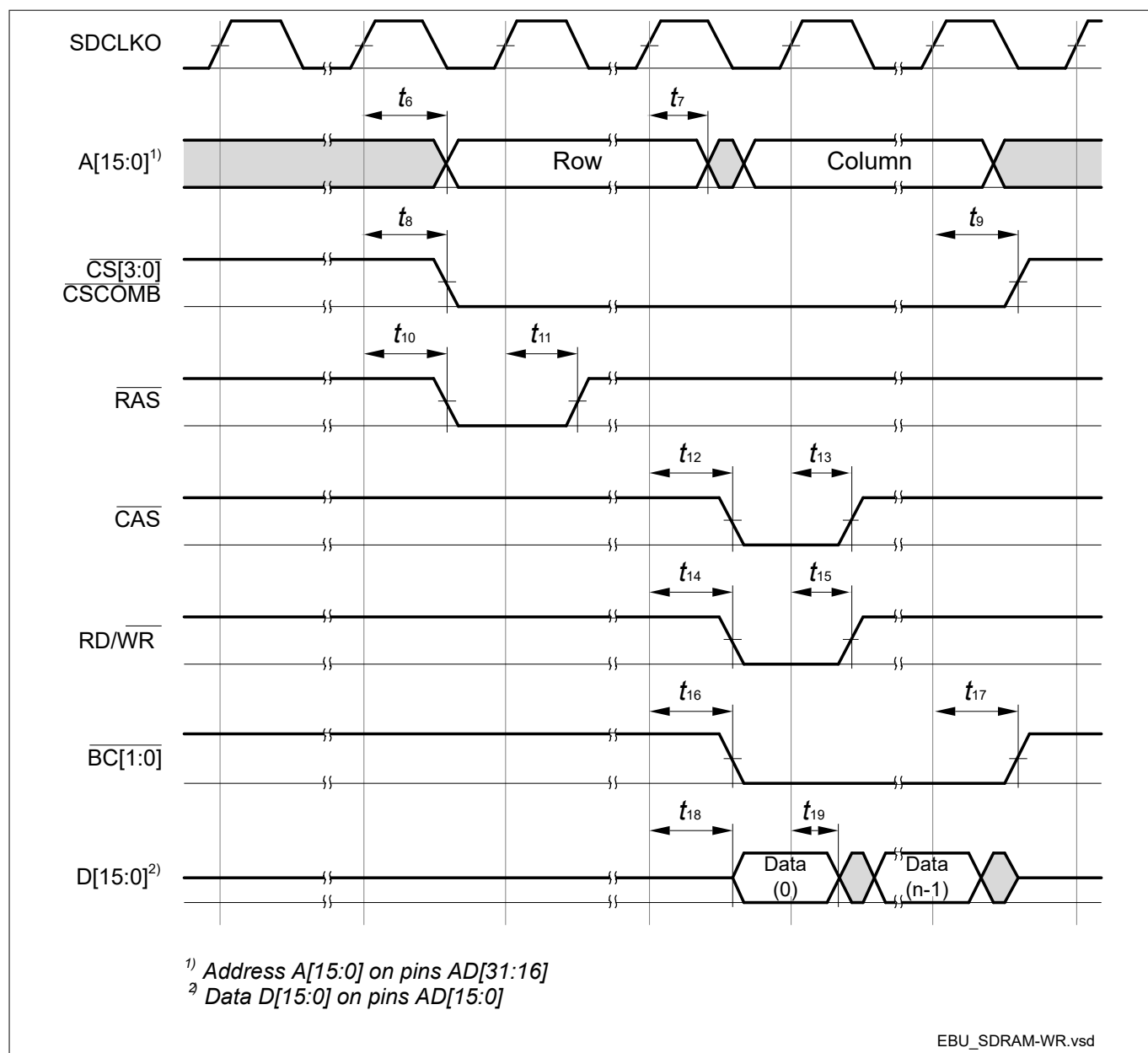


Figure 49 EBU SDRAM Write Access Timing

3 Electrical Parameters

3.3.11 USB Interface Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 63 USB Timing Parameters (operating conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Rise time	t_R CC	4	–	20	ns	$C_L = 50$ pF
Fall time	t_F CC	4	–	20	ns	$C_L = 50$ pF
Rise/Fall time matching	t_R/t_F CC	90	–	111.11	%	$C_L = 50$ pF
Crossover voltage	V_{CRS} CC	1.3	–	2.0	V	$C_L = 50$ pF

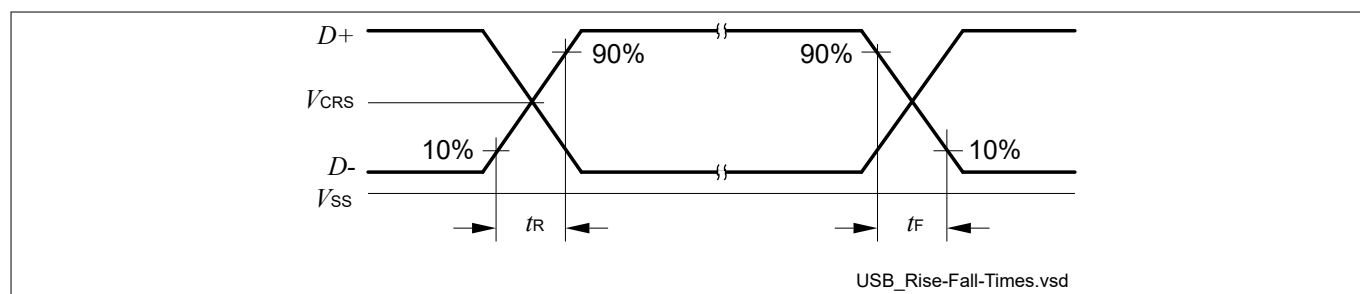


Figure 50 USB Signal Timing

3.3.12 Ethernet Interface (ETH) Characteristics

For proper operation of the Ethernet Interface it is required that $f_{SYS} \geq 100$ MHz.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.12.1 ETH Measurement Reference Points

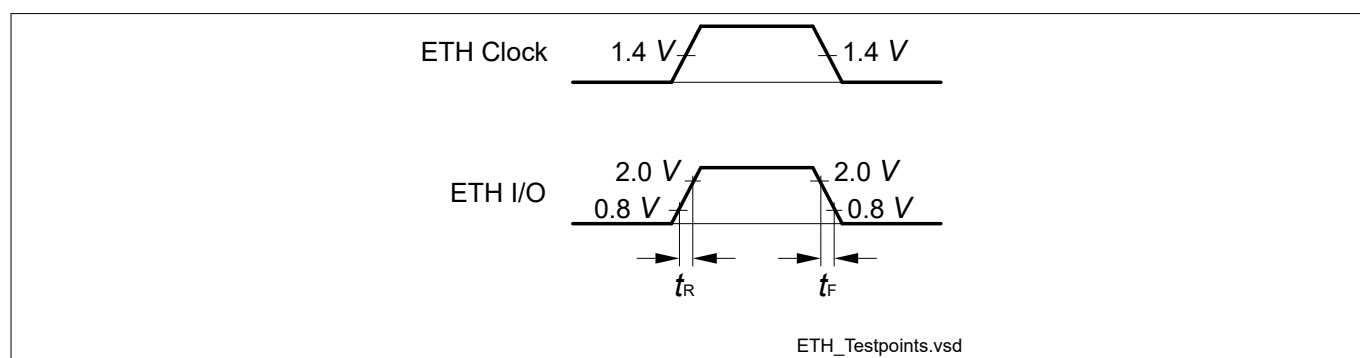


Figure 51 ETH Measurement Reference Points

3 Electrical Parameters

3.3.12.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 64 ETH Management Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
ETH_MDC period	t_1 CC	400	–	–	ns	$C_L = 25$ pF
ETH_MDC high time	t_2 CC	160	–	–	ns	
ETH_MDC low time	t_3 CC	160	–	–	ns	
ETH_MDIO setup time (output)	t_4 CC	10	–	–	ns	
ETH_MDIO hold time (output)	t_5 CC	10	–	–	ns	
ETH_MDIO data valid (input)	t_6 SR	0	–	300	ns	

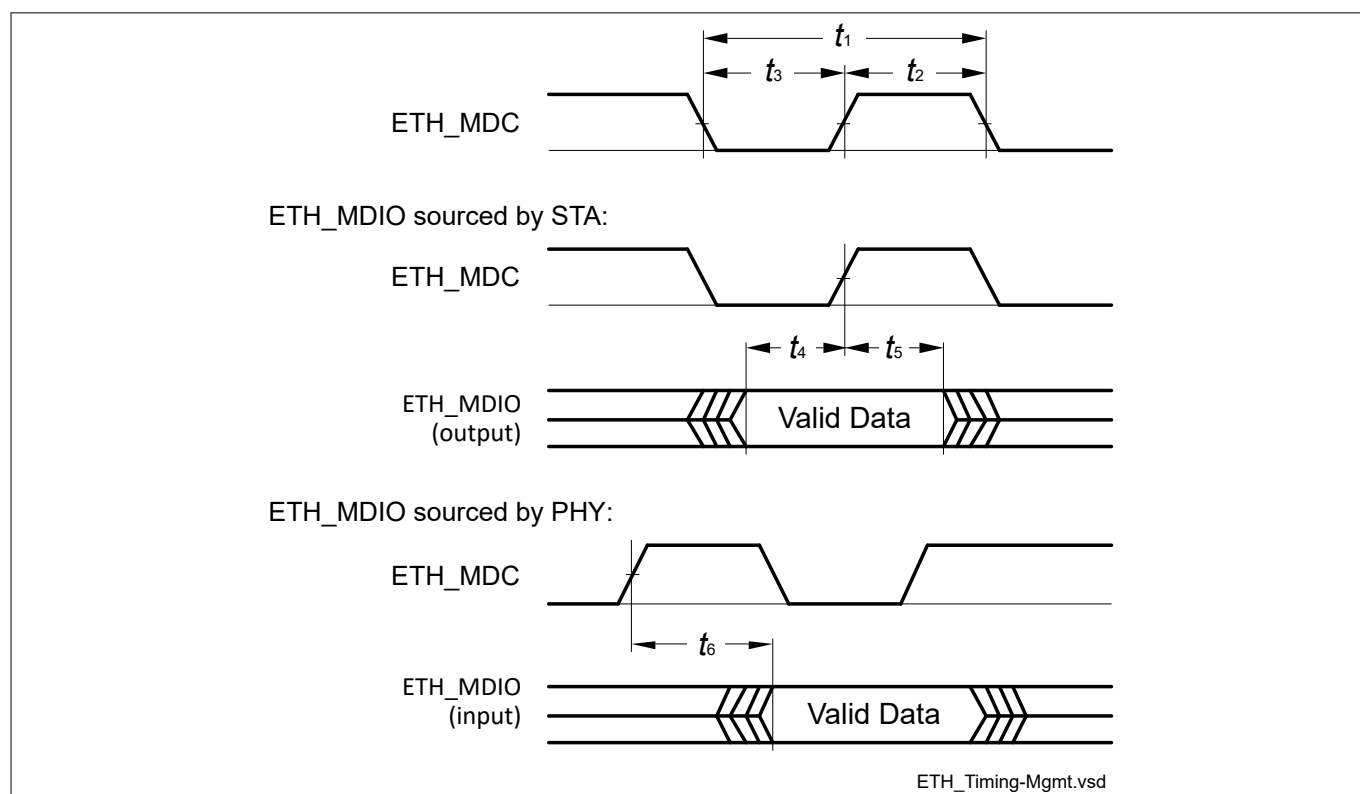


Figure 52 ETH Management Signal Timing

3 Electrical Parameters

3.3.12.3 ETH MII Parameters

In the following, the parameters of the MII (Media Independent Interface) are described.

Table 65 ETH MII Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Clock period, 10 Mbps	t_7 SR	400	–	–	ns	$C_L = 25$ pF
Clock high time, 10 Mbps	t_8 SR	140	–	260	ns	
Clock low time, 10 Mbps	t_9 SR	140	–	260	ns	
Clock period, 100 Mbps	t_7 SR	40	–	–	ns	
Clock high time, 100 Mbps	t_8 SR	14	–	26	ns	
Clock low time, 100 Mbps	t_9 SR	14	–	26	ns	
Input setup time	t_{10} SR	10	–	–	ns	
Input hold time	t_{11} SR	10	–	–	ns	
Output valid time	t_{12} CC	0	–	25	ns	

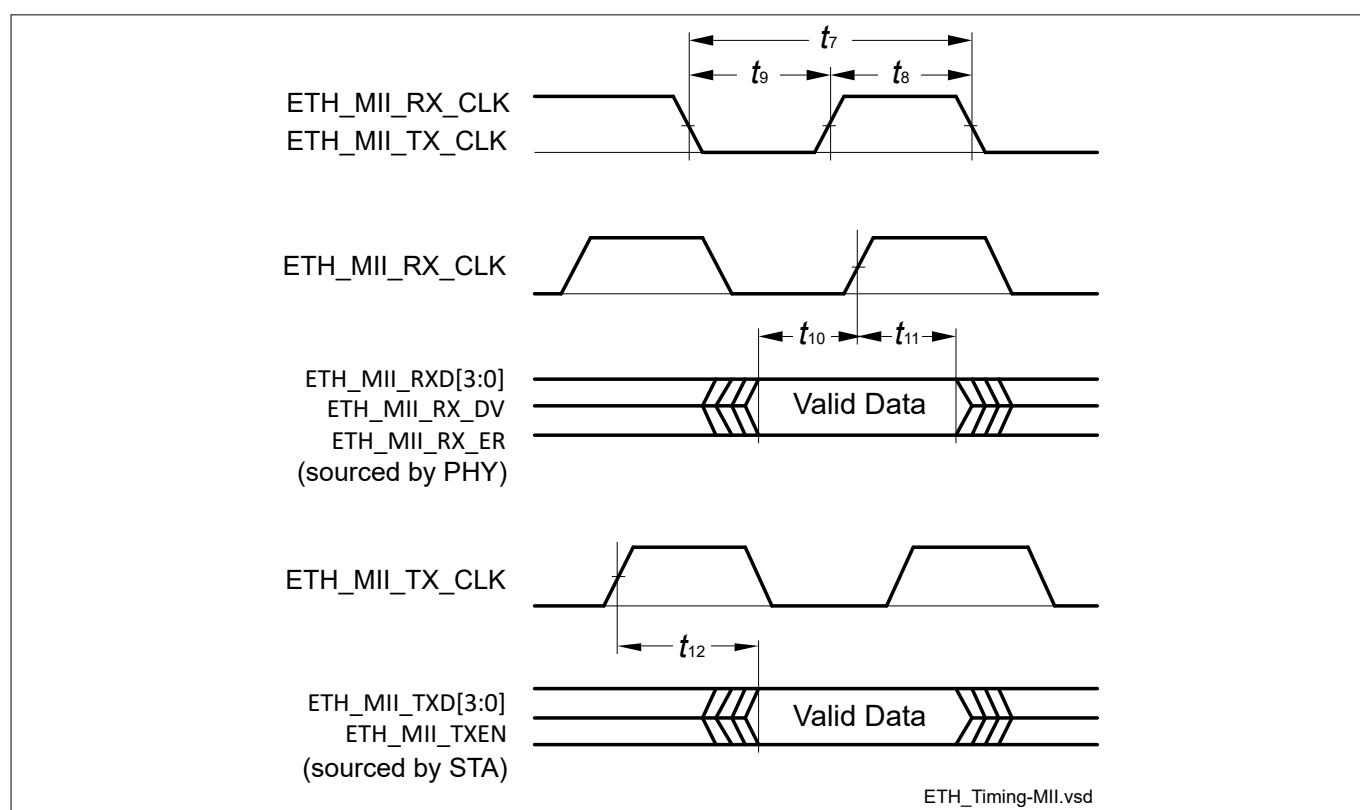


Figure 53 ETH MII Signal Timing

3 Electrical Parameters

3.3.12.4 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

Table 66 ETH RMII Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13} SR	20	–	–	ns	$C_L = 25 \text{ pF}; 50 \text{ ppm}$
ETH_RMII_REF_CL clock high time	t_{14} SR	7	–	13	ns	$C_L = 25 \text{ pF}$
ETH_RMII_REF_CL clock low time	t_{15} SR	7	–	13	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS setup time	t_{16} SR	4	–	–	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS hold time	t_{17} SR	2	–	–	ns	
ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid	t_{18} CC	4	–	15	ns	

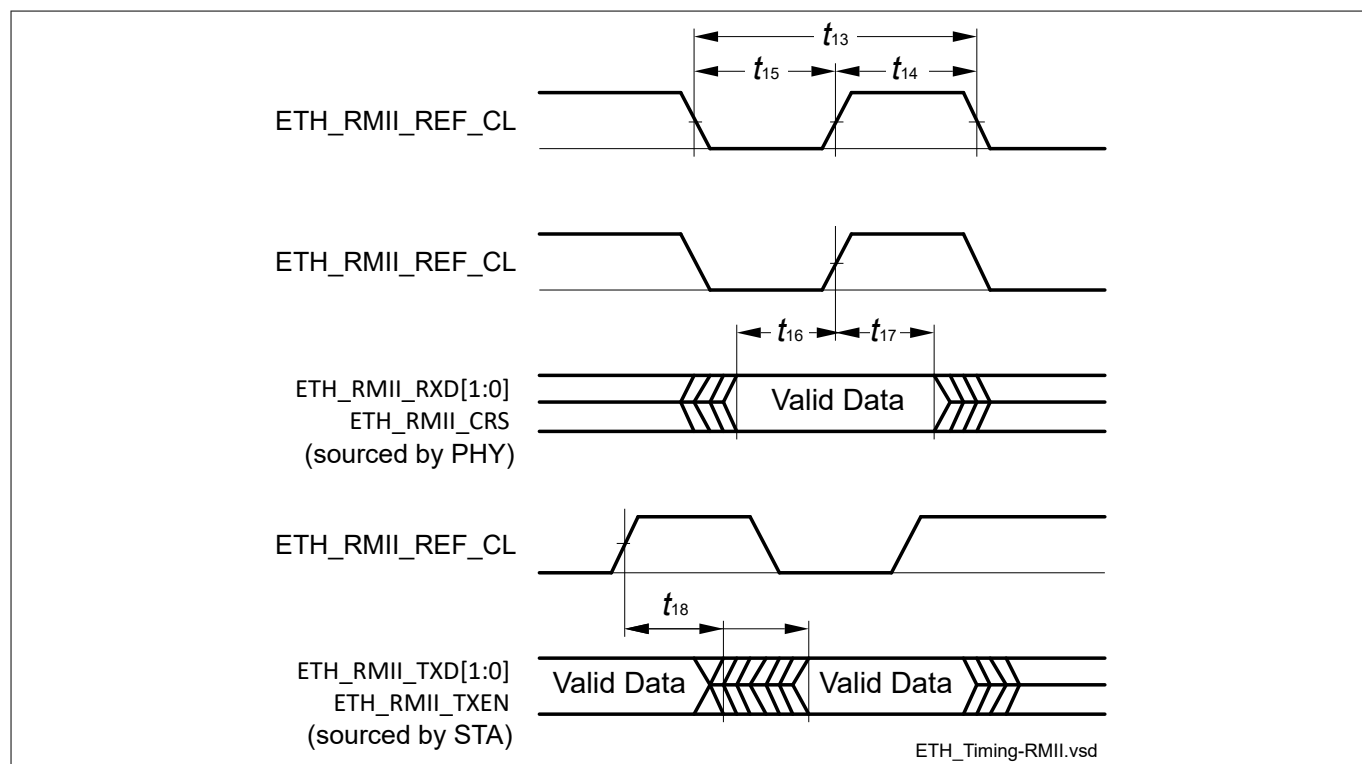


Figure 54 ETH RMII Signal Timing

3 Electrical Parameters

3.3.13 EtherCAT (ECAT) Characteristics

3.3.13.1 ECAT Measurement Reference Points

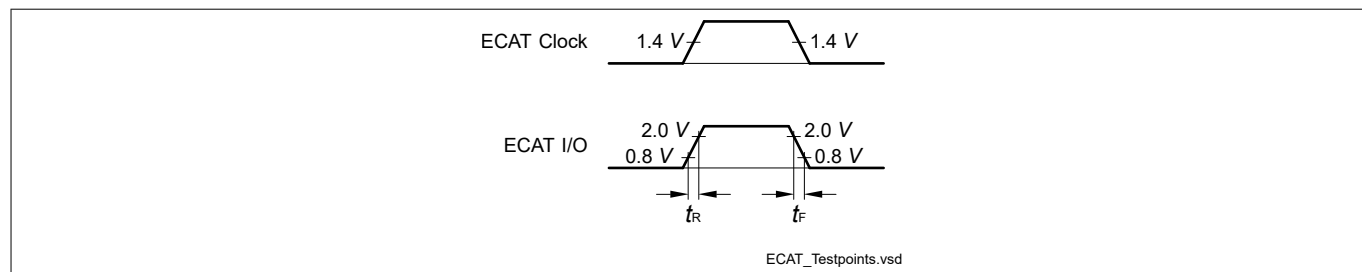


Figure 55 Measurement Reference Points

3.3.13.2 ETH Management Signal Parameters (MCLK, MDIO)

Table 67 ECAT Management Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
ECAT_MCLK period	$t_{\text{MCLK CC}}$	–	400	–	ns	IEEE802.3 requirement (2.5 MHz) $C_L = 25 \text{ pF}$
ECAT_MCLK high time	$t_{\text{MCLK}_h \text{ CC}}$	160	–	–	ns	
ECAT_MCLK low time	$t_{\text{MCLK}_l \text{ CC}}$	160	–	–	ns	
ECAT_MDIO setup time (output)	$t_{\text{D_setup CC}}$	10	–	–	ns	
ECAT_MDIO hold time (output)	$t_{\text{D_hold CC}}$	10	–	–	ns	
ECAT_MDIO data valid (input)	$t_{\text{D_valid SR}}$	0	–	300	ns	

3 Electrical Parameters

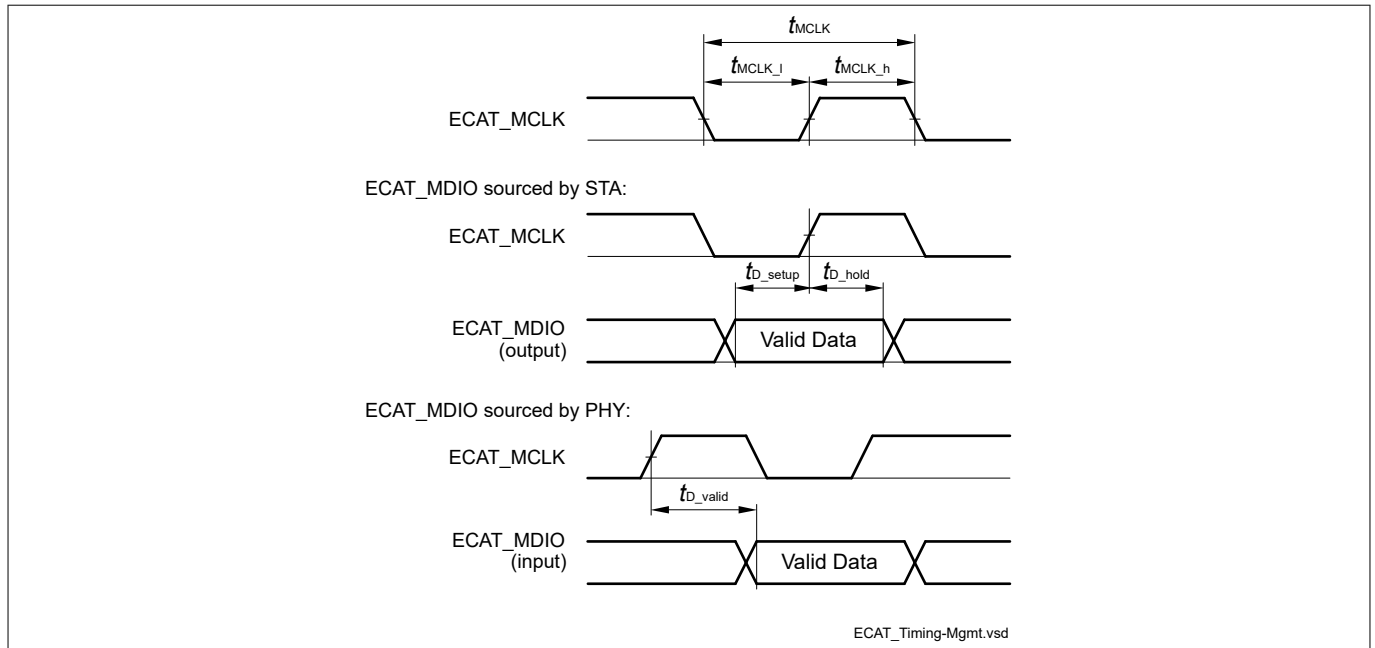


Figure 56 **ECAT Management Signal Timing**

3.3.13.3 MII Timing TX Characteristics

Table 68 **ETH MII TX Signal Timing Parameters**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
PHY_CLK25, TX_CLK period	t_{TX_CLK} SR	–	40	–	ns	
Delay between PHY clock source PHY_CLK25 and TX_CLK output of the PHY	t_{PHY_delay} SR	–	–	–	ns	PHY dependent
PHY setup requirement: TXEN/TXD[3:0] with respect to TX_CLK	t_{TX_setup} SR	15	–	0	ns	PHY dependent IEEE802.3 limit is 15 ns
PHY hold requirement: TXEN/TXD[3:0] with respect to TX_CLK	t_{TX_hold} CC	0	–	25	ns	PHY dependent IEEE802.3 limit is 0 ns

Note: *ECAT0_CONPx.TX_SHIFT can be adjusted by displaying TX_CLK of a PHY and TXEN/TXD[3:0] on an oscilloscope. TXEN/TXD[3:0] is allowed to change between 0 ns and 25 ns after a rising edge of TX_CLK (according to IEEE802.3 – check your PHY's documentation). Configure TX_SHIFT so that TXEN/TXD[3:0] change near the middle of this range. It is sufficient to check just one of the TXEN/TXD[3:0] signals, because they are nearly generated at the same time.*

3 Electrical Parameters

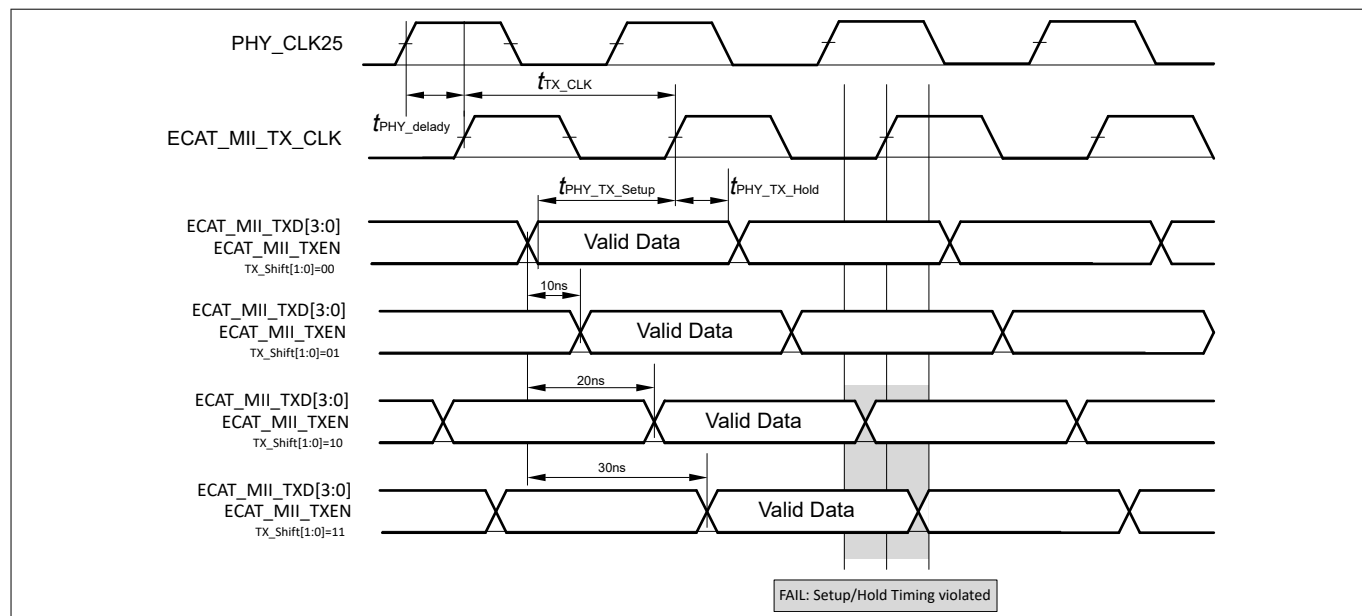


Figure 57 MII TX Characteristics

3.3.13.4 MII Timing RX Characteristics

Table 69 ETH MII RX Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
RX_CLK period	t_{RX_CLK} SR	–	40	–	ns	$C_L = 25$ pF, IEEE802.3 requirement
RX_DV/RX_DV/RXD[3:0] valid before rising edge of RX_CLK	t_{RX_setup} SR	10	–	–	ns	
RX_DV/RX_DV/RXD[3:0] valid after rising edge of RX_CLK	t_{RX_hold} SR	10	–	–	ns	

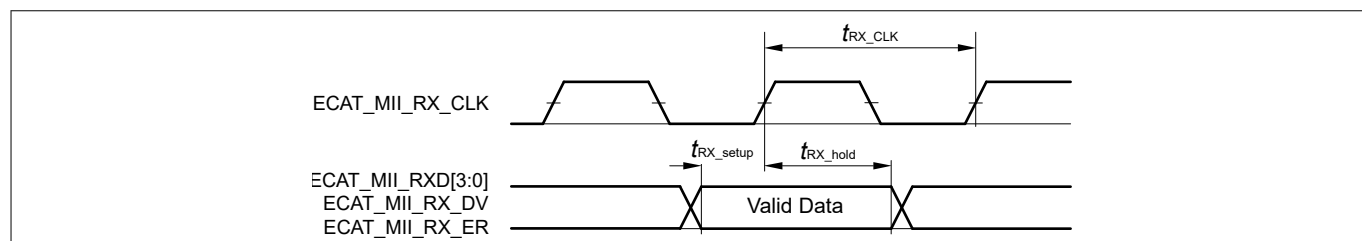


Figure 58 MII RX characteristics

3 Electrical Parameters

3.3.13.5 Sync/Latch Timings

Table 70 Sync/Latch Timings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
SYNC0/1	$t_{DC_SYNC_Jitter}$ SR	–	–	$11 + m^{1)}$	ns	
LATCH0/1	t_{DC_LATCH} SR	$12 + n^{2)}$	–	–	ns	

1) additional delay form logic and pad, number is added after characterization

2) additional shaping delay, number is added after characterization

Note: SYNC0/1 pulse length are initially loaded by EEPROM content ADR 0x0002. The actual used value can be read back from Register DC_PULSE_LEN.

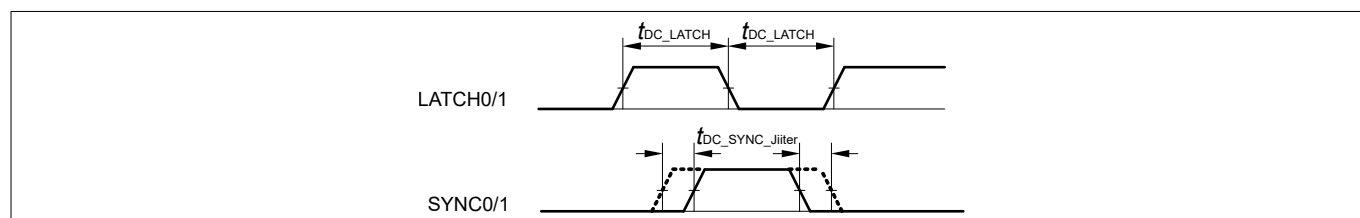


Figure 59 Sync/Latch Timings

4 Package and Reliability

4 Package and Reliability

The XMC4[78]00 is a member of the XMC4000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Die Pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 71 provides the thermal characteristics of the packages used in XMC4[78]00.

Table 71 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad dimensions including U-Groove	$E_x \times E_y$ CC	–	7.0×7.0	mm	PG-LQFP-144-24 PG-LQFP-100-25
Exposed Die Pad dimensions excluding U-Groove	$A_x \times A_y$ CC	–	6.2×6.2	mm	PG-LQFP-144-24 PG-LQFP-100-25
Exposed Die Pad dimensions	–	–	7.0×7.0	mm	PG-LQFP-144-28 PG-LQFP-100-29
Thermal resistance Junction-Ambient $T_J \leq 150^\circ\text{C}$	$R_{\Theta JA}$ CC	–	27.0	K/W	PG-LFBGA-196-2
		–	19.5	K/W	PG-LQFP-144-24 ¹⁾ PG-LQFP-144-28 ¹⁾
		–	22.5	K/W	PG-LQFP-100-25 ¹⁾ PG-LQFP-100-29 ¹⁾

1) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SS} , independent of EMC and thermal requirements.

4 Package and Reliability

4.1.1 Thermal Considerations

When operating the XMC4[78]00 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$ ” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150°C.

The difference between junction temperature and ambient temperature is determined by

$$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$$

The internal power consumption is defined as

$$P_{INT} = V_{DDP} \times I_{DDP} \text{ (switching current and leakage current).}$$

The static external power consumption caused by the output drivers is defined as

$$P_{IOSTAT} = \Sigma((V_{DDP} - V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP} , if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4 Package and Reliability

4.2 Package Outlines

The availability of different packages for different devices types is listed in [Table 1](#). The exposed die pad dimensions are listed in [Table 71](#).

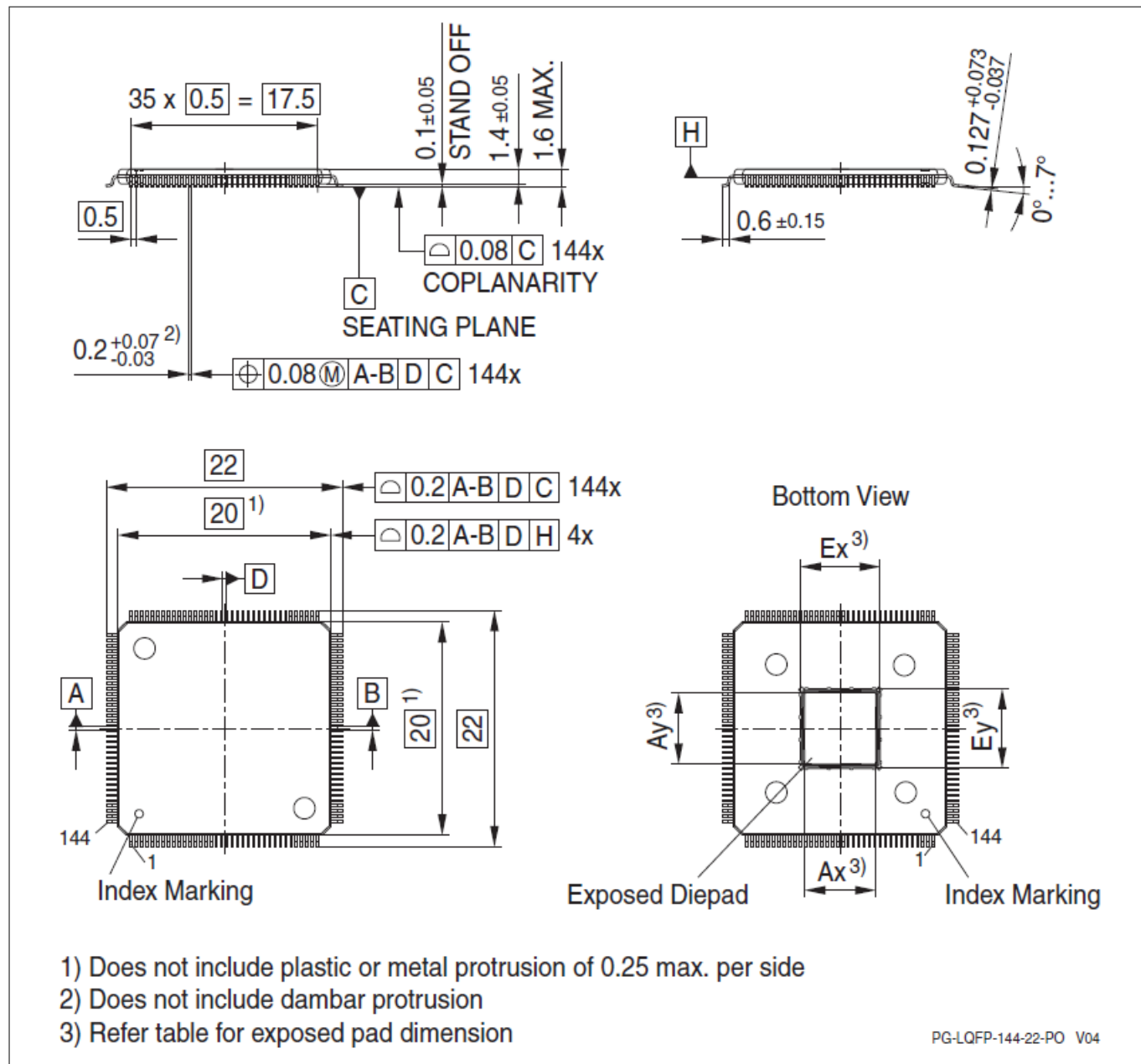


Figure 60 PG-LQFP-144-24 (Plastic Green Low Profile Quad Flat Package)

4 Package and Reliability

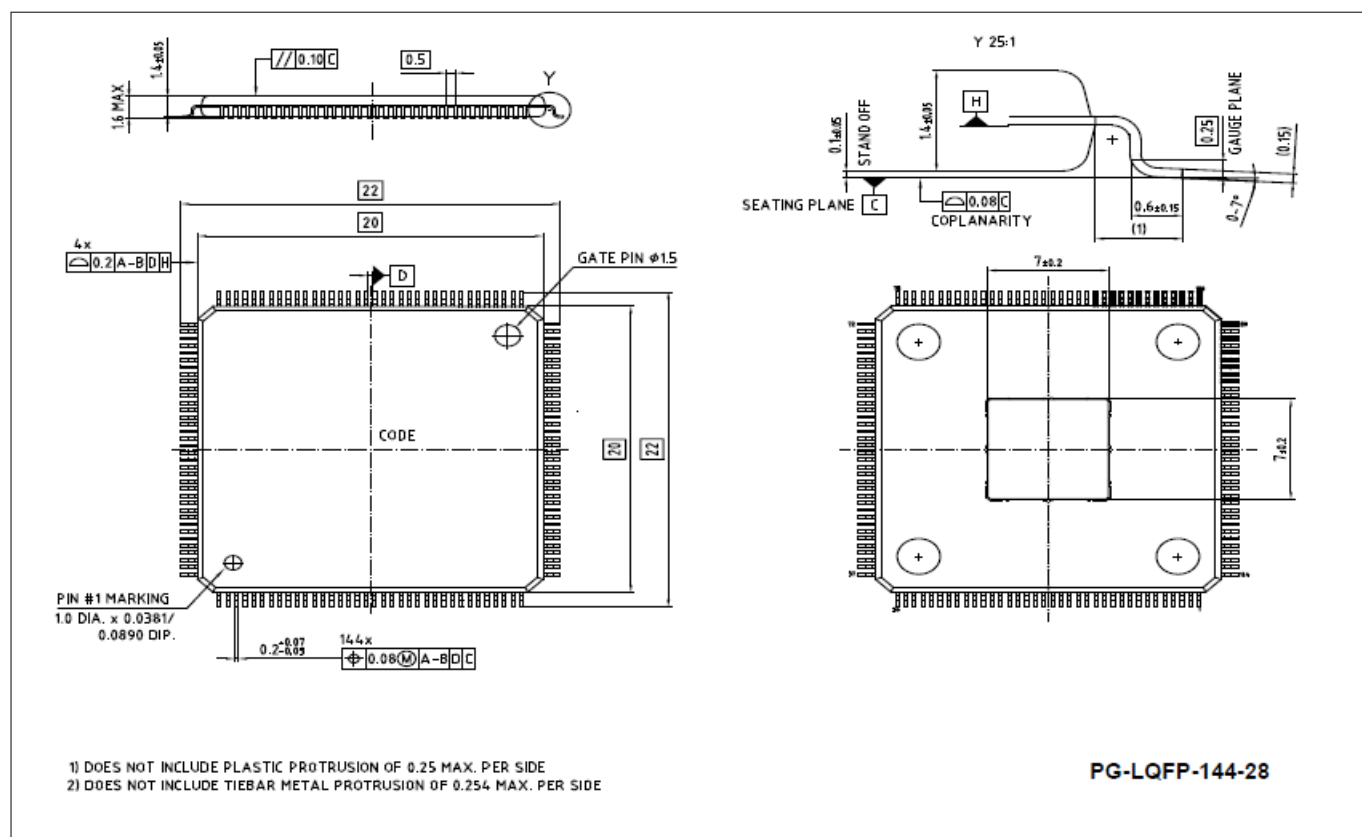


Figure 61 PG-LQFP-144-28 (Plastic Green Low Profile Quad Flat Package)

4 Package and Reliability

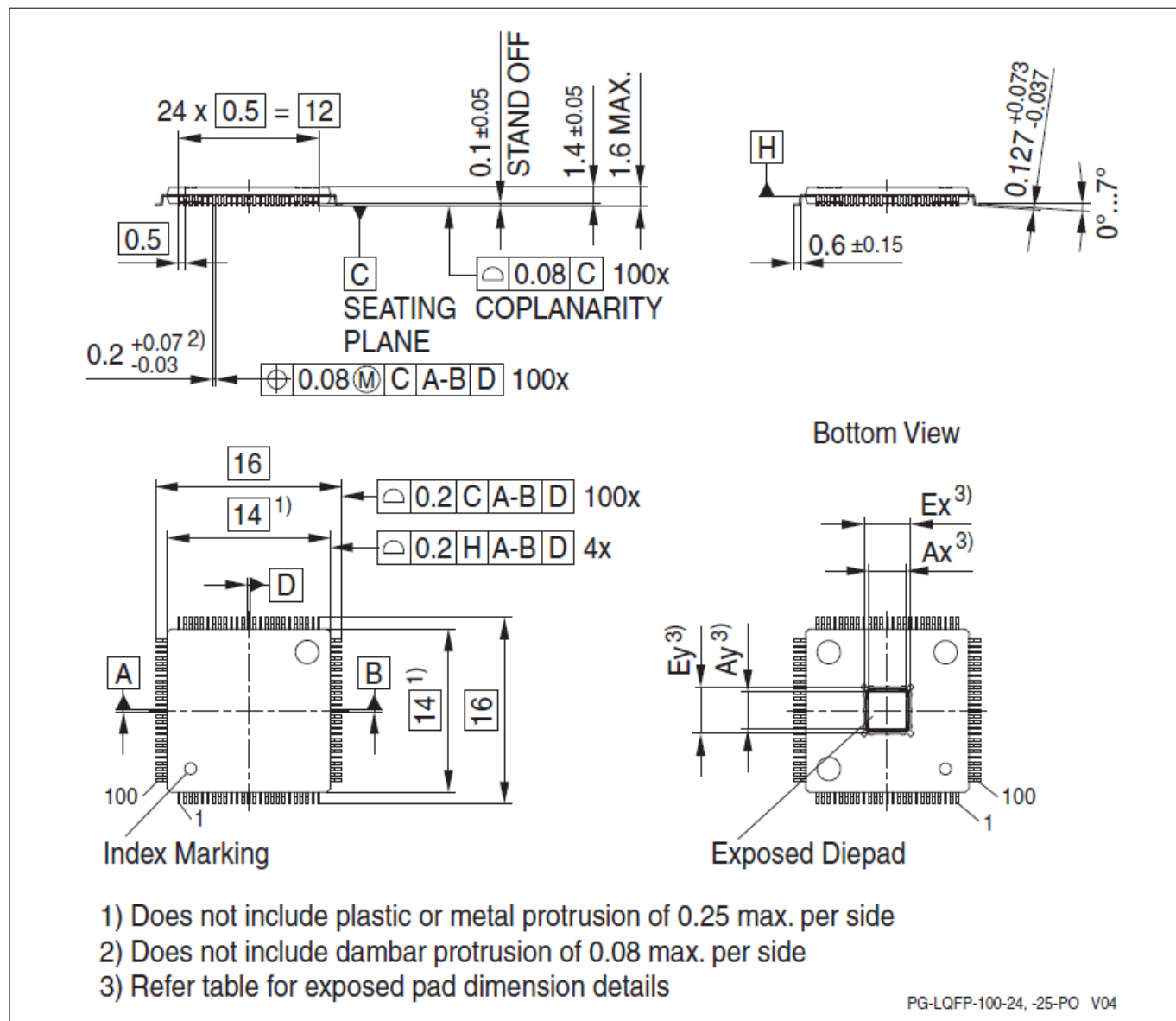


Figure 62 PG-LQFP-100-25 (Plastic Green Low Profile Quad Flat Package)

[illegible][illegible]

5 Quality Declarations

5 Quality Declarations

The qualification of the XMC4[78]00 is executed according to the JEDEC standard JESD471.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 72 **Quality Parameters**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109^\circ\text{C}$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	3000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	1000	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	$^\circ\text{C}$	Profile according to JEDEC J-STD-020D

Revision history

Revision history

Document revision	Date	Description of changes
V1.2	2023-04-01	Table 71 : Added PG-LQFP-144-28 and PG-LQFP-100-29 details in Table 71. Figure 64 : Added package diagram: PG-LQFP-100-29. Figure 61 : Added package diagram: PG-LQFP-144-28.
V1.3	2024-12-02	Template update; no content update

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-12-02

Published by

Infineon Technologies AG
81726 Munich, Germany

© 2024 Infineon Technologies AG
All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-wci1723472564656

Important notice

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenhheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.