ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	IM67D130AXTSA2
Manufacturer:	Infineon Technologies
Package:	Tape & Reel (TR),Cut Tape (CT)
Availability:	Please confirm with sales

Product Page:

https://antrexco.com/product/details/infineon-technologies/im67d130axtsa2.html

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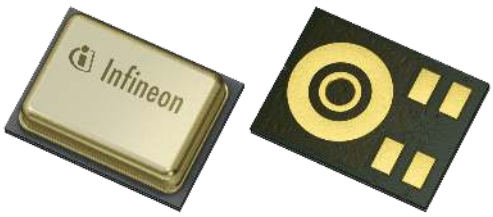
Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

IM67D130A

AEC-Q103 qualified high performance digital XENSIV™ MEMS microphone



Features

- Dynamic range of 103dB for best speech performance
  - Signal to noise ratio of 67dB(A) SNR
  - <1% total harmonic distortions up to high SPL levels
  - Acoustic overload point at 130dBSPL
- Automotive qualification
- Close sensitivity and phase matching for use in arrays
- Flat frequency response with low frequency roll off and very fast analog to digital conversion speed for best ANC performance
- Digital PDM output
- Extended availability to match automotive design cycles

Product validation

Technology qualified for industrial applications.
Product qualified according to AEC-Q103-003.

Potential applications

- Hands free calling
- Emergency call
- Voice control
- Active noise cancellation / Road noise cancellation (ANC/RNC)
- Siren detection
- Road condition detection

Ordering Information

Table 1 Order information

Product name	Package	Marking	Ordering code
IM67D130A	PG-LLGA-5-4	IM67DA	SP005582032

Product description

The device is designed for applications where low self-noise (high SNR), wide dynamic range, low distortions and a high acoustic overload point is required.

Infineon's Dual Backplate MEMS technology is based on a miniaturized symmetrical microphone design, similar as utilized in studio condenser microphones and results in high linearity of the output signal within a high dynamic range. The microphone distortion does not exceed 1% even up to very high sound pressure levels. With its low equivalent noise floor the microphone is no longer the limiting factor in the audio signal chain and enables higher performance of voice recognition algorithms.

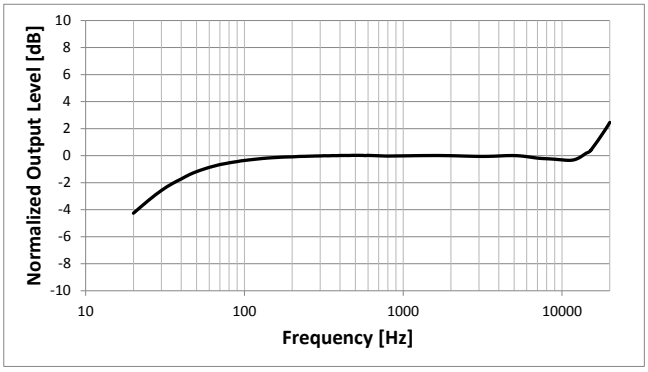
The digital microphone ASIC contains an extremely low-noise preamplifier and a high-performance sigma-delta ADC. Different power modes can be selected in order to suit specific current consumption requirements.

The tight manufacturing tolerance, combined with the fact that each device is calibrated with an advanced Infineon calibration algorithm, results in small sensitivity and phase matching tolerances. This makes it a perfect device for beam forming arrays and multi-microphone applications.

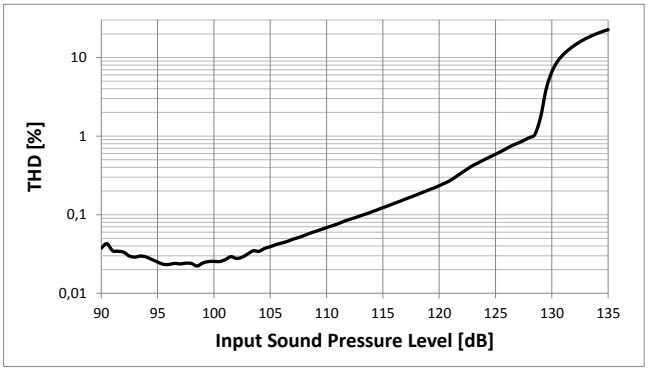
Table of contents

1 Typical performance characteristics

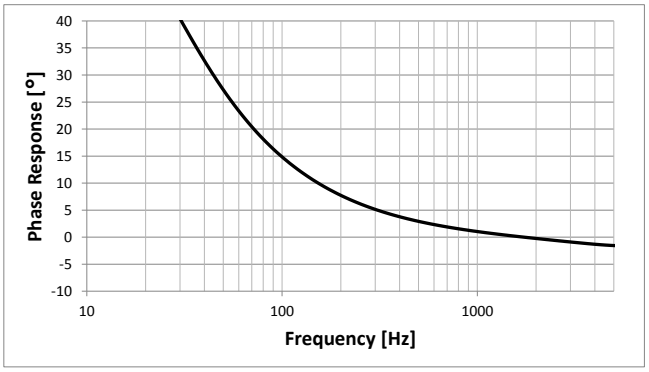
Test conditions: V_{DD} = 1.8V, f_{CLK} = 3.072 MHz, no load on DATA



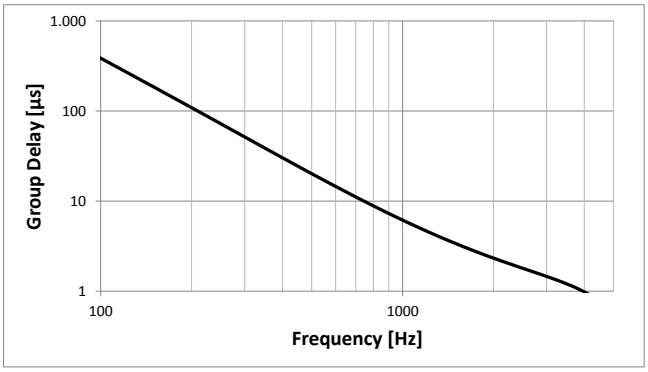
Plot 1: Typical free field response



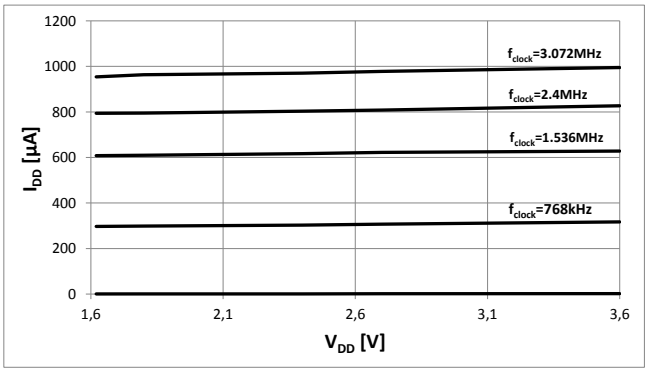
Plot 2: Typical THD vs. SPL



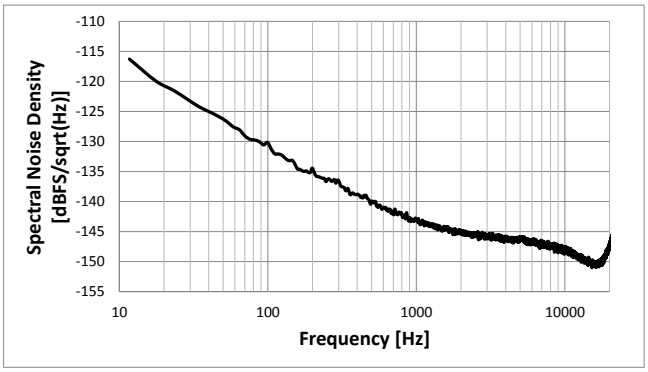
Plot 3: Typical phase response vs. frequency



Plot 4: Typical group delay vs. frequency



Plot 5: I_{DD} vs. V_{DD}



Plot 6: Typical noise floor (unweighted)

Figure 1 Typical performance characteristics

2 Block diagram

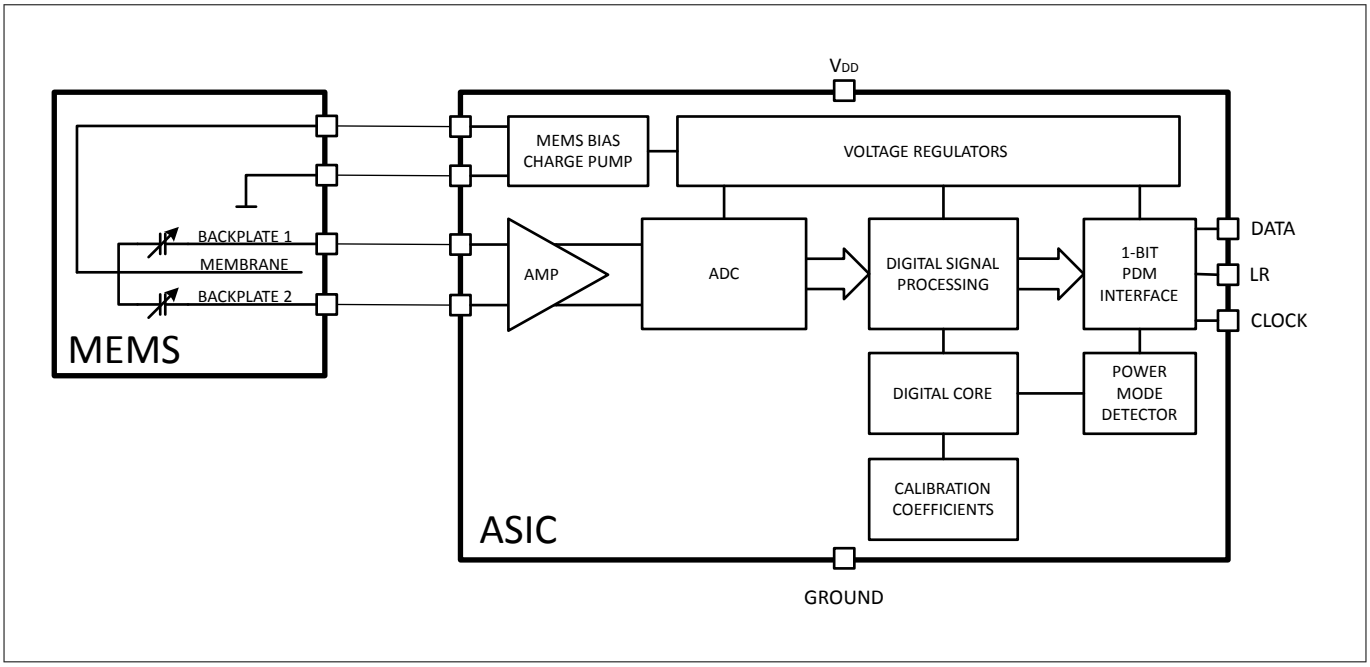


Figure 2 Block diagram

3 Pin configuration

The figure below shows the pin configuration of the device

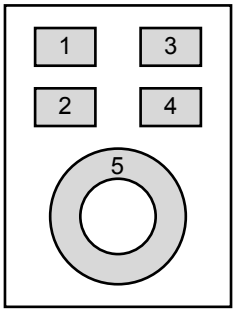


Figure 3 Pin configuration

Table 2 Pin configuration

Pin number	Name	Description
1	DATA	PDM data output
2	V_{DD}	Power supply
3	CLOCK	PDM clock input
4	LR	PDM left/right select
5	GND	Ground

4 General product characteristics

4.1 Acoustic characteristics

Test conditions (unless otherwise specified in the table): V_{DD} = 1.8V±0.1V, f_{CLK} = 3.072MHz, T_A = 25°C±5°C, audio bandwidth 20Hz to 20kHz, LR pin grounded, no load on DATA, t_{CR} = t_{CF} = 9ns

Table 3 Acoustic specifications

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Sensitivity	Sens	-37	-36	-35	dBFS	1kHz, 94 dBSPL, all operating modes
Acoustic Overload Point	AOP	-	130	-	dBSPL	THD = 10%, all operating modes
Signal to Noise Ratio, fCLK=3.072MHz	SNR	-	67	-	dB(A)	A-Weighted
Signal to Noise Ratio, fCLK=2.4MHz	SNR_{M2}	-	67	-	dB(A)	A-Weighted
Signal to Noise Ratio, fCLK=1.536MHz	SNR_{M3}	-	66	-	dB(A)	A-Weighted
Signal to Noise Ratio, fCLK=768kHz	SNR_{LPM}	-	64	-	dB(A)	20Hz to 8kHz bandwidth, A-Weighted
Noise Floor, fCLK = 3.072MHz	NF	-	-103	-	dBFS(A)	A-Weighted
Noise Floor - Mode2, fCLK = 2.4MHz	NF_{M2}	-	-103	-	dBFS(A)	A-Weighted
Noise Floor - Mode3, fCLK = 1.536MHz	NF_{M3}	-	-102	-	dBFS(A)	A-Weighted
Noise Floor - LPM, fCLK = 768kHz	NF_{LPM}	-	-100	-	dBFS(A)	20Hz to 8kHz bandwidth, A-Weighted
Total Harmonic Distortion, 94dBSPL	THD_{94}	-	0.5	-	%	Measuring 2nd to 5th harmonics; 1kHz, all operating modes
Total Harmonic Distortion, 128dBSPL	THD_{128}	-	1.0	-	%	Measuring 2nd to 5th harmonics; 1kHz, all operating modes
Total Harmonic Distortion, 129dBSPL	THD_{129}	-	2.0	-	%	Measuring 2nd to 5th harmonics; 1kHz, all operating modes
Total Harmonic Distortion, 130dBSPL	THD_{130}	-	10.0	-	%	Measuring 2nd to 5th harmonics; 1kHz, all operating modes
Low Frequency Cutoff Point	f_{C_LP}	-	28	-	Hz	-3dB point relative to 1kHz

(table continues...)

Table 3 (continued) Acoustic specifications

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Group Delay, 250Hz	t_{gd_250}	-	70	-	µs	
Group Delay, 600Hz	t_{gd_600}	-	15	-	µs	
Group Delay, 1kHz	t_{gd_1000}	-	6	-	µs	
Group Delay, 4kHz	t_{gd_4000}	-	1	-	µs	
Phase Response, 75Hz	Φ_{75}	-	19	-	°	
Phase Response, 1kHz	Φ_{1000}	-	2	-	°	
Phase Response, 3kHz	Φ_{3000}	-	-1	-	°	

Directivity: The device has an omnidirectional pickup pattern.

Polarity: The device has a positive polarity. Positive pressure increases density of 1's, negative pressure decreases density of 1's in data output)

4.1.1 Free field frequency response

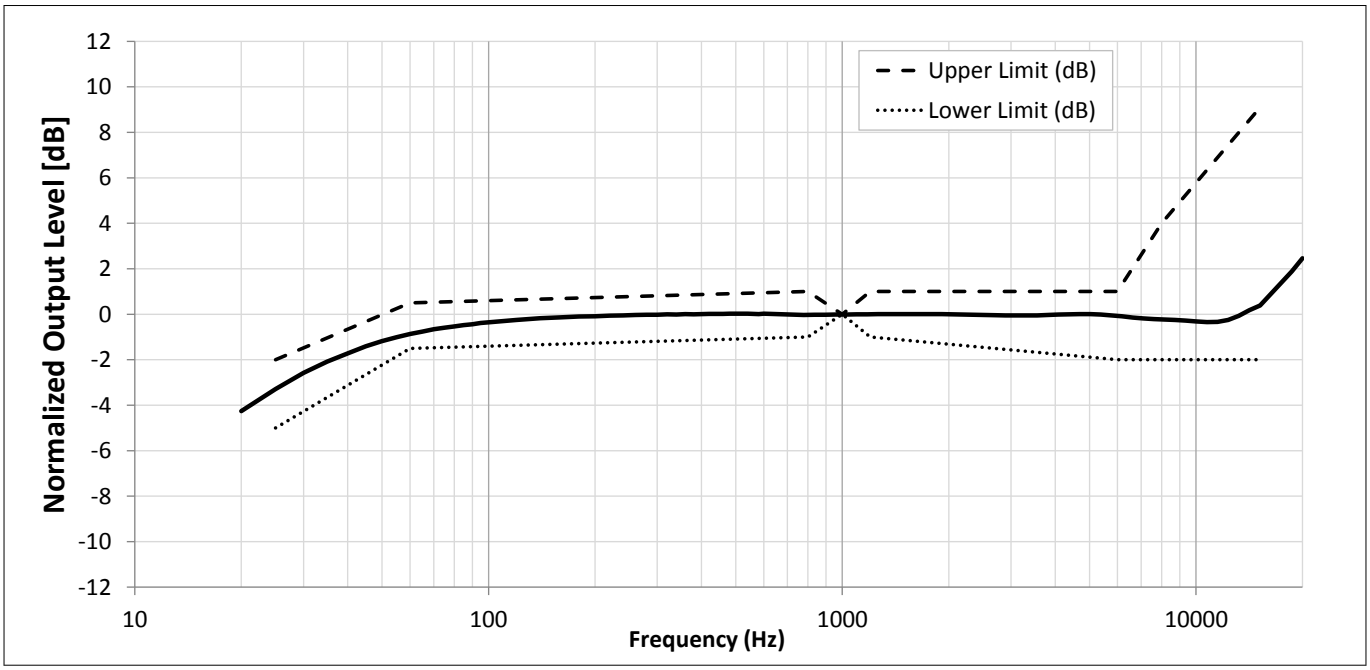


Figure 4 Free field frequency response

Table 4 Free field frequency response, normalized to 1kHz sensitivity value

Frequency (Hz)	Upper Limit (dB)	Lower Limit (dB)
25	-2	-5
60	+0.5	-1.5
800	+1	-1
1000	0	0
1200	+1	-1
6000	+1	-2
8000	+4	-2
15000	+9	-2

4.2 Electrical parameters and characteristics

4.2.1 Absolute maximum ratings

Table 5 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage on any Pin	V_{max}	-	-	4	V	
Storage Temperature	T_S	-40	-	125	°C	

***Attention**: Stresses above those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the section "Functional range" of this datasheet is not implied. Furthermore, only single error cases are assumed. More than one stress/error case may also damage the device.*
Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions the voltage on V_{DD} pins with respect to ground (GND) must not exceed the values defined by the absolute maximum ratings. Lifetime statements are an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. Lifetime statements shall in no event extend the agreed warranty period.

4.2.2 Functional range

Table 6 Functional range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	1.62	-	3.60	V	A 100nF bypass capacitor should be placed close to the microphone's V_{DD} pin to ensure best SNR performance
Ambient operating temperature	T_A	-40	-	+105	°C	
Clock Frequency Range, HPM	f_{CLK_HPM}	2.9	3.072	3.3	MHz	
Clock Frequency Range, Mode2	f_{CLK_M2}	2.1	2.4	2.65	MHz	
Clock Frequency Range, Mode3	f_{CLK_M3}	1.05	1.536	1.9	MHz	
Clock Frequency Range, LPM	f_{CLK_LPM}	400	768	950	kHz	
Clock Frequency Range, Standby mode	f_{CLK_sb}	-	-	250	kHz	DATA = high-Z
PDM Clock Frequency	f_{CLK}	0.4	-	3.30	MHz	
VDD Ramp-up Time	V_{DD_ru}	-	-	50	ms	Time until $V_{DD} \geq V_{DD\_min}$
Clock Duty Cycle	CLK_{duty}	40	-	60	%	$f_{CLK} < 2.65MHz$
Clock Duty Cycle, High performance mode	CLK_{duty_HPM}	48	-	52	%	$f_{CLK} \geq 2.9MHz$
Clock Rise/Fall Time	t_{CR} / t_{CF}	-	-	13	ns	
Input Logic Low Level	V_{IL}	-0.3	-	$0.35xV_{DD}$	V	
Input Logic High Level	V_{IH}	$0.65xV_{DD}$	-	$V_{DD}+0.3$	V	
Output Load Capacitance on DATA	C_{load}	-	-	200	pF	

4.2.3 Electrical characteristics

Test conditions (unless otherwise specified in the table): $V_{DD} = 1.8V \pm 0.1V$, $T_A = 25°C \pm 5°C$

Table 7 General electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current Consumption, HPM	I_{DD_HPM}	-	980	1300	µA	No load on DATA
Current Consumption, Mode2	I_{DD_M2}	-	800	1050	µA	No load on DATA
Current Consumption, Mode3	I_{DD_M3}	-	620	800	µA	No load on DATA
Current Consumption, LPM	I_{DD_LPM}	-	300	380	µA	No load on DATA
Current Consumption, Standby mode	$I_{standby}$	-	25	50	µA	No load on DATA
Current Consumption, Clock off mode	I_{clock_off}	-	-	1	µA	CLOCK pulled low
Short Circuit Current	I_{short}	1	-	20	mA	Grounded DATA pin
Power Supply Rejection	PSR_{1k_NM}	-	-80	-	dBFS	100mV$_{pp}$ sine wave on V_{DD} swept from 200Hz to 20kHz
Power Supply Rejection	PSR_{217_NM}	-	-86	-	dBFS(A)	100mV$_{rms}$, 217Hz square wave on V_{DD}, A-weighted
Startup Time, ±0.5dB sensitivity accuracy	$t_{start\text{-}up}$	-	-	20	ms	Time to start up in all operating modes after V_{DD_min} and CLOCK have been applied
Startup Time, ±0.2dB sensitivity accuracy	$t_{start\text{-}up\_HP}$	-	-	50	ms	Time to start up in all operating modes after V_{DD_min} and CLOCK have been applied
Mode Switch Time, ±0.5dB sensitivity accuracy	$t_{mode\text{-}switch}$	-	-	20	ms	Time to switch between operating modes. V_{DD} remains on during the mode switch
Mode Switch Time, ±0.2dB sensitivity accuracy	$t_{mode\text{-}switch\_HP}$	-	-	50	ms	Time to switch between operating modes. V_{DD} remains on during the mode switch
Hysteresis Width	V_{hys}	0.1xV_{DD}	-	0.29xV_{DD}	V	
Output Logic Low Level	V_{OL}	-	-	0.3xV_{DD}	V	I_{out}= 2mA
Output Logic High Level	V_{OH}	0.7xV_{DD}	-	-	V	I_{out}= 2mA

(table continues...)

Table 7 (continued) General electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Delay Time for DATA Driven	t_{DD}	40	-	80	ns	Delay time from CLOCK edge ($0.5xV_{DD}$) to DATA driven
Delay Time for DATA High-Z	t_{HZ}	5	-	30	ns	Delay time from CLOCK edge ($0.5xV_{DD}$) to DATA high impedance state [1)]
Delay Time for DATA Valid	t_{DV}	-	-	100	ns	Delay time from CLOCK edge ($0.5xV_{DD}$) to DATA valid ($<0.3xV_{DD}$ or $>0.7xV_{DD}$) [2)]

4.2.4 Timing diagram

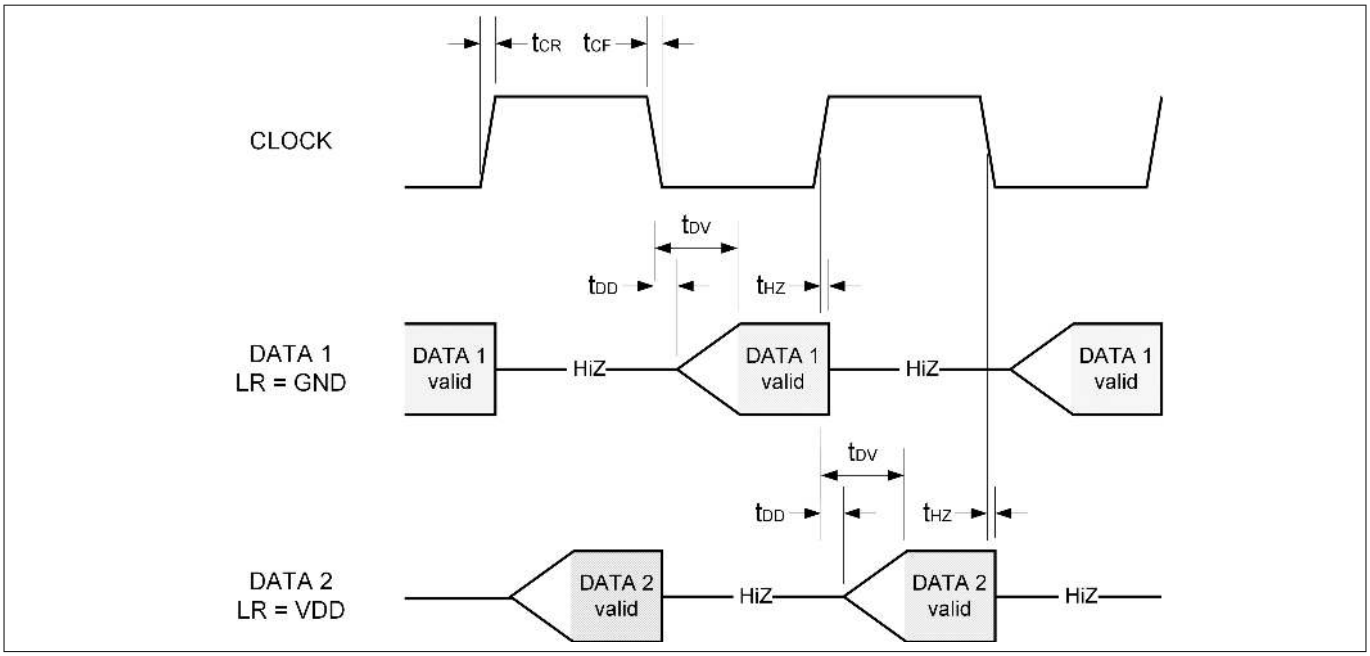


Figure 5 Timing diagram

1 t_{HZ} is dependent upon C_{load}
2 Load on DATA: C_{load} = 100pF, R_{load} = 100kΩ

5 Application information

5.1 Use cases

- Total Harmonic Distortion (THD) below 1% up to high sound pressure levels (SPL)
  - Clear speech in a wide dynamic range
  - Reliable voice commands during high background noise
  - Effective active noise cancellation even close to loud noise source
- High Signal to Noise Ratio (SNR)
  - Far field audio signal pick-up
  - Low volume audio and whispered voice capturing
  - Good performance with speech recognition algorithms
  - Microphone noise is no longer limiting the audio chain
- Close sensitivity and phase matching
  - Good performance in audio beamforming
  - High and precise attenuation of background noise
  - Full utilization of voice algorithms capability
- Flat frequency response with low f_{C_LP} (low frequency cutoff point) and small group delay
  - Good performance in active noise cancellation systems
  - Excellent speech quality over full frequency range
- Power optimized modes
  - Low current consumption for always on applications
  - Long operating time of battery powered devices

5.2 Typical stereo application circuit

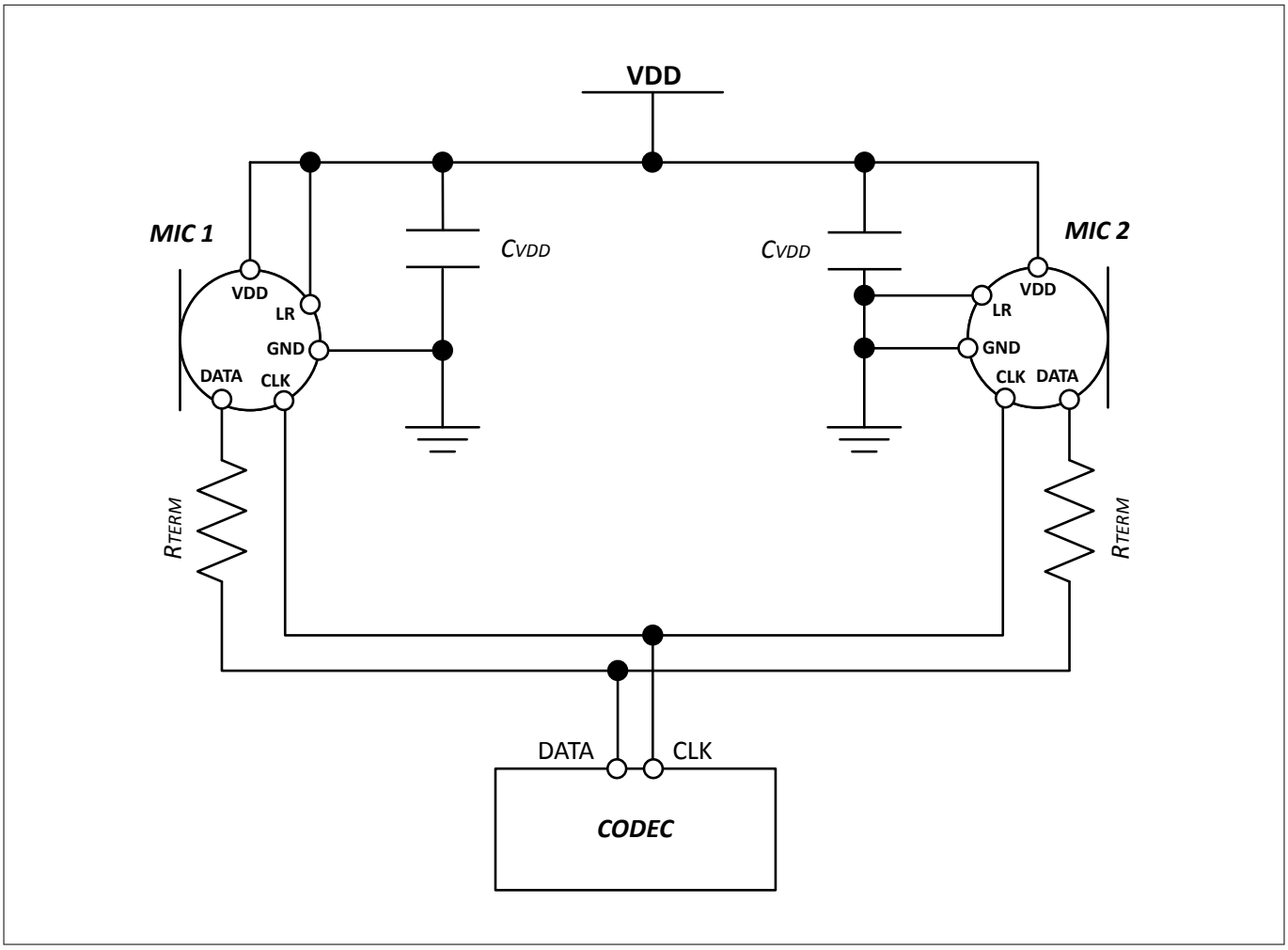


Figure 6 Typical stereo application circuit

Note: For best performance it is strongly recommended to place a 100nF ($C_{VDD\_typical}$) capacitor between V_{DD} and ground. The capacitor should be placed as close to V_{DD} as possible. A termination resistor (R_{TERM}) of about 100Ω may be added to reduce the ringing and overshoot on the output signal.

6 Package information

This product is compliant to RoHS

6.1 Package outline

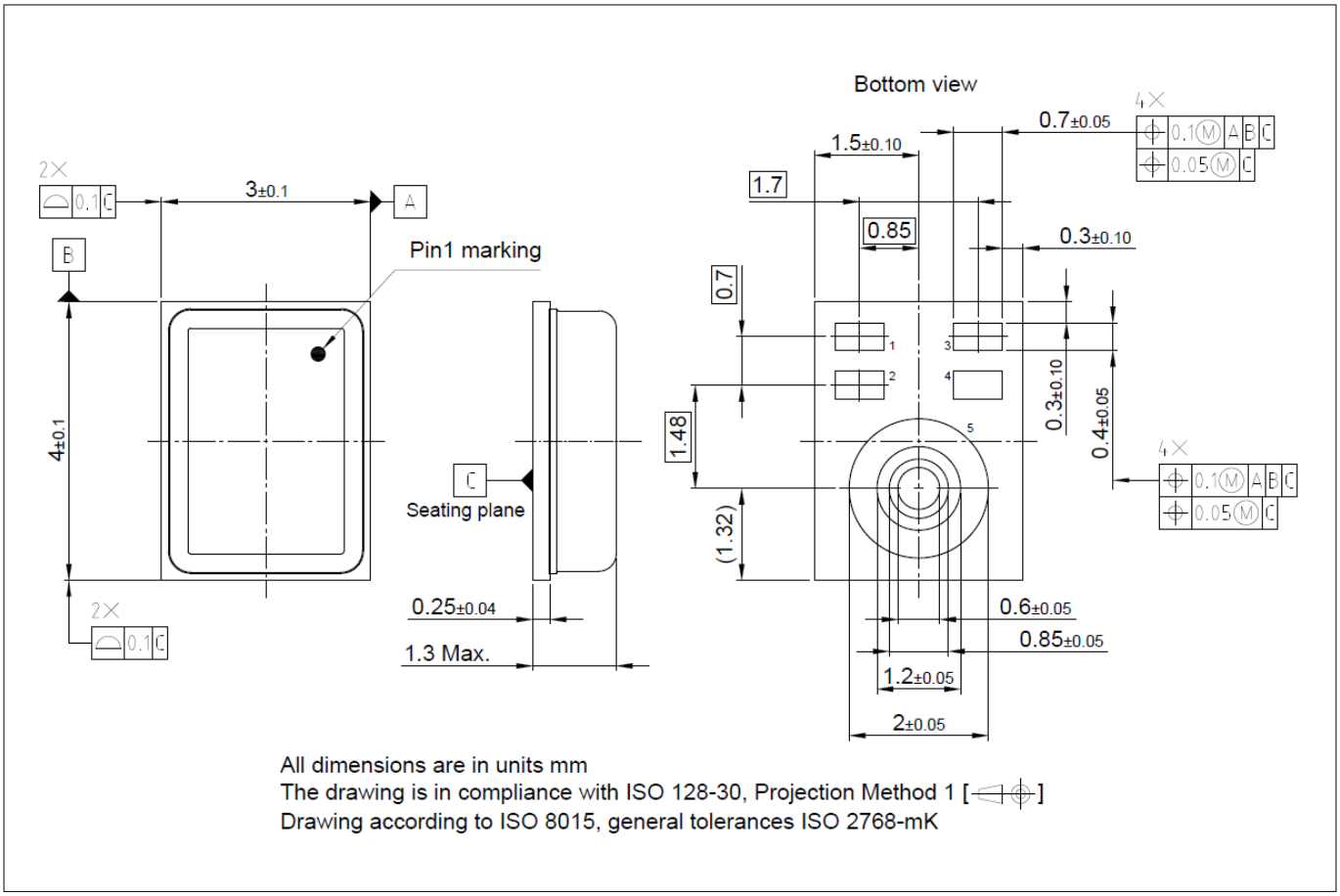


Figure 7 Package outline drawing

6.2 Footprint and stencil recommendation

The acoustic port hole diameter in the PCB should be larger than the acoustic port hole diameter of the MEMS microphone to ensure optimal performance. A PCB sound port size of radius 0.4 mm (diameter 0.8mm) is recommended.

The board pad and stencil aperture recommendations shown in the figure below are based on Solder Mask Defined (SMD) pads. The specific design rules of the board manufacturer should be considered for individual design optimizations or adaptations.

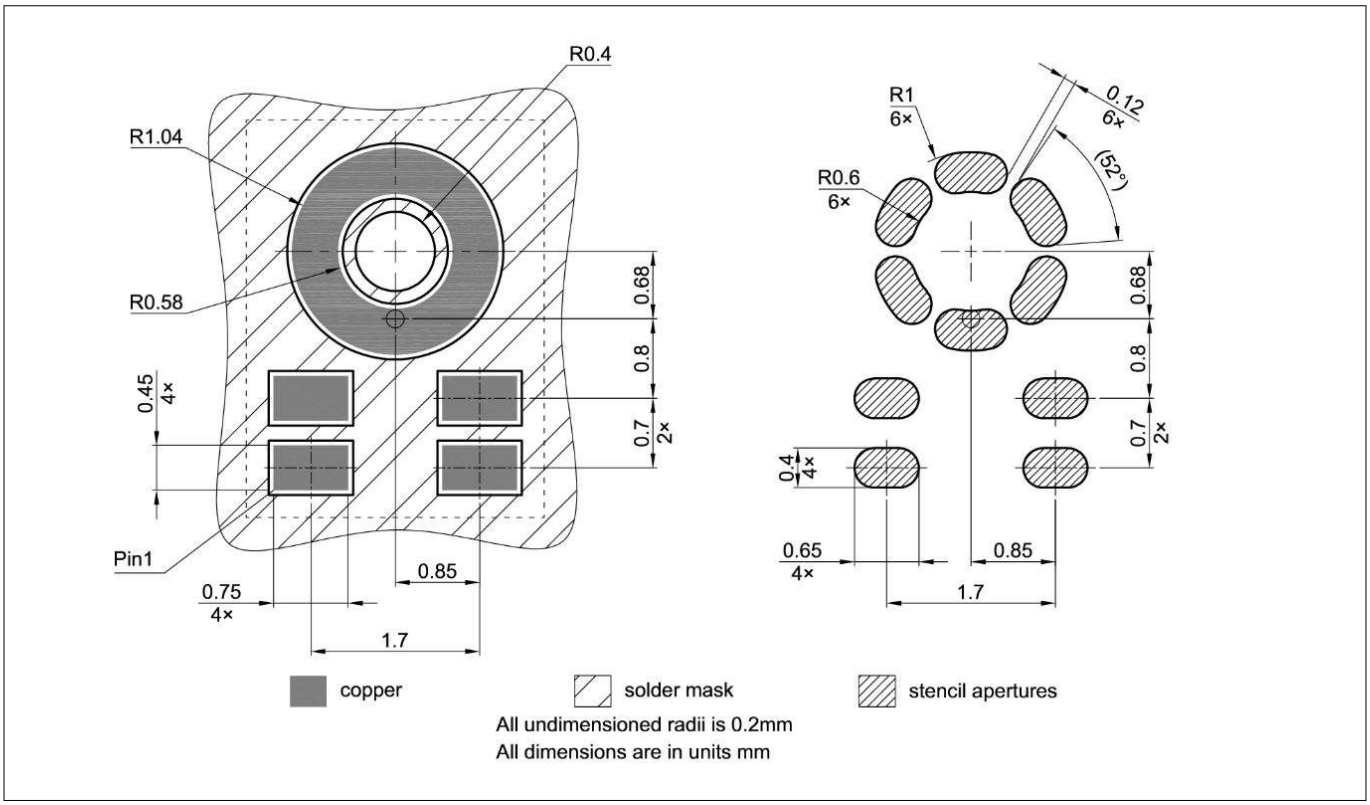


Figure 8 Footprint and stencil recommendation

6.3 Reflow soldering and board assembly

Infineon MEMS microphones are qualified in accordance with the IPC/JEDEC J-STD-020D-01. The moisture sensitivity level of MEMS microphones is rated as MSL1. For PCB assembly of the MEMS microphone the widely used reflow soldering using a forced convection oven is recommended.

The soldering profile should be in accordance with the recommendations of the solder paste manufacturer to reach an optimal solder joint quality. The reflow profile shown in the figure below is recommended for board manufacturing with Infineon MEMS microphones.

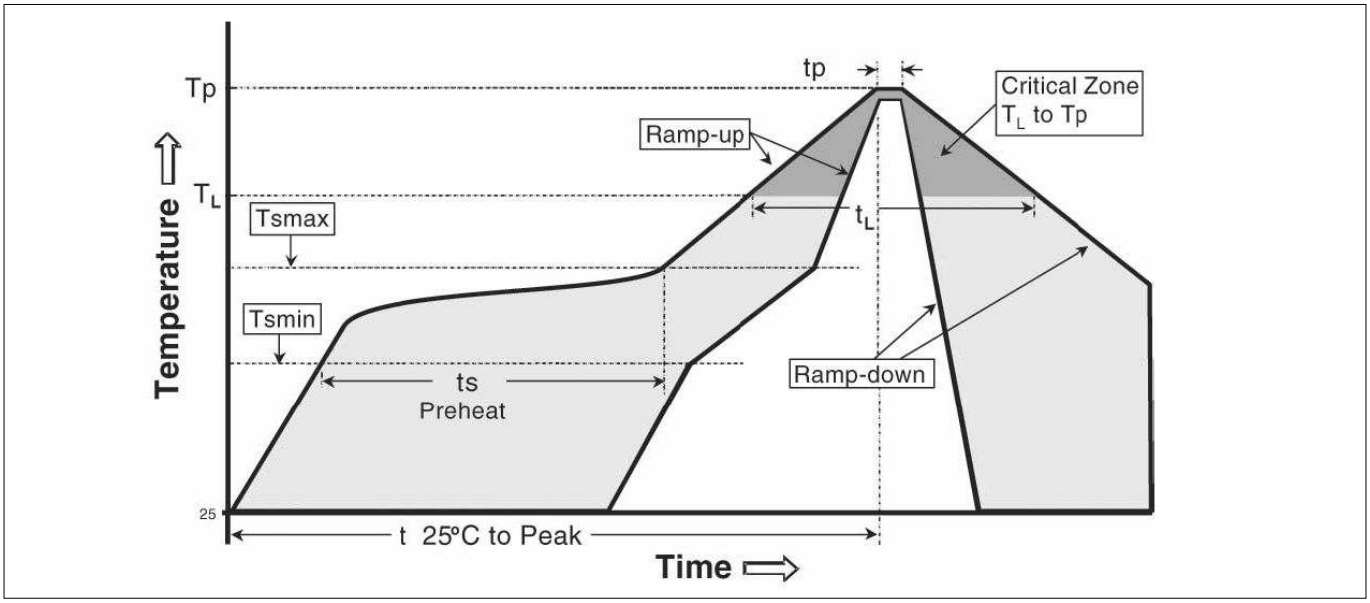


Figure 9 Recommended reflow profile

Table 8 Reflow profile limits

Profile feature	Symbol	Pb-free assembly	Sn-Pb Eutectic assembly
Preheat temperature min.	T_{smin}	150°C	100°C
Preheat temperature max.	T_{smax}	200°C	150°C
Preheat time (T_{smin} to T_{smax})	t_s	60-120 seconds	60-120 seconds
Ramp-up rate (T_L to T_P)		3°C/second max.	3°C/second max.
Liquidous temperature	T_L	217°C	183°C
Time maintained above T_L	t_L	60-150 seconds	60-150 seconds
Peak temperature	T_P	260°C +0°C/-5°C	235°C +0°C/-5°C
Time within 5°C of actual peak temperature (see note below)	t_P	20-40 seconds	10-30 seconds
Ramp-down rate		6°C/second max.	6°C/second max.
Time 25°C to peak temperature	t	8 minutes max.	6 minutes max.

Note: Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

The MEMS microphones can be handled using industry standard pick and place equipment. Care should be taken to avoid damage to the microphone structure as follows:

- Do not pick the microphone with vacuum tools which make contact with the microphone acoustic port hole.
- The microphone acoustic port hole should not be exposed to vacuum. This can destroy or damage the MEMS.
- Do not blow air into the microphone acoustic port hole. If an air blow cleaning process is used, the port hole must be sealed to prevent particle contamination.
- It is recommended to perform the PCB assembly in a clean room environment in order to avoid microphone contamination.
- Air blow and ultrasonic cleaning procedures shall not be applied to MEMS Microphones. A no-clean paste is recommended for the assembly to avoid subsequent cleaning steps. The microphone MEMS can be severely damaged by cleaning substances.
- To prevent the blocking or partial blocking of the sound port during PCB assembly, it is recommended to cover the sound port with protective tape during PCB sawing or system assembly.
- Do not use excessive force to place the microphone on the PCB. The use of industry standard pick and place tools is recommended in order to limit the mechanical force exerted on the package.

*Note: For further information please consult the "General recommendation for assembly of Infineon packages" document, which is available on the Infineon Technologies **web page**.*

6.4 Packing

For shipping and assembly the Infineon microphones are packed in product specific tape-and-reel carriers. A detailed drawing of the carrier can be seen in the figure below.

6 Package information

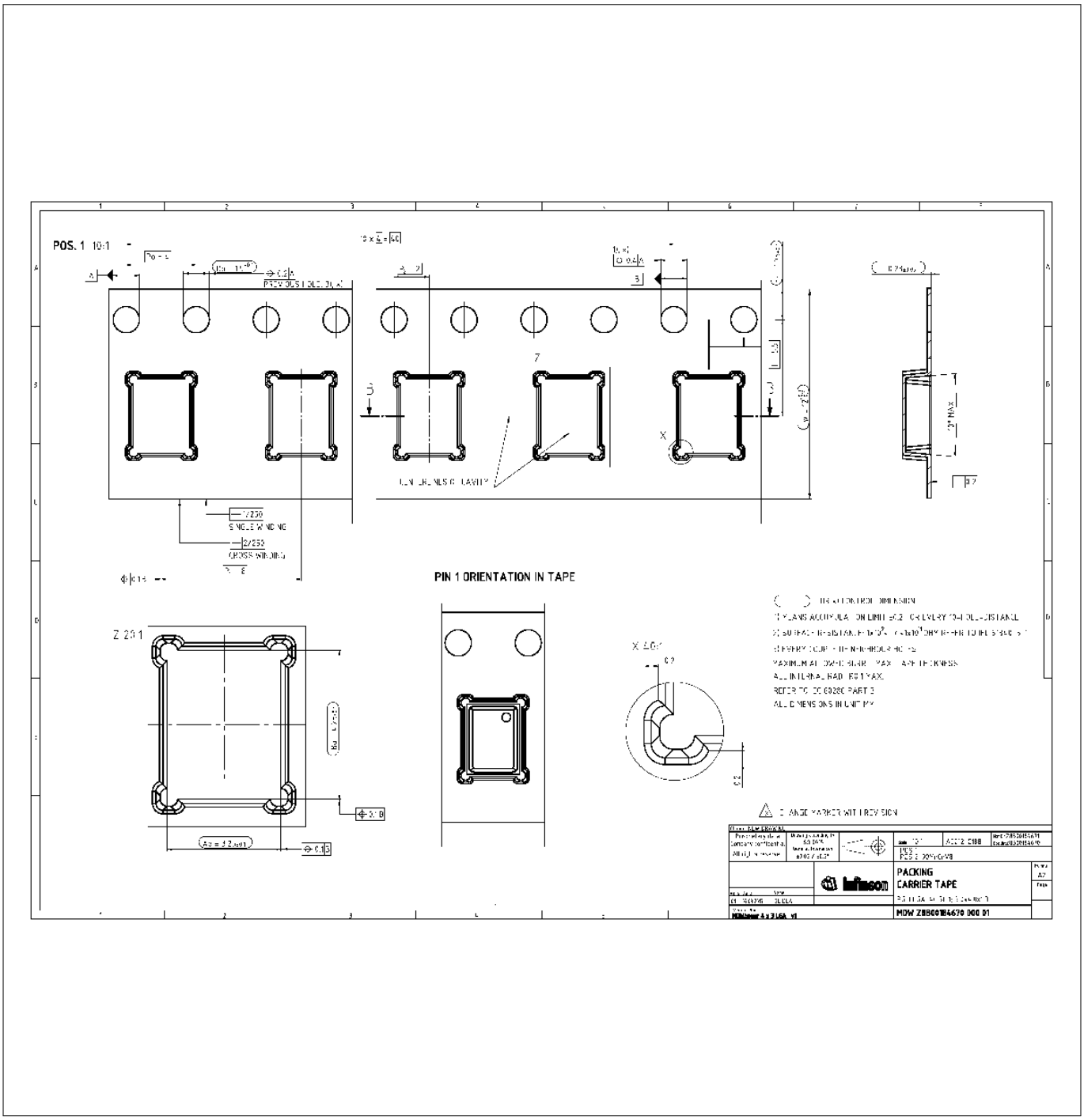


Figure 10 Tape dimensions

More information can be found on the Infineon website:
https://www.infineon.com/cms/en/product/packages/PG-LLGA/PG-LLGA-5-4/

7 Reliability specifications

The microphone sensitivity after stress and over temperature does not deviate by no more than +/- 3dB from the initial value.

Table 9 Qualification tests according to AEC-Q103-003

Test	Stress condition	Standard
Temperature humidity bias	T_A = +85°C, R.H. = 85%, V_{DD} = 3.6V, cyclical bias, 1000 hours	AEC Q100 Rev.H.
Temperature humidity storage	T_A = +85°C, R.H = 85%, 1000 hours	AEC Q100 Rev.H.
Temperature cycling	T_A = -55°C ... +125°C, 30 min cycle time, 1000cycles	AEC Q100 Rev.H.
High temperature storage life	T_A = +125°C, 1000 hours	AEC Q100 Rev.H.
High temperature operating life	T_A = +125°C, V_{DD} = 3.6V, 1000 hours	AEC Q100 Rev.H.
Early life failure rate	T_A = +125°C, V_{DD} = 2.5V, 48 hours Read out after stress at room temperature	JESD22-A108
Wire bond shear	Bump shear test	AEC Q100-001
Wire bond pull	-	MIL-STD883 Method 2011
Solderability	-	JESD22-B102
Physical dimensions	-	JESD22-B100 and B108
Solder ball shear	-	AEC Q103-003
Mechanical shock	3 pulses, 0.5msec duration, 10,000g peak acceleration in x,y and z planes	JESD22-B104
Variable frequency vibration	20Hz to 2kHz to 20Hz (logarithmic variation) in 12 minutes, 4x in each orientation, 20g peak acceleration	JESD22-B103
Package drop	10x on each of 6 axes (60 drops total) from a high of 1.2m onto a concrete surface	AEC Q100 Rev.H.
Die shear	-	MIL-STD-883 Method 2019
Humidity and temperature cycle	5 cycles (24h/cycle)	IEC 60068-2-38
Low temperature operating life	T_A = -40°C, V_{DD} = 3.6V, 1000 hours	JESD22-A108
Low temperature storage	T_A = -40°C, 1000 hours	JESD22-A119
Endurance life test	96 hours at 130dB continuous signal	AEC Q103-003
Electrostatic discharge, Human body model (HBM)	all pins, U_{ESD} = ±2000V	EIA/JESD22/A114
Electrostatic discharge, Charged device model (CDM)	all pins, U = ±500V	ESD STM 5.3.1
Electrostatic discharge, SLT - Contact discharge	3 contact discharges of ±6kV to lid while V_{dd} and f_{CLK} are supplied according to the operational modes; V_{dd} and f_{CLK} ground is separated from earth ground	IEC-61000-4-2

(table continues...)

7 Reliability specifications

Table 9 (continued) Qualification tests according to AEC-Q103-003

Test	Stress condition	Standard
Electrostatic discharge, SLT - Air discharge	3 air discharges of ±8kV to lid while V_{dd} and f_{CLK} are supplied according to the operational modes; V_{dd} and f_{CLK} ground is separated from earth ground	IEC-61000-4-2
Latch-up	T_A = 105°C, I = ±200mA	AEC Q100 Rev.H.
Electromagnetic compatibility (EMC)	IC strip line radiated emmissions	IEC 61967-8 / Generic IC EMC Test Specification 2.1

8 Revision history

Table 10 Revision history

Document version	Date of release	Description of changes
1.00	18.05.2021	• First released version

Trademarks

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