

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: IAUCN04S7N005ATMA1

Manufacturer: Infineon Technologies

Package: Please confirm with sales

Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/infineon-technologies/iaucn04s7n005atma1.html>

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Quality & Trust

New & Original Components

Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

Secure sourcing support for OEM / EMS projects

Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

Automotive MOSFET

OptiMOS™ 7 Power-Transistor



Features

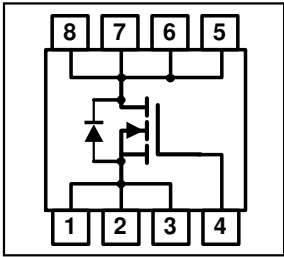
- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.



Product Summary

V_{DS}	40	V
$R_{DS(on)}$	0.55	mΩ
I_D (chip limited)	414	A

Type	Package	Marking
IAUCN04S7N005	PG-TDSON-8-43	7N04N005



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Maximum ratings

at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}$, Chip limitation ^{1,2)}	414	A
		$V_{GS}=10\text{ V}$, DC current ³⁾	175	
		$T_a=100\text{ °C}$, $V_{GS}=10\text{ V}$, R_{thJA} on 2s2p ^{2,4)}	53	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$, $t_p=100\text{ }\mu\text{s}$	1400	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=75\text{ A}$	332	mJ
Avalanche current, single pulse	I_{AS}	–	150	A
Gate source voltage	V_{GS}	–	± 20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	179	W
Operating and storage temperature	T_j, T_{stg}	–	-55 ... +175	°C

Thermal characteristics²⁾

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	—	—	0.42	0.84	K/W
Thermal resistance, junction - ambient ⁴⁾	R_{thJA}	—	—	26.9	—	

Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$	40	—	—	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=95\text{ }\mu\text{A}$	2.2	2.6	3.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	—	—	1	μA
		$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=100\text{ °C}^{2)}$	—	—	24	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	—	—	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=7\text{ V}$, $I_D=44\text{ A}$	—	0.61	0.70	m Ω
		$V_{GS}=10\text{ V}$, $I_D=88\text{ A}$	—	0.50	0.55	
Gate resistance ²⁾	R_G	—	—	1.1	—	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=20\text{ V}, f=1\text{ MHz}$	–	6400	8320	pF
Output capacitance	C_{oss}		–	3700	4810	
Reverse transfer capacitance	C_{rss}		–	125	188	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V}, I_D=88\text{ A}, R_G=3.5\ \Omega$	–	16	–	ns
Rise time	t_r		–	9	–	
Turn-off delay time	$t_{d(off)}$		–	34	–	
Fall time	t_f		–	21	–	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=20\text{ V}, I_D=88\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	–	26	34	nC
Gate to drain charge	Q_{gd}		–	20	30	
Gate charge total	Q_g		–	98	127	
Gate plateau voltage	$V_{plateau}$		–	4	–	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25\text{ °C}$	–	–	175	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C=25\text{ °C}, t_p=100\ \mu\text{s}$	–	–	1400	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=88\text{ A}, T_J=25\text{ °C}$	–	0.8	0.95	V
Reverse recovery time ²⁾	t_{rr}	$V_R=20\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$	–	49	74	ns
Reverse recovery charge ²⁾	Q_{rr}		–	46	92	nC

¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

²⁾ The parameter is not subject to production testing – specified by design.

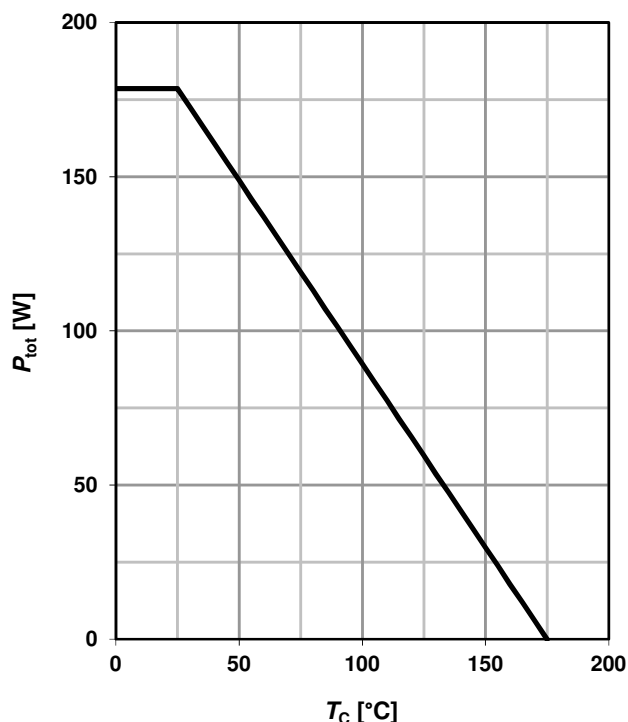
³⁾ Current is not limited by chip.

⁴⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Electrical characteristics diagrams

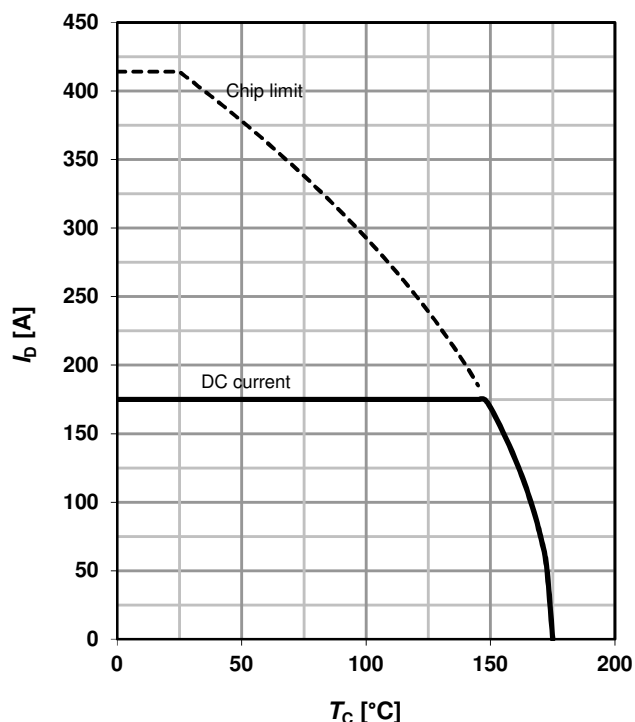
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



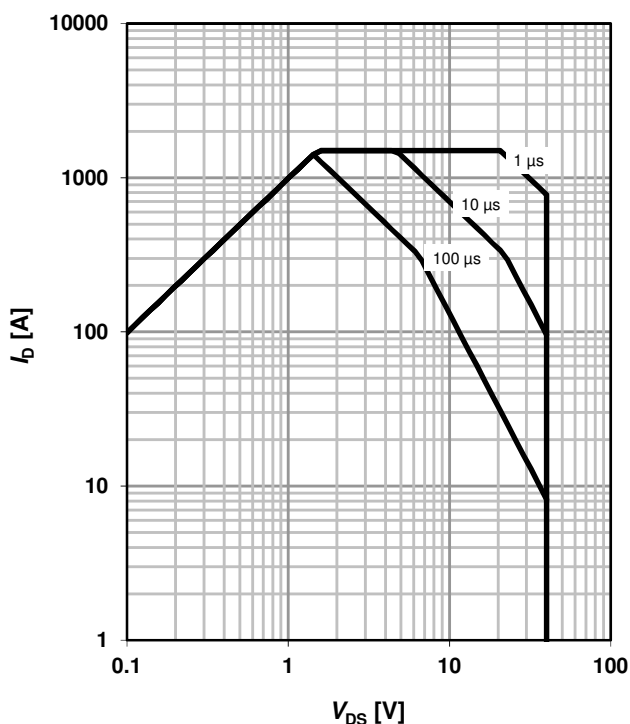
2 Drain current

$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



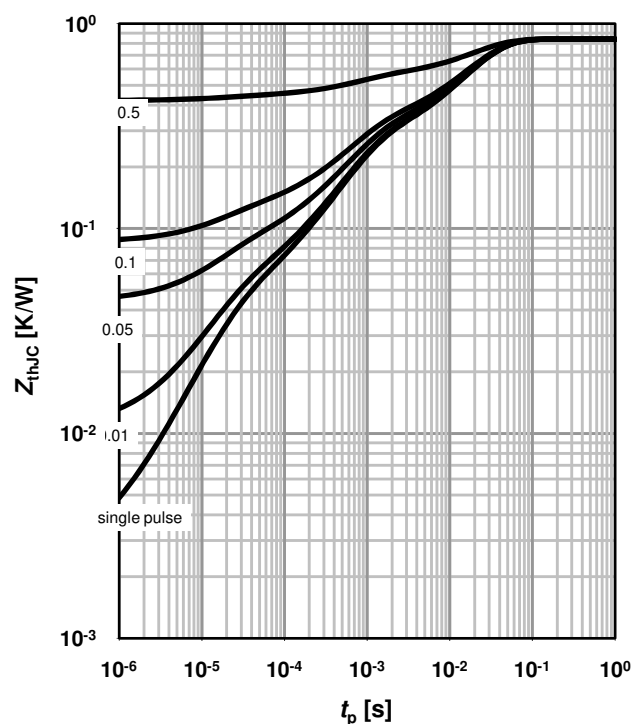
3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0; \text{parameter: } t_p$$



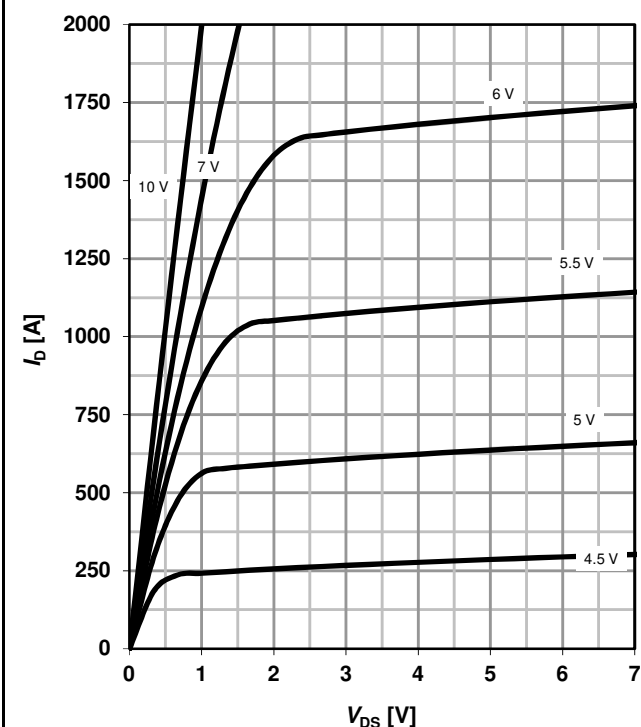
4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p); \text{parameter: } D = t_p/T$$



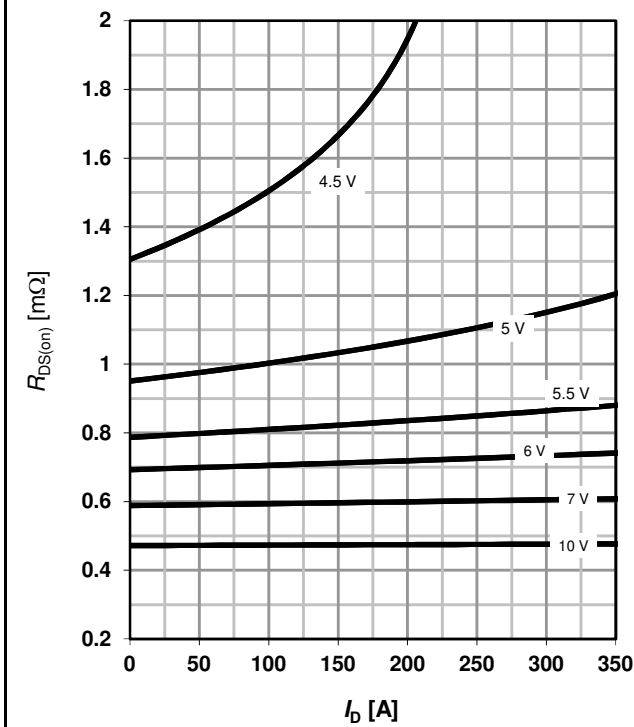
5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$



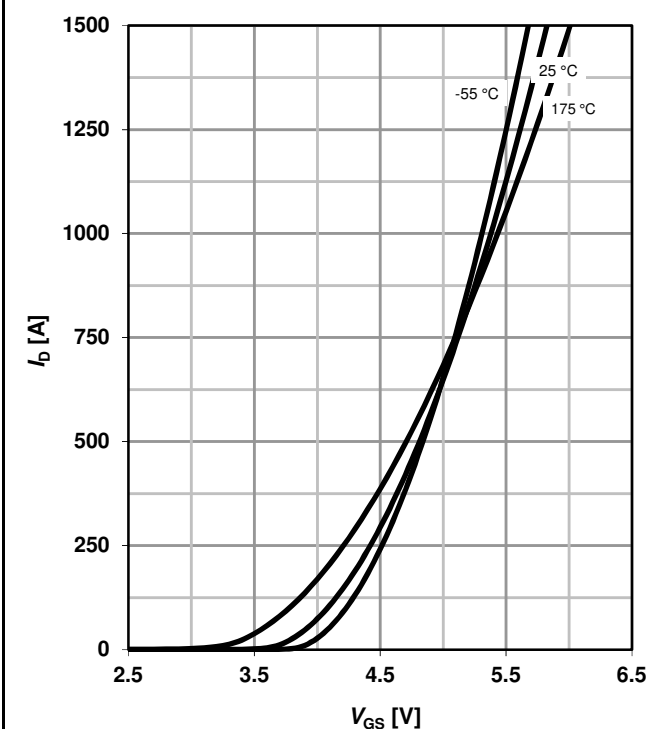
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$



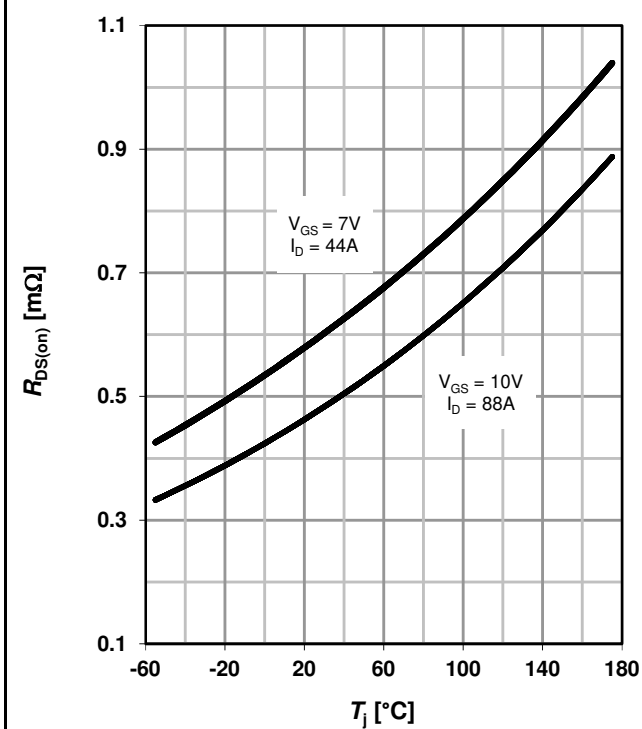
7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 6\text{ V}; \text{parameter: } T_j$



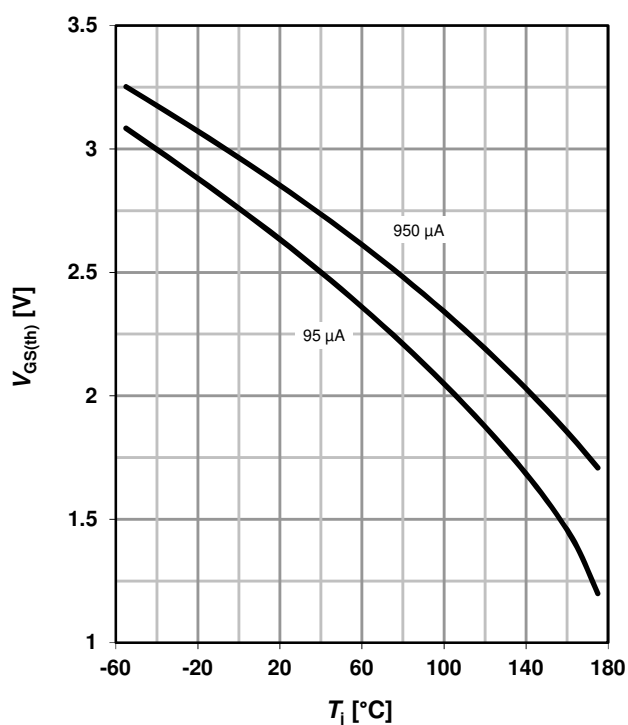
8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j); \text{parameter: } I_D, V_{GS}$



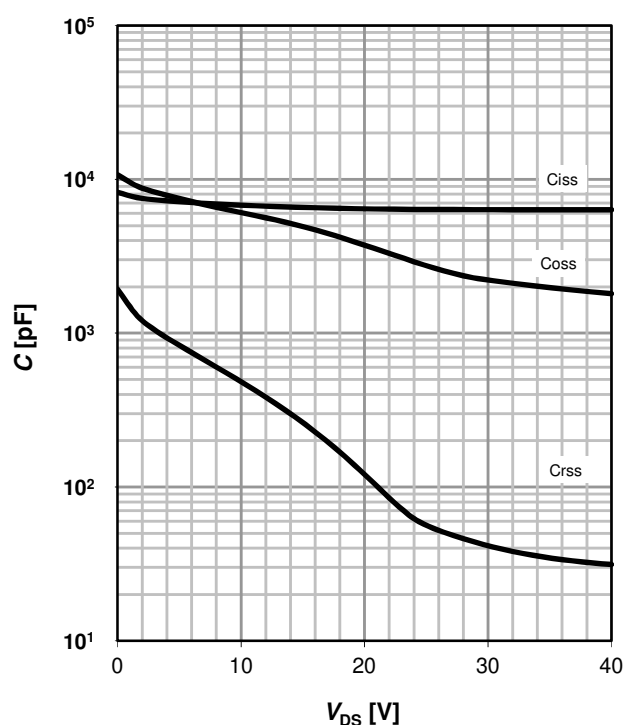
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



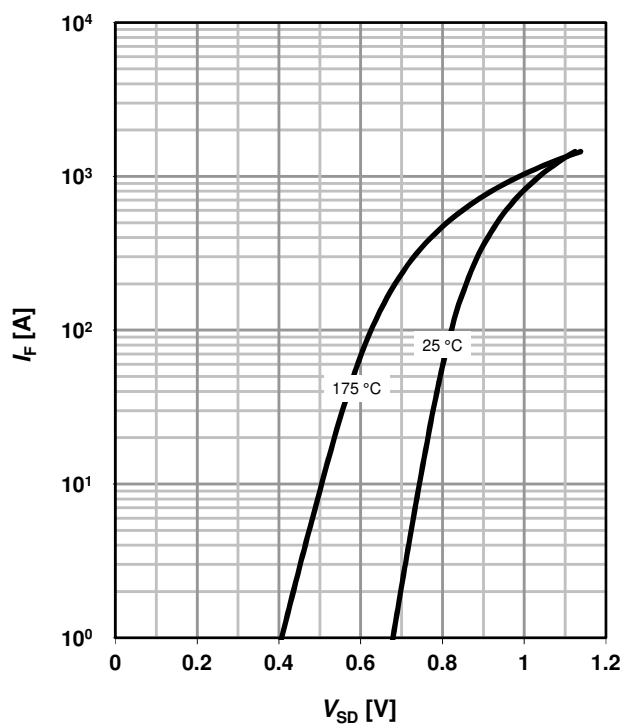
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



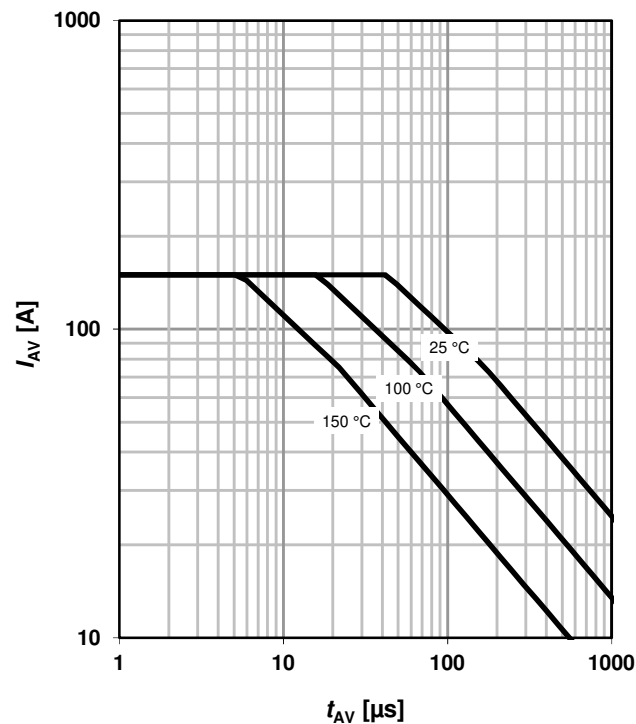
11 Typical forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



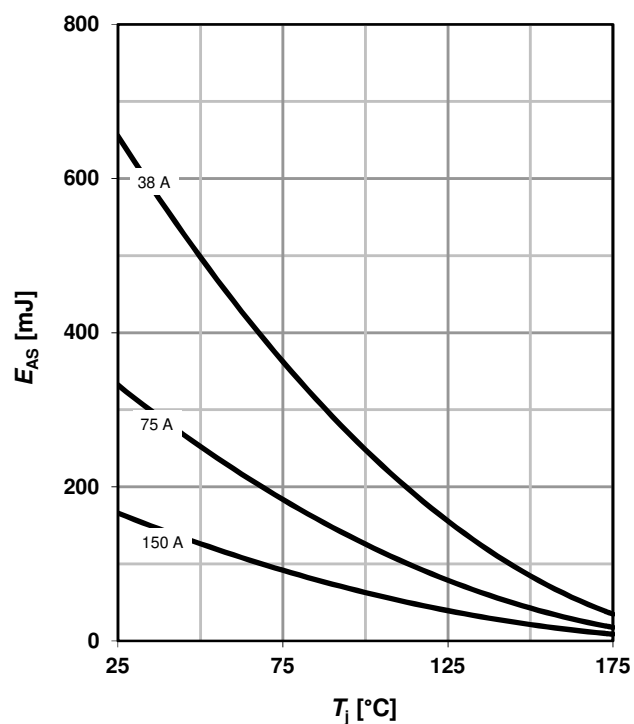
12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



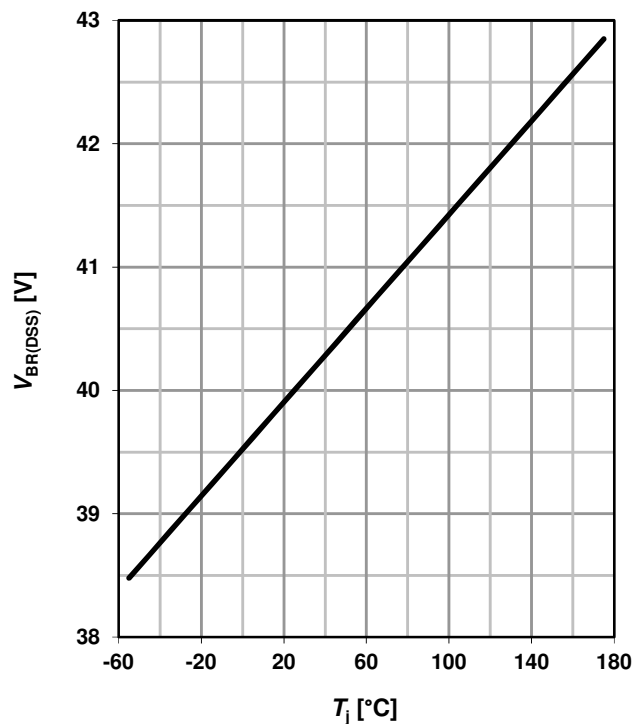
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: I_D



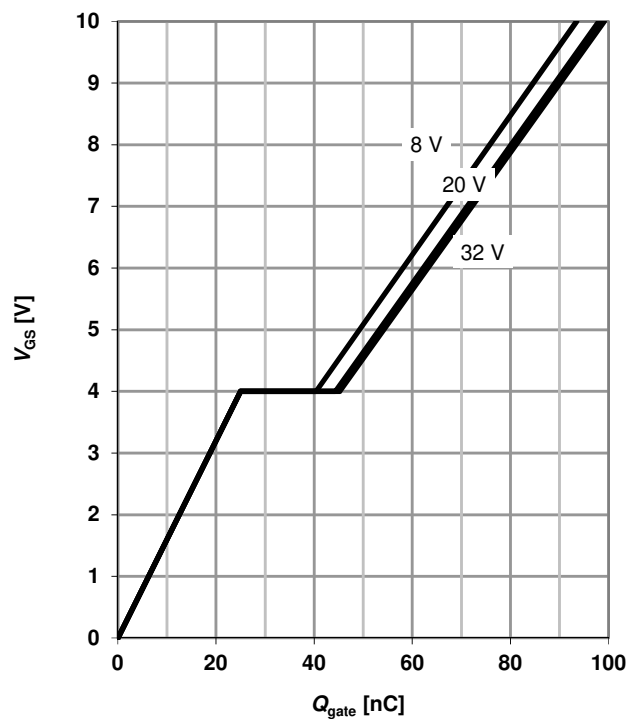
14 Drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j)$; $I_{D_typ} = 1$ mA

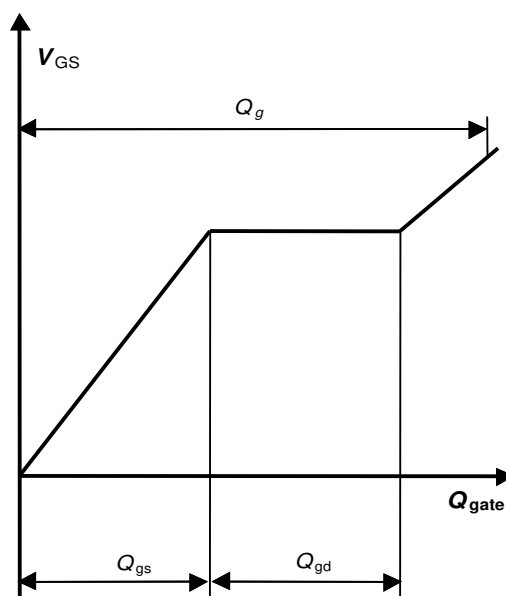


15 Typ. gate charge

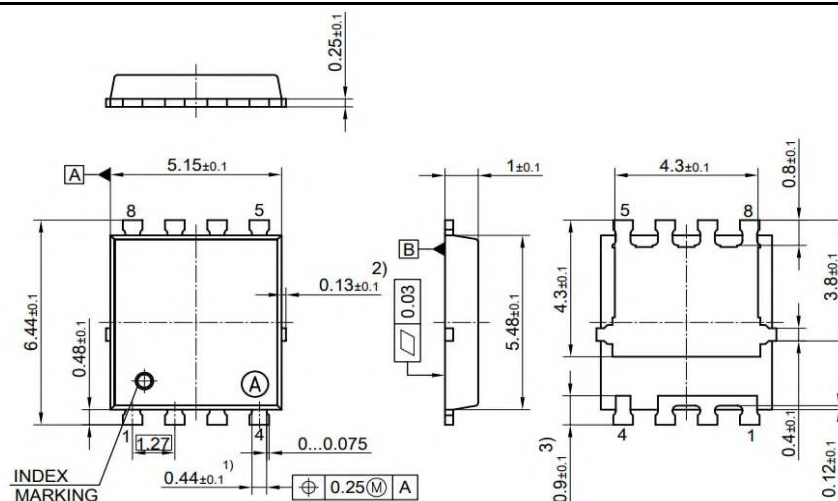
$V_{GS} = f(Q_{gate})$; $I_D = 88$ A pulsed; parameter: V_{DD}



16 Gate charge waveforms

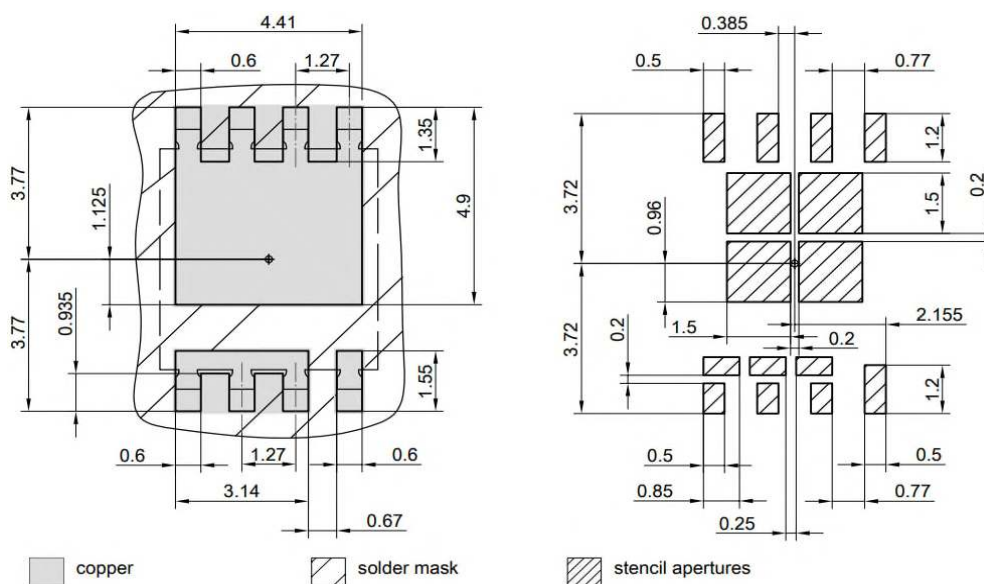


Package Outline



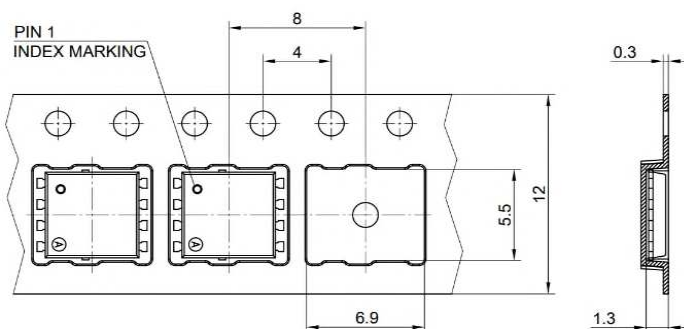
- 1) EXCLUDE MOLD FLASH
 - 2) REMOVAL ON MOLD GATE, INTRUSION 0.1MM AND PROTRUSION 0.1MM
 - 3) LEAD LENGTH UP TO ANTI FLASH LINE
 - 4) ALL METAL SURFACE ARE PLATED, EXCEPT AREA OF CUT
- ALL DIMENSIONS ARE IN UNITS MM
THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 []

Footprint



all dimensions in mm

Packaging



all dimensions in mm



Revision History

Revision	Date	Changes
Revision 1.0	30.05.2023	Final data sheet

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